8. External Memory Interfaces in the Cyclone III Device Family

CIII51009-3.1

In addition to an abundant supply of on-chip memory, Cyclone® III device family (Cyclone III and Cyclone III LS devices) can easily interface to a broad range of external memory, including DDR2 SDRAM, DDR SDRAM, and QDRII SRAM. External memory devices are an important system component of a wide range of image processing, storage, communications, and general embedded applications.

Altera® recommends that you construct all DDR2 or DDR SDRAM external memory interfaces using the Altera ALTMEMPHY megafunction. You can implement the controller function using the Altera DDR2 or DDR SDRAM memory controllers, third-party controllers, or a custom controller for unique application needs. Cyclone III device family supports QDR II interfaces electrically, but Altera does not supply controller or physical layer (PHY) megafunctions for QDR II interfaces.

This chapter includes a description of the hardware interfaces for external memory interfaces available in Cyclone III device family.

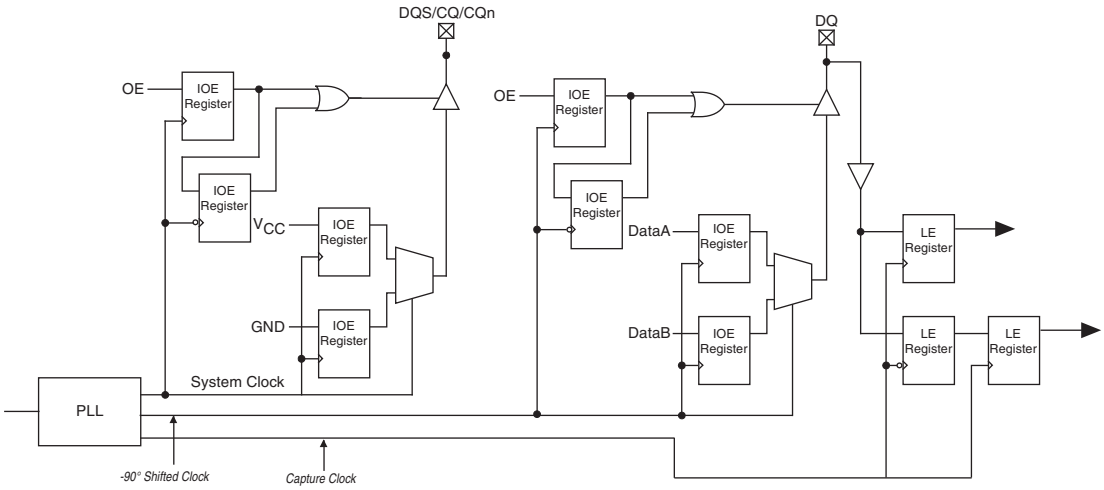
This chapter contains the following sections:

- "Cyclone III Device Family Memory Interfaces Pin Support" on page 8–2
- "Cyclone III Device Family Memory Interfaces Features" on page 8–11

For more information about external memory system performance specifications, board design guidelines, timing analysis, simulation, and debugging information, refer to the External Memory Interfaces page.

Figure 8–1 shows the block diagram of a typical external memory interface data path in Cyclone III device family.

Figure 8–1. Cyclone III Device Family External Memory Data Path *(1)*



Note to Figure 8–1:

(1) All clocks shown here are global clocks.

Cyclone III Device Family Memory Interfaces Pin Support

Cyclone III device family uses data (DQ), data strobe (DQS), clock, command, and address pins to interface with external memory. Some memory interfaces use the data mask (DM) or byte write select (BWS#) pins to enable data masking. This section describes how Cyclone III device family supports all these different pins.

Data and Data Clock/Strobe Pins

Cyclone III device family data pins for external memory interfaces are called D for write data, Q for read data, or DQ for shared read and write data pins. The read-data strobes or read clocks are called DQS pins. Cyclone III device family supports both bidirectional data strobes and unidirectional read clocks. Depending on the external memory standard, the DQ and DQS are bidirectional signals (in DDR2 and DDR SDRAM) or unidirectional signals (in QDR II SRAM). Connect the bidirectional DQ data signals to the same Cyclone III device family DQ pins. For unidirectional D or Q signals, connect the read-data signals to a group of DQ pins and the write-data signals to a different group of DQ pins.

In QDR II SRAM, the Q read-data group must be placed at a different V_{REF} bank location from the D write-data group, command, or address pins.

In Cyclone III device family, DQS is used only during write mode in DDR2 and DDR SDRAM interfaces. Cyclone III device family ignores DQS as the read-data strobe because the PHY internally generates the read capture clock for read mode. However, you must connect the DQS pin to the DQS signal in DDR2 and DDR SDRAM interfaces, or to the CQ signal in QDR II SRAM interfaces.

Cyclone III device family does not support differential strobe pins, which is an optional feature in the DDR2 SDRAM device.

When you use the Altera Memory Controller MegaCore®, the PHY is instantiated for you. For more information about the memory interface data path, refer to the External Memory Interfaces page.

ALTMEMPHY is a self-calibrating megafunction, enhanced to simplify the implementation of the read-data path in different memory interfaces. The auto-calibration feature of ALTMEMPHY provides ease-of-use by optimizing clock phases and frequencies across process, voltage, and temperature (PVT) variations. You can save on the global clock resources in Cyclone III device family through the ALTMEMPHY megafunction because you are not required to route the DQS signals on the global clock buses (because DQS is ignored for read capture). Resynchronization issues do not arise because no transfer occurs from the memory domain clock (DQS) to the system domain for capturing data DQ.

All I/O banks in Cyclone III device family can support DQ and DQS signals with DQ-bus modes of ×8, ×9, ×16, ×18, ×32, and ×36. DDR2 and DDR SDRAM interfaces use ×8 mode DQS group regardless of the interface width. For wider interface, you can use multiple ×8 DQ groups to achieve the desired width requirement.

In the ×9, ×18, and ×36 modes, a pair of complementary DQS pins (CQ and CQ#) drives up to 9, 18, or 36 DQ pins, respectively, in the group, to support one, two, or four parity bits and the corresponding data bits. The ×9, ×18, and ×36 modes support the QDR II memory interface. CQ# is the inverted read-clock signal which is connected to the complementary data strobe (DQS or CQ#) pin. You can use any unused DQ pins as regular user I/O pins if they are not used as memory interface signals.

Table 8–1 lists the number of DQS or DQ groups supported on each side of the Cyclone III device only.

Table 8–1. Cyclone III Device DQS and DQ Bus Mode Support for Each Side of the Device (Part 1 of 4)

Device	Package	Side	Number ×8 Groups	Number ×9 Groups	Number ×16 Groups	Number ×18 Groups	Number ×32 Groups	Number ×36 Groups
EP3C5	144-pin EQFP (1)	Left	0	0	0	0	—	—
		Right	0	0	0	0	—	—
		Top (2)	1	0	0	0	—	—
		Bottom (3), (4)	1	0	0	0	—	—
	164-pin MBGA (1)	Left	0	0	0	0	—	—
		Right	0	0	0	0	—	—
		Top (2)	1	0	0	0	—	—
		Bottom (3), (4)	1	0	0	0	—	—
	256-pin FineLine BGA/256-pin Ultra FineLine BGA (1)	Left (4), (5)	1	1	0	0	—	—
		Right (4), (6)	1	1	0	0	—	—
		Top	2	2	1	1	—	—
		Bottom	2	2	1	1	—	—

Table 8–1. Cyclone III Device DQS and DQ Bus Mode Support for Each Side of the Device (Part 2 of 4)

Device	Package	Side	Number ×8 Groups	Number ×9 Groups	Number ×16 Groups	Number ×18 Groups	Number ×32 Groups	Number ×36 Groups
EP3C10	144-pin EQFP (1)	Left	0	0	0	0	—	—
		Right	0	0	0	0	—	—
		Top (2)	1	0	0	0	—	—
		Bottom (3), (4)	1	0	0	0	—	—
	164-pin MBGA (1)	Left	0	0	0	0	—	—
		Right	0	0	0	0	—	—
		Top (2)	1	0	0	0	—	—
		Bottom (3), (4)	1	0	0	0	—	—
	256-pin FineLine BGA/256-pin Ultra FineLine BGA (1)	Left (4), (5)	1	1	0	0	—	—
		Right (4), (6)	1	1	0	0	—	—
		Top	2	2	1	1	—	—
		Bottom	2	2	1	1	—	—
EP3C16	144-pin EQFP (1)	Left	0	0	0	0	—	—
		Right	0	0	0	0	—	—
		Top (2)	1	0	0	0	—	—
		Bottom (3), (4)	1	0	0	0	—	—
	164-pin MBGA (1)	Left	0	0	0	0	—	—
		Right	0	0	0	0	—	—
		Top (2)	1	0	0	0	—	—
		Bottom (3), (4)	1	0	0	0	—	—
	240-pin PQFP (1)	Left (4), (7)	1	1	0	0	—	—
		Right (3), (4)	1	0	0	0	—	—
		Top	1	1	0	0	—	—
		Bottom	1	1	0	0	—	—
	256-pin FineLine BGA/256-pin Ultra FineLine BGA (1)	Left (4), (5)	1	1	0	0	—	—
		Right (4), (6)	1	1	0	0	—	—
		Top	2	2	1	1	—	—
		Bottom	2	2	1	1	—	—
	484-pin FineLine BGA/484-pin Ultra FineLine BGA	Left	4	2	2	2	1	1
		Right	4	2	2	2	1	1
		Top	4	2	2	2	1	1
		Bottom	4	2	2	2	1	1

Table 8–1. Cyclone III Device DQS and DQ Bus Mode Support for Each Side of the Device (Part 3 of 4)

Device	Package	Side	Number ×8 Groups	Number ×9 Groups	Number ×16 Groups	Number ×18 Groups	Number ×32 Groups	Number ×36 Groups
EP3C25	144-pin EQFP (1)	Left	0	0	0	0	—	—
		Right	0	0	0	0	—	—
		Top (2)	1	0	0	0	—	—
		Bottom (3), (4)	1	0	0	0	—	—
	240-pin PQFP (1)	Left (4), (7)	1	1	0	0	—	—
		Right (3), (4)	1	0	0	0	—	—
		Top	1	1	0	0	—	—
		Bottom	1	1	0	0	—	—
	256-pin FineLine BGA/256-pin Ultra FineLine BGA (1)	Left (4), (5)	1	1	0	0	—	—
		Right (4), (6)	1	1	0	0	—	—
		Top	2	2	1	1	—	—
		Bottom	2	2	1	1	—	—
	324-pin FineLine BGA (1)	Left	2	2	1	1	—	—
		Right (8)	2	2	1	1	—	—
		Top	2	2	1	1	—	—
		Bottom	2	2	1	1	—	—
EP3C40	240-pin PQFP	Left (4), (7)	1	1	0	0	0	0
		Right (3), (4)	1	0	0	0	0	0
		Top	1	1	0	0	0	0
		Bottom	1	1	0	0	0	0
	324-pin FineLine BGA	Left	2	2	1	1	0	0
		Right (8)	2	2	1	1	0	0
		Top	2	2	1	1	0	0
		Bottom	2	2	1	1	0	0
	484-pin FineLine BGA/484-pin Ultra FineLine BGA	Left	4	2	2	2	1	1
		Right	4	2	2	2	1	1
		Top	4	2	2	2	1	1
		Bottom	4	2	2	2	1	1
	780-pin FineLine BGA	Left	4	2	2	2	1	1
		Right	4	2	2	2	1	1
		Top	6	2	2	2	1	1
		Bottom	6	2	2	2	1	1

Table 8–1. Cyclone III Device DQS and DQ Bus Mode Support for Each Side of the Device (Part 4 of 4)

Device	Package	Side	Number ×8 Groups	Number ×9 Groups	Number ×16 Groups	Number ×18 Groups	Number ×32 Groups	Number ×36 Groups
EP3C55	484-pin FineLine BGA/484-pin Ultra FineLine BGA	Left	4	2	2	2	1	1
		Right	4	2	2	2	1	1
		Top	4	2	2	2	1	1
		Bottom	4	2	2	2	1	1
	780-pin FineLine BGA	Left	4	2	2	2	1	1
		Right	4	2	2	2	1	1
		Top	6	2	2	2	1	1
		Bottom	6	2	2	2	1	1
EP3C80	484-pin FineLine BGA/484-pin Ultra FineLine BGA	Left	4	2	2	2	1	1
		Right	4	2	2	2	1	1
		Top	4	2	2	2	1	1
		Bottom	4	2	2	2	1	1
	780-pin FineLine BGA	Left	4	2	2	2	1	1
		Right	4	2	2	2	1	1
		Top	6	2	2	2	1	1
		Bottom	6	2	2	2	1	1
EP3C120	484-pin FineLine BGA	Left	4	2	2	2	1	1
		Right	4	2	2	2	1	1
		Top	4	2	2	2	1	1
		Bottom	4	2	2	2	1	1
	780-pin FineLine BGA	Left	4	2	2	2	1	1
		Right	4	2	2	2	1	1
		Top	6	2	2	2	1	1
		Bottom	6	2	2	2	1	1

Notes to Table 8–1:

(1) This device package does not support ×32 or ×36 mode.

(2) For the top side of the device, RUP, RDN, PLLCLKOUT3n, and PLLCLKOUT3p pins are shared with the DQ or DM pins to gain ×8 DQ group. You cannot use these groups if you are using the RUP and RDN pins for on-chip termination (OCT) calibration or if you are using PLLCLKOUT3n and PLLCLKOUT3p.

(3) There is no DM pin support for these groups.

(4) The RUP and RDN pins are shared with the DQ pins. You cannot use these groups if you are using the RUP and RDN pins for OCT calibration.

(5) The ×8 DQ group can be formed in Bank 2.

(6) The ×8 DQ group can be formed in Bank 5.

(7) There is no DM and BWS# pins support for these groups.

(8) The RUP pin is shared with the DQ pin to gain ×9 or ×18 DQ group. You cannot use these groups if you are using the RUP and RDN pins for OCT calibration.

Table 8–2 lists the numbers of DQS or DQ groups supported on each side of the Cyclone III LS device only.

Table 8–2. Cyclone III LS Device DQS and DQ Bus Mode Support for Each Side of the Device

Device	Package	Side	Number of ×8 Groups	Number of ×9 Groups	Number of ×16 Groups	Number of ×18 Groups	Number of ×32 Groups	Number of ×36 Groups
EP3CLS70	484-pin FineLine BGA/ 484-pin Ultra FineLine BGA (1)	Left	2	2	1	1	—	—
		Right	2	2	1	1	—	—
		Top	2	2	1	1	—	—
		Bottom	2	2	1	1	—	—
	780-pin FineLine BGA	Left	4	2	2	2	1	1
		Right	4	2	2	2	1	1
		Top	6	2	2	2	1	1
		Bottom	6	2	2	2	1	1
EP3CLS100	484-pin FineLine BGA/ 484-pin Ultra FineLine BGA (1)	Left	2	2	1	1	—	—
		Right	2	2	1	1	—	—
		Top	2	2	1	1	—	—
		Bottom	2	2	1	1	—	—
	780-pin FineLine BGA	Left	4	2	2	2	1	1
		Right	4	2	2	2	1	1
		Top	6	2	2	2	1	1
		Bottom	6	2	2	2	1	1
EP3CLS150	484-pin FineLine BGA (1)	Left	2	2	1	1	—	—
		Right	2	2	1	1	—	—
		Top	2	2	1	1	—	—
		Bottom	2	2	1	1	—	—
	780-pin FineLine BGA	Left	4	2	2	2	1	1
		Right	4	2	2	2	1	1
		Top	6	2	2	2	1	1
		Bottom	6	2	2	2	1	1
EP3CLS200	484-pin FineLine BGA (1)	Left	2	2	1	1	—	—
		Right	2	2	1	1	—	—
		Top	2	2	1	1	—	—
		Bottom	2	2	1	1	—	—
	780-pin FineLine BGA	Left	4	2	2	2	1	1
		Right	4	2	2	2	1	1
		Top	6	2	2	2	1	1
		Bottom	6	2	2	2	1	1

Note to Table 8–2:

(1) This device package does not support x32 or 36 mode.

For more information about device package outline, refer to the Package and Thermal Resistance page.

DQS pins are listed in the Cyclone III and Cyclone III LS pin tables as DQSXY, in which X indicates the DQS grouping number and Y indicates whether the group is located on the top (T), bottom (B), left (L) or right (R) side of the device. Similarly, the corresponding DQ pins are marked as DQXY, in which the X denotes the DQ grouping number and Y denotes whether the group is located on the top (T), bottom (B), left (L) or right (R) side of the device. For example, DQS2T indicates a DQS pin belonging to group 2, located on the top side of the device. Similarly, the DQ pins belonging to that group is shown as DQ2T.

Each DQ group is associated with its corresponding DQS pins, as defined in the Cyclone III and Cyclone III LS pin tables; for example:

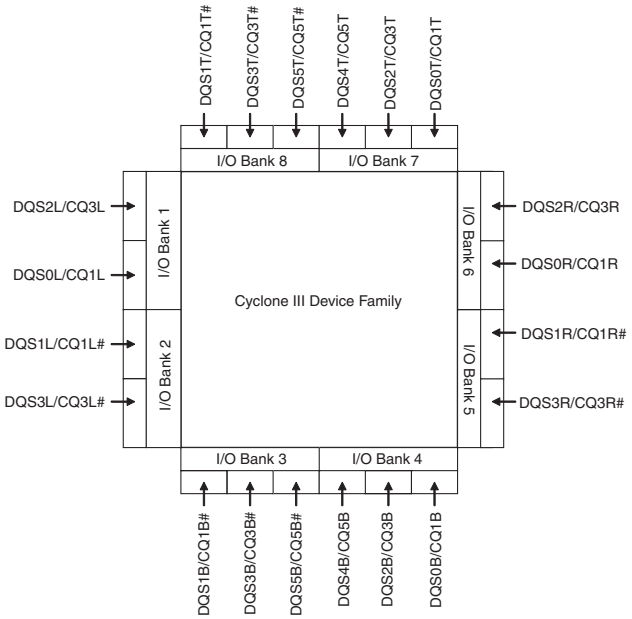
- For DDR2 or DDR SDRAM, ×8 DQ group DQ3B[7:0] pins are associated with the DQS3B pin (same 3B group index)
- For QDR II SRAM, ×9 Q read-data group DQ3L[8..0] pins are associated with DQS2L/CQ3L and DQS3L/CQ3L# pins (same 3L group index)

The Quartus® II software issues an error message if a DQ group is not placed properly with its associated DQS.

Figure 8–2 shows the location and numbering of the DQS, DQ, or CQ# pins in the Cyclone III device family I/O banks.

For maximum timing performance, Altera recommends that the data groups for external memory interfaces must always be within the same side of a device.

Figure 8–2. DQS, CQ, or CQ# Pins in Cyclone III Device Family I/O Banks *(1)*

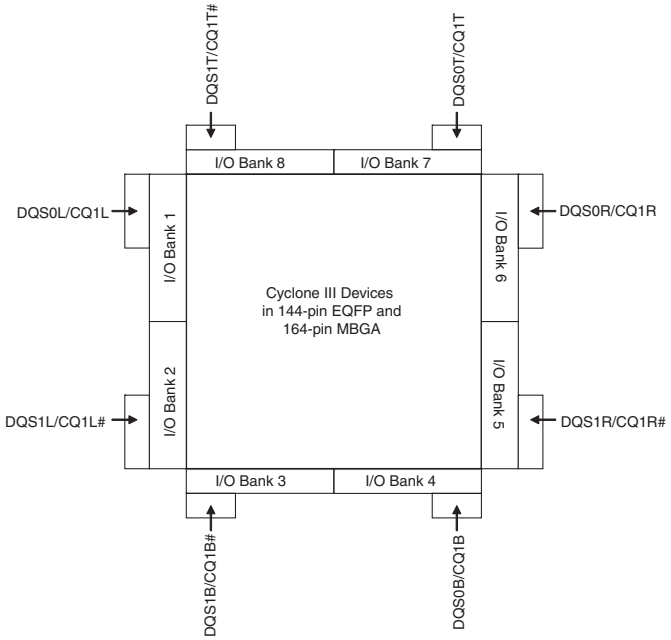


Note to Figure 8–2:

(1) The DQS, CQ, or CQ# pin locations in this diagram apply to all packages in Cyclone III device family except devices in 144-pin EQFP and 164-pin MBGA.

Figure 8–3 shows the location and numbering of the DQS, DQ, or CQ# pins in I/O banks of the Cyclone III device in the 144-pin EQFP and 164-pin MBGA packages only.

Figure 8–3. DQS, CQ, or CQ# Pins for Devices in the 144-Pin EQFP and 164-Pin MBGA Packages



In Cyclone III device family, the ×9 mode uses the same DQ and DQS pins as the ×8 mode, and one additional DQ pin that serves as a regular I/O pin in the ×8 mode. The ×18 mode uses the same DQ and DQS pins as ×16 mode, with two additional DQ pins that serve as regular I/O pins in the ×16 mode. Similarly, the ×36 mode uses the same DQ and DQS pins as the ×32 mode, with four additional DQ pins that serve as regular I/O pins in the ×32 mode. When not used as DQ or DQS pins, the memory interface pins are available as regular I/O pins.

Optional Parity, DM, and Error Correction Coding Pins

Cyclone III device family supports parity in ×9, ×18, and ×36 modes. One parity bit is available per eight bits of data pins. You can use any of the DQ pins for parity in Cyclone III device family because the parity pins are treated and configured similar to DQ pins.

DM pins are only required when writing to DDR2 and DDR SDRAM devices. QDR II SRAM devices use the BWS# signal to select the byte to be written into memory. A low signal on the DM or BWS# pin indicates the write is valid. Driving the DM or BWS# pin high causes the memory to mask the DQ signals. Each group of DQS and DQ signals has one DM pin. Similar to the DQ output signals, the DM signals are clocked by the -90° shifted clock.

In Cyclone III device family, the DM pins are preassigned in the device pinouts. The Quartus II Fitter treats the DQ and DM pins in a DQS group equally for placement purposes. The preassigned DQ and DM pins are the preferred pins to use.

Some DDR2 SDRAM and DDR SDRAM devices support error correction coding (ECC), a method of detecting and automatically correcting errors in data transmission. In 72-bit DDR2 or DDR SDRAM, there are eight ECC pins and 64 data pins. Connect the DDR2 and DDR SDRAM ECC pins to a separate DQS or DQ group in Cyclone III device family. The memory controller needs additional logic to encode and decode the ECC data.

Address and Control/Command Pins

The address signals and the control or command signals are typically sent at a single data rate. You can use any of the user I/O pins on all I/O banks of Cyclone III device family to generate the address and control or command signals to the memory device.

Cyclone III device family does not support QDR II SRAM in the burst length of two.

Memory Clock Pins

In DDR2 and DDR SDRAM memory interfaces, the memory clock signals (CK and CK#) are used to capture the address signals and the control or command signals. Similarly, QDR II SRAM devices use the write clocks (K and K#) to capture the address and command signals. The CK/CK# and K/K# signals are generated to resemble the write-data strobe using the DDIO registers in Cyclone III device family.

For more information about CK/CK# pins placement, refer to the "Pin Connection Guidelines Tables" section in the *Planning Pin and FPGA Resources* chapter of the *External Memory Interface Handbook*.

Cyclone III Device Family Memory Interfaces Features

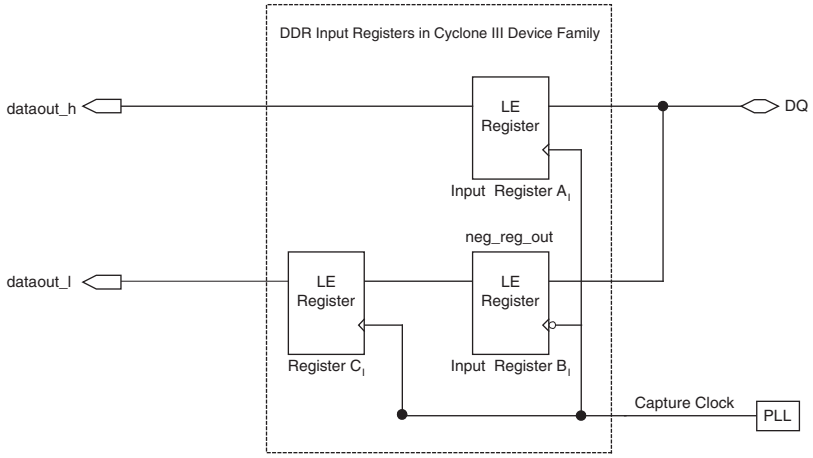
This section describes Cyclone III device family memory interfaces, including DDR input registers, DDR output registers, OCT, and phase-lock loops (PLLs).

DDR Input Registers

The DDR input registers are implemented with three internal logic element (LE) registers for every DQ pin. These LE registers are located in the logic array block (LAB) adjacent to the DDR input pin.

Figure 8–4 shows Cyclone III device family DDR input registers.

Figure 8–4. Cyclone III Device Family DDR Input Registers



The DDR data is first fed to two registers, input register A_I and input register B_I.

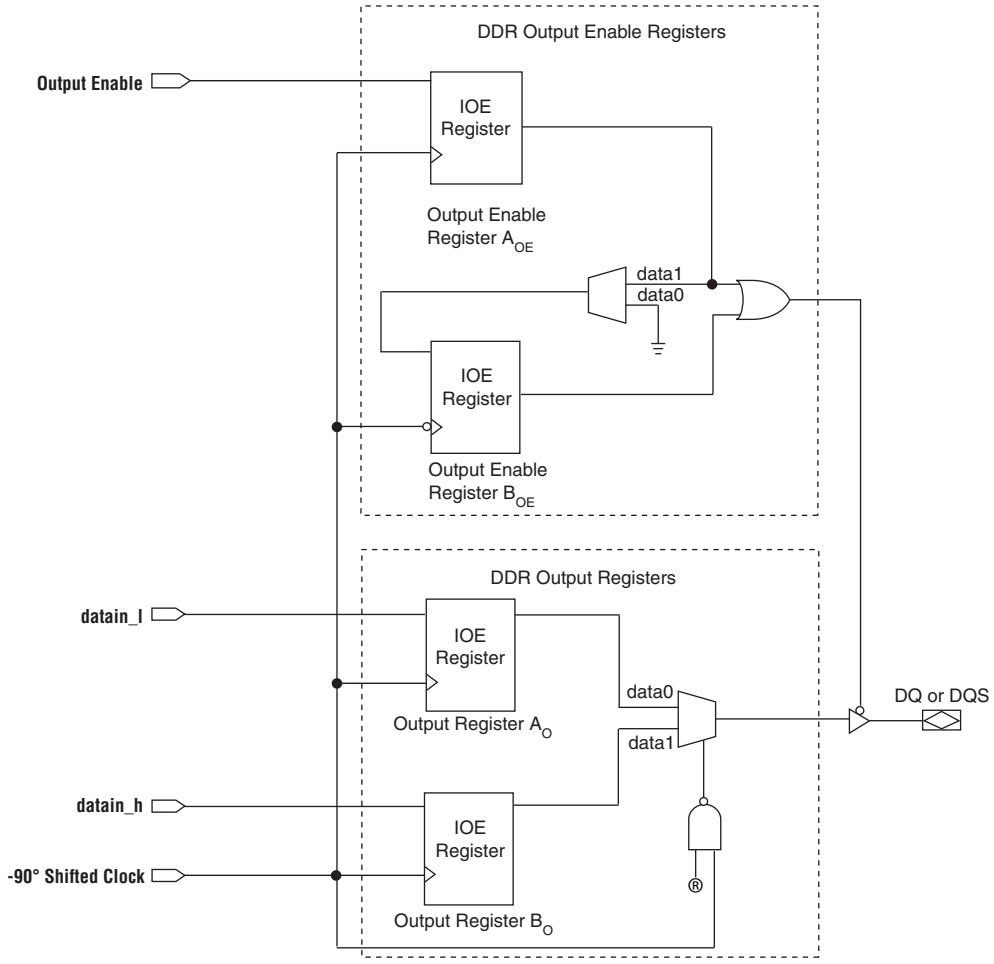
- Input register A_I captures the DDR data present during the rising edge of the clock
- Input register B_I captures the DDR data present during the falling edge of the clock
- Register C_I aligns the data before it is synchronized with the system clock

The data from the DDR input register is fed to two registers, sync_reg_h and sync_reg_l, then the data is typically transferred to a FIFO block to synchronize the two data streams to the rising edge of the system clock. Because the read-capture clock is generated by the PLL, the read-data strobe signal (DQS or CQ) is not used during read operation in Cyclone III device family; hence, postamble is not a concern in this case.

DDR Output Registers

A dedicated write DDIO block is implemented in the DDR output and output enable paths. Figure 8–5 shows how Cyclone III device family dedicated write DDIO block is implemented in the I/O element (IOE) registers.

Figure 8–5. Cyclone III Device Family Dedicated Write DDIO



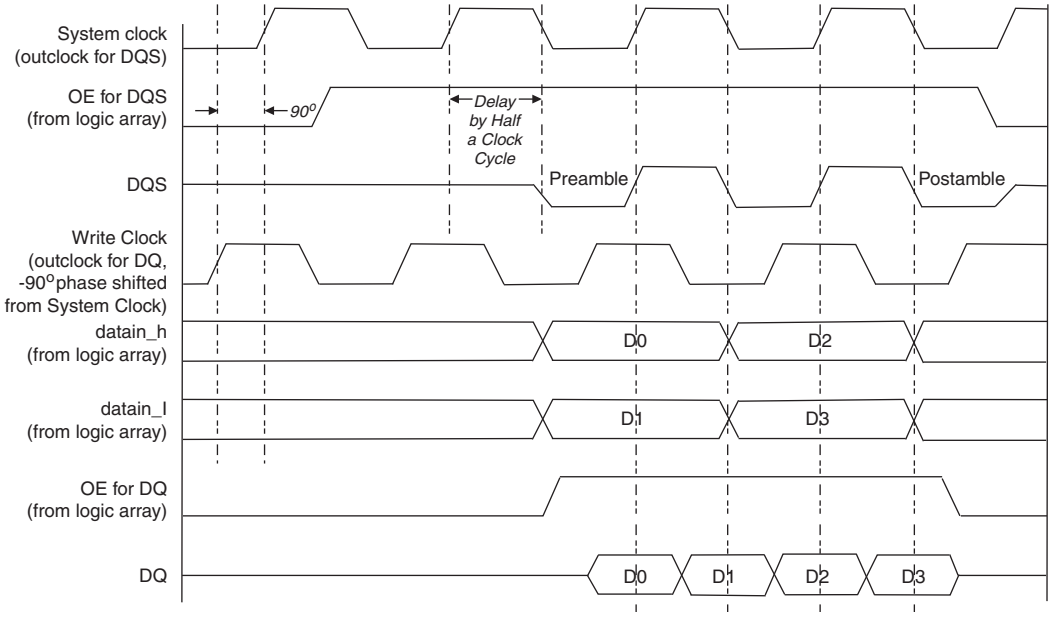
The two DDR output registers are located in the I/O element (IOE) block. Two serial data streams routed through `datain_l` and `datain_h`, are fed into two registers, `output register Ao` and `output register Bo`, respectively, on the same clock edge. The output from `output register Ao` is captured on the falling edge of the clock, while the output from `output register Bo` is captured on the rising edge of the clock. The registered outputs are multiplexed by the common clock to drive the DDR output pin at twice the data rate.

The DDR output enable path has a similar structure to the DDR output path in the IOE block. The second output enable register provides the write preamble for the `DQS` strobe in DDR external memory interfaces. This active-low output enable register extends the high-impedance state of the pin by half a clock cycle to provide the external memory's `DQS` write preamble time specification.

For more information about Cyclone III device family IOE registers, refer to the *I/O Features in the Cyclone III Device Family* chapter.

Figure 8–6 shows how the second output enable register extends the DQS high-impedance state by half a clock cycle during a write operation.

Figure 8–6. Extending the OE Disable by Half a Clock Cycle for a Write Transaction *(1)*



Note to Figure 8–6:

(1) The waveform reflects the software simulation result. The OE signal is an active low on the device. However, the Quartus II software implements the signal as an active high and automatically adds an inverter before the A_{OE} register D input.

OCT

Cyclone III device family supports calibrated on-chip series termination (R_S OCT) in both vertical and horizontal I/O banks. To use the calibrated OCT, you must use the RUP and RDN pins for each R_S OCT control block (one for each side). You can use each OCT calibration block to calibrate one type of termination with the same V_{CCIO} for that given side.

For more information about Cyclone III device family OCT calibration block, refer to the *Cyclone III Device I/O Features* chapter.

PLL

When interfacing with external memory, the PLL is used to generate the memory system clock, the write clock, the capture clock and the logic-core clock. The system clock generates the DQS write signals, commands, and addresses. The write-clock is shifted by -90° from the system clock and generates the DQ signals during writes. You can use the PLL reconfiguration feature to calibrate the read-capture phase shift to balance the setup and hold margins.

The PLL is instantiated in the ALTMEMPHY megafunction. All outputs of the PLL are used when the ALTMEMPHY megafunction is instantiated to interface with external memories.

For more information about the usage of PLL outputs by the ALTMEMPHY megafunction, refer to the External Memory Interfaces page.

For more information about Cyclone III device family PLL, refer to the *Clock Networks and PLLs in the Cyclone III Device Family* chapter.

Document Revision History

Table 8–3 lists the revision history for this document.

Table 8–3. Document Revision History

Date	Version	Changes
July 2012	3.1	Finalized Table 8–2.
December 2011	3.0	■ Updated "Data and Data Clock/Strobe Pins" on page 8–2 and "Memory Clock Pins" on page 8–10. ■ Updated hyperlinks. ■ Minor text edits.
January 2010	2.3	■ Removed Tables 8-1, 8-2, 8-3, and 8-4. ■ Changed links to reference *Literature: External Memory Interfaces*.
December 2009	2.2	Minor changes to the text.
July 2009	2.1	Made minor correction to the part number.
June 2009	2.0	■ Updated chapter part number. ■ Updated "Introduction" on page 8–1. ■ Updated Table 8–1 on page 8–1, Table 8–2 on page 8–2, Table 8–3 on page 8–3, Table 8–4 on page 8–4, and Table 8–5 on page 8–7. Updated notes to Table 8–6 on page 8–10. Updated "Data and Data Clock/Strobe Pins" on page 8–5. ■ Updated note to Figure 8–2 on page 8–12. ■ Updated "Optional Parity, DM, and Error Correction Coding Pins" on page 8–13. ■ Updated "Address and Control/Command Pins" on page 8–14.
October 2008	1.3	■ Updated "Introduction", "DDR Input Registers" and "Conclusion" sections. ■ Updated chapter to new template.
May 2008	1.2	■ Added *(Note 4)* to Figure 8–3. ■ Updated Table 8–3 and Table 8-5. Added new Table 8–4. ■ Updated *(Note 1)* to Figure 8-4. Updated Figure 8–5 and 8–14.
July 2007	1.1	■ Updated "Data and Data Clock/Strobe Pins" section. ■ Updated Table 8–5. ■ Added chapter TOC and "Referenced Documents" section.
March 2007	1.0	Initial release.