These pin connection guidelines should only be used as a recommendation, not as a specification. The use of the pin connection guidelines for any particular design should be verified for device operation, with the datasheet and Altera.

PLEASE REVIEW THE FOLLOWING TERMS AND CONDITIONS CAREFULLY BEFORE USING THE PIN CONNECTION GUIDELINES("GUIDELINES") PROVIDED TO YOU. BY USING THESE GUIDELINES, YOU INDICATE YOUR ACCEPTANCE OF SUCH TERMS AND CONDITIONS, WHICH CONSTITUTE THE LICENSE AGREEMENT ("AGREEMENT") BETWEEN YOU AND ALTERA CORPORATION ("ALTERA"). IF YOU DO NOT AGREE WITH ANY OF THESE TERMS AND CONDITIONS, DO NOT DOWNLOAD, COPY, INSTALL, OR USE OF THESE GUIDELINES.

1. Subject to the terms and conditions of this Agreement, Altera grants to you the use of this pin connection guideline to determine the pin connections of an Altera® programmable logic device-based design. You may not use this pin connection guideline for any other purpose.

2. Altera does not guarantee or imply the reliability, or serviceability, of the pin connection guidelines or other items provided as part of these guidelines. The files contained herein are provided 'AS IS'. ALTERA DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

3. In no event shall the aggregate liability of Altera relating to this Agreement or the subject matter hereof under any legal theory (whether in tort, contract, or otherwise), exceed One US Dollar (US$1.00). In no event shall Altera be liable for any lost revenue, lost profits, or other consequential, indirect, or special damages caused by your use of these guidelines even if advised of the possibility of such damages.

4. This Agreement shall be governed by the laws of the State of California, without regard to conflict of law or choice of law principles. You agree to submit to the exclusive jurisdiction of the courts in the County of Santa Clara, State of California for the resolution of any dispute or claim arising out of or relating to this Agreement. The parties hereby agree that the party who is not the substantially prevailing party with respect to a dispute, claim, or controversy relating to this Agreement shall pay the costs actually incurred by the substantially prevailing party in relation to such dispute, claim, or controversy, including attorneys' fees.

BY DOWNLOADING OR USING THESE GUIDELINES, YOU ACKNOWLEDGE THAT YOU HAVE READ THIS AGREEMENT, UNDERSTAND IT, AND AGREE TO BE BOUND BY ITS TERMS AND CONDITIONS. YOU AND ALTERA FURTHER AGREE THAT IT IS THE COMPLETE AND EXCLUSIVE STATEMENT OF THE AGREEMENT BETWEEN YOU AND ALTERA, WHICH SUPERSEDES ANY PROPOSAL OR PRIOR AGREEMENT, ORAL OR WRITTEN, AND ANY OTHER COMMUNICATIONS BETWEEN YOU AND ALTERA RELATING TO THE SUBJECT MATTER OF THIS AGREEMENT.

Pin Connection Guidelines Agreement © 2015 Altera Corporation. All rights reserved.

Arria V GZ Pin Connection Guidelines

Arria V GZ Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
Clock and PLL Pins			
CLK[0:23]p	I/O, Clock Input	Dedicated high speed clock input pins that can also be used for data inputs/outputs. Differential input OCT Rd, single ended input OCT Rt, and single ended output OCT Rs are supported on these pins.	You can tie unused pins to GND or leave them unconnected. If unconnected, use the Quartus II software programmable options to internally bias these pins. You can reserve them as inputs tristate with weak pull-up resistor enabled, or as outputs driving GND.
CLK[0:23]n	I/O, Clock Input	Dedicated high speed clock input pins that can also be used for data inputs/outputs. Differential input OCT Rd, single ended input OCT Rt, and single ended output OCT Rs are supported on these pins.	You can tie unused pins to GND or leave them unconnected. If unconnected, use the Quartus II software programmable options to internally bias these pins. You can reserve them as inputs tristate with weak pull-up resistor enabled, or as outputs driving GND.
FPLL_[B,T][L,C,R]_FB/CLKOUTp	I/O, Clock	Dual purpose I/O pins that can be used as two single-ended outputs or one differential external feedback input pin.	You can tie unused pins to GND or leave them unconnected. If unconnected, use the Quartus II software programmable options to internally bias these pins. You can reserve them as inputs tristate with weak pull-up resistor enabled, or as outputs driving GND.
FPLL_[B,T][L,C,R]_FB/CLKOUTn	I/O, Clock		You can tie unused pins to GND or leave them unconnected. If unconnected, use the Quartus II software programmable options to internally bias these pins. You can reserve them as inputs tristate with weak pull-up resistor enabled, or as outputs driving GND.
FPLL_[B,T][L,C,R]_CLKOUTp	I/O, Clock	I/O pins that can be used as two single-ended clock output pins or one differential clock output pair.	You can tie these pins to GND or leave them unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. You can reserve them as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
FPLL_[B,T][L,C,R]_CLKOUTn	I/O, Clock		You can tie these pins to GND or leave them unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. You can reserve them as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
Dedicated Configuration/JTAG Pins			
nIO_PULLUP	Input	Dedicated input that chooses whether the internal pull-ups on the user I/O pins and dual-purpose I/O pins (DATA[0:31], CLKUSR, INIT_DONE, DEV_OE, DEV_CLRn) are on or off before and during configuration. A logic high turns off the weak pull-up, while a logic low turns them on.	The nIO_PULLUP pin must be tied to GND.

Arria V GZ Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
TEMPDIODEp	Input	Pin used in conjunction with the temperature sensing diode (bias-high input) inside the FPGA.	If the temperature sensing diode is not used with an external temperture sensing device, then connect this pin to GND. When connecting the TEMPDIODE pins to an external temperture sense device, refer to the "Power Management in Arria V Devices" chapter in the Arria V Handbook.
TEMPDIODEn	Input	Pin used in conjunction with the temperature sensing diode (bias-low input) inside the FPGA.	If the temperature sensing diode is not used with an external temperture sensing device, then connect this pin to GND. When connecting the TEMPDIODE pins to an external temperture sense device, refer to the "Power Management in Arria V Devices" chapter in the Arria V Handbook.
MSEL[0:4]	Input	Configuration input pins that set the FPGA device configuration scheme.	These pins are internally connected through a 25-kΩ resistor to GND. Do not leave these pins floating. When these pins are unused connect them to GND. Depending on the configuration scheme used you should tie these pins to VCCPGM or GND. Refer to the "Configuration, Design Security, and Remote System Upgrades in Arria V Devices" chapter in the Arria V Handbook for the configuration scheme options. If only JTAG configuration is used, connect these pins to GND.
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled.	In multi-device configuration, nCE of the first device is tied low while its nCEO pin drives the nCE of the next device in the chain. In single device configuration and JTAG programming, you should connect nCE to GND.
nCONFIG	Input	Dedicated configuration control input. Pulling this pin low during user-mode will cause the FPGA to lose its configuration data, enter a reset state, and tri-state all I/O pins. Returning this pin to a logic high level will initiate reconfiguration.	You should connect nCONFIG directly to the configuration controller when the FPGA uses a passive configuration scheme, or through a 10-kΩ resistor tied to VCCPGM when using an active serial configuration scheme. If this pin is not used, it requires a connection directly or through a 10-kΩ resistor to VCCPGM.
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration done pin. As a status output, the CONF_DONE pin drives low before and during configuration. After all configuration data is received without error and the initialization cycle starts, CONF_DONE is released. As a status input, CONF_DONE goes high after all data is received. Then the device initializes and enters user mode. It is not available as a user I/O pin.	If internal pull-up resistors on the configuration controller or enhanced configuration device are used, you should not use external 10-kΩ pull-up resistors on this pin. Otherwise you should use an external 10-kΩ pull-up resistor to VCCPGM. When you use passive configuration schemes, this pin should also be monitored by the configuration controller. The CONF_DONE error checking is not supported in the active serial multi-device configuration mode.
nCEO	I/O, Output (open-drain)	Output that drives low when device configuration is complete. If this pin is not enabled for use as a configuration pin, it can be used as a user I/O pin.	During multi-device configuration, this pin feeds the nCE pin of a subsequent device. Connect this pin to an external 10-kΩ pull-up resistor to VCCPGM. During single device configuration, you may leave this pin floating.

Arria V GZ Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin. The FPGA drives nSTATUS low immediately after power-up and releases it after POR time. As a status output, the nSTATUS is pulled low if an error occurs during configuration. As a status input, the device enters an error state when nSTATUS is driven low by an external source during configuration or initialization. It is not available as a user I/O pin.	The OE and nCE pins of the enhanced configuration devices have optional internal programmable pull-up resistors. If internal pull-up resistors on the enhanced configuration device are used, you should not use external 10-kΩ pull-up on these pins. Otherwise, an external 10-KΩ pull-up resistors to VCCPGM should be used. When using Passive configuration schemes this pin should also be monitored by the configuration controller.
TCK	Input	Dedicated JTAG test clock input pin.	Connect this pin to a 1-kΩ pull-down resistor to GND. This pin has an internal 25-kΩ pull-down.
TMS	Input	Dedicated JTAG test mode select input pin.	Connect this pin to a 1-kΩ - 10-kΩ pull-up resistor to VCCPD. If the JTAG connections are not used, connect TMS to VCCPD using a 1-kΩ resistor. This pin has an internal 25-kΩ pull-up.
TDI	Input	Dedicated JTAG test data input pin.	Connect this pin to a 1-kΩ - 10-kΩ pull-up resistor to VCCPD. If the JTAG connections are not used, connect TDI to VCCPD using a 1-kΩ resistor. This pin has an internal 25-kΩ pull-up.
TDO	Output	Dedicated JTAG test data output pin.	You can disable the JTAG circuitry by leaving TDO unconnected. In cases where TDO uses VCCPD = 2.5 V to drive a 3.3 VJTAG interface, there may be leakage current in the TDI input buffer of the interfacing devices. You may use an external pull-up resistor tied to 3.3 V on their TDI pin to eliminate the leakage current if needed.
TRST	Input	Dedicated active low JTAG test reset input pin. TRST is used to asynchronously reset the JTAG boundary-scan circuit.	Utilization of TRST is optional. When you use this pin ensure that TMS is held high or TCK is static when TRST is changed from low to high. If not using TRST, tie this pin to a 1-kΩ pull-up resistor to VCCPD. If the JTAG connections are not used, tie this pin to GND. This pin has an internal 25-kΩ pull-up.
Optional/Dual-Purpose Configuration Pins			
nCSO	Output	Dedicated output control signal from the FPGA to the serial configuration device in AS mode that enables the configuration device.	When not programming the device in AS mode nCSO is not used. Also, when this pin is not used as an output then it is recommended to leave the pin unconnected.

Arria V GZ Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
DCLK	Input (PS, FPP) Output (AS)	Dedicated configuration clock pin. In PS and FPP configuration, DCLK is used to clock configuration data from an external source into the FPGA. In AS mode, DCLK is an output from the FPGA that provides timing for the configuration interface.	Do not leave this pin floating. Drive this pin either high or low.
CRC_ERROR	I/O, Output (open-drain)	Active high signal that indicates that the error detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error detection circuit is enabled.	When using as optionally open-drain output dedicated CRC_ERROR pin, connect this pin to an external 10-kΩ pull-up resistor to VCCPGM. When not using as the dedicated CRC_ERROR optionally open-drain output, and when this pin is not used as an I/O pin, then connect this pin as defined in the Quartus II software.
DEV_CLRn	I/O, Input	Optional pin that allows designers to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high (VCCPGM), all registers behave as programmed.	When the dedicated input DEV_CLRn is not used and this pin is not used as an I/O then it is recommended to tie this pin to ground.
DEV_OE	I/O, Input	Optional pin that allows designers to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high (VCCPGM), all I/O pins behave as defined in the design.	When the dedicated input DEV_OE is not used and this pin is not used as an I/O then it is recommended to tie this pin to ground.
DATA0	I/O, Input	Dual-purpose configuration data input pin. The DATA0 pin can be used for PS or FPP configuration or as an I/O pin after configuration is complete.	When the dedicated input for DATA[0] is not used and this pin is not used as an I/O then it is recommended to leave this pin unconnected.
DATA[1:31]	I/O, Input	Dual-purpose configuration input data pins. Use DATA [1:7] pins for FPP x8, DATA [1:15] pins for FPP x16, and DATA [1:31] pins for FPP x32 configuration or as regular I/O pins. These pins can also be used as user I/O pins after configuration.	When the dedicated inputs for DATA[1:31] are not used and these pins are not used as an I/O then it is recommended to leave these pins unconnected.
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration.	When using as optionally open-drain output dedicated INIT_DONE pin, connect this pin to an external 10-kΩ pull-up resistor to VCCPGM. When using in an AS or PS multi-device configuration mode ensure that the INIT_DONE pin is enabled in the Quartus II designs. When not using as the dedicated INIT_DONE optionally open-drain output, and when this pin is not used as an I/O pin, then connect this pin as defined in the Quartus II software. In the active serial multi-device configuration mode, do not tie the INIT_DONE pin together with other devices. Tie the INIT_DONE pin independently to a pull-up resistor.

Arria V GZ Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin.	If the CLKUSR pin is not used as a configuration clock input and the pin is not used as an I/O then it is recommended to connect this pin to ground.
nPERSTL0	I/O, Input	Dedicated Fundamental Reset pin is only available when used in conjunction with PCIe HIP. When low the transcievers are in reset. When high the transcievers are out of reset. When this pin is not used as the fundamental reset, this pin may be used as a user I/O.	Connect this pin as defined in the Quartus II software. You may drive this pin by 3.3V regardless of the VCCIO voltage level of the bank without a level translator as long as: • the input signal meets the LVTTL VIH/VIL specification, and • as long as it meets the overshoot specifications for 100% operation as listed in the Arria V device datasheet. Only one nPERST pin is used per PCIe HIP. nPERSTL0 = Bottom Left PCIe HIP.
AS_DATA0 / ASDO	Bidirectional	Dedicated AS configuration pin. When using an EPCS device (x1 mode) this is the ASDO pin and used to send address and control signals between the FPGA and the EPCS/EPCQ.	When not programming the device in AS mode ASDO is not used. Also, when this pin is not used it is recommended to leave the pin unconnected.
AS_DATA[1:3]	Bidirectional	Dedicated AS configuration data pins. Configuration data is transported on these pins when connected to the EPCQ devices.	When this pin is not used it is recommended to leave the pin unconnected.
Partial Reconfiguration Pins			
PR_REQUEST	I/O, Input	Partial Reconfiguration Request pin. Drive this pin high to start partial reconfiguration. Drive this pin low to end reconfiguration. This pin can only be used in Partial Reconfiguration using external host mode in FPP x16 configuration scheme.	When the dedicated input PR_REQUEST is not used and this pin is not used as an I/O, then it is recommended to tie this pin to GND.
PR_READY	I/O, Output or Output (open-drain)	The partial reconfiguration ready pin is driven low until the device is ready to begin partial reconfiguration. When the device is ready to start reconfiguration, this signal is released and is pulled high by an external pull-up resistor.	When using as optionally open-drain output dedicated PR_READY pin, connect this pin to an external 10-kΩ pull-up resistor to VCCPGM. When not using as the dedicated PR_READY optionally open-drain output, and when this pin is not used as an I/O pin, then connect this pin as defined in the Quartus II software.
PR_ERROR	I/O, Output or Output (open-drain)	The partial reconfiguration error pin is driven low during partial reconfiguration unless the device detects an error. If an error is detected, this signal is released and pulled high by an external pull-up resistor.	When using as optionally open-drain output dedicated PR_ERROR pin, connect this pin to an external 10-kΩ pull-up resistor to VCCPGM. When not using as the dedicated PR_ERROR optionally open-drain output, and when this pin is not used as an I/O pin, then connect this pin as defined in the Quartus II software.

Arria V GZ Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
PR_DONE	I/O, Output or Output(open-drain)	The partial reconfiguration done pin is driven low until the partial reconfiguration is complete. When the reconfiguration is complete, this signal is released and is pulled high by an external pull-up resistor.	When using as optionally open-drain output dedicated PR_DONE pin, connect this pin to an external 10-kΩ pull-up resistor to VCCPGM. When not using as the dedicated PR_DONE optionally open-drain output, and when this pin is not used as an I/O pin, then connect this pin as defined in the Quartus II software.
CvP_CONFDONE	I/O, Output (open-drain)	Configuration Via Protocol Done pin is driven low during configuration. When configuration via PCIe is complete, this signal is released and is pulled high by an external pull-up resistor. Status of this pin is only valid if CONF_DONE is high.	When using as optionally open-drain output dedicated CvP_CONFDONE pin, connect this pin to an external 10-kΩ pull-up resistor to VCCPGM. When not using as the dedicated CvP_CONFDONE optionally open-drain output, and when this pin is not used as an I/O pin, then connect this pin as defined in the Quartus II software.
Differential I/O Pins			
DIFFIO_RX_[T,B][#:#]p, DIFFIO_RX_[T,B][#:#]n	I/O, RX channel	These are true LVDS receiver channels on row and column I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins. OCT Rd is supported on all DIFFIO_RX pins when VCCPD is 2.5V.	Connect unused pins as defined in Quartus II software.
DIFFIO_TX_[T,B][#:#]p, DIFFIO_TX_[T,B][#:#]n	I/O, TX channel	These are true LVDS transmitter channels on side I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.	Connect unused pins as defined in Quartus II software.
DIFFOUT_[T,B][##]p, DIFFOUT_[T,B][##]n	I/O, TX channel	These are emulated LVDS output channels. All user I/Os, including I/Os with true LVDS input buffers, can be configured as emulated LVDS output buffers. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.	Connect unused pins as defined in Quartus II software.

Arria V GZ Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
External Memory Interface Pins			
DQS[1:66]T, DQS[1:70]B	I/O,DQS	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry. The shifted DQS signal can also drive to internal logic.	Connect unused pins as defined in Quartus II software. See Note 11.
DQSn[1:66]T, DQSn[1:70]B	I/O,DQSn	Optional complementary data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry.	Connect unused pins as defined in Quartus II software. See Note 11.
DQ[1:66]T, DQ[1:70]B	I/O,DQ	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important; however, use caution when making pin assignments if you plan on migrating to a different memory interface that has a different DQ bus width. Analyze the available DQ pins across all pertinent DQS columns in the pin list.	Connect unused pins as defined in Quartus II software. See Note 11.
CQ[1:27]T, CQ[1:29]B	DQS	Optional data strobe signal for use in QDRII SRAM. These are the pins for echo clocks.	Connect unused pins as defined in Quartus II software. See Note 12.
CQn[1:27]T, CQn[1:29]B	DQS	Optional complementary data strobe signal for use in QDRII SRAM. These are the pins for echo clocks.	Connect unused pins as defined in Quartus II software. See Note 12.
Reference Pins			
RREF_[T,B][L,R]	Input	Reference resistor for transceiver, specific to the left (L) side or right (R) side of the device.	If any PLL, REFCLK pin, or transceiver channel on one side (left or right) of the device is used, you must connect each RREF pin on that side of the device to its own individual 1.8kΩ +/- 1% resistor to GND. Otherwise, you may connect each RREF pin on that side of the device directly to GND. In the PCB layout, the trace from this pin to the resistor needs to be routed so that it avoids any aggressor signals.
RZQ_[#]	I/O, Input	Reference pins for I/O banks. The RZQ pins share the same VCCIO with the I/O bank where they are located. The external precision resistor must be connected to the designated pin within the bank. If not required, this pin is a regular I/O pin.	When the device does not use this dedicated input for the external precision resistor or as an I/O it is recommended that you connect the pin to GND. When using OCT tie these pins to GND through either a 240W or 100W resistor, depending on the desired OCT impedence. Refer to the Arria V handbook for the OCT impedence options for the desired OCT scheme.

Arria V GZ Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
DNU	Do Not Use	Do Not Use (DNU).	Do not connect to power, ground or any other signal. You must leave these pins floating.
NC	No Connect	Do not drive signals into these pins.	When designing for device migration you may connect these pins to power, ground, or a signal trace depending on the pin assignment of the devices selected for migration. However, if device migration is not a concern leave these pins floating.
Supply Pins (See Notes 4 through 7)			
VCC	Power	VCC supplies power to the core and periphery.	VCC is 0.85V. Connect all VCC pins to a low noise switching regulator. When VCCHIP and VCCHSSI are used, tie these pins to the same plane as VCC. For data rates less than 6.5 Gbps and with a proper isolation filter, you may source VCCR_GXB and VCCT_GXB from the same regulator as VCC when the power rails require the same voltage level. Use the Arria V Early Power Estimator to determine the current requirements for VCC and other power supplies. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 2, 3, 4, and 6.
VCCD_FPLL	Power	PLL digital power.	Connect all VCCD_FPLL pins to a 1.5V linear or low noise switching power supply. You may tie these pins to the same regulator as VCCPT, VCCBAT, and VCCH_GXB. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 2, 3, and 4.
VCCPT	Power	Power supply for the programmable power technology.	Connect all VCCPT pins to a 1.5V linear or low noise switching power supply. You may tie these pins to the same regulator as VCCD_FPLL, VCCBAT and VCCH_GXB. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 2, 3, 4 and 7.
VCCA_FPLL	Power	PLL analog power.	Connect these pins to a 2.5V low noise switching power supply through a proper isolation filter. You may share this power rail with VCC_AUX. With a proper isolation filter you may source these pins from the same regulator as VCCIO, VCCPD and VCCPGM when each of these power supplies require 2.5V. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 2, 3, 4, and 7.

Arria V GZ Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
VCC_AUX	Power	Auxiliary supply for the programmable power technology.	Connect all VCC_AUX pins to a 2.5V low noise switching power supply through a proper isolation filter. You may share this power rail with VCCA_FPLL. With a proper isolation filter you may source these pins from the same regulator as VCCIO, VCCPD and VCCPGM when each of these power supplies require 2.5V. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 2, 3, 4, and 7.
VCCIO[3,4,7,8][A,B,C,D]	Power	These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. supported VCCIO standards include LVDS, LVCMOS(3.0V), HSTL(12, 15, 18), SSTL(12, 125, 135, 15, 18, 2), LVTTL (3.0V), HSUL(12), LVPECL(2.5V),1.2V, 1.5V, 1.8V, 2.5V I/O standards.	Connect these pins to 1.2V, 1.25V, 1.35V, 1.5V, 1.8V, 2.5V or 3.0V supplies, depending on the I/O standard connected to the specified bank. When these pins require the same voltage level as VCCPD and/or VCCPGM, you may tie them to the same regulator as VCCPD and/or VCCPGM, but only if each of these supplies requires the same voltage level. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 2, 3, 4, and 8.
VCCPGM	Power	Configuration pins power supply.	Connect these pins to either 1.8V, 2.5V or 3.0V power supply. When these pins require the same voltage level as VCCPD and/or VCCIO, you may tie them to the same regulator as VCCPD and/or VCCIO, but only if each of these supplies requires the same voltage level. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 2, 3, and 4.
VCCPD3[AB][CD] VCCPD[4,7,8]	Power	Dedicated power pins. This supply is used to power the I/O pre-drivers. This can be connected to 2.5V or 3.0V. For 1.2V, 1.25V, 1.35V, 1.5V, 1.8V or 2.5V I/O standards connect VCCPD to 2.5V and for 3.0V I/O standard connect VCCPD to 3.0V.	The VCCPD pins require 2.5V or 3.0V. When these pins have the same voltage requirements as VCCPGM and VCCIO, you may tie them to the same regulator. The voltage on VCCPD is dependent on the VCCIO voltage. When VCCIO is 3.0V, VCCPD must be 3.0V. When VCCIO is 2.5V or less, VCCPD must be 2.5V. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 2, 3, 4, and 8. For details about VCCPD pin sharing for VCCIO groups, refer to the I/O Design Guidelines section in the I/O Features in Arria V Devices chapter.
VCCBAT	Power	Battery back-up power supply for design security volatile key register.	Connect this pin to a non-volatile battery power source in the range of 1.2V - 3.0V when using design security volatile key. In this case, do not connect this pin to a volatile power source on the board. 3.0V is the typical battery power selected for this supply. When not using the volatile key, tie this to a 1.5V, 2.5V or 3.0V supply. Arria V devices will not exit POR if VCCBAT is not powered up.

Arria V GZ Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
GND	Ground	Device ground pins.	You must connect all GND pins to the board ground plane.
VREF[3,4,7,8][A,B,C,D]N0	Power	Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for the bank.	If VREF pins are not used, you should connect them to either the VCCIO in the bank in which the pin resides or GND. Decoupling depends on the design decoupling requirements of the specific board. See Note 2 and 8.
Transceiver Pins (See Notes 4 through 10)			
VCCHIP_L	Power	PCIe Hard IP digital power supply, specific to the left (L) side the device.	VCCHIP is 0.85V. When VCCHIP is used, tie it to the same plane as VCC. When you do not use the device's HIP, you may connect VCCHIP pins to GND. For data rates less than 6.5Gbps and with a proper isolation filter, you may source VCCR_GXB and VCCT_GXB from the same regulator as VCC, VCCHIP, and VCCHSSI. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 2, 3, 4, and 5.
VCCHSSI_[L,R]	Power	PCS power supply, specific to the left (L) side or right (R) side of the device.	VCCHSSI is 0.85V. When VCCHSSI is used, tie it to the same plane as VCC. When you do not use any of the transceivers on one side of the device, you may tie VCCHSSI on that side of the device to GND. For data rates less than 6.5Gbps and with a proper isolation filter, you may source VCCR_GXB and VCCT_GXB from the same regulator as VCC, VCCHIP, and VCCHSSI. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 2, 3, 4, and 5.

Arria V GZ Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
VCCR_GXB[L,R][0:2]	Power	Analog power, receiver, specific to the left (L) side or right (R) side of the device.	Connect VCCR_GXB pins to a linear or low noise switching regulator. Set VCCR_GXB and VCCT_GXB to either 1.0V, or to match the VCC of the device. Set VCCR_GXB and VCCT_GXB to 1.0V when: • ATX PLL is used, the CMU data rate is > 6.5Gbps, or • DFE/AEQ/EyeQ are used, or • Provisions are made to use any of the above capabilities in the future If the above features are not used, and when there is no future provision to use them, you can set VCCR_GXB and VCCT_GXB to the same level as VCC or to 1.0V. Ensure that the choice you make for VCCR_GXB and VCCT_GXB tracks the choice made for VCCA_GXB as follows: • VCCR_GXB/VCCT_GXB = VCC and VCCA_GXB = 2.5V, or • VCCR_GXB/VCCT_GXB = 1.0V and VCCA_GXB = 3.0V For data rates less than 6.5Gbps and ATX PLL, DFE, AEQ, or EyeQ is not used, you may tie these pins to the same regulator as VCC, VCCHIP and VCCHSSI with a proper isolation filter. For data rates greater than 10.3Gbps and DFE is used, you must connect VCCR_GXB and VCCT_GXB to 1.05V +/-20mV. For data rates less than 12.5Gbps these pins may share the same power rail as VCCT_GXB. However, for better performance you should isolate VCCR_GXB and VCCT_GXB by at least 60dB for a 1MHz to 100MHz bandwidth. Decoupling for these pins depends on the design decoupling requirements of the specific board design. See Notes 2, 3, 4, 5, 7, and 10.

Arria V GZ Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
VCCT_GXB[L,R][0:2]	Power	Analog power, transmitter, specific to the left (L) side or right (R) side of the device.	Connect VCCT_GXB pins to a linear or low noise switching regulator. Set VCCR_GXB and VCCT_GXB to either 1.0V, or to match the VCC of the device. Set VCCR_GXB and VCCT_GXB to 1.0V when: • ATX PLL is used, the CMU data rate is > 6.5Gbps, or • DFE/AEQ/EyeQ are used, or • Provisions are made to use any of these capabilities in the future If the above features are not used, and when there is no future provision to use them, you can set VCCR_GXB and VCCT_GXB to the same level as VCC, or to 1.0V. Ensure that the choice you make for VCCR_GXB and VCCT_GXB tracks the choice made for VCCA_GXB as follows: • VCCR_GXB/VCCT_GXB = VCC and VCCA_GXB = 2.5V, or • VCCR_GXB/VCCT_GXB = 1.0V and VCCA_GXB = 3.0V For data rates less than 6.5Gbps and ATX PLL, DFE, AEQ, or EyeQ is not used, you may tie these pins to the same regulator as VCC, VCCHIP and VCCHSSI with a proper isolation filter. For data rates >10.3Gbps and DFE is used, you must connect VCCT_GXB and VCCR_GXB to 1.05V +/-20mV. For data rates less than 12.5Gbps these pins may share the same power rail as VCCR_GXB. However, for better performance you should isolate VCCR_GXB and VCCT_GXB by at least 60dB for a 1MHz to 100MHz bandwidth. Decoupling for these pins depends on the design decoupling requirements of the specific board design. See Notes 2, 3, 4, 5, 7, and 10.
VCCH_GXB[L,R][0:2]	Power	Analog power, block level TX buffers.	Connect VCCH_GXB to a 1.5V linear or low noise switching regulator. You may source these pins from the same regulator as VCCPT, VCCD_FPLL and VCCBAT. Decoupling for these pins depends on the design decoupling requirements of the specific board design. See Notes 2, 3, 4, 5, 7, and 10.

Arria V GZ Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
VCCA_GXB[L,R][0:2]	Power	Analog power, TX driver, RX receiver, CDR, specific to the left (L) side or right (R) side of the device.	Use a linear or low noise switching regulator to supply power to this power plane. Set VCCA_GXB to either 2.5V or 3.0V. Set VCCA_GXB to 3.0V when: • ATX PLL is used, the CMU data rate is > 6.5Gbps, or • DFE/AEQ/EyeQ are used, or • Provisions are made to use any of these capabilities in the future If the above features are not used, and when there is no future provision to use them, you can set VCCA_GXB to 2.5V or 3.0V Ensure that the choice you make for VCCA_GXB must track the choice you make for VCCR_GXB and VCCT_GXB as follows: • VCCR_GXB/VCCT_GXB = VCC and VCCA_GXB = 2.5V, or • VCCR_GXB/VCCT_GXB = 1.0V and VCCA_GXB = 3.0V This power rail may be shared with VCCA_FPLL and VCC_AUX. With a proper isolation filter you may source these pins from the same regulator as VCCIO, VCCPD and VCCPGM when each of these power supplies require 2.5V. Decoupling depends on the design decoupling requirements of the specific board design. See Notes 2, 3, 5, 7, and 10.
GXB_RX_[L,R][0:17]p, GXB_REFCLK[L,R][0:17]p	Input	High speed positive differential receiver channels. Specific to the left (L) side or right (R) side of the device.	These pins may be AC-coupled or DC-coupled when used. Connect all unused GXB_RXp/GXB_REFCLKp pins directly to GND or VCCR_GXB or VCCT_GXB. See Note 9.
GXB_RX_[L,R][0:17]n, GXB_REFCLK[L,R][0:17]n	Input	High speed negative differential receiver channels. Specific to the left (L) side or right (R) side of the device.	These pins may be AC-coupled or DC-coupled when used. Connect all unused GXB_RXn/GXB_REFCLKn pins directly to GND. See Note 9.
GXB_TX_[L,R][0:17]p	Output	High speed positive differential transmitter channels. Specific to the left (L) side or right (R) side of the device.	Leave all unused GXB_TXp pins floating.
GXB_TX_[L,R][0:17]n	Output	High speed negative differential transmitter channels. Specific to the left (L) side or right (R) side of the device.	Leave all unused GXB_TXn pins floating.
REFCLK_ [0:5] [L,R]p	Input	High speed differential reference clock positive receiver channels, specific to the left (L) side or right (R) side of the device.	In the PCI Express configuration, DC-coupling is allowed on the REFCLK if the selected REFCLK I/O standard is HCSL. These pins must be AC-coupled if the selected REFCLK I/O standard is not HCSL. See Note 9 for non-HCSL I/O standard. Connect all unused pins directly to GND.

Arria V GZ Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
REFCLK_ [0:5] [L,R]n	Input	High speed differential reference clock complement, complementary receiver channel, specific to the left (L) side or right (R) side of the device.	In the PCI Express configuration, DC-coupling is allowed on the REFCLK if the selected REFCLK I/O standard is HCSL. These pins must be AC-coupled if the selected REFCLK I/O standard is not HCSL. See Note 9 for non-HCSL I/O standard. Connect all unused pins directly to GND.

Notes to Arria V GZ Pin Connection Guidelines

Altera provides these guidelines only as recommendations. It is the responsibility of the designer to apply simulation results to the design to verify proper device functionality.

1. These pin connection guidelines are created based on the Arria V GZ device family.
2. Capacitance values for the power supply should be selected after consideration of the amount of power they need to supply over the frequency of operation of the particular circuit being decoupled. A target impedance for the power plane should be calculated based on current draw and voltage droop requirements of the device/supply. The power plane should then be decoupled using the appropriate number of capacitors. On-board capacitors do not decouple higher than 100 MHz because "Equivalent Series Inductance" of the mounting of the packages. Proper board design techniques such as interplane capacitance with low inductance should be considered for higher frequency decoupling.
3. Use the Arria V Early Power Estimator to determine the current requirements for VCC and other power supplies.
4. These supplies may share power planes across multiple Arria V devices.
5. Examples 1 - 3 and Figures 1 - 3 illustrate power supply sharing guidelines that are data rate dependent.
   - Example 1 and Figure 1, ""Power Regs <= 6.5Gbps"", show recommendations for designs using the Arria V GZ transceivers that will not exceed 6.5Gbps option 1.
   - Example 2 and Figure 2, ""Power Regs <= 6.5Gbps"", show recommendations for designs using the Arria V GZ transceivers that will not exceed 6.5Gbps option 2.
   - Example 3 and Figure 3, ""Power Regs > 6.5Gbps <= 12.5Gbps"", show recommendations for designs using the Arria V GZ transceivers that are between 6.5Gbps and 12.5Gbps.
6. Power pins should not share breakout vias from the BGA. Each ball on the BGA needs to have its own dedicated breakout via. VCC must not share breakout vias.
7. Low Noise Switching Regulator - defined as a switching regulator circuit encapsulated in a thin surface mount package containing the switch controller, power FETs, inductor, and other support components. The switching frequency is usually between 800kHz and 1MHz and has fast transient response. The switching frequency range is not an Altera requirement. However, Altera does require the Line Regulation and Load Regulation meet the following specifications:
   - Line Regulation < 0.4%
   - Load Regulation < 1.2%
   You have the option to use a linear regulator depending on your design and your system's power and thermal budget considerations.
8. The number of modular I/O banks on Arria V GZ devices depends on the device density. For the indexes available for a specific device, please refer to the I/O Bank section in the Arria V device handbook.
9. For AC-coupled links, the AC-coupling capacitor can be placed anywhere along the channel. PCI Express protocol requires the AC-coupling capacitor to be placed on the transmitter side of the interface that permits adapters to be plugged and unplugged.
10. All transceiver power pins on the same side of the device must be connected either to the required supply or to GND. When ALL transceiver channels on the same side are unused, you have the option to connect all of the transceiver power pins on the same side of the device to GND or to the required supply.
11. For DQS, DQSn, and DQ groups, group 31B to group 42B, group 3T and 4T, and group 29T to group 40T are unavailable.
12. For CQ and CQn groups, group 2T is unavailable.

Power Reqs ≤ 6.5Gbps Option 1

Example 1. Power Supply Sharing Guidelines for Arria V GZ Transceivers with Data Rates <= 6.5Gbps, and all of the following conditions are true:
ATX PLL is not being used, DFE/AEQ/EyeQ are not being used, and no provision is being made to use any of these features in the future (Option 1)
Example Requiring 3 Power Regulators

| Power Pin Name	Regulator Count	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC VCCHIP_L VCCHSSI_[L,R]	1	0.85	± 30mV	Switcher (*)	Share	VCC, VCCHIP, and VCCHSSI must share regulators. If not using HIP, VCCHIP may be tied to GND. Also, when you do not use any of the transceivers on one side of the device, VCCHSSI on that side of the device may be tied to GND.
VCCR_GXB[L,R] VCCT_GXB[L,R]					Isolate	May be able to share VCCR_GXB and VCCT_GXB with VCC, VCCHIP, and VCCHSSI with a proper isolation filter.
VCCIO VCCPD VCCPGM	2	Varies	± 5%	Switcher (*)	Share if 2.5V	If all of these supplies require 2.5V and the regulator selected satisfies the power specifications, these supplies may all be tied in common. However, for any other voltage you will require as many regulators as there are variations of supplies in your specific design. VCCPD must be greater than or equal to VCCIO. Use the EPE tool to assist in determining the power required for your specific design.
VCC_AUX VCCA_GXB[L,R] VCCA_FPLL		2.5			Isolate	May be able to share VCCA_GXB, VCC_AUX, and VCCA_FPLL with the same regulator as VCCIO, VCCPD, and VCCPGM when all power rails require 2.5V, but only with a proper isolation filter. Depending on the regulator capabilities, this supply may be shared with multiple Arria V GZ devices.
VCCPT VCCH_GXB[L,R] VCCD_FPLL VCCBAT	3	1.5	± 50mV	Linear or Switcher (*)	Share	If not sharing a regulator, the VCCPT supply should not exceed a tolerance of ± 50mV, however the other power supplies in this group can tolerate ± 5%. Depending on the regulator capabilities this supply may be shared with multiple Arria V GZ devices.

(*) When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 7.
Use the EPE (Early Power Estimation) tool to assist in determining the power required for your specific design.
Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Arria V GZ transceiver-based device with data rates less than or equal to 6.5Gbps is provided in Figure 1.

Refer to power up sequence recommendation in Arria V Devices Handbook: Power Managament in Arria V Devices.

Figure 1. Example Power Supply Block Diagram for Arria V GZ Transceivers with Data Rates <= 6.5Gbps, and all of the following conditions are true: ATX PLL is not being used, DFE/AEQ/EyeQ are not being used, and no provision is being made to use any of these features in the future (Option 1)
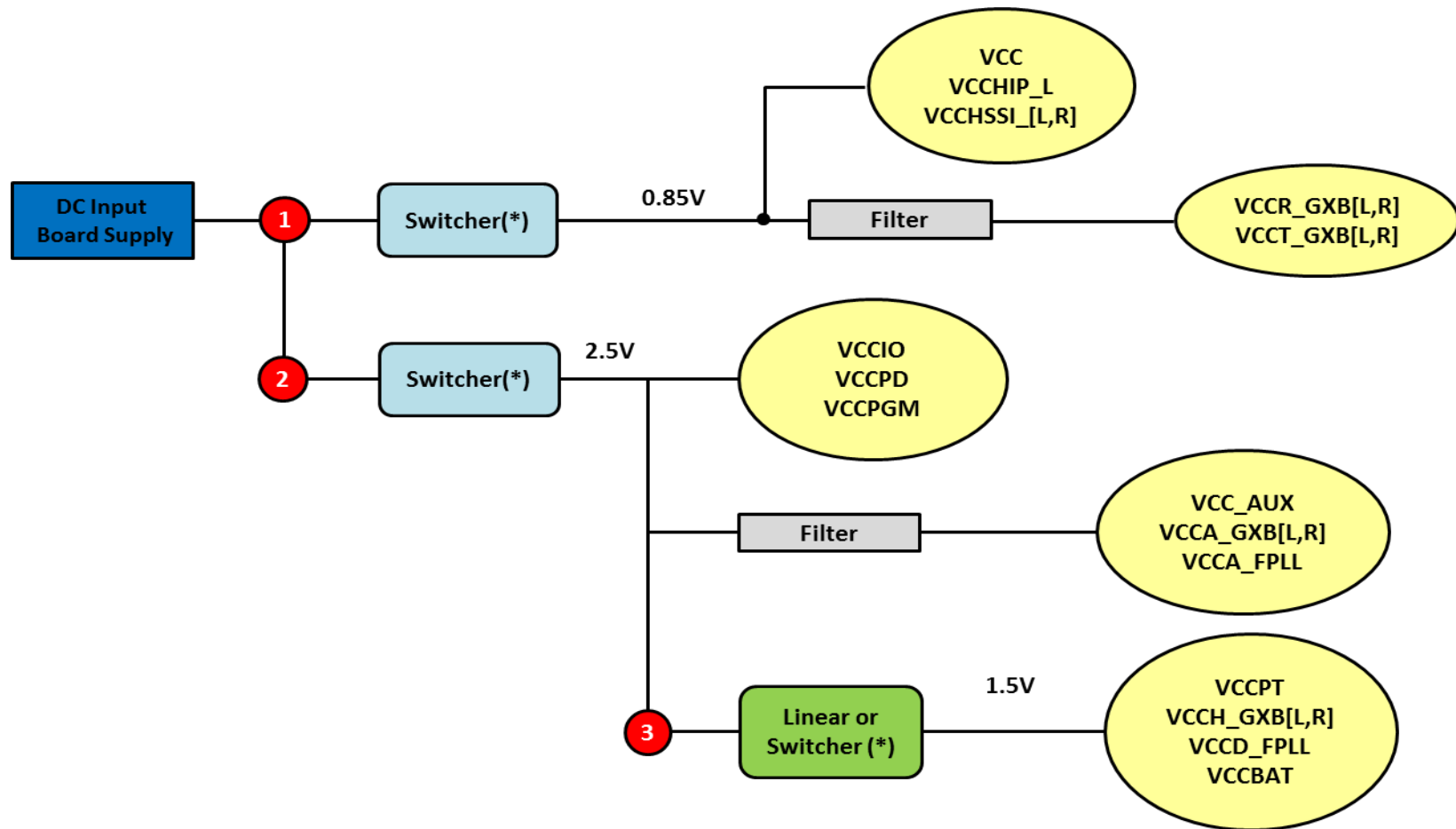
*When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 7.
Refer to power up sequence recommendation in Arria V Devices Handbook: Power Managament in Arria V Devices.

Power Reqs ≤ 6.5Gbps Option 2

Example 2. Power Supply Sharing Guidelines for Arria V GZ Transceivers with Data Rates <= 6.5Gbps, and at least one of the following conditions is true:
ATX PLL is being used, DFE/AEQ/EyeQ are being used, or provision is being made to use any of these features in the future (Option 2)
Example Requiring 5 Power Regulators

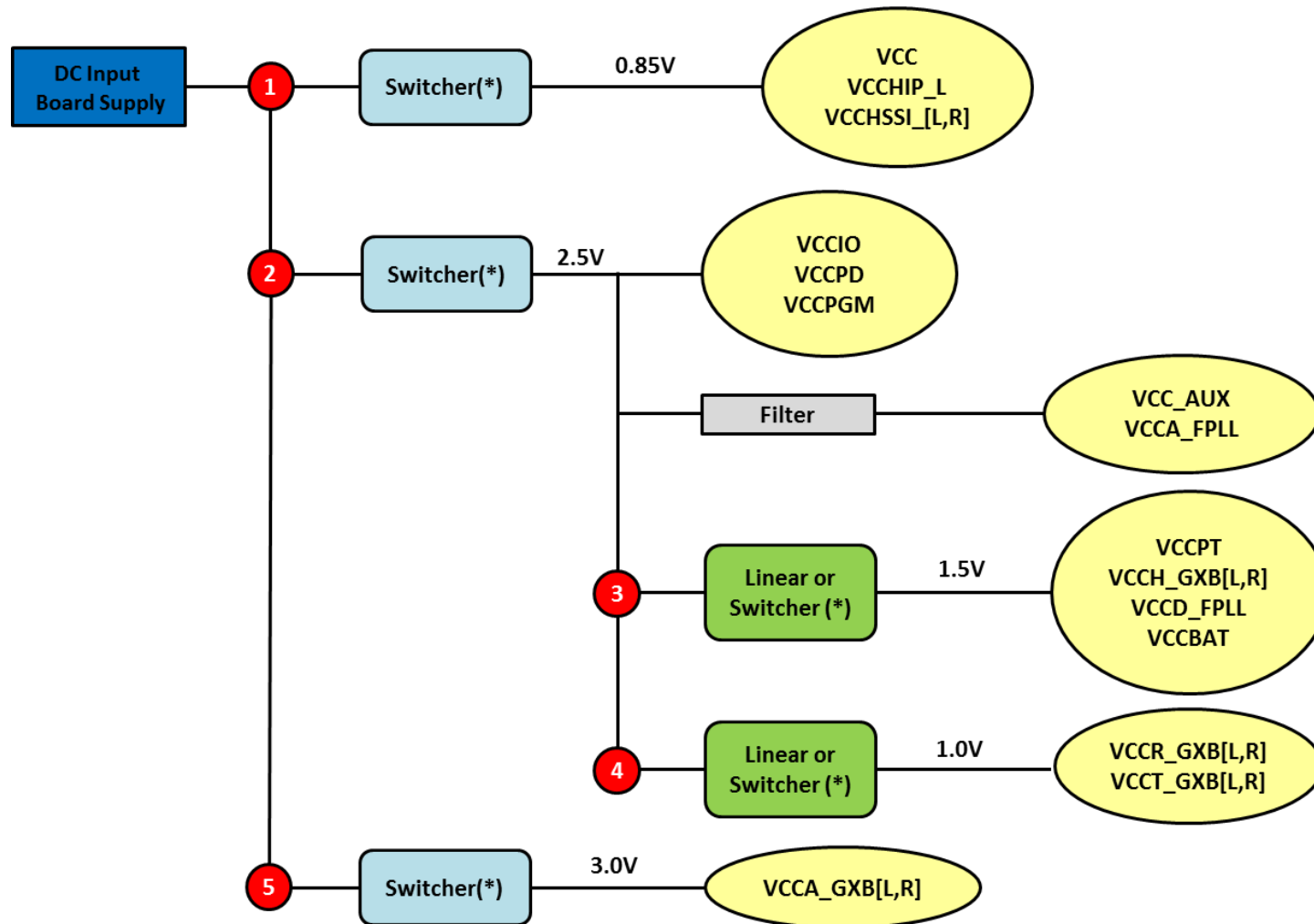| Power Pin Name	Regulator Count	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC VCCHIP_L VCCHSSI_[L,R]	1	0.85	± 30mV	Switcher (*)	Share	VCC, VCCHIP, and VCCHSSI must share regulators. If not using HIP, VCCHIP may be tied to GND. Also, when you are not using any of the transceivers on one side of the device, VCCHSSI on that side of the device may be tied to GND.
VCCR_GXB[L,R] VCCT_GXB[L,R]	2	1.0	± 30mV	Linear or Switcher (*)	Isolate	
VCCIO VCCPD VCCPGM	3	Varies	± 5%	Switcher (*)	Share if 2.5V	If all of these supplies require 2.5V and the regulator selected satisfies the power specifications then these supplies may all be tied in common. However, for any other voltage you will require as many regulators as there are variations of supplies in your specific design. VCCPD must be greater than or equal to VCCIO. Use the EPE tool to assist in determining the power required for your specific design.
VCC_AUX VCCA_FPLL		2.5				May be able to share VCC_AUX and VCCA_FPLL with the same regulator as VCCIO, VCCPD, and VCCPGM when all power rails require 2.5V, but only with a proper isolation filter. Depending on the regulator capabilities this supply may be shared with multiple Arria V GZ devices.
VCCA_GXB[L,R]	4	3.0	± 5%	Linear or Switcher (*)	Isolate	
VCCPT VCCH_GXB[L,R] VCCD_FPLL VCCBAT	5	1.5	± 50mV	Linear or Switcher (*)	Share	If not sharing a regulator, the VCCPT supply should not exceed a tolerance of ± 50mV, however the other power supplies in this group can tolerate ± 5%. Depending on the regulator capabilities this supply may be shared with multiple Arria V GZ devices.

(*) When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 7.
Use the EPE (Early Power Estimation) tool to assist in determining the power required for your specific design.
Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Arria V GZ transceiver-based device with data rates less than or equal to 6.5Gbps is provided in Figure 2.
Refer to power up sequence recommendation in Arria V Devices Handbook: Power Managament in Arria V Devices.

Figure 2. Example Power Supply Block Diagram for Arria V GZ Transceivers with Data Rates <= 6.5Gbps, and at least one of the following conditions is true: ATX PLL is being used, DFE/AEQ/EyeQ are being used, or provision is being made to use any of these features in the future (Option 2)

*When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 7.
Refer to power up sequence recommendation in Arria V Devices Handbook: Power Managment in Arria V Devices.

Power Regs > 6.5Gbps ≤ 12.5Gbps

Example 3. Power Supply Sharing Guidelines for Arria V GZ Transceivers with Data Rates Between 6.5Gbps and 12.5Gbps

Example Requiring 5 Power Regulators

| Power Pin Name	Regulator Count	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC VCCHIP_L VCCHSSI_[L,R]	1	0.85	± 30mV	Switcher (*)	Share	VCC, VCCHIP, and VCCHSSI must share regulators. If not using HIP, VCCHIP may be tied to GND. Also, when you are not using any of the transceivers on one side of the device, VCCHSSI on that side of the device may be tied to GND.
VCCIO VCCPD VCCPGM	2	Varies	± 5%	Switcher (*)	Share if 2.5V	If all of these supplies require 2.5V and the regulator selected satisfies the power specifications then these supplies may all be tied in common. However, for any other voltage you will require as many regulators as there are variations of supplies in your specific design. VCCPD must be greater than or equal to VCCIO. Use the EPE tool to assist in determining the power required for your specific design.
VCC_AUX VCCA_FPLL		2.5			Isolate	May be able to share VCC_AUX and VCCA_FPLL with the same regulator as VCCIO, VCCPD, and VCCPGM when all power rails require 2.5V, but only with a proper isolation filter. Depending on the regulator capabilities this supply may be shared with multiple Arria V GZ devices.
VCCR_GXB[L,R] VCCT_GXB[L,R]	3	1.0 or 1.05 (**)	± 30mV or ± 20mV (**)	Linear or Switcher (*)	Share	Although VCCR_GXB and VCCT_GXB may share a regulator, for a better performance and to meet PCIe Gen. 3 jitter specifications, these power supplies should be isolated from each other with at least 60dB of isolation for a 1MHz to 100MHz bandwidth.
VCCPT VCCH_GXB[L,R] VCCD_FPLL VCCBAT	4	1.5	± 50mV	Linear or Switcher (*)	Share	If not sharing a regulator, the VCCPT supply should not exceed a tolerance of ± 50mV, however the other power supplies in this group can tolerate ± 5%. Depending on the regulator capabilities this supply may be shared with multiple Arria V GZ devices.
VCCA_GXB[L,R]	5	3.0	± 5%	Linear or Switcher (*)	Isolate	

(*) When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 7.
 (**) When data rate is >10.3Gbps and DFE is used.
Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Arria V GZ transceiver-based device with data rates between 6.5Gbps and 12.5Gbps is provided in Figure 3.
Refer to power up sequence recommendation in Arria V Devices Handbook: Power Managment in Arria V Devices.

Figure 3. Example Power Supply Block Diagram for Arria V GZ Transceivers with Data Rates Between 6.5Gbps and 12.5Gbps
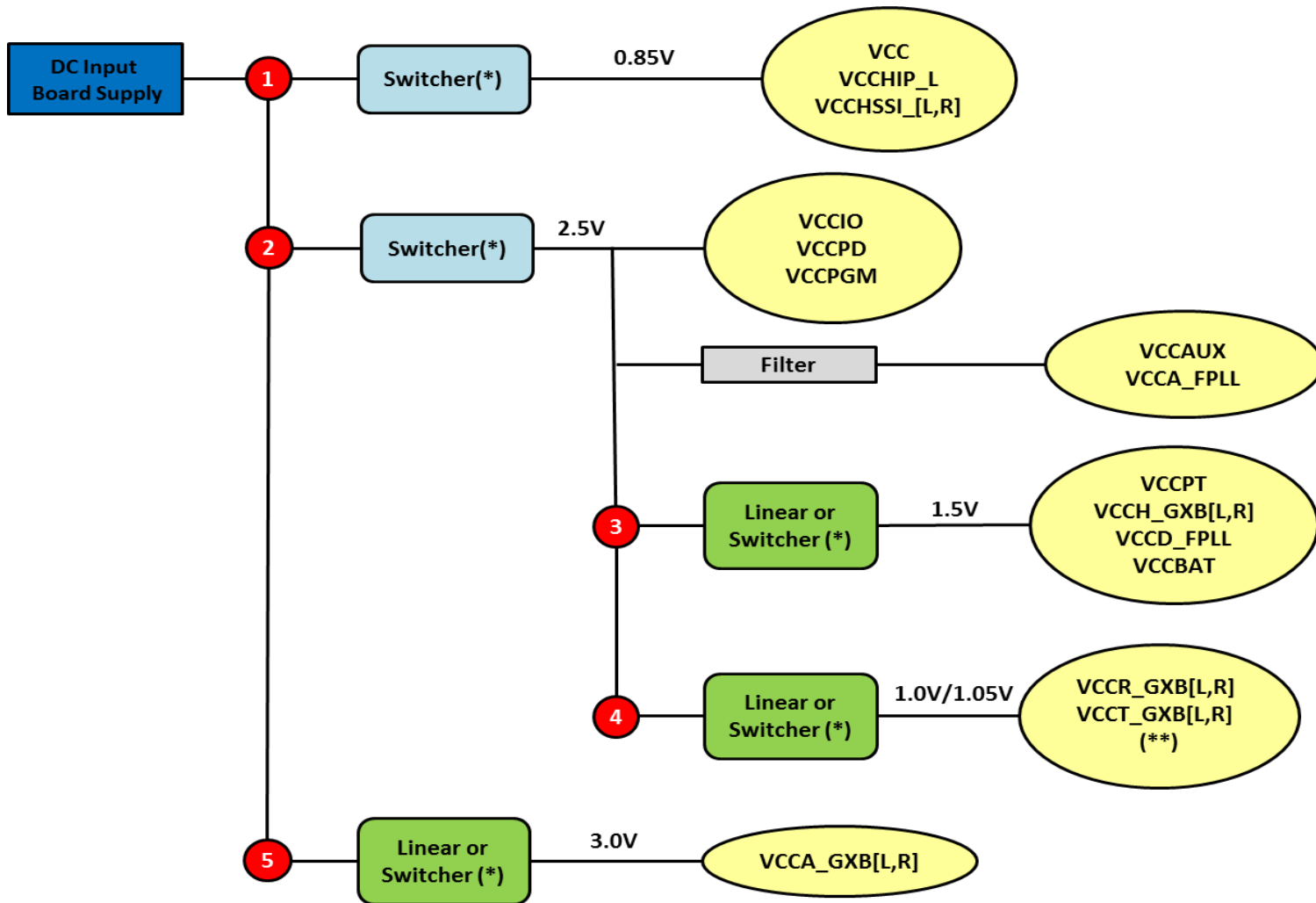
*When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 7.
***Although VCCR_GXB and VCCT_GXB may share a regulator, for better performance these power supplies should be isolated from each other with at least 60dB of isolation for 1MHz o 100MHz bandwidth.
Refer to power up sequence recommendation in Arria V Devices Handbook: Power Managament in Arria V Devices.

Revision History

Revision	Description of Changes	Date
1.0	Initial release.	11/19/2012
1.1	- Added note (4) to VCC, VCCD_FPLL, VCCIO[1:8], VCCPGM, VCCPD[1:8], VCCHIP_L, and VCCHSSI_[L,R] pins. - Added note (5) to VCCA_GXB[L,R][0:2], VCCH_GXB[L,R][0:2], VCCT_GXB[L,R][0:2], VCCR_GXB[L,R][0:2], VCCHIP_L, and VCCHSSI_[L,R] pins. - Added note (11) to DQS, DQSn, and DQ pins. - Added note (12) to CQ and CQn pins. - Updated notes (7) and (10) in the Pin Connection Guidelines. - Updated the connection guidelines to nIO_PULLUP, REFCLK_[L,R][0:5]p, REFCLK_[L,R][0:5]n, VCCR_GXB[L,R][0:2], and VCCT_GXB[L,R][0:2] pins. - Moved the RREF_[T,B][L,R] pin to the Reference Pins section.	4/19/2013
1.2	- Updated the pin description of the DIFFIO_RX_[T,B][#:#]p and DIFFIO_RX_[T,B][#:#]n pins. - Updated the connection guidelines to the TMS, TDI, TRST, REFCLK_ [0:5] [L,R]p, and REFCLK_ [0:5] [L,R]n pins. - Updated note (10) in the Pin Connection Guidelines.	10/7/2013
1.3	-This document is no longer preliminary. -Updated the connection guidelines of the VCCBAT pin. -Updated the connection guidelines of REFCLK_ [0:5] [L,R]p and REFCLK_ [0:5] [L,R]n pins.	11/14/2014
1.4	-Updated content in the Disclaimer section. -Added links referring to Arria V Device Handbook: Power Management in Arria V Devices for all power sharing guidelines tables and figures.	5/19/2015