Stratix IV Device Handbook

Volume 3: Transceiver Configuration Guide

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Contents

Chapter 3. ALTGX_RECONFIG Megafunction User Guide for Stratix IV Devices

Additional Information

Chapter Revision Dates

The chapters in this document, *Stratix IV Device Handbook Volume 3*, were revised on the following dates. Where chapters or groups of chapters are available separately, part numbers are listed.

Chapter 1. ALTGX Transceiver Setup Guide for Stratix IV Devices
Revised: *January 2014*
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Chapter 2. Transceiver Design Flow Guide for Stratix IV Devices
Revised: *February 2011*
Part Number: *SIV53002-4.1*

Chapter 3. ALTGX_RECONFIG Megafunction User Guide for Stratix IV Devices
Revised: *February 2011*
Part Number: *SIV53004-3.1*

Section I. Transceiver Configuration Guide

This section includes the following chapters:

- Chapter 1, ALTGX Transceiver Setup Guide for Stratix IV Devices
- Chapter 2, Transceiver Design Flow Guide for Stratix IV Devices
- Chapter 3, ALTGX_RECONFIG Megafunction User Guide for Stratix IV Devices

Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the full handbook.

1. ALTGX Transceiver Setup Guide for Stratix IV Devices

SIV53001-4.4

This chapter describes the options you can choose in the ALTGX MegaWizard™ Plug-In Manager in the Quartus® II software to configure Stratix® IV GX and GT devices in different functional modes.

The MegaWizard Plug-In Manager in the Quartus II software creates or modifies design files that contain custom megafunction variations that can then be instantiated in a design file. You can use the MegaWizard Plug-In Manager to set the ALTGX megafunction features in the design. The ALTGX megafunction allows you to configure one or more transceiver channels. You can select the physical coding sublayer (PCS) and physical medium attachment (PMA) functional blocks depending on your transceiver configuration.

This chapter contains the following sections:

Start the MegaWizard Plug-In Manager using one of the following methods:

- From the Tools menu, select **MegaWizard Plug-In Manager**.
- When working in the Block Editor, click **MegaWizard Plug-In Manager** in the **Symbol** dialog box (Edit menu).
- Start the standalone version of the MegaWizard Plug-In Manager by typing the following command at the command prompt: `qmegawiz`.

Figure 1–1 shows the first page of the MegaWizard Plug-In Manager. To generate an ALTGX custom megafunction variation, select **Create a new custom megafunction variation**.

Figure 1–1. MegaWizard Plug-In Manager (Page 1)

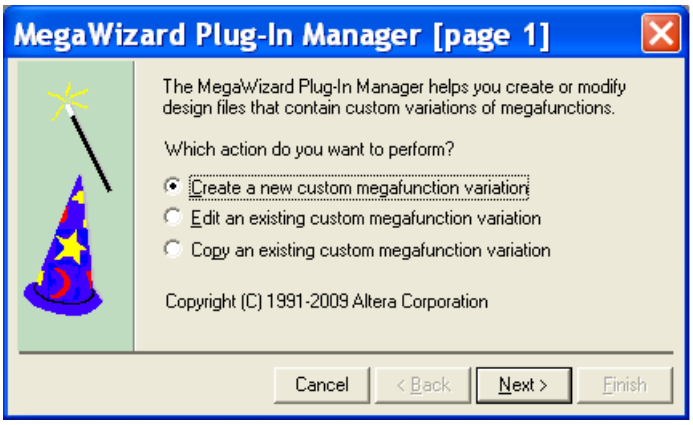


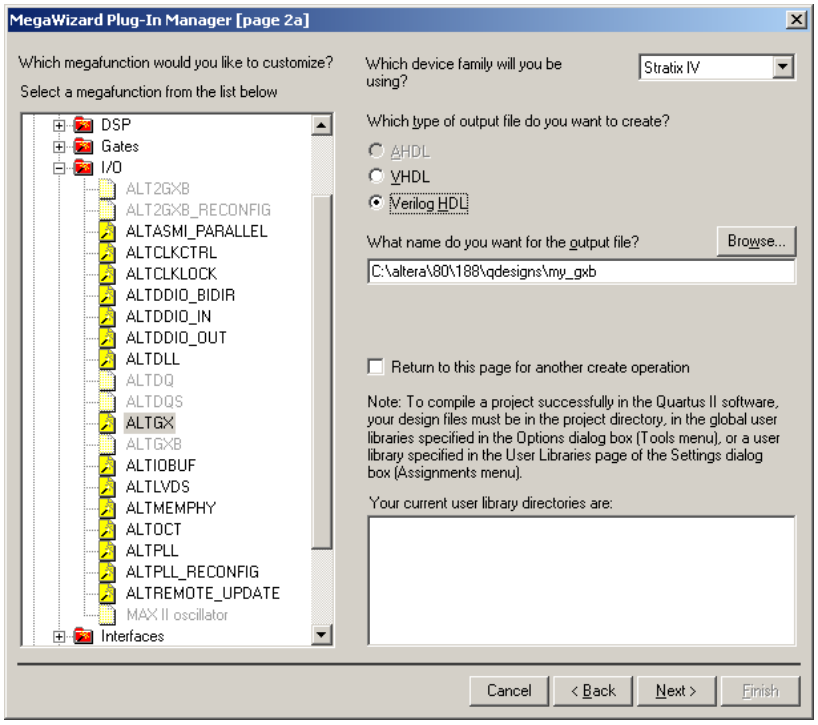
Figure 1–2 shows the second page of the MegaWizard Plug-In Manager.

To use the MegaWizard Plug-In Manager to configure a Stratix IV device, follow these steps:

1. Select **Stratix IV** as the device family.
2. Select either **VHDL** or **Verilog HDL** depending on the type of output files you want to create.
3. Select the **ALTGX** megafunction under the I/O section of the available megafunctions.

4. Name the output file, then **Browse** to the folder you want to save your file in and click **Next**. The **General** screen of the ALTGX MegaWizard Plug-In Manager opens (Figure 1–3).

Figure 1–2. MegaWizard Plug-In Manager (Page 2)



All reset and control signals are active high unless otherwise mentioned.

All output ports are synchronous to the data path unless otherwise specified.

Throughout this chapter, the various functional modes and their settings are explained for Stratix IV GX and GT devices.

Parameter Settings

This section describes the options available on the individual pages of the ALTGX MegaWizard Plug-In Manager for the Parameter Settings. The MegaWizard Plug-In Manager provides a warning if any of the settings you choose are illegal.

General Screen for the Parameter Settings

Figure 1–3 shows the **General** screen of the ALTGX MegaWizard Plug-In Manager for the Parameter Settings.

Figure 1–3. MegaWizard Plug-In Manager—ALTGX (General Screen for the Parameter Settings)

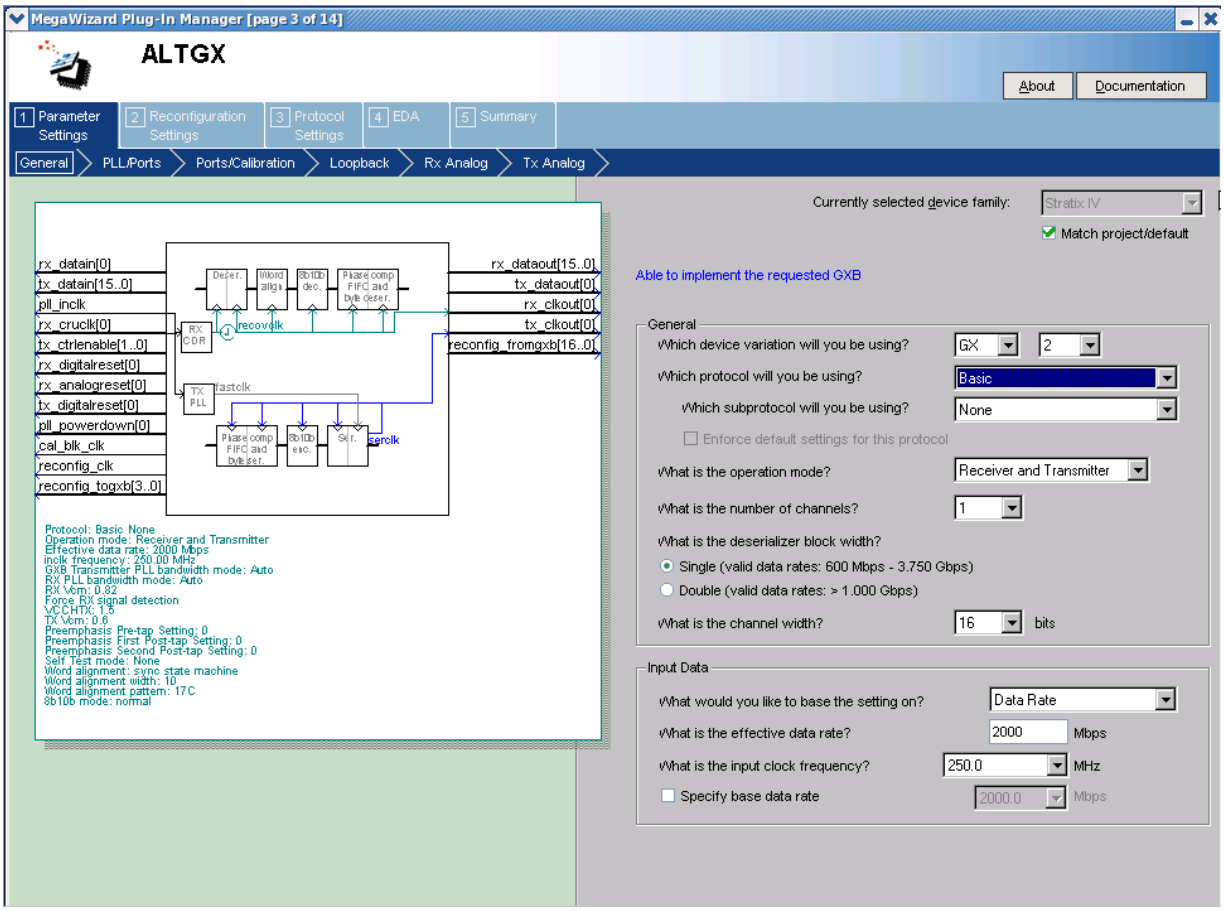


Table 1–1 lists the available functional modes and their options on the **General** screen of the MegaWizard Plug-In Manager. Depending on your configuration, you will select one of the following functional modes:

- **Basic**
- **Basic (PMA Direct)**
- **Deterministic Latency**
- **GIGE**
- **(OIF) CEI Phy Interface**
- **PCI Express® (PCIe)**
- **SDI**
- **Serial RapidIO®**
- **SONET/SDH**
- **XAUI**

If you select Basic (PMA Direct) mode, all the channels are configured with only the PMA blocks. These channels are called PMA-only channels throughout this chapter. The PMA-only channels include:

- Regular transceiver channels with PMA blocks only
- CMU channels (clock multiplier unit phase-locked loops [CMU PLLs] configured as additional transceiver channels with PMA blocks only)

Table 1–1. MegaWizard Plug-In Manager Options (General Screen for Basic Mode) (Part 1 of 11)

ALTGX Setting	Description	Reference
Which device variation will you be using?	Select **GX** or **GT** based on the Stratix IV device used in your design. Select the speed grade of your device. The available speed grades for the Stratix IV GX device are 2, 2×, 3, and 4. The available speed grades for the Stratix IV GT device are 1, 2 and 3.	*DC and Switching Characteristics for Stratix IV Devices* chapter.
Which protocol will you be using?	Determines the specific protocol under which the transceiver operates. For a specific mode, you must select the desired protocol from the following list: ■ **(OIF) CEI PHY Interface** ■ **SDI** ■ **SONET/SDH** ■ **XAUI** ■ **Basic** ■ **Basic (PMA Direct)** ■ **Deterministic Latency** ■ **GIGE** ■ **PCIe** ■ **Serial RapidIO**	*Transceiver Architecture in Stratix IV Devices* chapter.

Table 1–1. MegaWizard Plug-In Manager Options (General Screen for Basic Mode) (Part 2 of 11)

ALTGX Setting	Description	Reference
Which subprotocol will you be using?	**Basic** In Basic mode, the subprotocols are diagnostic modes. The available options are as follows: ■ None—This is the normal operation of the transceiver. ■ ×4—In this mode, all four channels within the transceiver block are clocked from its central clock divider block to minimize transmitter channel-to-channel skew. ■ ×8—In this mode, all eight channels in two transceiver blocks are clocked from the central clock divider of the master transceiver block to minimize transmitter channel-to-channel skew. ■ BIST—This subprotocol is applicable only for **Receiver and Transmitter** operation mode. This mode loops the parallel data from the built-in self test (BIST) (non-PRBS) back to the BIST verifier in the receiver path. Parallel loopback is allowed only in Basic double-width mode. ■ PRBS—This subprotocol is applicable only for **Receiver and Transmitter** operation mode.This is another Serial Loopback mode but with the pseudo-random binary sequence (PRBS) BIST block active. The PRBS pattern depends on the serializer/deserializer (SERDES) factor.	"Basic Functional Mode" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
	Basic (PMA Direct) ■ None—This is the normal mode of operation in which each channel is treated independently. ■ XN—In this mode, the "N" in XN represents the number of channels in the bonded configuration. All N channels are clocked by the same transmit clock from the central clock divider block to minimize transmitter channel-to-channel skew.	"Basic PMA Direct Functional Mode" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
	Deterministic Latency ■ ×1—In this mode, you can have up to two configured channels per transceiver block. Each channel uses one CMU PLL and its feedback path to compensate for the uncertain latency. ■ ×4—In this mode, you can have up to four configured channels per transceiver block. All channels use one CMU PLL per block and its feedback path to compensate for the uncertain latency.	"Deterministic Latency Mode" section in the *Transceiver Architecture in Stratix IV Devices* chapter.

Table 1–1. MegaWizard Plug-In Manager Options (General Screen for Basic Mode) (Part 3 of 11)

ALTGX Setting	Description	Reference
Which subprotocol will you be using?	**PCIe** In PCIe mode, there are six subprotocols: ■ Gen1 ×1—The transceiver is configured as a single-lane PCIe link for a 2.5 Gbps data rate. ■ Gen1 ×4—The transceiver is configured as a four-lane PCIe link for a data rate of 2.5 Gbps. ■ Gen1 ×8—The transceiver is configured as an eight-lane PCIe link for a data rate of 2.5 Gbps. ■ Gen2 ×1—The transceiver is configured as a single-lane PCIe link for a 5.0 Gbps data rate. ■ Gen2 ×4—The transceiver is configured as a four-lane PCIe link for a data rate of 5.0 Gbps. ■ Gen2 ×8—The transceiver is configured as an eight-lane PCIe link for a data rate of 5.0 Gbps.	"PCIe Mode" in the *Transceiver Architecture in Stratix IV Devices* chapter.
	SDI In SDI mode, the two available subprotocols are: ■ 3G—third-generation (3 Gbps) SDI at 2967 Mbps or 2970 Mbps. ■ HD—high-definition SDI at 1483.5 Mbps or 1485 Mbps.	"SDI Mode" in the *Transceiver Architecture in Stratix IV Devices* chapter.
	SONET/SDH In SONET/SDH mode, the three available subprotocols and their data rates are: ■ OC-12—622 Mbps ■ OC-48—2488.32 Mbps ■ OC-96—4976.64 Mbps	"SONET/SDH Mode" in the *Transceiver Architecture in Stratix IV Devices* chapter.
Enforce default settings for this protocol.	**Deterministic Latency** **GIGE** **(OIF) CEI PHY Interface** **PCIe** **SONET/SDH** **XAUI** If you select this option, all mode-specific ports and settings are used.	—

Table 1–1. MegaWizard Plug-In Manager Options (General Screen for Basic Mode) (Part 4 of 11)

ALTGX Setting	Description	Reference
What is the operation mode?	**Basic** **Basic (PMA Direct)** **Deterministic Latency** **SDI** **Serial RapidIO** **SONET/SDH** The available operation modes are **Receiver only**, **Transmitter only,** and **Receiver and Transmitter**. For Basic (PMA Direct) xN mode, the available operation modes are **Transmitter only** and **Receiver and Transmitter**. However, if you set the subprotocol to **None**, the available operation modes are **Receiver only**, **Transmitter only,** and **Receiver and Transmitter.**	—
	GIGE The available operation modes are **Transmitter only,** and **Receiver and Transmitter**.	—
	PCIe **XAUI** Only **Receiver and Transmitter** mode is allowed.	—

Table 1–1. MegaWizard Plug-In Manager Options (General Screen for Basic Mode) (Part 5 of 11)

ALTGX Setting	Description	Reference
What is the number of channels?	**Basic** **Basic (PMA Direct)** **Deterministic Latency** **SDI** **Serial RapidIO** The number of channels required with the same configuration. This option determines how many identical channels this ALTGX instance contains.	—
	GIGE **(OIF) CEI PHY Interface** **SONET/SDH** This option allows you to select how many channels this ALTGX instance contains. In these modes, the number of channels increments by one.	—
	PCIe This is the number of channels required with the same configuration. ■ In a ×4 subprotocol, the number of channels increments by 4. ■ In a ×8 subprotocol, the number of channels increment by 8.	—
	XAUI This option allows you to select how many identical channels this ALTGX instance contains. In XAUI mode, the number of channels increments by 4.	—

Table 1–1. MegaWizard Plug-In Manager Options (General Screen for Basic Mode) (Part 6 of 11)

ALTGX Setting	Description	Reference
What is the deserializer block width?	**Basic** **Basic (PMA Direct)** **Deterministic Latency** This option sets the transceiver data path width. ■ **Single-width**—This mode operates from 600 Mbps to 3.75 Gbps. ■ **Double-width**—This mode operates from 1 Gbps to 8.5 Gbps.	"Basic Single-Width Mode Configurations" and "Basic Double-Width Mode Configurations" sections in the *Transceiver Architecture in Stratix IV Devices* chapter.
	GIGE **PCIe** **SDI** **Serial RapidIO** **XAUI** These modes only operate in single-width mode. Double-width mode is not allowed.	—
	(OIF) CEI PHY Interface The (OIF) CEI PHY Interface mode only operates in double-width mode. Single-width mode is not allowed.	—
	SONET/SDH This option allows you to set the transceiver data path width. ■ **Single-width**—Selected automatically in OC-12 and OC-48 configurations. The transceiver data path width is 8 bits. ■ **Double-width**—Selected automatically in OC-96 configurations. The transceiver data path width is 16 bits.	—

Table 1–1. MegaWizard Plug-In Manager Options (General Screen for Basic Mode) (Part 7 of 11)

ALTGX Setting	Description	Reference
What is the channel width?	**Basic** **Deterministic Latency** This option determines the FPGA fabric-Transceiver interface width. ■ Single-width mode—Selecting 8 or 10 bits bypasses the byte serializer/deserializer. Selecting 16 or 20 bits uses the byte serializer/deserializer. ■ Double-width mode—Selecting 16 or 20 bits bypasses the byte serializer/deserializer. Selecting 32 or 40 bits uses the byte serializer/deserializer.	"Byte Serializer" and "Byte Deserializer" sections in the *Transceiver Architecture in Stratix IV Devices* chapter.
	Basic (PMA Direct) This option determines the FPGA fabric-Transceiver interface width. ■ Single-width mode—You can select 8 or 10 bits. ■ Double-width mode— You can select 16 or 20 bits.	
	GIGE This option determines the FPGA fabric-Transceiver interface width. In GIGE mode, only 8 bits are allowed.	
	(OIF) CEI PHY Interface This option selects the FPGA fabric-Transceiver width. In (OIF) CEI PHY Interface mode, only 32 bits are allowed.	
	PCIe This option determines the FPGA fabric-Transceiver interface width. ■ In PCIe Gen1 (2.5 Gbps) mode, 8 and 16 bits are allowed. ■ In PCIe Gen2 (5 Gbps) mode, only 16 bits are allowed.	
	SDI This option determines the FPGA fabric-Transceiver interface width: ■ HD mode—10-bit and 20-bit channel widths are allowed. ■ 3G mode—only 20-bit channel width is allowed. ■ 10-bit configuration—the byte serializer is not used. ■ 20-bit configuration—the byte serializer is used.	
	Serial RapidIO The channel width is fixed to 16 in Serial RapidIO mode.	

Table 1–1. MegaWizard Plug-In Manager Options (General Screen for Basic Mode) (Part 8 of 11)

ALTGX Setting	Description	Reference
What is the channel width?	**SONET/SDH** This option selects the FPGA fabric-Transceiver interface width. Depending on your subprotocol selection, choose one of the following: ■ **8 bits** for OC-12 mode ■ **16 bits** for OC-48 mode ■ **32 bits** for OC-96 mode	"Byte Serializer" and "Byte Deserializer" sections in the *Transceiver Architecture in Stratix IV Devices* chapter.
	XAUI XAUI mode only operates in single-width mode.	
What would you like to base the setting on?	**Basic** **Basic (PMA Direct)** You can select one of the following options: ■ **Data rate**—Selecting this option allows you to enter the transceiver channel serial data rate. Based on the value you enter, the ALTGX MegaWizard Plug-In Manager populates the input reference clock frequency options in the **What is the input clock frequency?** field. The ALTGX MegaWizard Plug-In Manager determines these input reference clock frequencies depending on the available multiplier settings. ■ **Input clock frequency**—Selecting this option allows you to enter your input clock frequency. Based on the value you enter, the ALTGX MegaWizard Plug-In Manager populates the data rate options in the **What is the effective data rate?** field. The ALTGX MegaWizard Plug-In Manager determines these data rate options depending on the available multipler settings.	—

Table 1–1. MegaWizard Plug-In Manager Options (General Screen for Basic Mode) (Part 9 of 11)

ALTGX Setting	Description	Reference
What is the effective data rate?	**Basic** **Basic (PMA Direct)** **Deterministic Latency** ■ If you select the **Data Rate** option in the **What would you like to base the setting on?** field, the ALTGX MegaWizard Plug-In Manager allows you to specify the effective serial data rate value in this field. ■ If you select the **Input Clock Frequency** option in the **What would you like to base the setting on?** field, the ALTGX MegaWizard Plug-In Manager displays the list of effective serial data rates in this field.	—
	GIGE This option is not available in **GIGE** mode. The transceiver channel serial data rate is fixed to 1250 Mbps in this mode.	—
	(OIF) CEI PHY Interface The allowed effective data rate is between 3125 Mbps and 6500 Mbps. Enter the transceiver channel's serial data rate in this field.	—
	PCIe This option is not available in PCIe mode. The defaults are: ■ 2500 Mbps for PCIe Gen1 mode. ■ 5000 Mbps for PCIe Gen 2 mode.	—
	SDI The effective data rate is fixed at: ■ 2967 Mbps or 2970 Mbps in 3G mode. ■ 1483.5 Mbps or 1485 Mbps in HD mode.	—
	Serial RapidIO Enter one of these three data rates in this option: ■ 1250 Mbps. ■ 2500 Mbps. ■ 3125 Mbps.	—
	SONET/SDH The effective data rate is fixed at: ■ 622 Mbps in OC-12 mode. ■ 2488.32 Mbps in OC-48 mode. ■ 4976 Mbps in OC-96 mode.	—
	XAUI The effective data rate can be from 3125 Mbps to 3750 Mbps.	—

Table 1–1. MegaWizard Plug-In Manager Options (General Screen for Basic Mode) (Part 10 of 11)

ALTGX Setting	Description	Reference
What is the input clock frequency?	**Basic** **Basic (PMA Direct)** ■ If you select the **Input Clock Frequency** option in the **What would you like to base the setting on?** field, the ALTGX MegaWizard Plug-In Manager allows you to specify the input reference clock frequency in this field. ■ If you select the **Data Rate** option in the **What would you like to base the setting on?** field, the ALTGX MegaWizard Plug-In Manager displays the list of input reference clock frequencies in this field.	"Input Reference Clocking" section in the *Transceiver Clocking in Stratix IV Devices* chapter.
	Deterministic Latency **GIGE** **(OIF) CEI PHY Interface** **SDI** **SONET/SDH** Based on the effective data rate value in the **What is the effective data rate?** field, the ALTGX MegaWizard Plug-In Manager determines the input reference clock frequencies depending on the available multiplier settings.	
	PCIe This option is not available in PCIe mode. The input reference clock frequency is fixed to 100 MHz in PCIe mode.	
	Serial RapidIO This option provides the available input reference clock frequencies depending on whether your effective serial data rate is 1250 Mbps, 2500 Mbps, or 3125 Mbps and the available multiplier settings.	
	XAUI This option provides the available input reference clock frequencies depending on whether your effective serial data rate is 3125 Mbps or 3750 Mbps and the available multiplier settings.	

Table 1–1. MegaWizard Plug-In Manager Options (General Screen for Basic Mode) (Part 11 of 11)

ALTGX Setting	Description	Reference
Specify base data rate.	**Basic** **Basic (PMA Direct)** The ALTGX MegaWizard Plug-In Manager provides you the **base data rate** options for the CMU/advanced technology extended (ATX) PLL and receiver clock data recovery (CDR). If you select a value in this field that is greater than the value in the **What is the effective data rate?** field, the ALTGX MegaWizard Plug-In Manager enables the appropriate local clock divider values. The local divider is present in the receiver channels.	—
	GIGE This option is not available in this mode because the data rate is fixed. The ALTGX MegaWizard Plug-In Manager provides you the base data rate options for the CMU PLL and receiver CDR.	—
	(OIF) CEI PHY Interface **Serial RapidIO** **XAUI** This option is not available in these modes. The ALTGX MegaWizard Plug-In Manager provides you the base data rate options for the CMU PLL and receiver CDR.	—
	PCIe For Gen1 ×1, an optional base data rate of either 2500 or 5000 Mbps is available.	—
	SDI This option is not available this mode as the data rate is fixed in 3G and HD modes. The ALTGX MegaWizard Plug-In Manager provides you the base data rate options for the CMU PLL and receiver CDR.	—
	SONET/SDH This option is not available in this mode as the data rates are fixed in OC-12, OC-48, and OC-96 modes. The ALTGX MegaWizard Plug-In Manager provides you the base data rate options for the CMU PLL and receiver CDR in this option.	—

PLL/Ports Screen for the Parameter Settings

Figure 1–4 shows the **PLL/Ports** screen of the ALTGX MegaWizard Plug-In Manager for the Parameter Settings.

Figure 1–4. MegaWizard Plug-In Manager—ALTGX (PLL/Ports Screen)

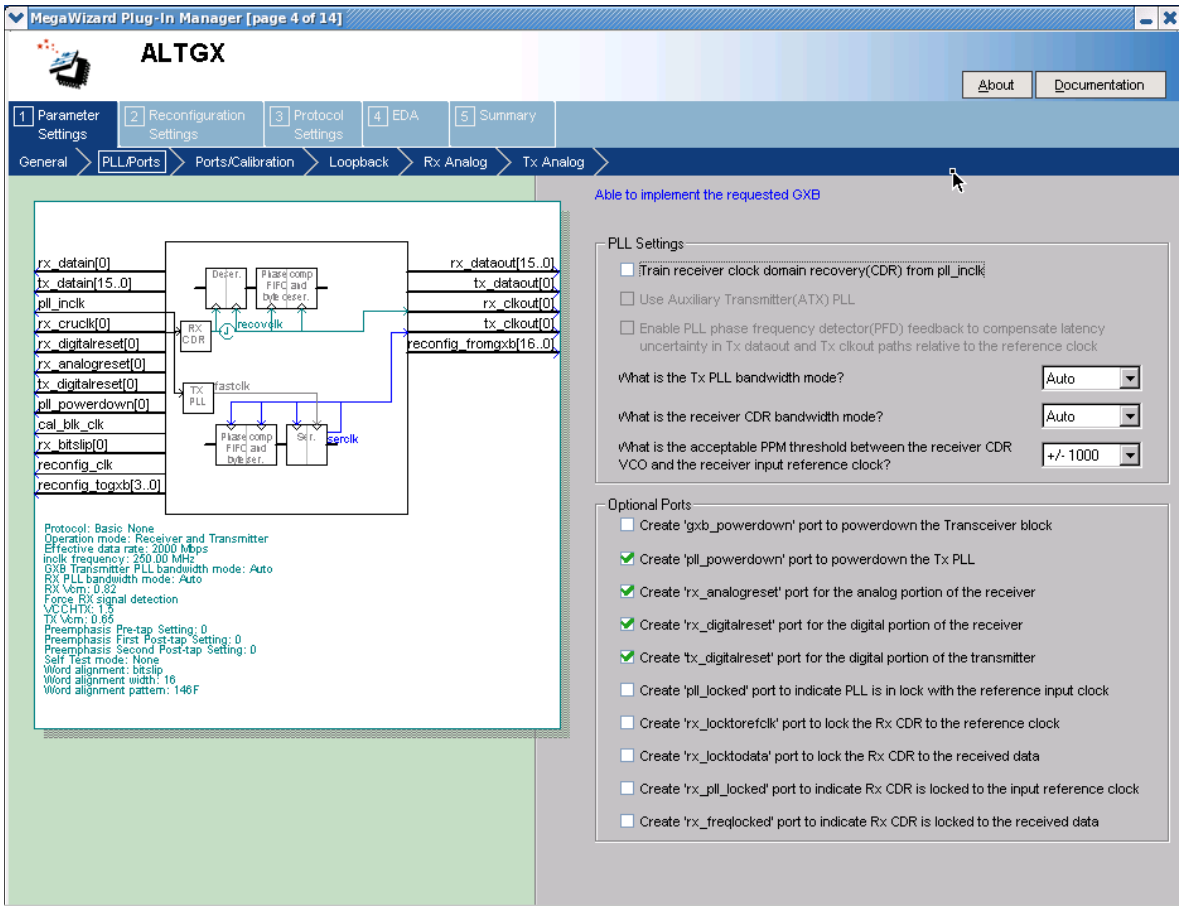


Table 1–2 lists the available options on the **PLL/ports** screen of the MegaWizard Plug-In Manager for your ALTGX custom megafunction variation.

Table 1–2. MegaWizard Plug-In Manager Options (PLL/Ports Screen) (Part 1 of 3)

ALTGX Setting	Description	Reference
Train receiver clock and data recovery (CDR) from `pll_inclk`.	If you select this option, the input reference clock to the CMU PLL trains the receiver CDR.	Table 1-77 in the *Transceiver Architecture in Stratix IV Devices* chapter.
Use ATX Transmitter PLL	This option is only available for certain data rates. Refer to the *DC and Switching Characteristics for Stratix IV Devices* chapter for the supported data rates. This option enables the auxiliary transmitter PLL. This is a low-jitter PLL that resides between the transceiver blocks and can be used as a transmitter PLL.	"Auxiliary Transmit (ATX) PLL Block" section in the *Transceiver Architecture in Stratix IV Devices*, the *Transceiver Clocking in Stratix IV Devices* chapter, and the *DC and Switching Characteristics for Stratix IV Devices* section.

Table 1–2. MegaWizard Plug-In Manager Options (PLL/Ports Screen) (Part 2 of 3)

ALTGX Setting	Description	Reference
Enable PLL phase frequency detector (PFD) feedback to compensate latency uncertainty in `tx_dataout` and `tx_clkout` paths relative to the reference clock.	This option applies only when you select **Deterministic Latency** functional mode.	"CMU PLL Feedback" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
What is the TX PLL bandwidth mode?	The available options are **Auto, Low**, **Medium**, and **High**. Select the appropriate option based on your system requirements.	"PLL Bandwidth Setting" section in the *Transceiver Architecture in Stratix IV Devices* chapter and the *DC and Switching Characteristics for Stratix IV Devices* section.
What is the receiver CDR bandwidth mode?	The available options are **Auto, Low**, **Medium**, and **High**. Select the appropriate option based on your system requirements.	"Clock and Data Recovery Unit" section in the *Transceiver Architecture in Stratix IV Devices* chapter and the *DC and Switching Characteristics for Stratix IV Devices* section.
What is the acceptable PPM threshold between the receiver CDR VCO and the receiver input reference clock?	In Automatic Lock mode, the CDR remains in Lock-to-Data (LTD) mode as long as the parts per million (PPM) difference between the CDR VCO output clock and the input reference clock is less than the PPM value that you set in this option. If the PPM difference is greater than the PPM value that you set in this option, the CDR switches to Lock-to-Reference (LTR) mode. The range of values available in this option is ±62.5 ppm to ±1000 ppm. (1)	"Automatic Lock Mode" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
Optional Ports		
Create a `gxb_powerdown` port to power down the transceiver block.	When asserted, this signal powers down the entire transceiver block. If none of the channels are instantiated in a transceiver block, the Quartus II software automatically powers down the entire transceiver block.	"User Reset and Power Down Signals" section in the *Reset Control and Power Down in Stratix IV Devices* chapter.
Create a `pll_powerdown` port to power down the TX PLL.	Each transceiver block has two CMU PLLs. Each CMU/ATX PLL has a dedicated power down signal called `pll_powerdown`. This signal powers down the CMU/ATX PLL.	"User Reset and Power Down Signals" section in the *Reset Control and Power Down in Stratix IV Devices* chapter.
Create a `rx_analogreset` port for the analog portion of the receiver.	The receiver analog reset port is available in **Receiver only** and **Receiver and Transmitter** operation modes. This resets part of the analog portion of the receiver CDR in the receiver channel. Altera recommends using this port to implement the recommended reset sequence. The minimum pulse width is two parallel clock cycles.	"User Reset and Power Down Signals" in the *Reset Control and Power Down in Stratix IV Devices* chapter.

Table 1–2. MegaWizard Plug-In Manager Options (PLL/Ports Screen) (Part 3 of 3)

ALTGX Setting	Description	Reference
Create a `rx_digitalreset` port for the digital portion of the receiver.	The receiver digital reset port is available in **Receiver only** and **Receiver and Transmitter** operation modes. This resets the PCS portion of the receiver channel. Altera recommends using this port to implement the recommended reset sequence. The minimum pulse width is two parallel clock cycles.	"User Reset and Power Down Signals" section in the *Reset Control and Power Down in Stratix IV Devices* chapter.
Create a `tx_digitalreset` port for the digital portion of the transmitter.	The transmitter digital reset port is available in **Transmitter only** and **Receiver and Transmitter** operation modes. This resets the PCS portion of the transmitter channel. Altera recommends using this port to implement the recommended reset sequence. The minimum pulse width is two parallel clock cycles.	"User Reset and Power Down Signals" section in the *Reset Control and Power Down in Stratix IV Devices* chapter.
Create a `pll_locked` port to indicate PLL is in lock with the reference input clock.	Each CMU/ATX PLL has a dedicated `pll_locked` signal that is fed to the FPGA fabric to indicate when the PLL is locked to the input reference clock.	"Transceiver Reset Sequences" section in the *Reset Control and Power Down in Stratix IV Devices* chapter.
Create an `rx_locktorefclk` port to lock the RX CDR to the reference clock.	When this signal is asserted high, the LTR/LTD controller forces the receiver CDR to lock to the phase and frequency of the input reference clock. (1), (2)	"LTR/LTD Controller" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
Create an `rx_locktodata` port to lock the RX CDR to the received data.	When this signal is asserted high, the LTR/LTD controller forces the receiver CDR to lock to the received data. (1), (2)	"LTR/LTD Controller" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
Create an `rx_pll_locked` port to indicate RX CDR is locked to the input reference clock.	■ In LTR mode, this signal is asserted high to indicate that the receiver CDR has locked to the phase and frequency of the input reference clock. ■ In LTD mode, this signal has no significance. (1)	"Lock-to-Reference (LTR) Mode" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
Create an `rx_freqlocked` port to indicate RX CDR is locked to the received data.	This signal is asserted high to indicate that the receiver CDR has switched from LTR to LTD mode. This signal has relevance only in Automatic Lock mode and may be required to control the transceiver resets, as described in the *User Reset and Power Down Signals* section in the *Reset Control and Power Down in Stratix IV Devices* chapter. (1)	"LTR/LTD Controller" section in the *Transceiver Architecture in Stratix IV Devices* chapter.

Notes to Table 1–2:

(1) LTR mode is lock-to-reference mode and LTD mode is lock-to-data mode.

(2) When `rx_locktorefclk` and `rx_locktodata` are both asserted high, `rx_locktodata` takes precedence over `rx_locktorefclk`, forcing the CDR to lock to the received data. When both these signals are de-asserted, the LTR/LTD controller is configured in Automatic Lock mode.

Ports/Calibration Screen for the Parameter Settings

Figure 1–5 shows the **Ports/Calibration** screen of the ALTGX MegaWizard Plug-In Manager for the Parameter Settings.

Figure 1–5. MegaWizard Plug-In Manager—ALTGX (Ports/Calibration Screen)

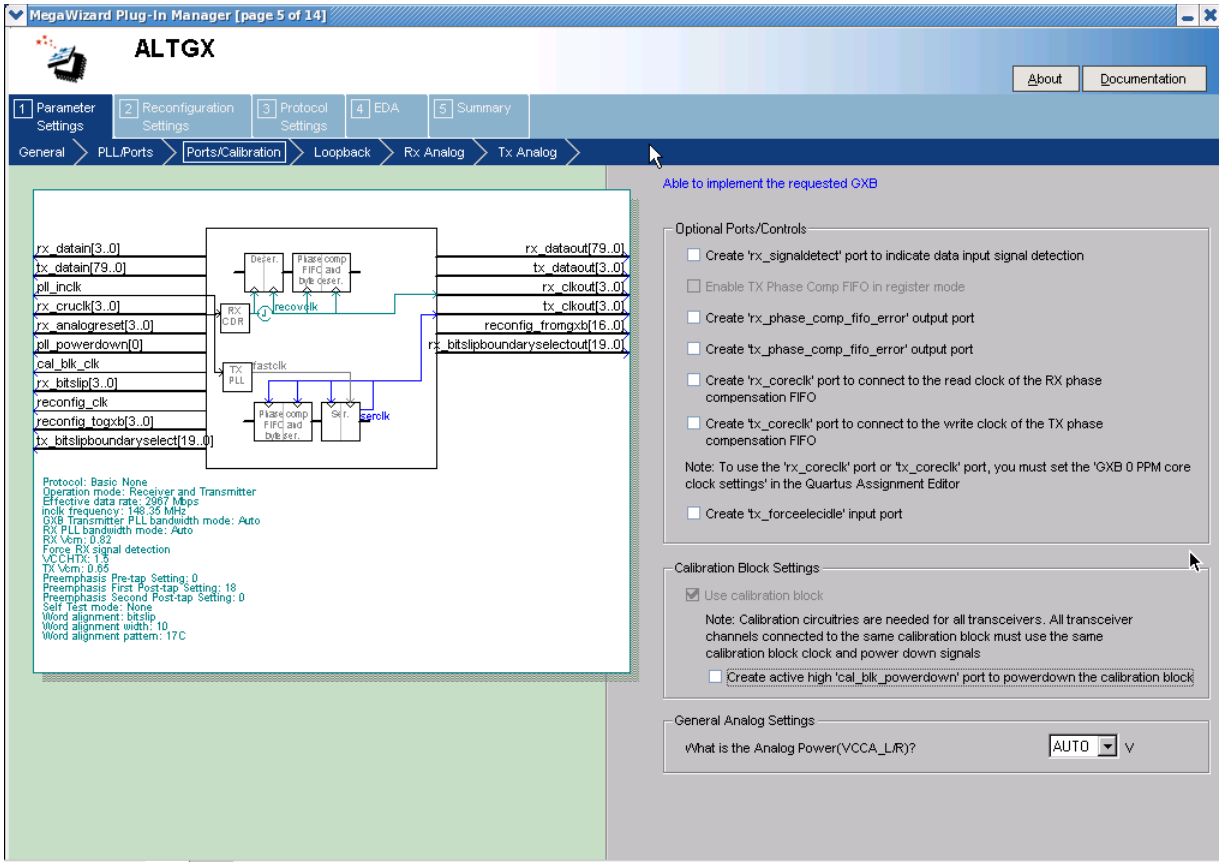


Table 1–3 lists the available options on the **Ports/Calibration** screen of the MegaWizard Plug-In Manager for your ALTGX custom megafunction variation. Unless indicated otherwise, the options apply to all functional modes.

Table 1–3. MegaWizard Plug-In Manager Options (Ports/Calibration Screen) (Part 1 of 3)

ALTGX Setting	Description	Reference
Optional Ports/Controls		
Create an `rx_signaldetect` port to indicate data input signal detection.	This port is only available in **Basic** and **PCIe** mode.	"Signal Threshold Detection Circuitry" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
Enable TX Phase Comp FIFO in register mode.	This option is only available in **Deterministic Latency** mode.	"Deterministic Latency" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
Create an `rx_phase_comp_fifo_error` output port.	This output port indicates a Receiver Phase Compensation FIFO overflow or under-run condition.	"Receiver Phase Compensation FIFO Error Flag" section in the *Transceiver Architecture in Stratix IV Devices* chapter.

Table 1–3. MegaWizard Plug-In Manager Options (Ports/Calibration Screen) (Part 2 of 3)

ALTGX Setting	Description	Reference
Create a `tx_phase_comp_fifo_error` output port.	This output port indicates a Transmitter Phase Compensation FIFO overflow or under-run condition.	"TX Phase Compensation FIFO Status Signal" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
Create an `rx_coreclk` port to connect to the read clock of the RX phase compensation FIFO.	You can clock the parallel output data from the receiver using this optional input port. This port allows you to clock the read side of the Receiver Phase Compensation FIFO with a user-provided clock (FPGA fabric clock, FPGA fabric-Transceiver interface clock, or input reference clock).	"FPGA Fabric-Transceiver Interface Clocking" section in the *Transceiver Clocking in Stratix IV Devices* chapter.
Create a `tx_coreclk` port to connect to the write clock of the TX phase compensation FIFO.	You can clock the parallel transmitter data generated in the FPGA fabric using this optional input port. This port allows you to clock the write side of the Transmitter Phase Compensation FIFO with a user-provided clock (FPGA fabric clock, FPGA fabric-Transceiver interface clock, or input reference clock).	"FPGA Fabric-Transceiver Interface Clocking" section in the *Transceiver Clocking in Stratix IV Devices* chapter.
Create a `tx_forceelecidle` input port	In Basic and PCIe modes, this optional input signal places the transmitter buffer in the electrical idle state.	"Transceiver Channel Architecture" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
Use calibration block.	The calibration block is always enabled.	"Calibration Blocks" section in the *Transceiver Architecture in Stratix IV Devices* chapter.

Table 1–3. MegaWizard Plug-In Manager Options (Ports/Calibration Screen) (Part 3 of 3)

ALTGX Setting	Description	Reference
Create an active high `cal_blk_powerdown` to power down the calibration block.	Asserting this signal high powers down the calibration block. A high-to-low transition on this signal restarts calibration.	"Input Signals to the Calibration Block" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
What is the Analog Power ($V_{CCA\_L/R}$)?	The options available for selection are based on what you specify in the **Specify base data rate** option: ■ **3.3 V**—Available up to 11.3 Gbps for Stratix IV GT devices only. ■ **3.0 V**—Available up to 8.5 Gbps. ■ **2.5 V**—Available up to 4.25 Gbps. ■ **AUTO**—The ALTGX MegaWizard Plug-In Manager automatically sets $V_{CCA\_L/R}$ to **2.5 V** for the VCO data rates less than 4.25 Gbps. or $V_{CCA\_L/R}$ to **3.0 V** for the VCO data rates greater than 4.25 Gbps. It is up to you to connect the correct voltage supply to the $V_{CCA\_L/R}$ pins on the board.	"General Requirements to Combine Channels" section in the *Configuring Multiple Protocols and Data Rates in Stratix IV Devices* chapter.

Loopback Screen for the Parameter Settings

Figure 1–6 shows the **Loopback** screen of the ALTGX MegaWizard Plug-In Manager for the Parameter Settings.

Figure 1–6. MegaWizard Plug-In Manager—ALTGX (Loopback Screen)

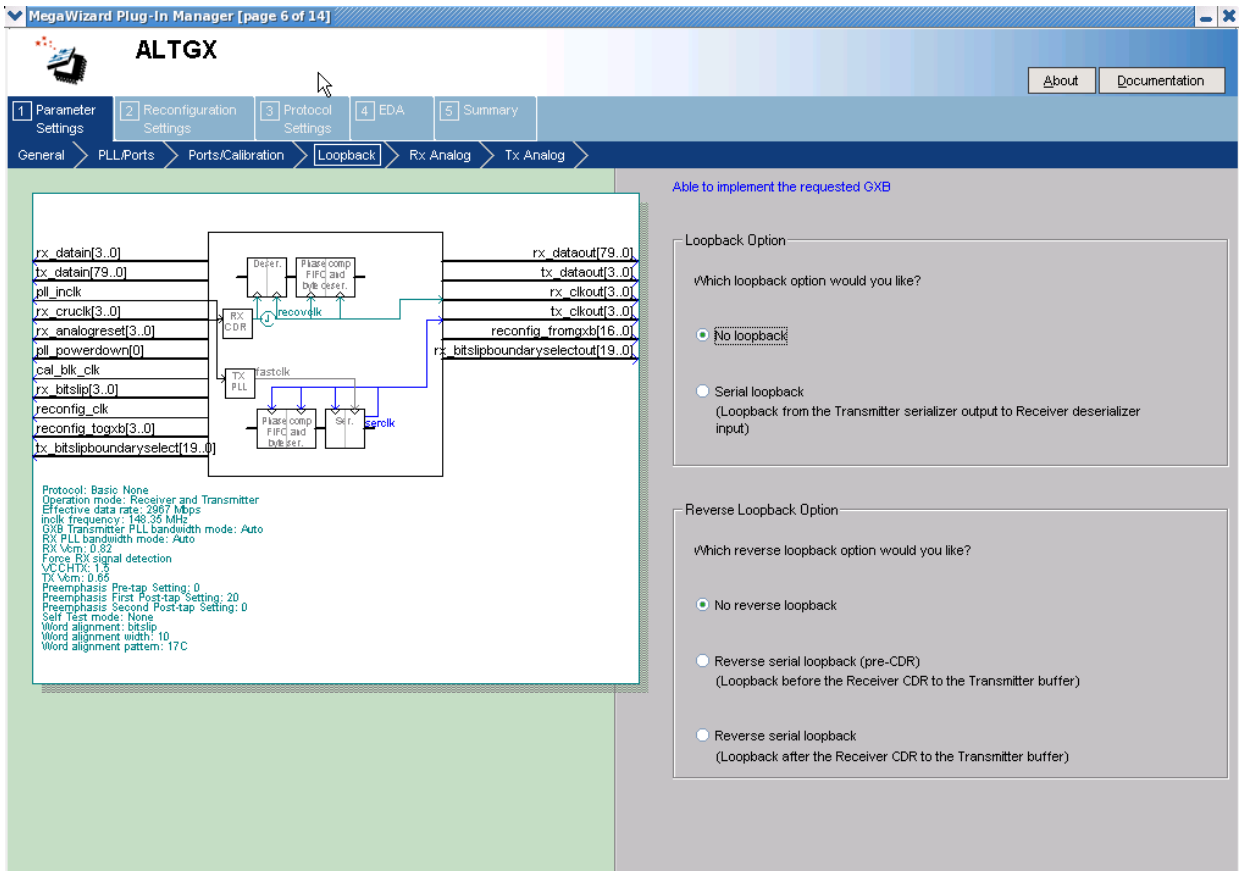


Table 1–4 lists the available options on the **Loopback** screen of the MegaWizard Plug-In Manager for your ALTGX custom megafunction variation.

Table 1–4. MegaWizard Plug-In Manager Options (Lpbk Screen)

ALTGX Setting	Description	Reference

Which loopback option would you like?	There are two options available:
	■ **No loopback**—This is the default mode.
	■ **Serial loopback**—If you select serial loopback, the `rx_seriallpbken` port is available to control the serial loopback feature dynamically.
	  ■ 1'b1—enables serial loopback
	  ■ 1'b0—disables serial loopback
	This signal is asynchronous to the receiver datapath.
		"Serial Loopback" section in the *Transceiver Architecture in Stratix IV Devices* chapter.

Which reverse loopback option would you like?	There are three options available: ■ **No reverse loopback**—This is the default mode. ■ **Reverse Serial loopback (pre-CDR)**—This is the loopback before the receiver's CDR block to the transmitter buffer. The receiver path in PCS is active but the transmitter side is not. ■ **Reverse Serial loopback**—This is a loopback after the receiver's CDR block to the transmitter buffer. The receiver path in PCS is active but the transmitter side is not.	"Loopback Modes" section in the *Transceiver Architecture in Stratix IV Devices* chapter.

RX Analog Screen for the Parameter Settings

Figure 1–7 shows the **RX Analog** screen of the ALTGX MegaWizard Plug-In Manager for the Parameter Settings.

Figure 1–7. MegaWizard Plug-In Manager—ALTGX (RX Analog Screen)

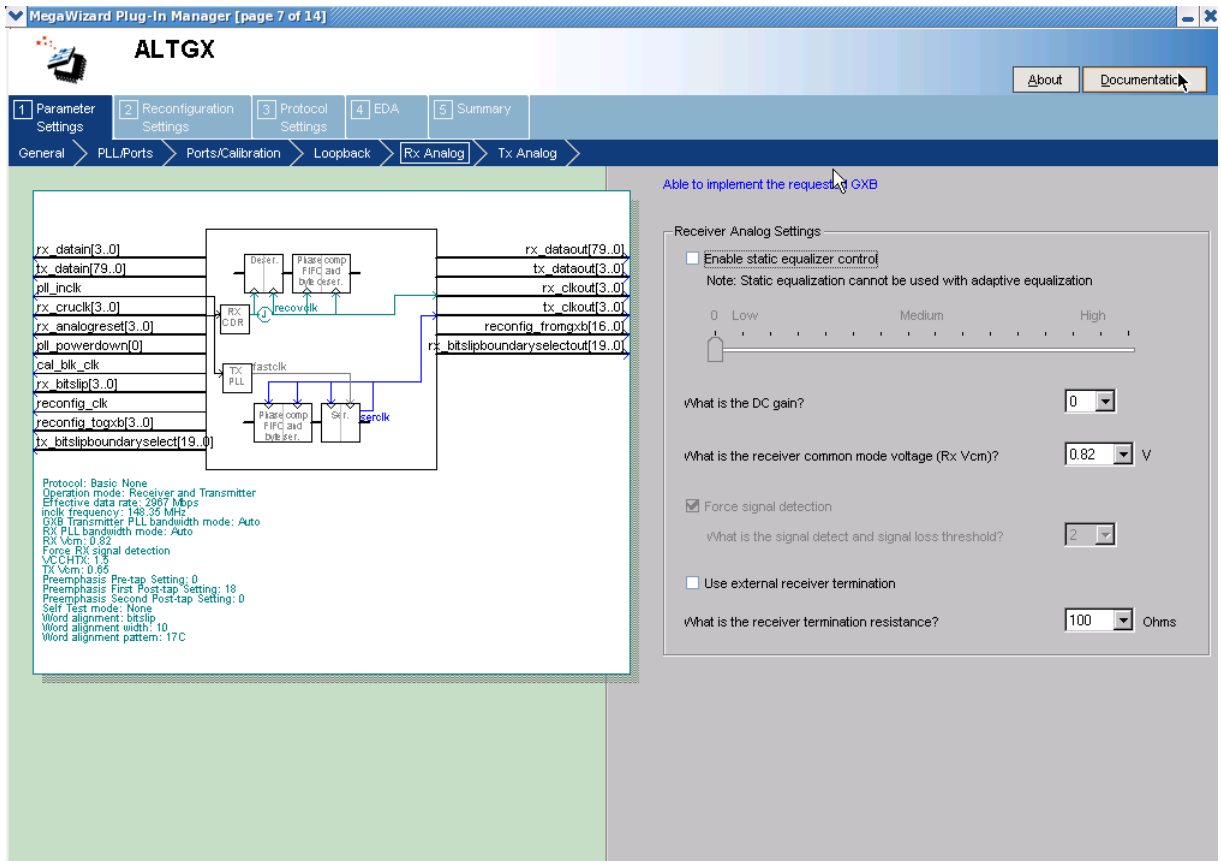


Table 1–5 lists the available options on the **RX Analog** screen of the MegaWizard Plug-In Manager for your ALTGX custom megafunction variation.

Table 1–5. MegaWizard Plug-In Manager Options (RX Analog Screen) (Part 1 of 2)

ALTGX Setting	Description	Reference
Enable static equalizer control.	This option enables the static equalizer settings.	"Programmable Equalization and DC Gain" section in the *Transceiver Architecture in Stratix IV Devices* chapter and the *DC and Switching Characteristics for Stratix IV Devices* section.
What is the DC gain?	This DC gain option has five settings: ■ 0 – 0 dB ■ 1 – 3 dB ■ 2 – 6 dB ■ 3 – 9 dB ■ 4 – 12 dB	"Programmable Equalization and DC Gain" section in the *Transceiver Architecture in Stratix IV Devices* chapter.

Table 1–5. MegaWizard Plug-In Manager Options (RX Analog Screen) (Part 2 of 2)

ALTGX Setting	Description	Reference
What is the receiver common mode voltage (RX V_{CM})?	The receiver common mode voltage is programmable to 0.82 V or 1.1 V.	"Receiver Channel Datapath" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
Force signal detection.	In **PCIe** mode, this option disables the signal threshold detect circuit for the receiver CDR. The receiver CDR no longer depends on the signal detect criterion to switch from LTR to LTD mode.	"Signal Threshold Detection Circuitry" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
What is the signal detect threshold?	Use this option in **PCIe** or **Basic** mode with the 8B/10B block enabled and the `rx_signaldetect` port selected to determine the threshold level for the signal detect circuit. ■ **PIPE** mode—The levels are fixed. ■ **Basic** mode—A range of values depending on the data rate are available. The levels will be determined after characterization. The ALTGX settings have the following threshold voltages (V_{th}): setting 8: 50 mV setting 7: 45 mV setting 6: 40 mV setting 5: 35 mV setting 4: 30 mV setting 3: 25 mV setting 2: 20 mV setting 1: 15 mV The `rx_signaldetect` status signal is asserted when the receiver peak-to-peak differential input voltage V_{ID} (diff p-p) is higher than V_{th} multiplied by 4.	"Signal Threshold Detection Circuitry" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
Use external receiver termination.	Select this option if you want to use an external termination resistor instead of differential on-chip termination (OCT). If checked, this option turns off the receiver OCT.	"Programmable Differential On-Chip Termination" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
What is the receiver termination resistance?	This option allows you to select the receiver differential termination value. The settings allowed are: ■ 85 Ω ■ 100 Ω ■ 120 Ω ■ 150 Ω.	"Programmable Differential On-Chip Termination" section in the *Transceiver Architecture in Stratix IV Devices* chapter, and the *DC and Switching Characteristics for Stratix IV Devices* section.

TX Analog Screen for the Parameter Settings

Figure 1–8 shows the **TX Analog** screen of the ALTGX MegaWizard Plug-In Manager for the Parameter Settings.

Figure 1–8. MegaWizard Plug-In Manager—ALTGX (TX Analog Screen)

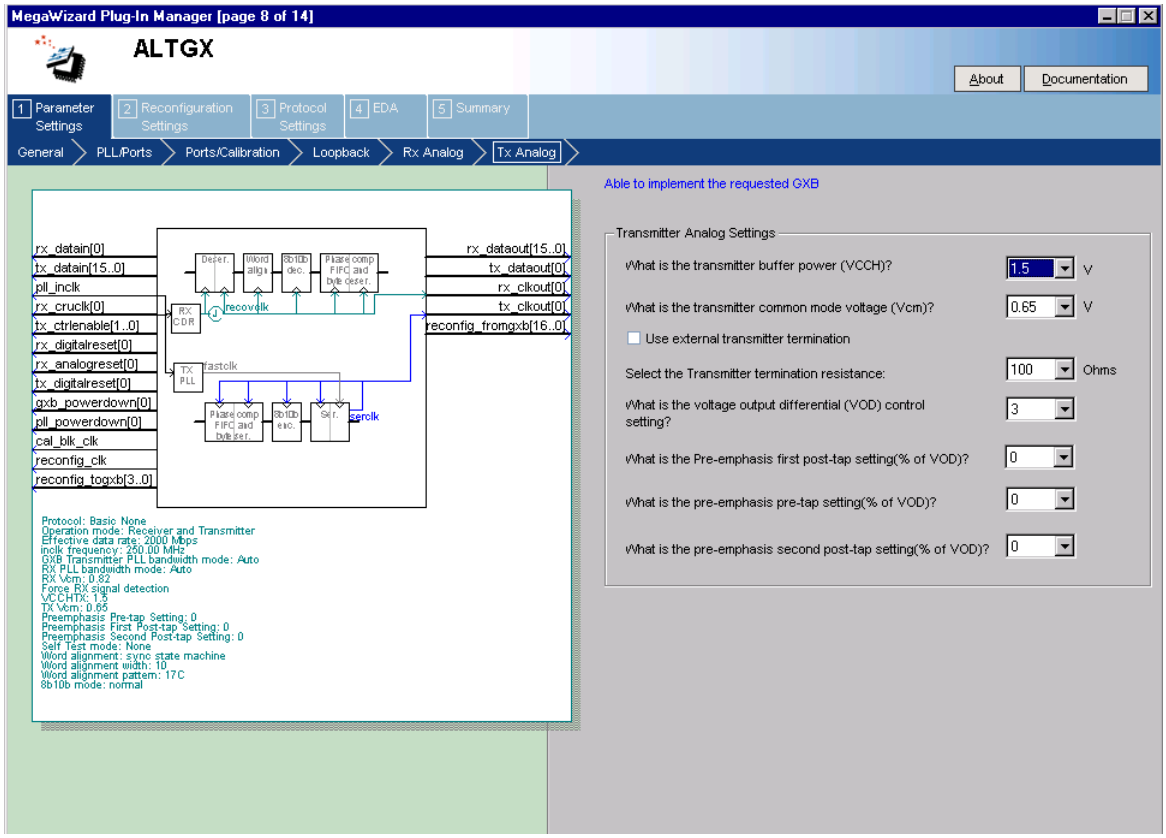


Table 1–6 lists the available options on the **TX Analog** screen of the MegaWizard Plug-In Manager for your ALTGX custom megafunction variation.

Table 1–6. MegaWizard Plug-In Manager Options (TX Analog Screen) (Part 1 of 2)

ALTGX Setting	Description	Reference
What is the transmitter buffer power (V_{CCH})?	The options available for selection are based on what you enter in the **What is the effective data rate?** option. ■ **1.4 V**—Available up to 8.5 Gbps. ■ **1.5 V** is available up to 6.5 Gbps (not available for Stratix IV GT). ■ **AUTO**—The ALTGX MegaWizard Plug-In Manager automatically sets V_{CCH} to **1.5 V** for the effective data rates less than 6.5 Gbps or V_{CCH} to **1.4 V** for effective data rates greater than 6.5 Gbps. It is up to you to connect the correct voltage supply to the V_{CCH} pins on the board.	"Programmable Transmit Output Buffer Power (V_{CCH})" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
What is the transmitter common mode voltage (V_{CM})?	The transmitter common mode voltage is fixed to 0.65 V.	"Transmitter Output Buffer" in the *Transceiver Architecture in Stratix IV Devices* chapter and the *DC and Switching Characteristics for Stratix IV Devices* section.
Use external transmitter termination.	This option is available if you want to use an external termination resistor instead of the differential OCT. Checking this option turns off the transmitter differential OCT.	"Programmable Transmitter Termination" section in the *Transceiver Architecture in Stratix IV Devices* chapter and the *DC and Switching Characteristics for Stratix IV Devices* section.
Select the transmitter termination resistance.	This option selects the transmitter differential termination value. The settings allowed are 85 Ω, 100 Ω, 120 Ω, and 150 Ω.	"Programmable Transmitter Termination" section in the *Transceiver Architecture in Stratix IV Devices* chapter and the *DC and Switching Characteristics for Stratix IV Devices* section.
What is the voltage output differential (V_{OD}) control setting?	This option selects the V_{OD} of the transmitter buffer. The available V_{OD} settings change based on the transmitter termination resistance value.	"Programmable Output Differential Voltage" section in the *Transceiver Architecture in Stratix IV Devices* chapter and the *DC and Switching Characteristics for Stratix IV Devices* section.
What is the pre-emphasis first post-tap setting (% of VOD)?	This option sets the amount of pre-emphasis on the transmitter buffer using first post-tap.	"Programmable Pre-Emphasis" section in the *Transceiver Architecture in Stratix IV Devices* chapter.

Table 1–6. MegaWizard Plug-In Manager Options (TX Analog Screen) (Part 2 of 2)

ALTGX Setting	Description	Reference
What is the pre-emphasis pre-tap setting (% of VOD)?	This option sets the amount of pre-emphasis on the transmitter buffer using pre-tap.	"Programmable Pre-Emphasis" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
What is the pre-emphasis second post-tap setting (% of VOD)?	This option sets the amount of pre-emphasis on the transmitter buffer using second post-tap.	"Programmable Pre-Emphasis" section in the *Transceiver Architecture in Stratix IV Devices* chapter.

Reconfiguration Settings

This section describes the various dynamic reconfiguration modes and settings for Stratix IV GX and GT transceivers.

In Reconfiguration Settings, when you enable the **Enable Channel and Transmitter PLL reconfiguration** option, the following screens become available:

- Modes
- Transmitter PLLs
- Clocking/Interface

The following sections describe these screens and their corresponding settings.

Modes Screen for the Reconfiguration Settings

Figure 1–9 shows the **Modes** screen, listing the various dynamic reconfiguration modes available.

Figure 1–9. MegaWizard Plug-In Manager—Reconfiguration Settings

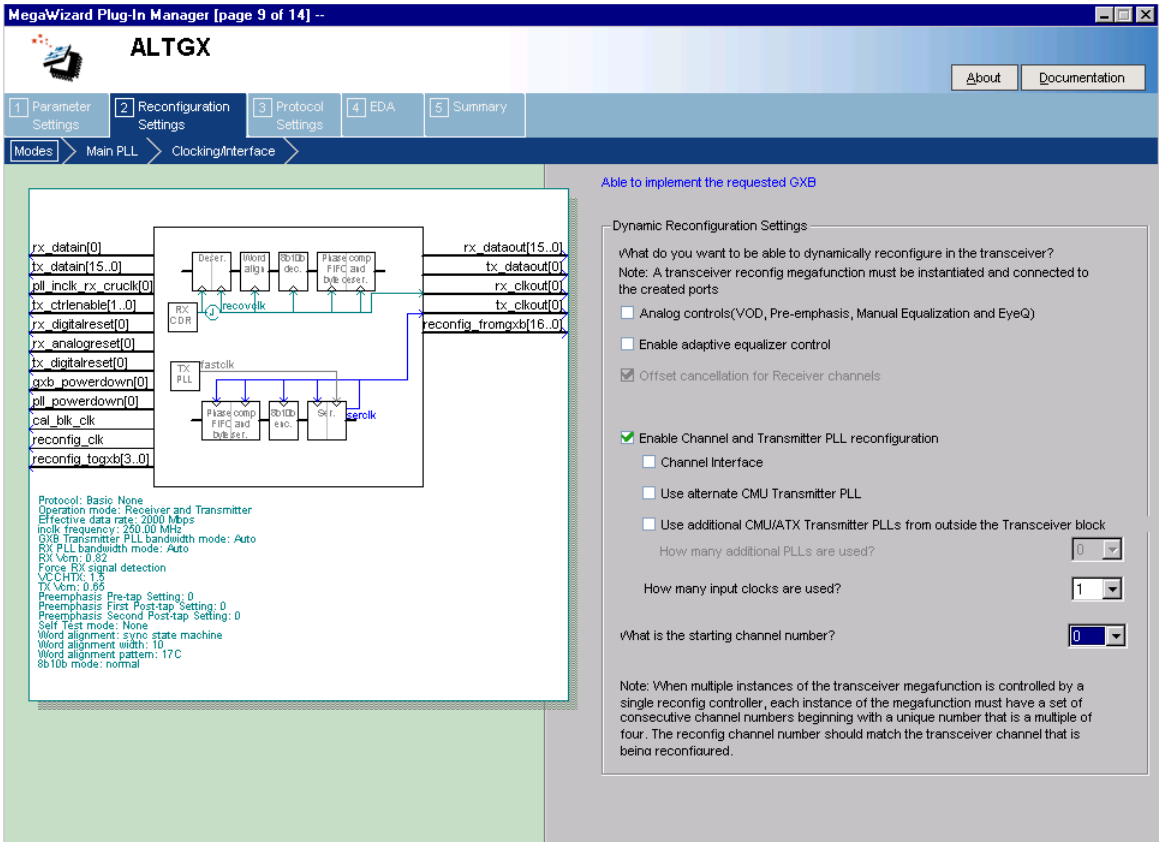


Table 1–7 lists the different options available in the **Modes** screen of the MegaWizard Plug-In Manager for your ALTGX custom megafunction variation.

Table 1–7. MegaWizard Plug-In Manager Options (Modes Screen) (Part 1 of 2)

ALTGX Setting	Description	Reference
Dynamic Reconfiguration Settings		
What do you want to be able to dynamically reconfigure in the transceiver?	The different dynamic reconfiguration modes available are listed in the **Reconfiguration Settings** screen. Based on which portion of the transceiver you want to reconfigure, select the corresponding options and connect the ALTGX_RECONFIG instance to the ALTGX instance. ■ Analog controls (VOD, Pre-emphasis, and Manual Equalization and EyeQ)—Enable this option to dynamically reconfigure the PMA control settings similar to VOD, pre-emphasis, manual equalization, DC gain, and EyeQ. ■ Enable adaptive equalizer control—Selecting this option enables the Adaptive Equalization (AEQ) hardware and provides the following additional ports: ■ `aeq_togxb[]` ■ `aeq_fromgxb[]` These ports provide the interface between the receiver channel and the dynamic reconfiguration controller. ■ Offset cancellation for receiver channels—This option is enabled by default for **Receiver only** and **Receiver and Transmitter** configurations. It is not available for **Transmitter only** configurations. Ensure that you connect a dynamic reconfiguration controller to all the transceiver channels in the design.	"Dynamic Reconfiguration Modes Implementation" section, "PMA Controls Reconfiguration Mode Details" *section,* "Enabling the AEQ Control Logic and AEQ Hardware" section, and the "Offset Cancellation Feature" section in the *Dynamic Reconfiguration in Stratix IV Devices* chapter.
Enable Channel and Transmitter PLL Reconfiguration	You must enable this option to reconfigure one of the following: Transmitter local divider block, CMU PLL, Transceiver channel, or Both the CMU PLL and transceiver channel. ■ Channel Interface—This option allows channel interface reconfiguration. ■ Use alternate CMU Transmitter PLL—This option sets up the alternate PLL so that the transceiver channel can optionally select between the output of the main and alternate transmitter PLL. Use additional CMU/ATX Transmitter PLLs from outside the Transceiver Block—This option allows you to select a maximum of four transmitter PLLs. For example, you can select the ATX PLL as the main PLL and three additional PLLs. ■ How many additional PLLs are used?—You can have a maximum of two PLLs outside the transceiver block.	"Transceiver Channel Reconfiguration Modes Details" *section,* "FPGA Fabric-Transceiver Channel Interface Selection" section, "Transceiver Channel Reconfiguration Modes Details" section. and the "Multi-PLL Settings" *section* in the *Transceiver Architecture in Stratix IV Devices* chapter.

Table 1–7. MegaWizard Plug-In Manager Options (Modes Screen) (Part 2 of 2)

ALTGX Setting	Description	Reference
How many input clocks are used?	Enter the number of input clocks available for selection for the transmitter PLLs and receiver PLL. You have a choice of up to 10 input clock sources (clock 1, clock 2, and so on).	"Guidelines for Specifying the Input Reference Clocks" *section* in the *Dynamic Reconfiguration in Stratix IV Devices* chapter.
What is the starting channel number?	You must set the starting channel number of the first ALTGX instance controlled by the dynamic reconfiguration controller to **0**. Set the starting channel number of the consecutive ALTGX instances controlled by the same dynamic reconfiguration controller, if any, in the next available multiples of 4.	"Logical Channel Addressing while Reconfiguring the PMA Controls" *section* in the *Dynamic Reconfiguration in Stratix IV Devices* chapter.

Transmitter PLL Settings

Depending on the number of additional PLLs you select in the **How many additional PLLs are used?** option in Reconfiguration Settings, the corresponding PLL screens become available.

Each of these PLL screens have the same settings available for selection. Table 1–8 lists each of these settings.

The Main PLL is the PLL you configure in the **General** screen. Therefore, some of the options are already enabled or disabled for this PLL. Some of the options differ when compared with the additional transmitter PLLs.

Figure 1–10 shows the options available on the **Main PLL** screen of the ALTGX MegaWizard Plug-In Manager.

Figure 1–10. MegaWizard Plug-In Manager Options—Main PLL Screen

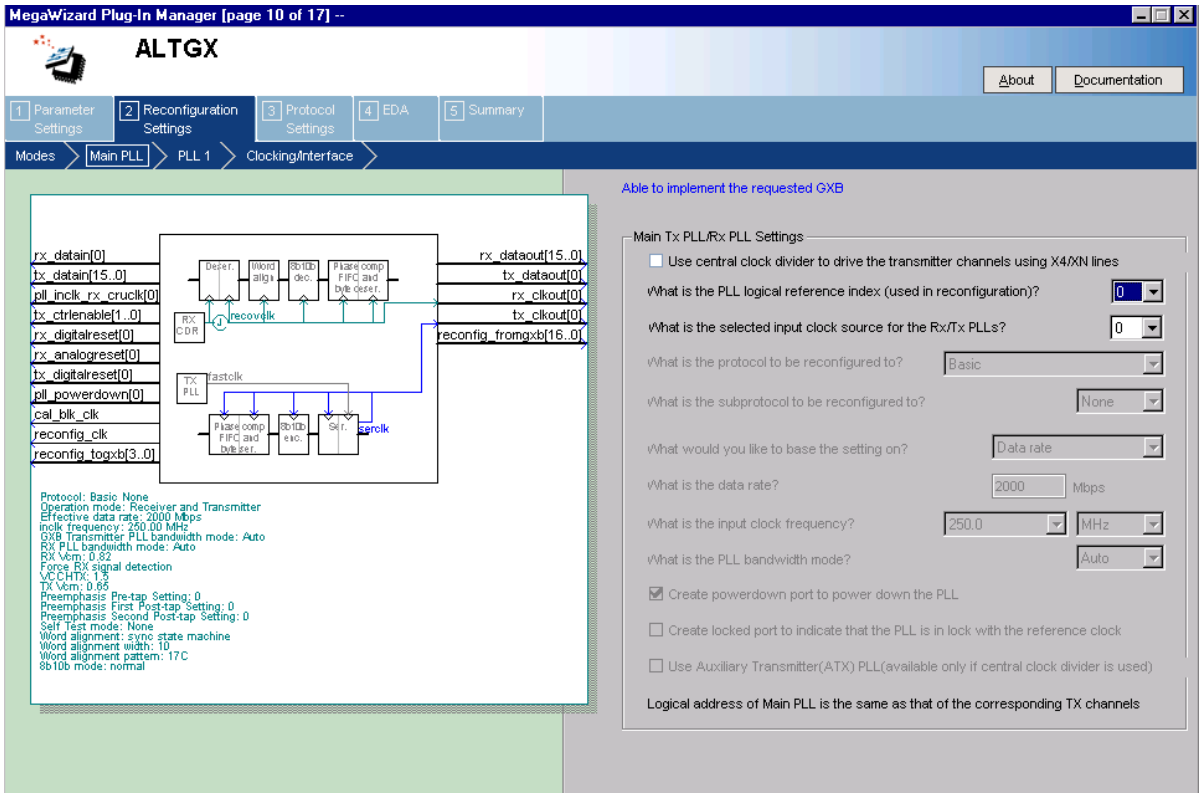


Table 1–8 lists the available options on the **Main PLL** screen of the MegaWizard Plug-In Manager for your ALTGX custom megafunction variation.

Table 1–8. MegaWizard Plug-In Manager Options (Main PLL Screen) (Part 1 of 3)

ALTGX Setting	Description	Reference
Main Tx PLL/Rx PLL Settings		
Use central clock divider to drive the transmitter channels using ×4/×N lines	If this option is enabled, the transmitter PLL is outside the transceiver block. If this option is disabled, the transmitter PLL is one of the CMU PLLs within the same transceiver block.	"Selecting the PLL Logical Reference Index for Additional PLLs" and the "Multi-PLL Settings" sections in the *Dynamic Reconfiguration in Stratix IV Devices* chapter.
What is the PLL logical reference index (used in reconfiguration)?	The PLL logical reference index is selected based on the location of the alternate PLL. If the **Use central clock divider to drive the transmitter channels using ×4/×N lines** option is unchecked this must be 0 or 1, otherwise this must be 2 or 3.	"Selecting the PLL Logical Reference Index for Additional PLLs" and "Selecting the Logical Reference Index of the CMU PLL" *sections* in the *Dynamic Reconfiguration in Stratix IV Devices* chapter.

Table 1–8. MegaWizard Plug-In Manager Options (Main PLL Screen) (Part 2 of 3)

ALTGX Setting	Description	Reference
What is the selected input clock source for the Rx/Tx PLLs?	Assign identification numbers to all input reference clocks that are used by the transmitter PLLs in their corresponding PLL screens. You can set up a maximum of 10 input reference clocks and assign identification numbers from 1 to 10.	"Guidelines for Specifying the Input Reference Clocks" *section* in the *Dynamic Reconfiguration in Stratix IV Devices* chapter.
What is the protocol to be reconfigured to?	Select the desired functional mode here, if you intend to dynamically reconfigure the transceiver channel to a different functional mode using the alternate transmitter PLL.	"Channel Reconfiguration with Transmitter PLL Select Mode Details" in the *Dynamic Reconfiguration in Stratix IV Devices* chapter.
What is the subprotocol to be reconfigured to?	This option is not available for **Basic**, **(OIF) CEI PHY Interface**, **Serial RapidIO**, **GIGE**, and **XAUI** functional modes. This option is available for the following protocols and subprotocols: ■ Protocol = **PCIe**; Subprotocols = Gen 1 and Gen 2 ■ Protocol = **SDI**; Subprotocols = 3G and HD ■ Protocol = **SONET/SDH**; Subprotocols = OC12, OC48, and OC96	—
What would you like to base the setting on?	This option is available only for **Basic** mode.You can select one of the following options for the alternate transmitter PLL: ■ **Input clock frequency**—Selecting this option allows you to enter your input clock frequency. Based on the value you enter, the ALTGX MegaWizard Plug-In Manager populates the data rate options in the **What is the effective data rate?** field. The ALTGX MegaWizard Plug-In Manager determines these data rate options depending on the available multiplier settings. ■ **Data rate**—Selecting this option allows you to enter the transceiver channel serial data rate. Based on the value you enter, the ALTGX MegaWizard Plug-In Manager populates the input reference clock frequency options in the **What is the input clock frequency?** field. The ALTGX MegaWizard Plug-In Manager determines these input reference clock frequencies depending on the available multiplier settings.	—
What is the data rate?	These settings are to dynamically reconfigure the transceiver channel to listen to the alternate transmitter PLL. ■ If you select the data rate option in the **What would you like to base the setting on?** field, the ALTGX MegaWizard Plug-In Manager allows you to specify the effective serial data rate value in this field. ■ If you select the **input clock frequency** option in the **What would you like to base the setting on?** field, the ALTGX MegaWizard Plug-In Manager displays the list of effective serial data rates in this field.	—

Table 1–8. MegaWizard Plug-In Manager Options (Main PLL Screen) (Part 3 of 3)

ALTGX Setting	Description	Reference
What is the input clock frequency?	These settings are to dynamically reconfigure the transceiver channel to listen to the alternate transmitter PLL. ■ If you select the **input clock frequency** option in the **What would you like to base the setting on?** field, the ALTGX MegaWizard Plug-In Manager displays the list of effective serial data rates in this field. ■ If you select the data rate option in the **What would you like to base the setting on?** field, the ALTGX MegaWizard Plug-In Manager allows you to specify the effective serial data rate value in this field.	"CMU PLL Reconfiguration Mode Details" section in the *Dynamic Reconfiguration in Stratix IV Devices* chapter.
What is the PLL bandwith mode?	The available options are **Auto**, **Low**, **Medium**, and **High**. Select the appropriate option based on your system requirements.	"PLL Bandwidth Setting" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
Create powerdown port to power down the PLL.	Each transceiver block has two CMU PLLs. Each CMU/ATX PLL has a dedicated power down signal called `pll_powerdown`. This signal powers down the CMU PLL.	"User Reset and Power-Down Signals" section in the *Reset Control and Power Down in Stratix IV Devices* chapter.
Create locked port to indicate that the PLL is in lock with the reference clock.	Each CMU/ATX PLL has a dedicated `pll_locked` signal that is fed to the FPGA fabric to indicate when the PLL is locked to the input reference clock.	"User Reset and Power-Down Signals" section in the *Reset Control and Power Down in Stratix IV Devices* chapter.
Use Auxiliary Transmitter (ATX) PLL (available only if central clock divider is used)	This option is only available for certain data rates. Refer to the *DC and Switching Characteristics for Stratix IV Devices* chapter for the supported data rates. This option enables the auxiliary transmitter PLL. This is a low-jitter PLL that resides between the transceiver blocks and can be used as a transmitter PLL.	"Auxiliary Transmit (ATX) PLL Block" section in the *Transceiver Architecture in Stratix IV Devices* chapter and the *DC and Switching Characteristics for Stratix IV Devices* section.

Clocking/Interface Screen for the Reconfiguration Settings

Figure 1–11 shows the **Clocking/Interface** screen of the ALTGX MegaWizard Plug-In Manager for the Reconfiguration settings.

Figure 1–11. MegaWizard Plug-In Manager Options (Clocking/Interface Screen)

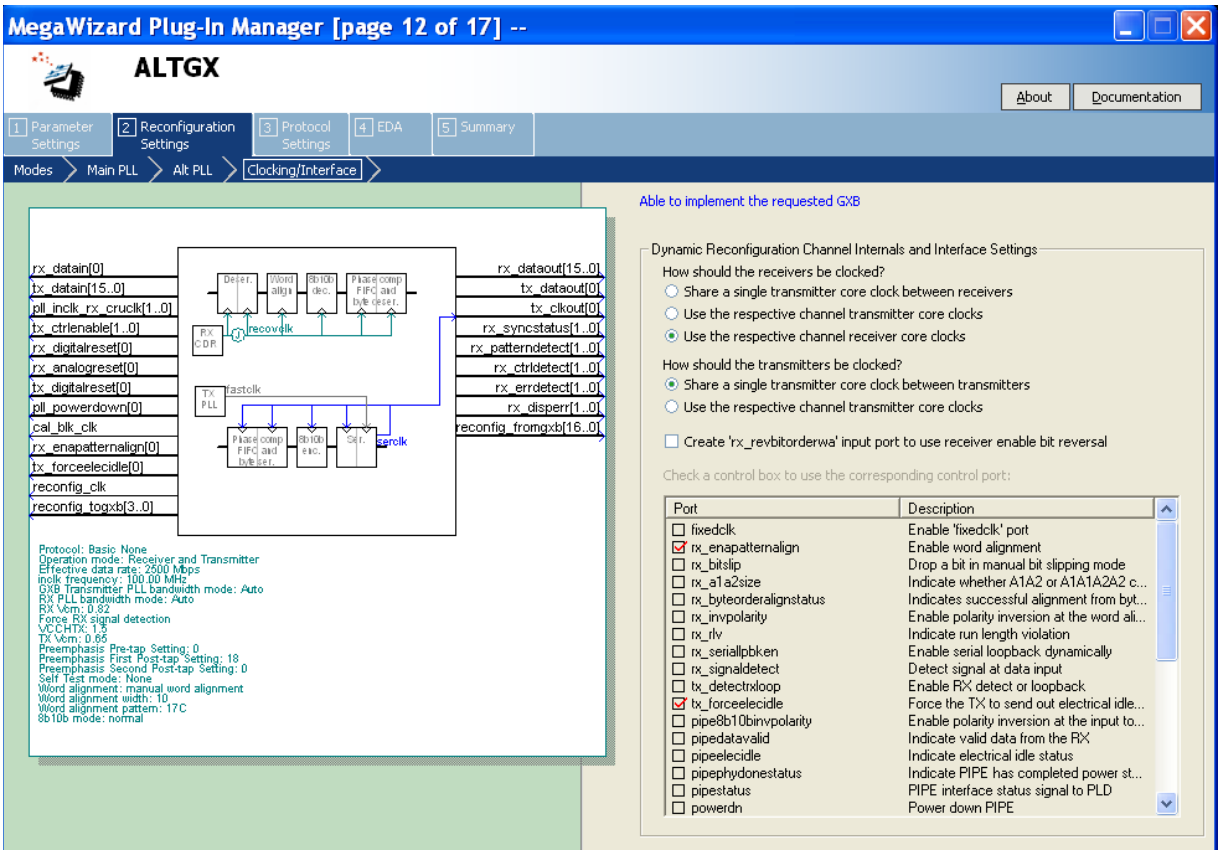


Table 1–9 lists the available options on the **Clocking/Interface** screen of the MegaWizard Plug-In Manager for your ALTGX custom megafunction variation.

This screen is not available for Basic (PMA Direct) ×1 and xN configurations.

Table 1–9. MegaWizard Plug-In Manager Options (Clocking/Interface Screen) (Part 1 of 2)

ALTGX Setting	Description	Reference
Dynamic Reconfiguration Channel Internal and Interface Settings		
How should the receivers be clocked?	Select one of the following available options: ■ **Share a single transmitter core clock between receivers** ■ **Use the respective channel transmitter core clocks** ■ **Use the respective channel receiver core clocks**	"Clocking/Interface Options" section in the *Dynamic Reconfiguration in Stratix IV Devices* chapter.

Table 1–9. MegaWizard Plug-In Manager Options (Clocking/Interface Screen) (Part 2 of 2)

ALTGX Setting	Description	Reference
How should the transmitters be clocked?	Select one of the following available options: ■ **Share a single transmitter core clock between transmitters** ■ **Use the respective channel transmitter core clocks**	"Clocking/Interface Options" section in the *Dynamic Reconfiguration in Stratix IV Devices* chapter.
Create an 'rx_revbitorderwa' input port to use receiver enable bit reversal	This optional input port allows you to dynamically reverse the bit order at the output of the receiver word aligner.	"Word Aligner" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
Check a control box to use the corresponding control port.	You can select various control and status signals depending on what protocol(s) you intend to dynamically reconfigure the transceiver channel to.	"FPGA Fabric-Transceiver Channel Interface Selection" section in the *Dynamic Reconfiguration in Stratix IV Devices* chapter.

Protocol Settings

This section describes the various screens available to set up the PCS blocks of the Stratix IV transceiver.

Protocol Settings are not available for Basic (PMA Direct) functional mode.

Based on the protocol you select in the **General** screen of Parameter Settings, the screens listed in Table 1–10 become available.

Table 1–10. Protocol Settings

Protocols	Protocol Settings Screens		
	8B/10B	Word Aligner	Rate match/Byte order
Basic	Y (Basic/8B10B)	Y	Y
Deterministic Latency	Y (Det. Latency/8B10B)	Y	—
SDI	Y (SDI/8B10B)	Y	—
Serial RapidIO	Y (Serial RapidIO/8B10B)	Y	Y

The following sections describe these screens and the available settings for each of them.

8B10B Screen for the Protocol Settings

Figure 1–12 shows the **8B10B** screen of the MegaWizard Plug-In Manager for the Protocol Settings.

Figure 1–12. MegaWizard Plug-In Manager—ALTGX (8B10B Screen)

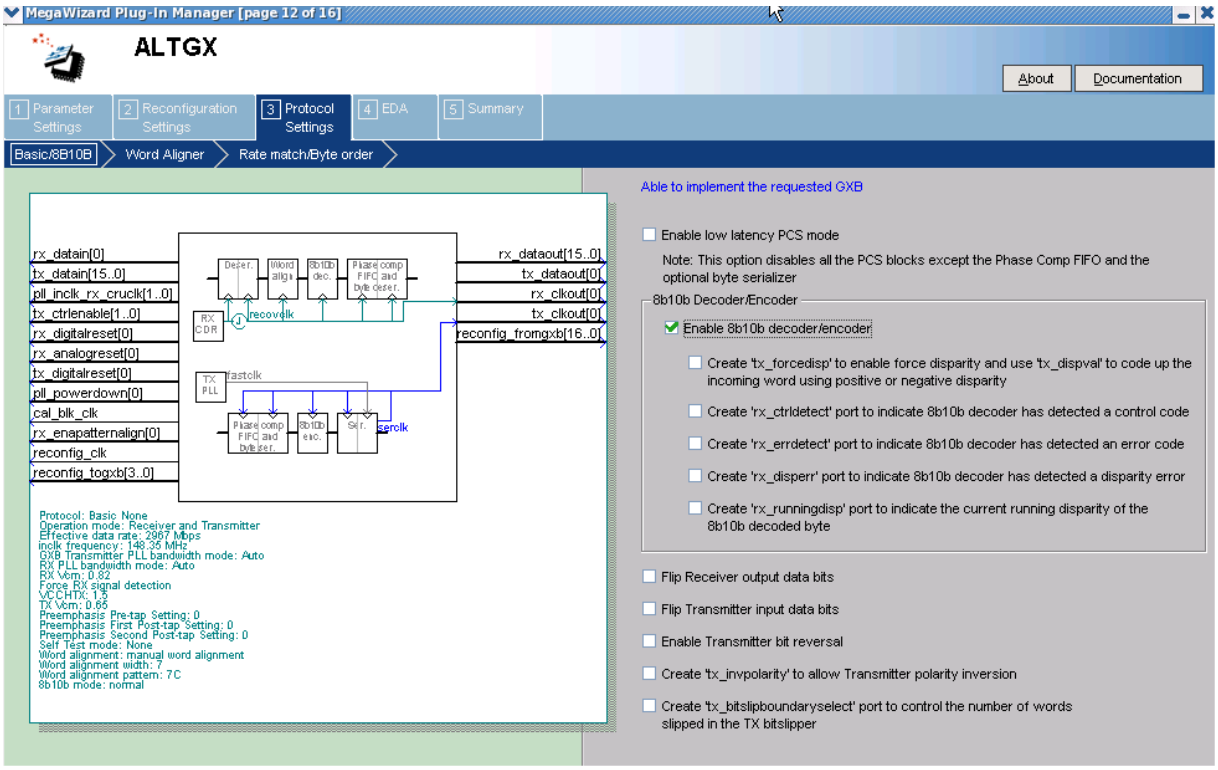


Table 1–11 lists the available options on the **8B10B** screen of the MegaWizard Plug-In Manager for your ALTGX custom megafunction variation.

Table 1–11. MegaWizard Plug-In Manager Options (8B10B Screen) (Part 1 of 3)

ALTGX Setting	Description	Reference
Enable low latency PCS mode.	This option disables all the PCS blocks except the Transmitter/Receiver Phase Comp FIFO and optional byte serializer/de-serializer.	"Low Latency PCS Datapath" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
Enable 8B/10B decoder/encoder.	This option is available if the channel width is 8-bits, 16-bits, or 32-bits.	"8B/10B Decoder" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
Create a `tx_forcedisp` to enable Force disparity and use `tx_dispval` to code up the incoming word using positive or negative disparity.	8B/10B encoder force disparity control: ■ When asserted high—forces the 8B/10B encoder to encode the data on the `tx_datain` port with a positive or negative disparity depending on the `tx_dispval` signal level. ■ When de-asserted low—the 8B/10B encoder encodes the data on the `tx_datain` port according to the 8B/10B running disparity rules.	"8B/10B Encoder" and "Transceiver Port Lists" sections in the *Transceiver Architecture in Stratix IV Devices* chapter.

Table 1–11. MegaWizard Plug-In Manager Options (8B10B Screen) (Part 2 of 3)

ALTGX Setting	Description	Reference
Create an rx_ctrldetect port to indicate 8B/10B decoder has detected a control code.	This is an output status signal that the 8B/10B decoder forwards to the FPGA fabric. This signal indicates whether the decoded 8-bit code group is a data or control code group on this port. If the received 10-bit code group is one of the 12 control code groups (/Kx.y/) specified in the IEEE802.3 specification, this signal is driven high. If the received 10-bit code group is a data code group (/Dx.y/), this signal is driven low. The signal width is 1, 2, and 4 bits for a channel width of 8 bits, 16 bits, and 32 bits, respectively.	"8B/10B Decoder" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
Create an rx_errdetect port to indicate 8B/10B decoder has detected an error code.	This is an output status signal that the 8B/10B decoder forwards to the FPGA fabric and indicates an 8B/10B code group violation. This signal is asserted high if the received 10-bit code group has a code violation or disparity error. It is used along with the rx_disperr signal to differentiate between a code violation error and/or a disparity error. The signal width is 1, 2 and 4 bits for a channel width of 8 bits, 16 bits, and 32 bits, respectively.	"8B/10B Decoder" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
Create an rx_disperr port to indicate 8B/10B decoder has detected a disparity error.	This is an output status signal that the 8B/10B decoder forwards to the FPGA fabric. This signal is asserted high if the received 10-bit code or data group has a disparity error. When this signal goes high, rx_errdetect is also asserted high. The signal width is 1, 2, and 4 bits for a channel width of 8 bits, 16 bits, and 32 bits, respectively.	"8B/10B Decoder" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
Create an rx_runningdisp port to indicate the current running disparity of the 8B10B decoded byte.	This is an output status signal that the 8B/10B decoder forwards to the FPGA fabric to indicate the current running disparity of the 8B/10B decoded byte.	"8B/10B Decoder" section of Table 1-77 in the *Transceiver Architecture in Stratix IV Devices* chapter.
Flip receiver output data bits.	This option reverses the bit order of the parallel receiver data at a byte level at the output of the receiver phase compensation FIFO. For example, if the 16-bit parallel receiver data at the output of the receiver phase compensation FIFO is '10111100 10101101' (16'hBCAD), enabling this option reverses the data on rx_dataout port to '00111101 10110101' (16'h3DB5).	—
Flip transmitter input data bits.	This option reverses the bit order of the parallel transmitter data at a byte level at the input of the transmitter phase compensation FIFO. For example, if the 16-bit parallel transmitter data at the tx_datain port is '10111100 10101101' (16'hBCAD), enabling this option reverses the input data to the transmitter phase compensation FIFO to '00111101 10110101' (16'h3DB5).	—

Table 1–11. MegaWizard Plug-In Manager Options (8B10B Screen) (Part 3 of 3)

ALTGX Setting	Description	Reference
Enable transmitter bit reversal.	Enabling this option in: ■ Single-width mode—the 8-bit `D[7:0]` or 10-bit `D[9:0]` data at the input of the serializer gets rewired to `D[0:7]` or `D[0:9]`, respectively. ■ Double-width mode—the 16-bit `D[15:0]` or 20-bit `D[19:0]` data at the input of the serializer gets rewired to `D[0:15]` or `D[0:19]`, respectively. For example, if the 8-bit parallel data at the input of the serializer is '00111101', enabling this option reverses this serializer input data to '10111100.'	"Transmitter Bit Reversal" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
Create a `tx_invpolarity` port to allow Transmitter polarity inversion.	This optional port allows you to dynamically reverse the polarity of every bit of the data word fed to the serializer in the transmitter data path. Use this option when the positive and negative signals of the differential output from the transmitter (`tx_dataout`) are erroneously swapped on the board.	"Transmitter Polarity Inversion" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
Create `tx_bitslipboundary select` port to control the number of words slipped in the TX bitslipper.	You can only select this option when you use the **Transmitter only** or **Receiver and Transmitter** operation mode. This option enables the `tx_bitslipboundaryselect` input to control the number of bits slipped in the TX bitslipper.	—

Word Aligner Screen for the Protocol Settings

Figure 1–13 shows the **Word Aligner** screen of the MegaWizard Plug-In Manager for the Protocol Settings.

Figure 1–13. MegaWizard Plug-In Manager—ALTGX (Word Aligner Screen)

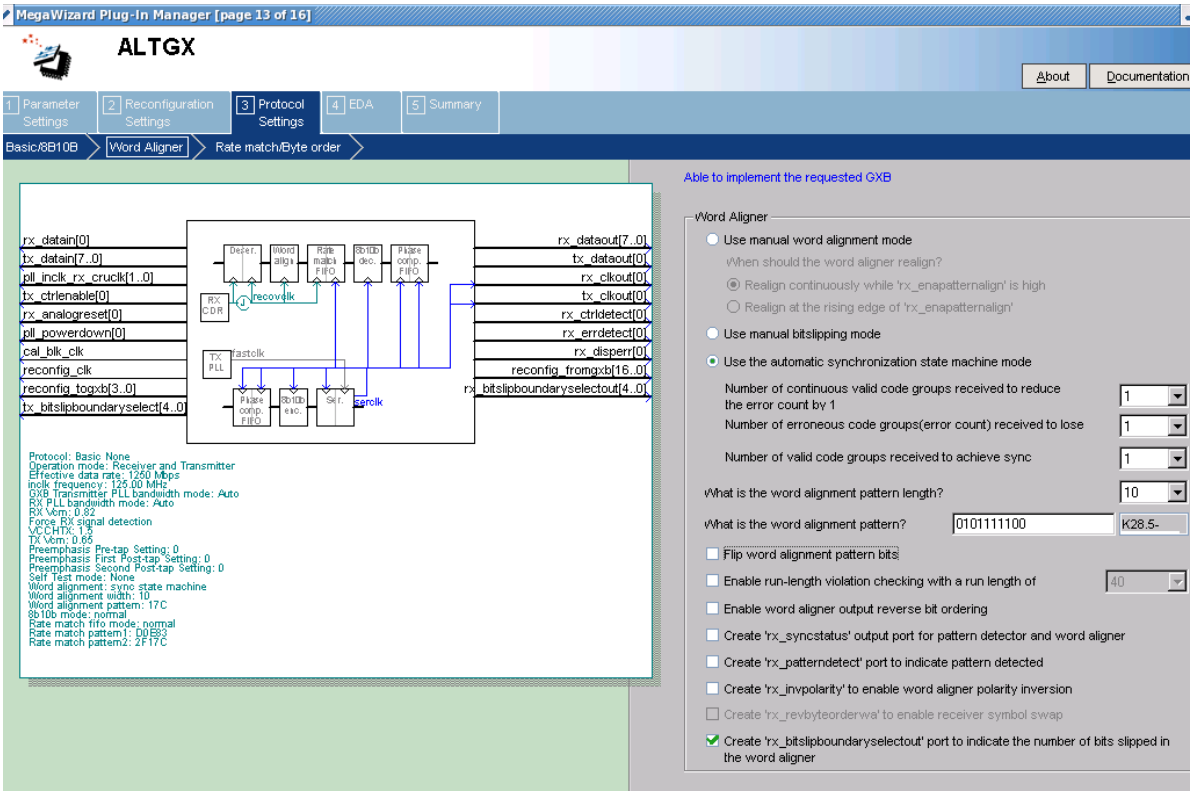


Table 1–12 lists the available options on the **Word Aligner** screen of the MegaWizard Plug-In Manager for your ALTGX custom megafunction variation.

The word aligner and rate matcher operations and patterns are pre-configured for PCIe, GIGE, and XAUI modes, and cannot be altered.

Table 1–12. MegaWizard Plug-In Manager Options (Word Aligner Screen) (Part 1 of 4)

ALTGX Setting	Description	Reference
Use manual word alignment mode.	Enabling this option sets the word aligner in Manual Alignment mode. In Manual Alignment mode, the word aligner operation is controlled by the input signal `rx_enapatternalign`.	"Manual Alignment Mode Word Aligner with 8-bit PMA-PCS Interface Modes" and "Manual Alignment Mode Word Aligner with 10-bit PMA-PCS Interface Modes" sections in the *Transceiver Architecture in Stratix IV Devices* chapter.
When should the word aligner realign?	Two options are available in manual mode: ■ Realign continuously while the `rx_enapatternalign` signal is high. ■ Realign at the rising edge of the `rx_enapatternalign` signal.	"Manual Alignment Mode Word Aligner with 8-bit PMA-PCS Interface Modes" and "Manual Alignment Mode Word Aligner with 10-bit PMA-PCS Interface Modes" sections in the *Transceiver Architecture in Stratix IV Devices* chapter.
Use manual bitslipping mode.	This option sets the word aligner in Bit-Slip mode. Enabling this option creates an input signal `rx_bitslip` to control the word aligner. At every rising edge of the `rx_bitslip` signal, the bit slip circuitry slips one bit into the received data stream, effectively shifting the word boundary by one bit. **SDI** Because word alignment and framing occur after de-scrambling, the word aligner in the receiver data path is not useful in SDI systems. Altera recommends driving the ALTGX `rx_bitslip` signal low to prevent the word aligner from inserting bits in the received data stream.	"Word Aligner" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
Use the Automatic synchronization state machine mode.	This option sets the word aligner in Automatic Synchronization State Machine mode. This mode is available only in Single-width mode for 8B/10B encoded data: ■ 10-bit PCS-PMA Interface where the 8B/10B encoder is enabled or ■ 10-bit PCS-PMA Interface where the 8B/10B is disabled but the data is already 8B/10B encoded	"Automatic Synchronization State Machine Mode Word Aligner with 10-bit PMA-PCS Interface Mode" section in the *Transceiver Architecture in Stratix IV Devices* chapter.

Table 1–12. MegaWizard Plug-In Manager Options (Word Aligner Screen) (Part 2 of 4)

ALTGX Setting	Description	Reference
Number of consecutive valid words before synch state is reached.	Use this option in Automatic Synchronization State Machine mode to indicate the number of consecutive valid words that it must receive between erroneous words to reduce the error count by one. The `rx_syncstatus` stays high as long as the error count is less than the programmed error count.	"Automatic Synchronization State Machine Mode Word Aligner with 10-bit PMA-PCS Interface Mode" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
Number of bad data words before loss of synch state.	Use this option in Automatic Synchronization State Machine mode to indicate the number of bad data words (error count) that it must receive to lose synchronization. The loss-of-synch is indicated by the `rx_syncstatus` signal going low.	"Automatic Synchronization State Machine Mode Word Aligner with 10-bit PMA-PCS Interface Mode" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
Number of valid patterns before synch state is reached.	Use this option in Automatic Synchronization State Machine mode to indicate the number of word alignment patterns that it must receive without intermediate erroneous code groups to achieve synchronization. The `rx_syncstatus` signal is driven high to indicate that synchronization has been achieved.	"Automatic Synchronization State Machine Mode Word Aligner with 10-bit PMA-PCS Interface Mode" section in the *Transceiver Architecture in Stratix IV Devices* chapter.

What is the word alignment pattern length?	This option sets the word alignment pattern length. The available choices depend on the following conditions:
	■ Whether the data is 8B/10B encoded or not
	■ Which mode is used in Single-width mode:
	  ■ for 8-bit PCS-PMA Interface (8B/10B encoder disabled), only 16 bits are allowed.
	  ■ for 10-bit PCS-PMA, 7 and 10 bits are allowed.
	■ Which mode is used in Double-width mode:
	  ■ for 16-bit PCS-PMA Interface (8B/10B encoder disabled), 8, 16, and 32 bits are allowed.
	  ■ for 20-bit PCS-PMA Interface, 7, 10, and 20 bits are allowed.
		"Word Aligner in Single-Width Mode" and "Word Aligner in Double-Width Mode" sections in the *Transceiver Architecture in Stratix IV Devices* chapter.

What is the word alignment pattern?	Enter the word alignment pattern in MSB to LSB order with MSB at the left most bit position. The length of the alignment pattern is based on the **What is the word alignment pattern length?** option. The word aligner restores the word boundary by looking for the pattern that you enter here. For example, if you want to set the word alignment pattern to /K28.5/: ■ You must enter the word alignment pattern length: **10**. ■ You must enter the word alignment pattern: **0101111100** (17C).	"Word Aligner in Single-Width Mode" and "Word Aligner in Double-Width Mode" sections in the *Transceiver Architecture in Stratix IV Devices* chapter.

Table 1–12. MegaWizard Plug-In Manager Options (Word Aligner Screen) (Part 3 of 4)

ALTGX Setting	Description	Reference
Flip word alignment pattern bits.	When this option is enabled, the ALTGX MegaWizard Plug-In Manager flips the bit order of the pattern that you enter in the **What is the word alignment pattern?** option and uses the flipped version as the word alignment pattern. For example, if you enter '0101111100' (17C) as the word alignment pattern and enable this option, the word aligner uses '0011111010' as the word alignment pattern.	—
Enable run-length violation checking with a run length of:	This option creates the output signal `rx_rlv`. Enabling this option also activates the run-length violation circuit. If the number of continuous 1s and 0s exceeds the number that you set in this option, the run-length violation circuit asserts the `rx_rlv` signal. The `rx_rlv` signal is asynchronous to the receiver data path and is asserted for a minimum of two recovered clock cycles in Single-width mode. Similarly, it is asserted for a minimum of three recovered clock cycles in Double-width mode. The run length limits are as follows: ■ Single-width mode: ■ 8-bit and 16-bit channel width: 4 to 128 in increments of four ■ 10-bit and 20-bit channel width: 5 to 160 in increments of five ■ Double-width mode: ■ 16-bit and 32-bit channel width: 8 to 512 in increments of eight ■ 20-bit and 40-bit channel width: 10 to 640 in increments of 10	"Programmable Run Length Violation Detection" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
Enable word aligner output reverse bit ordering.	In manual bit-slip mode, this option creates an input port `rx_revbitorderwa` to dynamically reverse the bit order at the output of the receiver word aligner.	"Receiver Bit Reversal" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
Create an `rx_syncstatus` output port for pattern detector and word aligner.	This is an output status signal that the word aligner forwards to the FPGA fabric to indicate that synchronization has been achieved. This signal is synchronous with the parallel receiver data on the `rx_dataout` port. This signal is not available in bit-slip mode. Signal width is 1, 2, and 4 bits for a channel width of 8-bits/10-bits, 16-bits/20-bits, and 32-bits/40-bits, respectively.	Table 1-77, "Word Aligner in Single-Width Mode" and "Word Aligner in Double-Width Mode" sections in the *Transceiver Architecture in Stratix IV Devices* chapter.
Create an `rx_patterndetect` port to indicate pattern detected.	This is an output status signal that the word aligner forwards to the FPGA fabric to indicate that the word alignment pattern programmed has been detected in the current word boundary. Signal width is 1, 2, and 4 bits for a channel width of 8-bits/10-bits, 16-bits/20-bits, and 32-bits/40-bits, respectively.	Table 1-77 *and* "Word Aligner in Single-Width Mode" and "Word Aligner in Double-Width Mode" sections in the *Transceiver Architecture in Stratix IV Devices* chapter.

Table 1–12. MegaWizard Plug-In Manager Options (Word Aligner Screen) (Part 4 of 4)

ALTGX Setting	Description	Reference
Create an rx_invpolarity port to enable word aligner polarity inversion.	This optional port allows you to dynamically reverse the polarity of every bit of the received data at the input of the word aligner. Use this option when the positive and negative signals of the differential input to the receiver (rx_datain) are erroneously swapped on the board.	"Receiver Polarity Inversion" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
Create an rx_revbyteorderwa to enable Receiver symbol swap.	This is an optional input port that is available only in the double-width mode. It creates an rx_revbyteorderwa port to dynamically swap the MSByte and LSByte of the data at the output of the word aligner in the receiver data path. Enabling this option compensates for the erroneous swapping of bytes at the upstream transmitter and corrects the data received by the downstream systems. For example, if the 16-bit output of the word aligner is 0B0A, asserting the rx_revbyteorderwa signal swaps the two bytes so the output becomes 0A0B.	"Receiver Byte Reversal in Basic Double-Width Modes" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
Create rx_bitslipboundaryselectout port to indicate the number of bits slipped in the word aligner.	This option is available for selection only when you are in **Receiver only** or **Receiver and Transmitter** operation mode. This option enables the rx_bitslipboundaryselectout output to indicate the number of bits slipped in the word aligner.	—

Rate Match/Byte Order Screen for the Protocol Settings

Figure 1–14 shows the **Rate Match/Byte Order** screen of the MegaWizard Plug-In Manager for the Protocol Settings.

Figure 1–14. MegaWizard Plug-In Manager—ALTGX (Rate Match/Byte Order Screen)

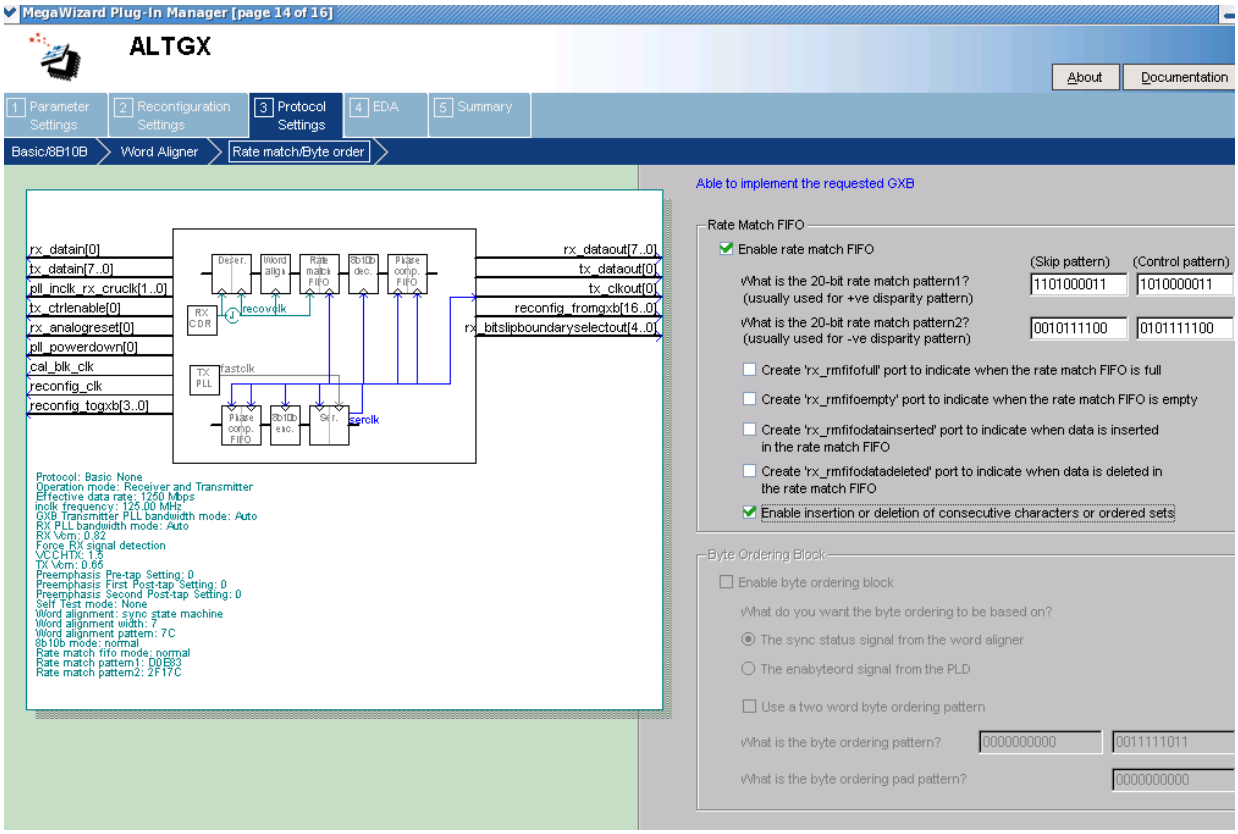


Table 1–13 lists the available options on the **Rate Match/Byte Order** screen of the MegaWizard Plug-In Manager for your ALTGX custom megafunction variation.

Table 1–13. MegaWizard Plug-In Manager Options (Rate Match/Byte Order Screen) (Part 1 of 3)

ALTGX Setting	Description	Reference
Enable rate match FIFO.	This option enables the rate match (clock rate compensation) FIFO. The rate match block consists of a 20-word deep FIFO. Depending on the PPM difference, the rate match FIFO controls insertion and deletion of skip characters based on the 20-bit rate match pattern you enter in the **What is the 20-bit rate match pattern1?** and **What is the 20-bit rate match pattern2?** options. To enable this block: ■ The transceiver channel must have both the transmitter and the receiver channels instantiated. You must select the **Receiver and Transmitter** option in the **What is the operation mode?** field in the **General** screen. ■ You must also enable the 8B/10B encoder/decoder in the **8B10B** screen. The rate match block is capable of compensating up to ±300 PPM difference between the upstream transmitter clock and the local receiver's input reference clock.	"Rate Match FIFO in Basic Single-Width Mode" and "Rate Match FIFO in Basic Double-Width Mode" sections in the *Transceiver Architecture in Stratix IV Devices* chapter.
What is the 20-bit rate match pattern1? (usually used for +ve disparity pattern)	Enter a 10-bit skip pattern and a 10-bit control pattern. In the **skip pattern** field, you must choose a 10-bit code group that has neutral disparity. When the rate matcher receives the 10-bit control pattern followed by the 10-bit skip pattern, it inserts or deletes the 10-bit skip pattern as necessary to avoid rate match FIFO overflow or underflow conditions. (1)	"Rate Match FIFO in Basic Single-Width Mode" and "Rate Match FIFO in Basic Double-Width Mode" sections in the *Transceiver Architecture in Stratix IV Devices* chapter.
What is the 20-bit rate match pattern2? (usually used for -ve disparity pattern)	Enter a 10-bit skip pattern and a 10-bit control pattern. In the **skip pattern** field, you must choose a 10-bit code group that has neutral disparity. When the rate matcher receives the 10-bit control pattern followed by the 10-bit skip pattern, it inserts or deletes the 10-bit skip pattern as necessary to avoid rate match FIFO overflow or underflow conditions. (1)	"Rate Match FIFO in Basic Single-Width Mode" and "Rate Match FIFO in Basic Double-Width Mode" sections in the *Transceiver Architecture in Stratix IV Devices* chapter.
Create the `rx_rmfifofull` port to indicate when the rate match FIFO is full.	This option creates the output port `rx_rmfifofull` when you enable the **Enable Rate Match FIFO** option. It is a status flag that the rate match block forwards to the FPGA fabric. It indicates when the rate match FIFO block is full (20 words). This signal remains high as long as the FIFO is full. It is asynchronous to the receiver data path.	"Rate Match FIFO in Basic Single-Width Mode" and "Rate Match FIFO in Basic Double-Width Mode" sections in the *Transceiver Architecture in Stratix IV Devices* chapter.

Table 1–13. MegaWizard Plug-In Manager Options (Rate Match/Byte Order Screen) (Part 2 of 3)

ALTGX Setting	Description	Reference
Create the `rx_rmfifoempty` port to indicate when the rate match FIFO is empty.	This option creates the output port `rx_rmfifoempty` when you enable the **Enable Rate Match FIFO** option. It is a status flag that the rate match block forwards to the FPGA fabric. It indicates when the rate match FIFO block is empty (5 words full). This signal remains high as long as the FIFO is empty. It is asynchronous to the receiver data path.	"Rate Match FIFO in Basic Single-Width Mode" and "Rate Match FIFO in Basic Double-Width Mode" sections in the *Transceiver Architecture in Stratix IV Devices* chapter.
Create the `rx_rmfifodatainserted` port to indicate when data is inserted in the rate match FIFO.	This option creates the output port `rx_rmfifodatainserted` flag when you enable the **Enable Rate Match FIFO** option. It is a status flag that the rate match block forwards to the FPGA fabric. This indicates the insertion of skip patterns. For every deletion, this signal is high for one parallel clock cycle.	"Rate Match FIFO in Basic Single-Width Mode" and "Rate Match FIFO in Basic Double-Width Mode" sections in the *Transceiver Architecture in Stratix IV Devices* chapter.
Create the `rx_rmfifodatadeleted` port to indicate when data is deleted in the rate match FIFO.	This option creates the output port `rx_rmfifodatadeleted` flag when you enable the **Enable Rate Match FIFO** option. It is a status flag that the rate match block forwards to the FPGA fabric. This indicates the deletion of skip patterns. For every insertion, this signal is high for one parallel clock cycle.	"Rate Match FIFO in Basic Single-Width Mode" and "Rate Match FIFO in Basic Double-Width Mode" sections in the *Transceiver Architecture in Stratix IV Devices* chapter.
Enable insertion or deletion of consecutive characters or ordered sets	This option enables the back-to-back insertion or deletion of skip characters in the rate match FIFO. This option is available for selection in Single-width mode. It is enabled by default in Double-width mode.	—
Enable byte ordering block.	This option enables the byte ordering block. It is available in both Single-width and Double-width modes. It is available only when the channel width is: ■ 16-bits/20-bits in Single-width mode ■ 32-bits/40-bits in Double-width mode As soon as the byte ordering block sees the rising edge of the appropriate signal, it compares the LSByte coming out of the byte deserializer with the byte ordering pattern. If they do not match, the byte ordering block inserts the pad character that you enter in the **What is the byte ordering pad pattern?** option such that the byte ordering pattern is seen in the LSByte position. Inserting this pad character enables the byte ordering block to restore the correct byte order.	"Byte Ordering Block" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
What do you want the byte ordering to be based on?	This option is available only when the byte ordering block is enabled. This option allows you to trigger the byte ordering block on the rising edge of either the `rx_syncstatus` signal or the user-controlled `rx_enabyteord` signal from the FPGA fabric.	"Byte Ordering Block" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
What is the byte ordering pattern?	This option is available only when the byte ordering block is enabled. Enter the 10-bit pattern that the byte ordering block must place in the LSByte position of the receiver parallel data on the `rx_dataout` port.	"Byte Ordering Block" section in the *Transceiver Architecture in Stratix IV Devices* chapter.

Table 1–13. MegaWizard Plug-In Manager Options (Rate Match/Byte Order Screen) (Part 3 of 3)

ALTGX Setting	Description	Reference
What is the byte ordering pad pattern?	When the byte ordering block does not find the byte ordering pattern in the LSByte position of the data coming out of the byte deseriazlier, it inserts this byte ordering pad pattern such that the byte ordering pattern is seen in the LSByte position of the receiver parallel data on the `rx_dataout` port. Inserting this pad character enables the byte ordering block to restore the correct byte order.	"Byte Ordering Block" section in the *Transceiver Architecture in Stratix IV Devices* chapter.

Note to Table 1–13:

(1) If you want the rate matcher to insert or delete both the positive and negative disparities of the 20-bit rate matching pattern, enter the positive disparity as pattern1 and negative disparity as pattern2.

Protocol Settings Screen for GIGE and XAUI

Figure 1–15 shows the Protocol Settings screen for the **GIGE** and **XAUI** modes of the MegaWizard Plug-In Manager.

Figure 1–15. MegaWizard Plug-In Manager—ALTGX (Protocol Settings Screen—GIGE and XAUI)

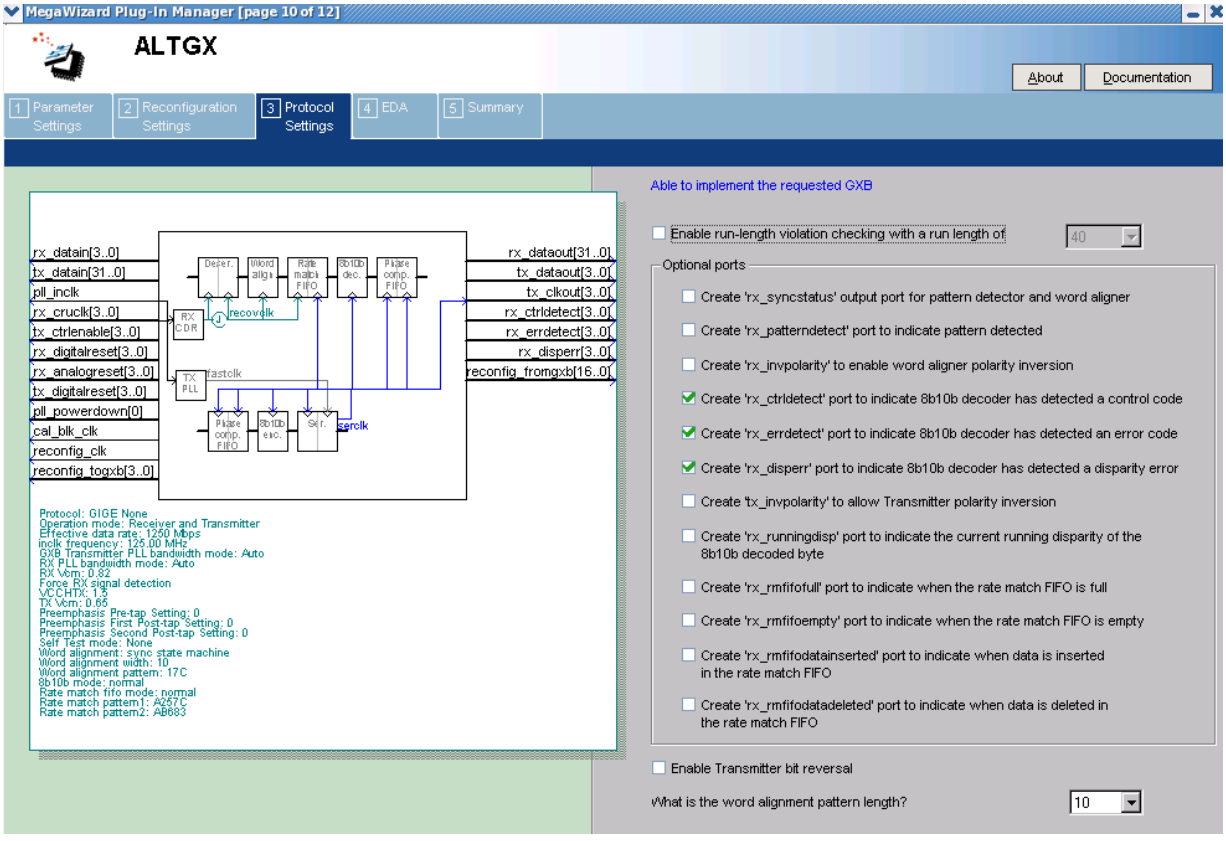


Table 1–14 lists the available options for the **GIGE** and **XAUI** modes in the Protocol Settings screen of the MegaWizard Plug-In Manager for your ALTGX custom megafunction variation.

Table 1–14. MegaWizard Plug-In Manager Options (Protocol Settings —GIGE and XAUI) (Part 1 of 3)

ALTGX Setting	Description	Reference
Enable run-length violation checking with a run length of __.	This option creates the output signal `rx_rlv`. Enabling this option also activates the run-length violation circuit. If the number of continuous 1s and 0s exceeds the number that you set in this option, the run-length violation circuit asserts the `rx_rlv` signal. The `rx_rlv` signal is asynchronous to the receiver data path and is asserted for a minimum of two recovered clock cycles. The run length limits are five to 160 in increments of five.	"Programmable Run Length Violation Detection" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
Create an `rx_syncstatus` output port for pattern detector and word aligner.	This is an output status signal that the word aligner forwards to the FPGA fabric to indicate that synchronization has been achieved. This signal is synchronous with the parallel receiver data on the `rx_dataout` port. Receiver synchronization is indicated on the `rx_syncstatus` port of each channel.	Table 1-33 and the "Word Aligner" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
Create an `rx_patterndetect` port to indicate pattern detected.	This is an output status signal that the word aligner forwards to the FPGA fabric to indicate that the word alignment pattern programmed has been detected in the current word boundary.	Table 1-33 and the "Word Aligner" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
Create an `rx_invpolarity` port to enable word aligner polarity inversion.	This optional port allows you to dynamically reverse the polarity of every bit of the received data at the input of the word aligner. Use this option when the positive and negative signals of the differential input to the receiver (`rx_datain`) are erroneously swapped on the board.	"Receiver Polarity Inversion" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
Create an `rx_ctrldetect` port to indicate 8B/10B decoder has detected a control code.	This is an output status signal that the 8B/10B decoder forwards to the FPGA fabric. This signal indicates whether the decoded 8-bit code group is a data or control code group on this port. If the received 10-bit code group is one of the 12 control code groups (/Kx.y/) specified in IEEE802.3 specification, this signal is driven high. If the received 10-bit code group is a data code group (/Dx.y/), this signal is driven low.	"8B/10B Decoder" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
Create an `rx_errdetect` port to indicate 8B/10B decoder has detected an error code.	This is an output status signal that the 8B/10B decoder forwards to the FPGA fabric. This signal indicates an 8B/10B code group violation. It is asserted high if the received 10-bit code group has a code violation or disparity error. It is used along with the `rx_disperr` signal to differentiate between a code violation error and/or a disparity error.	"8B/10B Decoder" section in the *Transceiver Architecture in Stratix IV Devices* chapter.

Table 1–14. MegaWizard Plug-In Manager Options (Protocol Settings —GIGE and XAUI) (Part 2 of 3)

ALTGX Setting	Description	Reference
Create an rx_disperr port to indicate 8B/10B decoder has detected a disparity error.	This is an output status signal that the 8B/10B decoder forwards to the FPGA fabric.This signal is asserted high if the received 10-bit code or data group has a disparity error. When this signal goes high, rx_errdetect also is asserted high.	"8B/10B Decoder" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
Create a tx_invpolarity port to allow Transmitter polarity inversion.	This optional port allows you to dynamically reverse the polarity of every bit of the data word fed to the serializer in the transmitter data path. Use this option when the positive and negative signals of the differential output from the transmitter (tx_dataout) are erroneously swapped on the board.	"Transmitter Polarity Inversion" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
Create an rx_runningdisp port to indicate the current running disparity of the 8B/10B decoded byte.	This is an output status signal that the 8B/10B decoder forwards to the FPGA fabric. This signal is asserted high when the current running disparity of the 8B/10B decoded byte is negative. This signal is low when the current running disparity of the 8B/10B decoded byte is positive.	—
Create an rx_rmfifofull port to indicate when the rate match FIFO is full.	This option creates the output port rx_rmfifofull. It is a status flag that the rate match block forwards to the FPGA fabric. This indicates when the rate match FIFO block is full (20 words). This signal remains high as long as the FIFO is full and is asynchronous to the receiver data path.	"Rate Match (Clock Rate Compensation) FIFO" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
Create an rx_rmfifoempty port to indicate when the rate match FIFO is empty.	This option creates the output port rx_rmfifoempty. It is a status flag that the rate match block forwards to the FPGA fabric. This indicates when the rate match FIFO block is empty (five words). This signal remains high as long as the FIFO is empty and is asynchronous to the receiver data path.	"Rate Match (Clock Rate Compensation) FIFO" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
Create an rx_rmfifodatainserted port to indicate when data is inserted in the rate match FIFO.	This option creates the output port rx_rmfifodatainserted flag. It is a status flag that the rate match block forwards to the FPGA fabric. The rx_rmfifodatainserted flag is asserted when a rate match pattern byte is inserted to compensate for the PPM difference in reference clock frequencies between the upstream transmitter and the local receiver.	"Rate Match (Clock Rate Compensation) FIFO" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
Create an rx_rmfifodatadeleted port to indicate when data is deleted in the rate match FIFO.	This option creates the output port rx_rmfifodatadeleted. It is a status flag that the rate match block forwards to the FPGA fabric. The rx_rmfifodatadeleted flag is asserted when a rate match pattern byte is deleted to compensate for the PPM difference in reference clock frequencies between the upstream transmitter and the local receiver.	"Rate Match (Clock Rate Compensation) FIFO" section in the *Transceiver Architecture in Stratix IV Devices* chapter.

Table 1–14. MegaWizard Plug-In Manager Options (Protocol Settings —GIGE and XAUI) (Part 3 of 3)

ALTGX Setting	Description	Reference
Enable transmitter bit reversal.	Enabling this option reverses every bit of the 10-bit parallel data at the input of the serializer. The 10-bit input to the serializer `D[9:0]` is reversed to `D[0:9]`.	"8B/10B Encoder" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
What is the word alignment pattern length?	This option sets the word alignment pattern length. The available choices are **7** and **10** for the GIGE and XAUI modes. The default setting for this option is **10**.	"Rate Match (Clock Rate Compensation) FIFO" section in the *Transceiver Architecture in Stratix IV Devices* chapter.

Protocol Settings Screen for the (OIF) CEI Phy Interface

Table 1–15 lists the available options for the **(OIF) CEI Phy Interface** mode in the Protocol Settings screen of the MegaWizard Plug-In Manager for your ALTGX custom megafunction variation.

Table 1–15. MegaWizard Plug-In Manager Options (Protocol Settings - [OIF] CEI PHY Interface)

ALTGX Setting	Description	Reference
Enable run-length violation checking with a run length of __.	This option creates the output signal `rx_rlv`. Enabling this option also activates the run-length violation circuit. If the number of continuous 1s and 0s exceeds the number that you set in this option, the run-length violation circuit asserts the `rx_rlv` signal. The `rx_rlv` signal is asynchronous to the receiver data path and is asserted for a minimum of two recovered clock cycles. For a 32-bit channel width, the run length limits are 8 to 512 in increments of eight.	"Programmable Run Length Violation Detection" section in the *Transceiver Architecture in Stratix IV Devices* chapter.

Protocol Settings Screen for PCIe

Figure 1–16 shows the **PCIe 1** screen for Protocol Settings of the MegaWizard Plug-In Manager.

Figure 1–16. MegaWizard Plug-In Manager—ALTGX (PCIe 1 Screen)

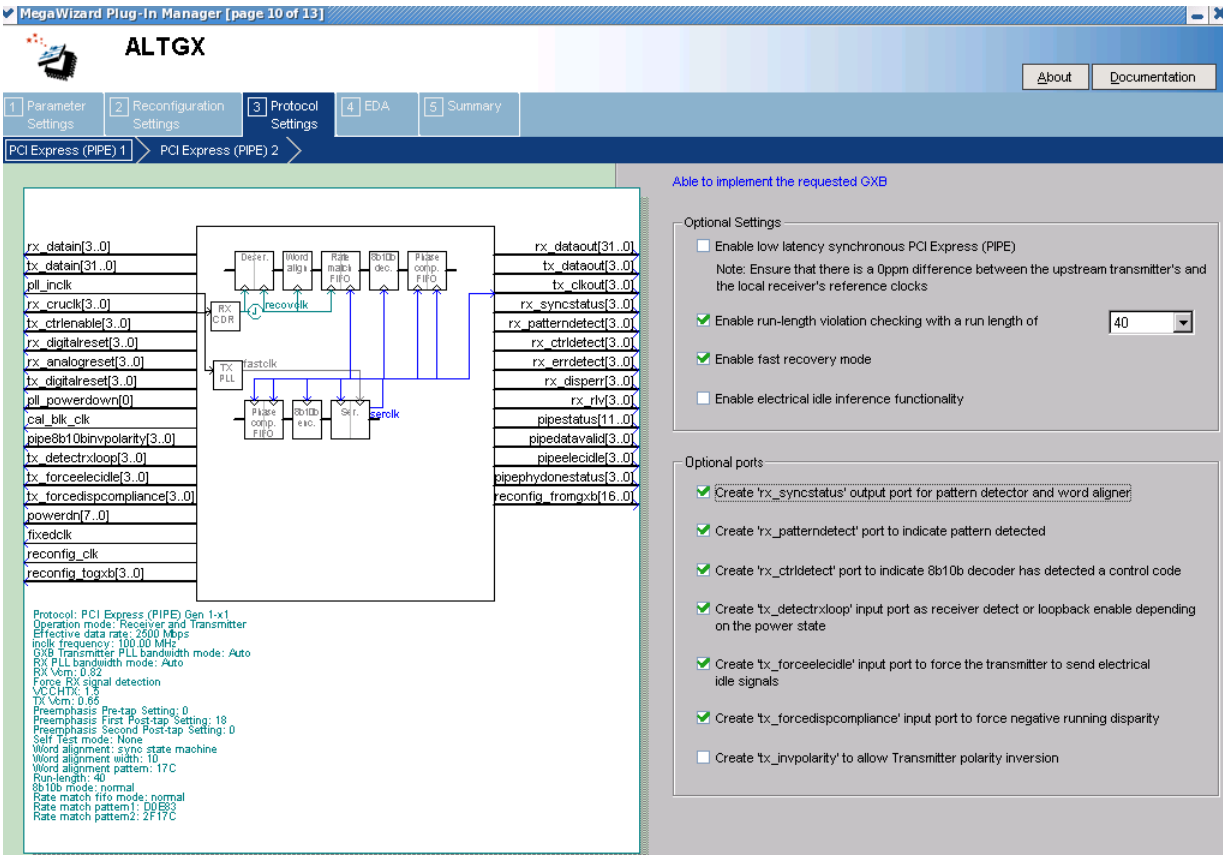


Table 1–16 lists the available options on the **PCIe 1** screen of the MegaWizard Plug-In Manager for your ALTGX custom megafunction variation.

Table 1–16. MegaWizard Plug-In Manager Options (PCIe 1) (Part 1 of 2)

ALTGX Setting	Description	Reference
Enable low latency synchronous PCIe.	This option puts the rate match FIFO into low latency mode, which forces the system into a 0 ppm mode. Ensure that there is a 0 ppm difference between the upstream transmitter's and the local receiver's input reference clocks.	"Rate Match (Clock Rate Compensation) FIFO" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
Enable run-length violation checking with a run length of __.	This option creates the output signal `rx_rlv`. Enabling this option also activates the run-length violation circuit. If the number of continuous 1s and 0s exceeds the number that you set in this option, the run-length violation circuit asserts the `rx_rlv` signal. The `rx_rlv` signal is asynchronous to the receiver data path. For both 8-bit and 16-bit channel widths, the run length limits are 5 to 160 in increments of five.	"Programmable Run Length Violation Detection" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
Enable fast recovery mode.	This option enables the CDR control block. When this block is enabled, the `rx_locktodata` and `rx_locktorefclk` signals are disabled.	"Fast Recovery Mode" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
Enable electrical idle inference functionality.	Enable the electrical idle inference module by selecting this option. In PCIe mode, the PCS has an optional electrical idle inference module designed to implement the electrical idle inference conditions specified in PCIe base specification 2.0. Enabling this option creates the `rx_elecidleinfersel[2:0]` input signal. The electrical idle Inference module infers electrical idle depending on the logic level driven on the `rx_elecidleinfersel[2:0]` input signal. For the electrical idle Inference module to correctly infer an electrical idle condition in each LTSSM sub-state, you must drive the `rx_elecidleinfersel[2:0]` signal appropriately.	"Electrical Idle Inference" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
Create an `rx_syncstatus` output port for pattern detector and word aligner.	The ALTGX MegaWizard Plug-In Manager automatically configures the word aligner in Automatic Synchronization State Machine mode for PCIe mode. This is an output status signal that the word aligner forwards to the FPGA fabric to indicate that synchronization has been achieved. This signal is synchronous with the parallel receiver data on the `rx_dataout` port. The signal width is 1 and 2 bits for a channel width of 8 bits and 16 bits, respectively.	Table 1-29 and "Automatic Synchronization State Machine Mode Word Aligner with 10-bit PMA-PCS Interface Mode" section in the *Transceiver Architecture in Stratix IV Devices* chapter.

Table 1–16. MegaWizard Plug-In Manager Options (PCIe 1) (Part 2 of 2)

ALTGX Setting	Description	Reference
Create an `rx_patterndetect` output port to indicate pattern detected.	This is an output status signal that the word aligner forwards to the FPGA fabric to indicate that the word alignment pattern programmed has been detected in the current word boundary. The signal width is 1 and 2 bits for a channel width of 8 bits and 16 bits, respectively.	"Automatic Synchronization State Machine Mode Word Aligner with 10-bit PMA-PCS Interface Mode" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
Create an `rx_ctrldetect` port to indicate 8B/10B decoder has detected a control code.	This is an output status signal that the 8B/10B decoder forwards to the FPGA fabric. This signal indicates whether the decoded 8-bit code group is a data or control code group on this port. If the received 10-bit code group is one of the 12 control code groups (/Kx.y/) specified in the IEEE802.3 specification, this signal is driven high. If the received 10-bit code group is a data code group (/Dx.y/), this signal is driven low. The signal width is 1 and 2 bits for a channel width of 8 bits and 16 bits, respectively.	"8B/10B Decoder" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
Create a `tx_detectrxloop` input port as Receiver detect or loopback enable, depending on the power state.	Depending on the power-down mode, asserting this signal enables either the receiver detect operation or Loopback mode. (1)	"Receiver Detection" and "PCIe Reverse Parallel Loopback" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
Create a `tx_forceelecidle` input port to force the Transmitter to send Electrical Idle signals.	Enabling this port sets the transmitter buffer in electrical idle mode. This port is available in all PCIe power-down modes and has a specific use in each mode. (1)	"Transmitter Buffer Electrical Idle" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
Create a `tx_forcedispcompliance` input port to force negative running disparity.	A high level on this port forces the associated parallel transmitter data on the `tx_datain` port to be transmitted with negative current running disparity. ■ For 8-bit transceiver channel width configurations, you must drive `tx_forcedispcompliance[1:0]` high in the same parallel clock cycle as the first /K28.5/ of the compliance pattern on the `tx_datain` port. ■ For 16-bit transceiver channel width configurations, you must drive only the LSB of `tx_forcedispcompliance[1:0]`high in the same parallel clock cycle as /K28.5/D21.5/ of the compliance pattern on the `tx_datain` port.	"Compliance Pattern Transmission Support" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
Create a `tx_invpolarity` port to allow Transmitter polarity inversion.	This optional port allows you to dynamically reverse the polarity of every bit of the data word fed to the serializer in the transmitter data path. Use this option when the positive and negative signals of the differential output from the transmitter (`tx_dataout`) are erroneously swapped on the board.	"Transmitter Polarity Inversion" section in the *Transceiver Architecture in Stratix IV Devices* chapter.

Note to Table 1–16:

(1) Refer to the table '*Power States and Functions Allowed in Each Power State*' in the *PIPE Interface* section in the *Transceiver Architecture in Stratix IV Devices* chapter.

Figure 1–17 shows the **PCIe 2** screen of Protocol Settings for the MegaWizard Plug-In Manager.

Figure 1–17. MegaWizard Plug-In Manager—ALTGX (PCIe 2 Screen)

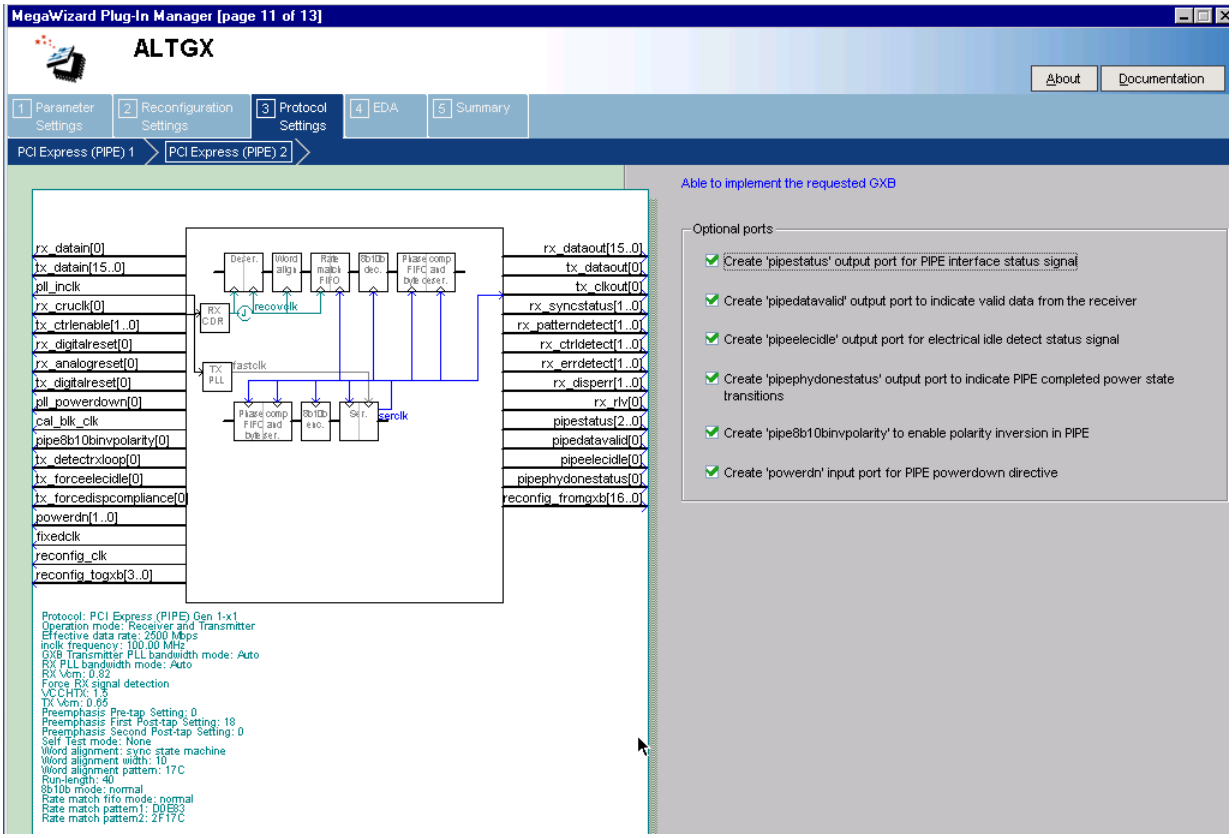


Table 1–17 lists the available options on the **PCIe 2** screen of the MegaWizard Plug-In Manager for your ALTGX custom megafunction variation.

Table 1–17. MegaWizard Plug-In Manager Options (PCIe 2 Screen) (Part 1 of 2)

ALTGX Setting	Description	Reference
Create a `pipestatus` output port for PIPE interface status signal.	The PCIe interface block receives status signals from the transceiver channel PCS and PMA blocks and encodes the status on a 3-bit output signal (`pipestatus[2:0]`) that is forwarded to the FPGA fabric.	"Receiver Status" section and Table 1-53 in the *Transceiver Architecture in Stratix IV Devices* chapter.
Create a `pipedatavalid` output port to indicate valid data from the receiver.	This is an output status port that indicates the receiver parallel data on the `rx_dataout` port is valid.	—

Table 1–17. MegaWizard Plug-In Manager Options (PCIe 2 Screen) (Part 2 of 2)

ALTGX Setting	Description	Reference
Create a `pipeelecidle` output port for Electrical Idle detect status signal.	Enabling this option creates the `pipeelecidle` output status port that is forwarded to the FPGA fabric. ■ If you select **Enable Electrical Idle Inference Module,** the `pipeelecidle` signal is driven high when the electrical idle inference module infers an electrical idle condition depending on the logic driven on the `rx_elecidleinfersel[2:0]` port. Otherwise, it is driven low. ■ If you do not select **Enable Electrical Idle Inference Module**, the `rx_signaldetect` output signal from the signal threshold detection circuitry is inverted and driven on the `pipeelecidle` port. The `pipeelecidle` signal is asynchronous to the receiver data path.	"Electrical Idle Inference" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
Create a `pipephydonestatus` output port to indicate PIPE completed power state transitions.	This is an output status signal forwarded to the FPGA fabric. The completion of various PHY functions; for example, receiver detection, power state transition, clock switch, and rate switch, are indicated on this `pipephydonestatus` signal by driving this signal high for one parallel clock cycle.	"PCIe Mode" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
Create a `pipe8b10binvpolarity` port to enable polarity inversion in PIPE.	This optional port allows you to dynamically reverse every bit of the received data at the input of the 8B/10B decoder.	"PCIe Mode" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
Create a `powerdn` input port for PIPE powerdown directive.	Enabling this option creates an input control port `powerdn[1:0]` for each transceiver channel.	"Power State Management" section and Table 1-51 in the *Transceiver Architecture in Stratix IV Devices* chapter.

Protocol Settings Screen for SONET/SDH

Figure 1–18 shows the **SONET/SDH** screen for Protocol Settings of the MegaWizard Plug-In Manager.

Figure 1–18. MegaWizard Plug-In Manager—ALTGX (Protocol Settings—SONET/SDH)

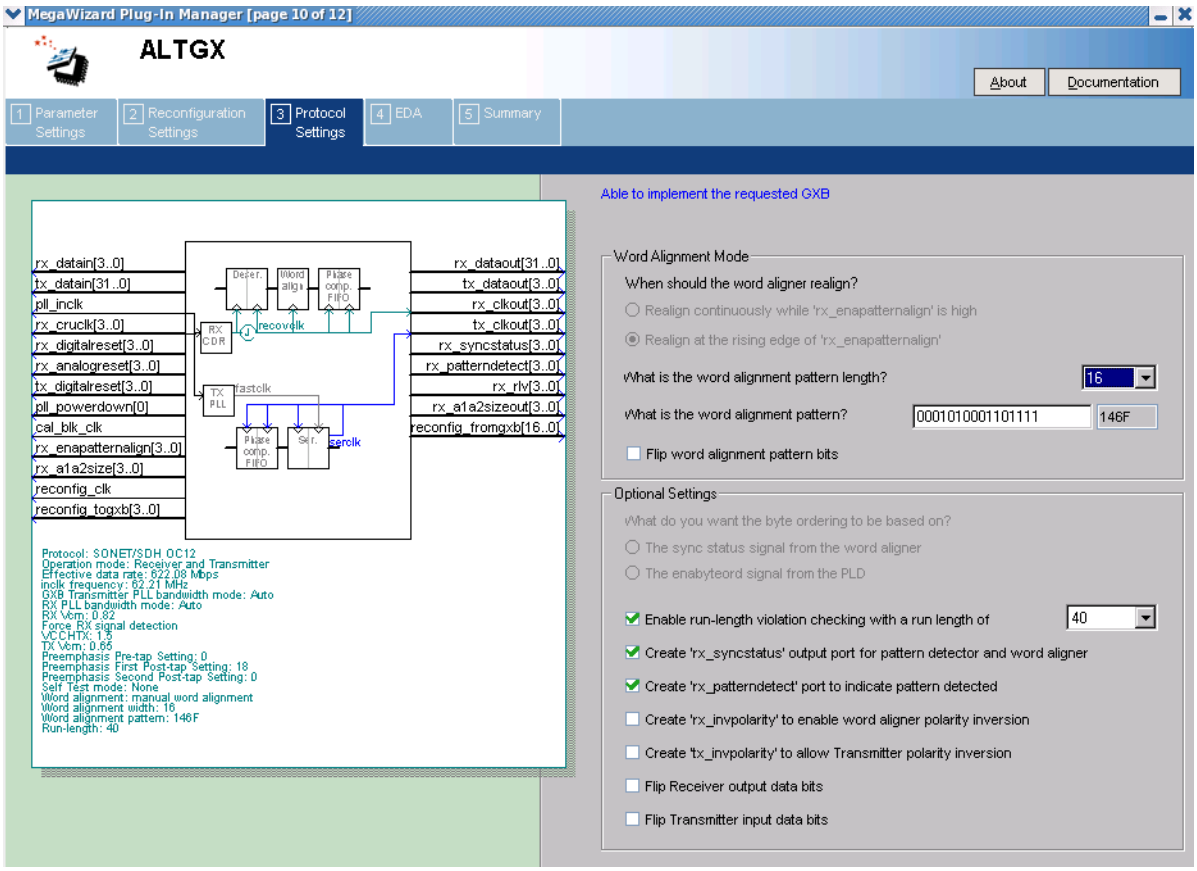


Table 1–18 lists the available options on the **SONET/SDH** screen for Protocol Settings of the MegaWizard Plug-In Manager for your ALTGX custom megafunction variation.

Table 1–18. MegaWizard Plug-In Manager Options (SONET/SDH Screen) (Part 1 of 3)

ALTGX Setting	Description	Reference
When should the word aligner realign?	This option is not available in SONET/SDH mode. In SONET/SDH mode, the word aligner operates in Manual Alignment mode. By default, the ALTGX MegaWizard Plug-In Manager sets the behavior of the word aligner such that re-alignment occurs when there is a rising edge of the `rx_enapatternalign` input signal in this mode.	"Word Aligner" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
What is the word alignment pattern length?	This option sets the length of the word alignment pattern. The following options are available: ■ **OC-12**—only 16-bit pattern is allowed. ■ **OC-48**—only 16-bit pattern is allowed. ■ **OC-96**—16-bit and 32-bit patterns are allowed.	"SONET/SDH Mode" (OC-12, OC-48, and OC-96) section in the *Transceiver Architecture in Stratix IV Devices* chapter.

Table 1–18. MegaWizard Plug-In Manager Options (SONET/SDH Screen) (Part 2 of 3)

ALTGX Setting	Description	Reference
What is the word alignment pattern?	Enter the word alignment pattern. By default, the pattern that appears in the MegaWizard Plug-In Manager is '0001010001101111' (16'h146F).	"SONET/SDH Mode" (OC-12, OC-48, and OC-96) section in the *Transceiver Architecture in Stratix IV Devices* chapter.
Flip word alignment pattern bits.	This option is enabled in the MegaWizard Plug-In Manager by default. This option reverses the order of the alignment pattern at a bit level to support MSB-to-LSB transmission in SONET/SDH mode. The ALTGX MegaWizard Plug-In Manager flips the bit order of the default word alignment pattern '0001010001101111 '(16'h146F) and uses the flipped version '1111011000101000' (16'hF628) as the word alignment pattern.	—
What do you want the byte ordering to be based on?	This option allows you to trigger the byte ordering block either on the rising edge of the `rx_syncstatus` signal or the user-controlled `rx_enabyteord` signal from the FPGA fabric. The byte ordering block is enabled only in OC-48 mode.	"Byte Ordering Block" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
Enable run-length violation checking with a run length of.	This option creates the output signal `rx_rlv`. Enabling this option also activates the run-length violation circuit. If the number of continuous 1s and 0s exceeds the number that you set in this option, the run-length violation circuit asserts the `rx_rlv` signal. The `rx_rlv` signal is asynchronous to the receiver data path and is asserted for a minimum of two recovered clock cycles in OC-12 and OC-48 modes. Similarly, it is asserted for a minimum of three recovered clock cycles in the OC-96 mode. For the OC-12 and OC-48 modes, the run length limits are 4 to 128 in increments of four. For the OC-96 mode, the run length limits are 5 to 160 in increments of five.	"Programmable Run Length Violation Detection" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
Create an `rx_syncstatus` output port for pattern detector and word aligner.	This is an output status signal that the word aligner forwards to the FPGA fabric to indicate that synchronization has been achieved. This signal is synchronous with the parallel receiver data on the `rx_dataout` port. The signal width is 1 bit, 2 bits, and 4 bits for a channel width of 8 bits, 16 bits, and 32 bits, respectively.	Table 1-77 and "Word Aligner" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
Create an `rx_patterndetect` port to indicate pattern detected.	This is an output status signal that the word aligner forwards to the FPGA fabric to indicate that the word alignment pattern programmed has been detected in the current word boundary. The signal width is 1 bit, 2 bits, and 4 bits for a channel width of 8 bits, 16 bits, and 32 bits, respectively.	Table 1-33 and "Word Aligner" section in the *Transceiver Architecture in Stratix IV Devices* chapter.

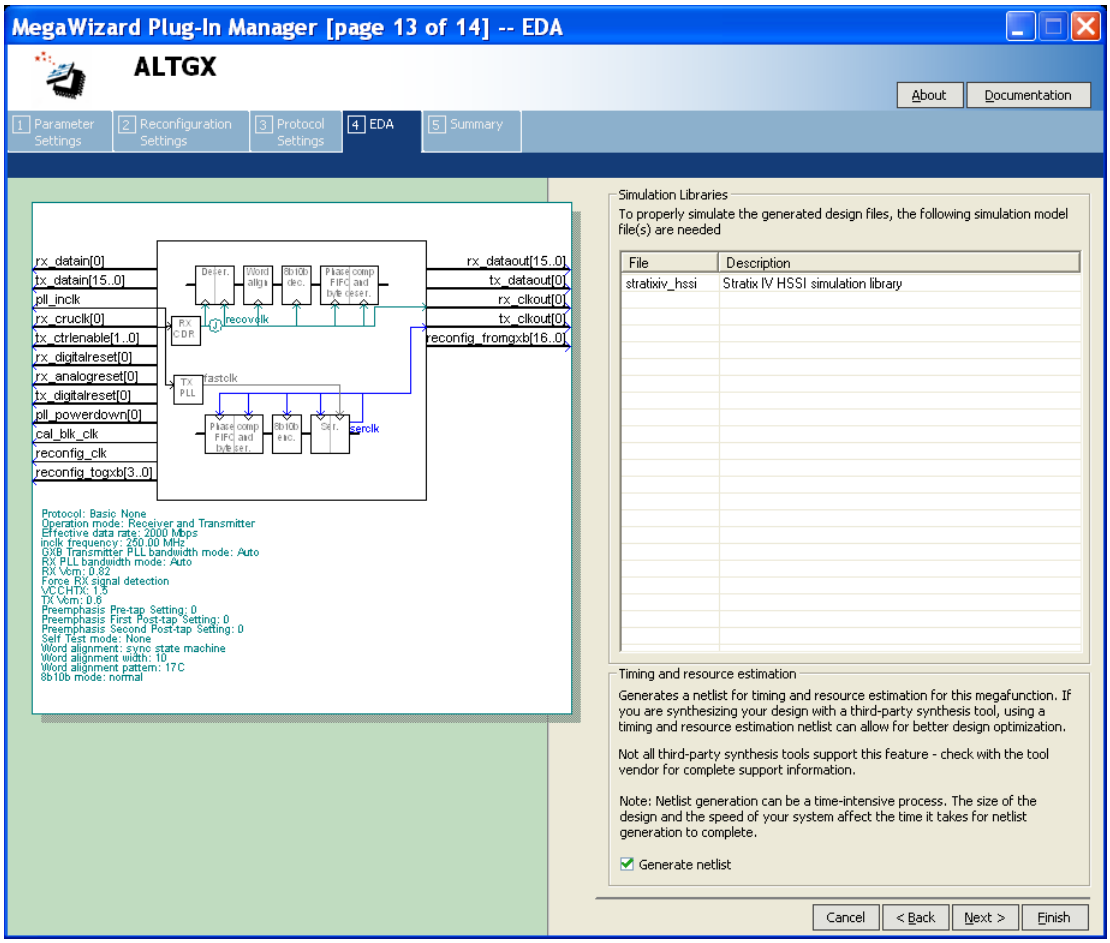
Table 1–18. MegaWizard Plug-In Manager Options (SONET/SDH Screen) (Part 3 of 3)

ALTGX Setting	Description	Reference
Create a `rx_invpolarity` port to enable word aligner polarity inversion.	This optional port allows you to dynamically reverse the polarity of every bit of the received data at the input of the word aligner. Use this option when the positive and negative signals of the differential input to the receiver (`rx_datain`) are erroneously swapped on the board.	"Receiver Polarity Inversion" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
Create a `tx_invpolarity` port to allow Transmitter polarity inversion.	This optional port allows you to dynamically reverse the polarity of every bit of the data word fed to the serializer in the transmitter data path. Use this option when the positive and negative signals of the differential output from the transmitter (`tx_dataout`) are erroneously swapped on the board.	"Transmitter Polarity Inversion" section in the *Transceiver Architecture in Stratix IV Devices* chapter.
Flip receiver output data bits.	This option reverses the bit order of the parallel receiver data at a byte level at the output of the receiver phase compensation FIFO to support MSB-to-LSB transmission in SONET/SDH mode. For example, if the 16-bit parallel receiver data at the output of the receiver phase compensation FIFO is '10111100 10101101' (16'hBCAD), enabling this option reverses the data on the `rx_dataout` port to '00111101 10110101' (16'h3DB5).	"SONET/SDH Mode" (OC-12, OC-48, and OC-96) section in the *Transceiver Architecture in Stratix IV Devices* chapter.
Flip transmitter input data bits.	This option reverses the bit order of the parallel transmitter data at a byte level at the input of the transmitter phase compensation FIFO to support MSB-to-LSB transmission protocols in SONET/SDH mode. For example, if the 16-bit parallel transmitter data at the `tx_datain` port is '10111100 10101101' (16'hBCAD), enabling this option reverses the input data to the transmitter phase compensation FIFO to '00111101 10110101' (16'h3DB5).	"SONET/SDH Mode" (OC-12, OC-48, and OC-96) section in the *Transceiver Architecture in Stratix IV Devices* chapter.

EDA Screen

Figure 1–19 shows the EDA screen of the MegaWizard Plug-In Manager. The **Generate Netlist** option generates a netlist for the third party EDA synthesis tool to estimate timing and resource utilization for the ALTGX instance.

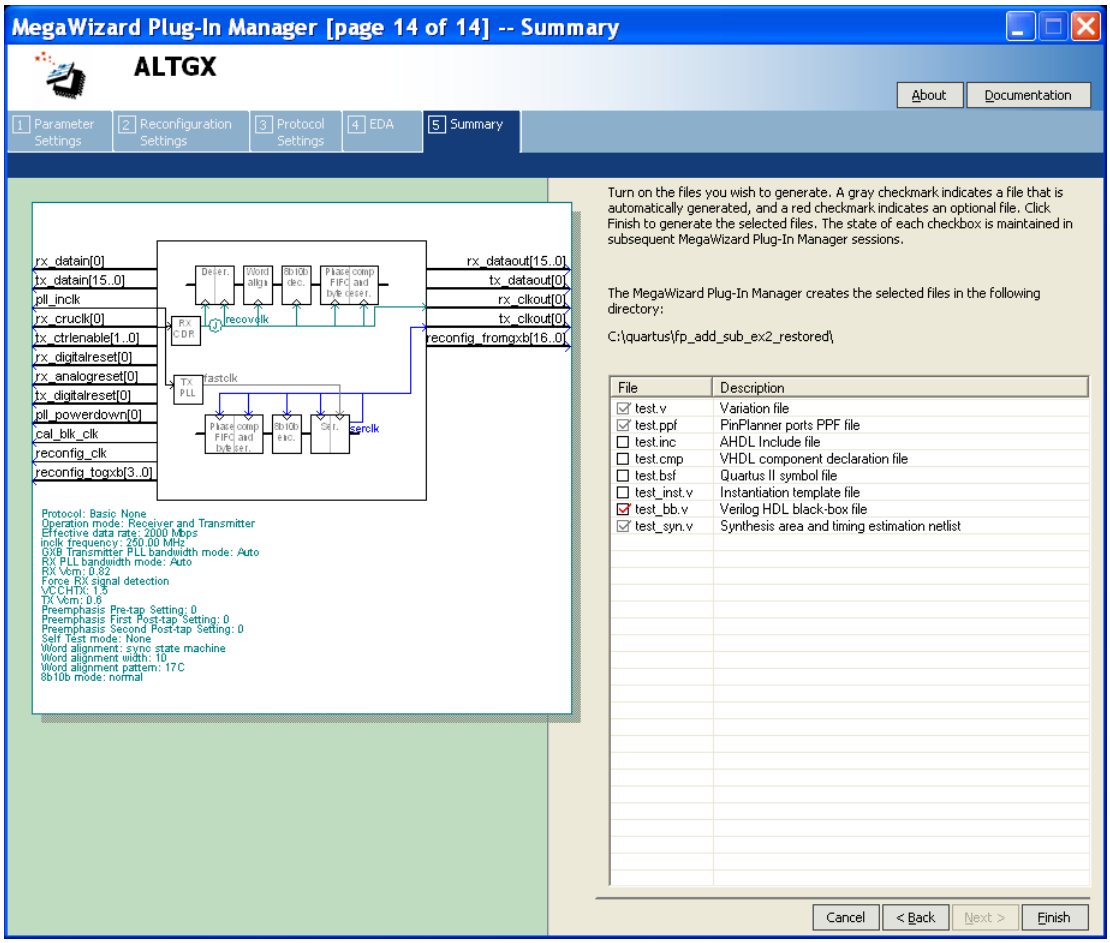
Figure 1–19. MegaWizard Plug-In Manager—ALTGX (EDA Screen)



Summary Screen

Figure 1–20 shows the Summary screen of the MegaWizard Plug-In Manager. You can select optional files on this page. After you make your selections, click **Finish** to generate the files.

Figure 1–20. MegaWizard Plug-In Manager—ALTGX (Summary Screen)



Document Revision History

Table 1–19 lists the revision history for this chapter.

Table 1–19. Document Revision History (Part 1 of 2)

Date	Version	Changes
January 2014	4.4	■ Updated Table 1–5.
September 2012	4.3	■ Updated Table 1–1 to close FB #65275. ■ Updated Table 1–12 to close FB #37243.
December 2011	4.2	Updated Table 1–1.

Table 1–19. Document Revision History (Part 2 of 2)

Date	Version	Changes
February 2011	4.1	■ Updated Table 1–1, Table 1–3, Table 1–7, and Table 1–17. ■ Updated chapter title. ■ Minor text edits. ■ Applied new template.
November 2009	4.0	■ Added Deterministic Latency protocol information. ■ Added AEQ information. ■ Updated PLL setting information. ■ Consolidated Parameter Settings information (Table 1–1 to Table 1–6). ■ Consolidated Reconfiguration Settings information (Table 1–7 to Table 1–9). ■ Consolidated Protocol Settings information (Table 1–10 to Table 1–18). ■ Minor text edits.
June 2009	3.1	■ Updated Table 1–9, Table 1–29 and Table 1–35. ■ Updated Figure 1–10. ■ Added introductory sentences to improve search ability. ■ Minor text edits.
March 2009	3.0	■ Updated the figures to match the software changes. ■ Removed the 'Deterministic Latency' subprotocol from Basic functional mode. ■ Removed the various clock frequencies from the **Reconfig Clks** screen for all the applicable functional modes.
November 2008	2.0	■ Updated Table 1–1, Table 1–6, and Table 1–11. ■ Updated Figure 1–8. ■ Added **Reconfig Clks** and **Reconfig 2** sections. ■ Added the “Use ATX Transmitter PLL” setting. ■ Changed the “Which device speed grade will you be using?” setting to the “Which device variation will you be using” setting.
June 2008	1.1	Minor text edit.
May 2008	1.0	Initial release.

2. Transceiver Design Flow Guide for Stratix IV Devices

SIV53002-4.1

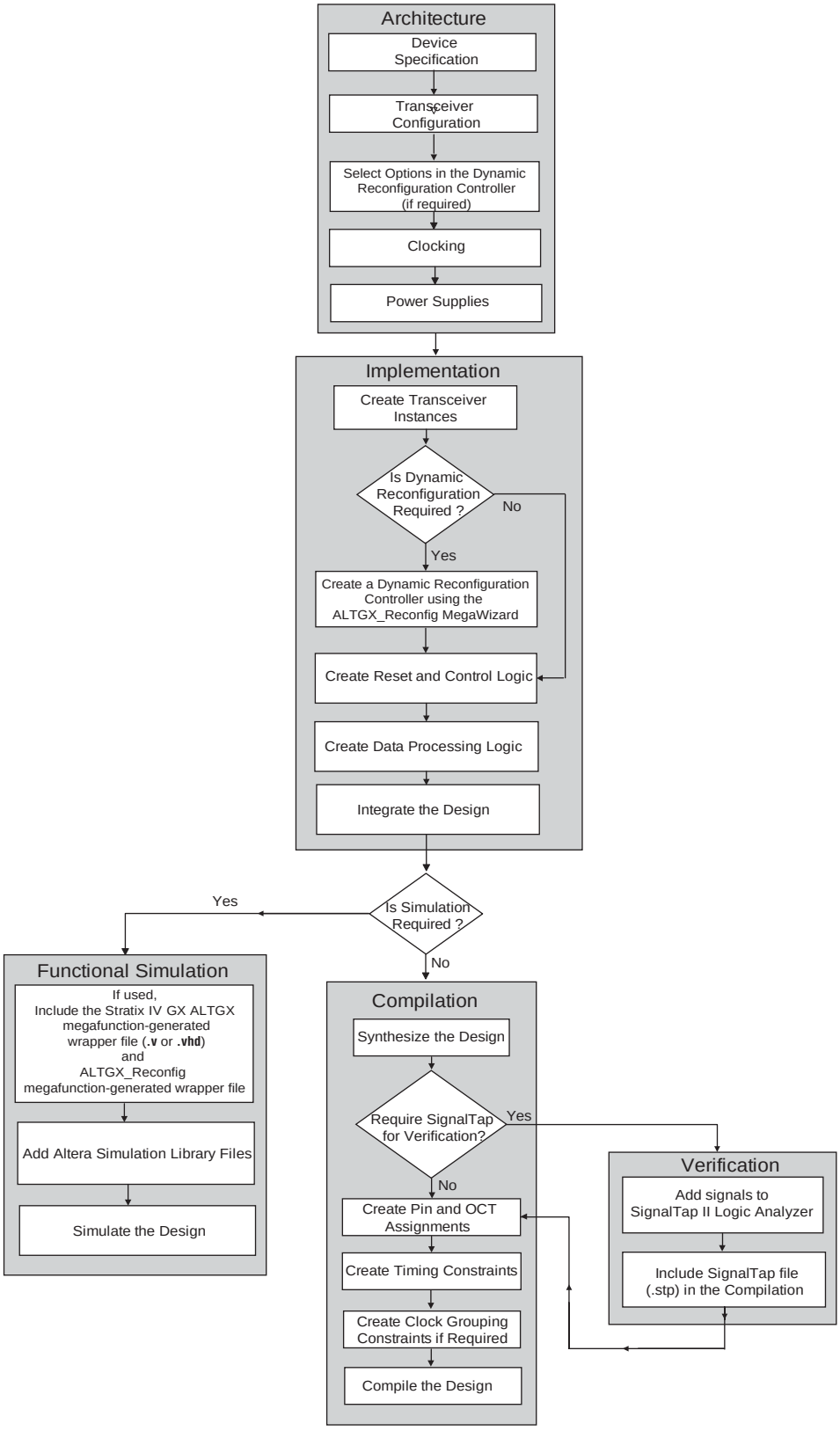
This chapter describes the Altera-recommended basic design flow that simplifies Stratix® IV GX transceiver-based designs.

Use the following design flow techniques to simplify transceiver implementation. The "Guidelines to Debug Transceiver-Based Designs" on page 2–14 provides guidelines to trouble-shoot transceiver-based designs. An example of a fibre channel protocol application is also described in this chapter.

The transceiver-based design is divided into phases and are detailed in the following sections:

Figure 2–1 shows the design flow chart of the different stages of the design flow. The design flow stages include architecture, functional simulation, compilation, and verification. Each stage of the design flow is explained in the sections that follow.

Figure 2–1. Flow Chart of the Different Stages in a Transceiver-Based Design



Architecture

The first step in creating a transceiver-based design is to map your system requirements with the Stratix IV GX device supported features. The Stratix IV GX device contains multiple transceiver channels that you can configure in multiple data rates and protocols. It also provides multiple transceiver clocking options. For your design, identify the transceiver capabilities and clocking options to ensure that the transceiver meets your system requirements.

This section describes the critical parameters that you need to identify as part of this architecture phase.

Device Specification

The following device specifications must meet your requirements:

- Refer to the device data sheet to ensure that the transceivers meet the data rate and electrical requirements for your target high-speed interface application; for example, the jitter specification and voltage output differential (V_{OD}) range.
- Check whether the device family that you select supports your design requirements; for example, the number of transceiver channels, FPGA logic density, memory elements, and DSP blocks.
- If you intend to migrate to a higher logic density or higher transceiver count device in the future, ensure that the migration device is available.

For information about device characteristics, refer to the "Transceiver Performance Specifications" section in the *DC and Switching Characteristics for Stratix IV Devices* chapter. For information about transceiver resources, refer to the *Overview for the Stratix IV Device Family* chapter.

Transceiver Configuration

Use the ALTGX MegaWizard™ Plug-In Manager interface to configure the Stratix IV transceiver channel's features and options.

When selecting a transceiver configuration, check for the following parameters:

- Check whether the transceiver physical coding sublayer (PCS) and physical medium attachment (PMA) functional blocks comply with your system requirements. For example, check whether the rate match (clock rate compensation) FIFO in the receiver channel PCS meets the parts per million (PPM) specifications required for your application.

For more information about transceiver specifications, refer to the "Transceiver Performance Specifications" section of the *DC and Switching Characteristics for Stratix IV Devices* chapter.

- Select a configuration that meets your latency requirements. If your system has maximum latency requirements through the transceiver data path, consider the appropriate functional configuration. The Stratix IV GX transceiver supports various configurations that differ in latency (for example, low latency PCS mode and Basic [PMA direct] mode).

- In some configurations, specific functional blocks in the transceiver are disabled or bypassed. Before you select a transceiver configuration, understand the functional blocks that must be implemented in the FPGA fabric. For example, Basic (PMA direct) mode provides reduced latency but does not have PCS functional blocks enabled (for example, word aligner and 8B/10B encoder). Therefore, implement these functional blocks in the FPGA fabric if you need them in your application. Some examples of functional blocks that you may need to implement in the FPGA fabric are shown in "Create Data Processing and Other User Logic" on page 2–8.

For more information about the ALTGX MegaWizard Plug-In Manager, refer to the *ALTGX Transceiver Setup Guide for Stratix IV Devices* chapter.

- Check whether the loopback features are available for your selected functional mode. The Stratix IV GX transceiver provides diagnostic loopback features between the transmitter channel and the receiver channel at the transceiver PCS and PMA interfaces. These loopback features help in debugging your design.
- If your design uses multiple transceiver channels within the same transceiver block, based on the transceiver channel configurations, the Quartus® II software might impose restrictions on combining these channels.

For more information about these restrictions, refer to the *Configuring Multiple Protocols and Data Rates in Stratix IV Devices* chapter.

Dynamic Reconfiguration

Use the Stratix IV transceivers in multiple-link interconnect environments by dynamically reconfiguring the PMA controls (for example, V_{OD}, Pre-emphasis, Equalization, DC gain, and the transceiver channel configuration). You can also reconfigure the PMA controls without affecting any other transceiver channel or the logic in the FPGA fabric.

Use the transceiver channel reconfiguration to dynamically switch a transceiver channel to multiple protocols and data rates. The Quartus II software allows you to generate a memory initialization file (**.mif**) that stores unique transceiver settings and provides a dynamic reconfiguration controller, which is soft logic that controls the transceiver reconfiguration with minimal user interface logic. You can generate this soft logic using the ALTGX_RECONFIG MegaWizard interface.

For more information about the ALTGX_RECONFIG interface, refer to the *ALTGX_RECONFIG Megafunction User Guide for Stratix IV Devices* chapter.

All receiver channels in the Stratix IV GX device require offset cancellation to counter offset variations in process, voltage, and temperature (PVT) on the receiver. The dynamic reconfiguration controller initiates the sequence to perform offset cancellation on the receiver channels. Therefore, if you configure the Stratix IV GX transceiver channel in **Receiver only** or **Transmitter and Receiver** configuration, you must instantiate a dynamic reconfiguration controller.

For more information about offset cancellation or dynamic reconfiguration of PMA controls or channel configuration, refer to the "Offset Cancellation Feature" section in the *Dynamic Reconfiguration in Stratix IV Devices* chapter.

Clocking

The Stratix IV GX transceiver is clocked by various input reference clocks, for example:

- Dedicated transceiver reference clock (`refclk`) pins. Altera recommends using `refclk` pins whenever possible because the `refclk` pins yield reduced jitter on the transmitted data.
- Clock sources connected to global clock lines.
- Clock outputs from the phase-locked loops (PLLs) in the FPGA fabric.

Identify the transceiver channels input reference clock sources, for example:

- Ensure that your selected device has the required number of input reference clock resources to implement your design.
- Ensure that the transceiver clock input supports the required I/O standards.
- Ensure that the clocking restrictions work with your selected device:
  - Check whether the allowed frequencies for the transceiver input reference clocks meet your system requirements.
  - If you use the PLL cascade clock, understand its restrictions.
  - If you are using the auxiliary transmit (ATX) PLL, understand the recommendations for the input reference clock sources and the restrictions on data rate ranges supported by the ATX PLL.

For transceiver-FPGA interface clocking:

- Ensure that the transceiver-FPGA interface clock frequency limits meet your system requirements.

For information about transceiver specifications, refer to the *DC and Switching Characteristics for Stratix IV Devices* chapter.

- Identify the clocking scheme to clock the transceiver data to the logic in the FPGA fabric. For example, if your design has multiple transceiver channels that run at the same data rate and are connected to the one upstream link, you might be able to use a single transceiver-FPGA clock to provide clocks to the transceiver data path, which can conserve clock routing resources.
- If you are using Basic (PMA direct) mode, determine whether you require a left/right PLL to provide phase shifted clocks to the FPGA fabric. The left/right PLL clocks the data received and transmitted between the transceiver and the FPGA fabric interface and may be required to meet the timing requirements of the data transfer.

For information about transceiver clocking, refer to the *Transceiver Clocking in Stratix IV Devices* chapter.

After you identify the required transceiver parameters, start the implementation and integration phase.

Power Supplies

The Stratix IV GX device requires multiple power supplies. The pin connection guidelines provide specific recommendations about the type of power supply regulator (linear or switching) and the voltage supply options and restrictions. For example, the transmitter buffer supply VCCHTx has two options—1.5 V and 1.4 V. There are specific data rate restrictions when using 1.5 V. You must understand these restrictions when you select a power supply value.

For more information, refer to the *Stratix IV GX and Stratix IV E Device Family Pin Connection Guidelines*.

Estimate the power required to run your design. This estimation allows you to select the appropriate power supply modules and to design the power distribution network on your board.

Use the Early Power Estimator tool to estimate the transient current requirements.

For more information about the Early Power Estimation tool, refer to the *Stratix III, Stratix IV, Stratix V, HardCopy III, and HardCopy IV PowerPlay Early Power Estimator*.

If your design is already complete, use the power optimization features available in the Stratix IV Devices.

For more information about optimizing power in Stratix IV FPGA devices, refer to *AN 514: Power Optimization in Stratix IV FPGAs*.

Board Design Requirements

For improved signal integrity on the high-speed serial interface, follow the best design practices for your power distribution network, PCB design, and stack up.

For detailed guidelines and recommendations about your power distribution network, PCB design, and stack up, refer to the Board Design Resource Center web site.

For more information about the Stratix IV GX design process, refer to *AN 519: Stratix IV Design Guidelines*.

Implementation and Integration

There are three steps to the implementation and integration phase:

- "Create Transceiver Instances" on page 2–7
- "Create Reset Logic to Control the FPGA Fabric and Transceivers" on page 2–34
- "Create Data Processing and Other User Logic" on page 2–36

Create Transceiver Instances

The ALTGX MegaWizard Plug-In Manager to creates the transceiver instance. In the architecture phase, you identified the transceiver configuration for your design. Using the ALTGX MegaWizard Plug-In Manager, select the appropriate parameters that apply to your architecture requirements.

Reset and Status Signals

The ALTGX MegaWizard Plug-In Manger provides various reset and status signals:

- Reset signals—`tx_digitalreset`, `rx_digitalreset`, `rx_analogreset`, and `pll_powerdown` are required to reset the transceiver PCS and PMA functional blocks.
- Status signals—`rx_freqlocked` and `pll_locked` indicate the state of the receiver CDR and transmitter PLL, respectively. Use these reset and status signals to implement the transceiver reset control logic in the FPGA fabric. For more information, refer to "Create Reset and Control Logic" on page 2–8.

If you determine that your application requires dynamic reconfiguration, select the options in the **Reconfig** screen of the ALTGX MegaWizard interface.

If you intend to dynamically reconfigure the channel into other protocol modes or data rates, the **Reconfig** screen provides multiple options (for example, the **channel interface** and **Use alternate PLL** options) to enable this feature.

To understand the **logical channel addressing**, **logical PLL index**, and **type of reconfiguration to select** options in the **Reconfig** screen, refer to the "Channel and CMU PLL Reconfiguration Mode Details" section in the *Dynamic Reconfiguration in Stratix IV Devices* chapter.

Depending on your system, when you use multiple transceiver channels, you might be able to share the transmitter and receiver parallel clocks of one channel with the other channels. If your design requires sharing a clock resource, select the `tx_coreclk` and `rx_coreclk` ports.

Transceiver-FPGA fabric interface clock sharing conditions are provided in the *Transceiver Clocking in Stratix IV Devices* chapter.

For more information about using the ALTGX MegaWizard Plug-In Manager and the functionality of the different options and signals available, refer to the *ALTGX Transceiver Setup Guide for Stratix IV Devices* chapter.

Create Dynamic Reconfiguration Controller Instances

Use the ALTGX_RECONFIG MegaWizard interface to create the dynamic reconfiguration controller instance. If you intend to use the channel and CMU PLL reconfiguration feature, select the relevant options in the ALTGX_RECONFIG Megawizard Plug-In Manager.

For descriptions of the options in the ALTGX_RECONFIG megafunction, refer to the *ALTGX_RECONFIG Megafunction User Guide for Stratix IV Devices* chapter.

For more information about using the signals, refer to the *Dynamic Reconfiguration in Stratix IV Devices* chapter.

Create Reset and Control Logic

The reset sequence is important for initializing the transceiver functional blocks to proper operating condition. Altera recommends a reset sequence for different transceiver configurations and protocol functional modes. The ALTGX MegaWizard Plug-In Manager provides the `tx_digitalreset`, `rx_analogreset`, `rx_digitalreset`, and `pll_powerdown` signals to reset the different functional blocks of the transceiver. You can reset the CMU PLL or the ATX PLL (based on your selection) using the `pll_powerdown` signal. For transceiver instances that share the same CMU PLL or ATX PLL, the `pll_powerdown` port of these instances must be driven by the same logic.

For more information about reset sequences, refer to the *Reset Control and Power Down in Stratix IV Devices* chapter.

Create Data Processing and Other User Logic

A typical transceiver-based design consists of custom data processing and other user logic that must be implemented in the FPGA fabric based on your application requirements. In addition to application-specific logic, for specific transceiver configurations, you may need additional logic to interface with the transceivers. This section provides examples of such logic.

PPM Detector When the Receiver CDR Is Used in Manual Lock Mode

Each receiver channel contains a clock data recovery (CDR) that you can use in automatic or manual lock mode.

If you use the receiver CDR in manual lock mode, you can control the timing of the CDR to lock to the input reference clock using the `rx_locktorefclk` port or lock to the recovered data using the `rx_locktodata` port.

When you use the receiver CDR in manual lock mode, you may need to implement the PPM detector in the FPGA fabric to determine the PPM difference between the upstream transmitter and the Stratix IV GX receiver.

Synchronization State Machine in Manual Word Alignment Mode

Each receiver channel contains a synchronization state machine in the PCS that you can enable in certain functional modes. The synchronization state machine triggers the loss of synchronization status to the FPGA fabric based on invalid 8B/10B code groups.

However, the synchronization state machine in the PCS is not available in some functional modes. You may need to implement custom logic in the FPGA fabric to indicate the loss-of-synchronization status of the received data.

Gear Boxing Logic

Some protocols require a wider data path than provided by the transceiver interface; for example, the Interlaken Protocol requires 64/67-bit encoding and decoding, but the maximum data path interface in the Stratix IV GX transceiver is 40 bits. Therefore, you must implement gear box logic to interface the 64/67-bit encoder-decoder with the transceiver interface.

Functional Blocks to Interface with the Transceiver Configured in Basic (PMA Direct) Mode

In Basic (PMA direct) mode, all the PCS functional blocks in the transceiver channel are disabled. Therefore, you may need to implement the following blocks in the FPGA fabric:

- Word Alignment—To align the byte boundary on the received data.
- Byte Deserializer—To increase the data path width to the rest of the user logic and to reduce the clock frequency of the data path by two.
- Phase Compensation FIFO (for bonded channel applications)—In bonded channel applications in which multiple transceiver channels are connected to the same upstream system (for example, one Interlaken Protocol link using 24 transceiver channels). To minimize the global clock routing resources you use, implement a phase compensation FIFO to interface the receiver side of the transceiver interface with the logic in the FPGA Fabric.
  - Use the recovered clock from each channel to clock the write side of the phase compensation FIFO.
  - Use the recovered clock from any of the channels to clock the read side of the phase compensation FIFO.

  With this method, you only use one clock resource and the subsequent receive-side logic in the FPGA fabric can operate in this single clock domain.
- Deskew Logic (for bonded channel applications)—In bonded channel applications in which multiple transceiver channels are connected to the same upstream system, the data received between multiple channels are not aligned due to potential skew in the interconnect and the upstream transmitter system. To compensate for the skew, use deskew logic in the FPGA fabric.
- Encoding/Decoding or Scrambling/Descrambling—Many protocols require the transmitter data to be encoded or scrambled to maintain signal integrity. This logic may be required in the FPGA fabric based on your application requirements.

Integrate the Design

After you implement all of the required logic, integrate the transceiver instances with the remaining logic and provide the appropriate transceiver-FPGA fabric interface clocking. Synthesize the design using third-party synthesis tools, such as Synopsys Synplicity or the Quartus II software synthesis tool. This allows you to detect syntax errors in your design.

If you are using the transceiver in Basic (PMA direct) mode, you must develop all the PCS functionality in the FPGA fabric.

Compilation

When you compile your design, the Quartus II software generates an SRAM Object File (**.sof)** or programmer object file (**.pof**) that you can download to the Stratix IV GX hardware. Typically, the first step in compiling the design is assigning pin locations for the I/Os and clocks. Use the pin planner tool in the Quartus II software to assign pins.

☞ For a basic tutorial about the Quartus II software, open the Quartus II software, click the **Help** menu and select **Tutorial**.

- Stratix IV GX transceivers support a variety of I/O standards for the input reference clocks and serial data pins. Assign pins and the logic level standard (for example, 1.5-V PCML and LVDS) for the input and output pins.

  For more information, refer to the *I/O Features in Stratix IV Devices* chapter.

- If you share the same transceiver-FPGA fabric interface clocks for multiple transceiver channels (`tx_coreclk` and `rx_coreclk`) in your design, set the **0 ppm** constraints. These constraints enable the Quartus II software to relax the legality check restrictions on clocking.

  For more information, refer to the "Common Clock Driver Selection Rules" section of the *Transceiver Clocking in Stratix IV Devices* chapter.

- For transceiver serial pins and `refclk` pins, set the on-chip termination (OCT) resistor settings.

  For more information about supported OCT settings, refer to "Transmitter Output Buffer" section of the *Transceiver Architecture in Stratix IV Devices* chapter.

- Create timing constraints for the clocks and data paths. Use the TimeQuest Timing Analyzer to set timing constraints.

  For more information about the TimeQuest Timing Analyzer, refer to the *Quartus II Development Software Handbook*.

- Compile the design. This generates a **.sof** that can be downloaded in the FPGA.

The Quartus II software generates multiple report files that contain information such as transceiver configuration and clock resource utilization. The following section describes the report files relevant to using transceivers and clock resource.

Report Files

The Quartus II software provides a report file in the synthesis, fitter, map, placement, and assembler stages. The report file provides useful information on the device and transceiver configuration generated by the Quartus II software. This section only describes the reports provided in the fitter stage. To access the report, click on the **Processing** menu, select the **Compilation Report** option and expand the **Fitter** tab.

Fitter Summary

The fitter summary provides high-level information on the FPGA fabric resources and transceiver channels used by your design. For example, to ensure that the Quartus II software has created the number of transceiver channels as specified in your design, refer to the GXB Receiver channels and GXB Transmitter channels field at the bottom of the report. For detailed information on resource utilization, expand the **Fitter** tab.

Pin-Out File

Select the **Pin-Out file** option under the **Fitter** tab. The Quartus II software displays the I/O standards and bank numbers of all the pins (used and unused) needed to connect to the board. The Quartus II software also generates a PIN file (**.pin**) with the above information. Altera recommends using the **.pin** as a guideline. Use the pin connection guidelines for board layout.

For more information about pin connection guidelines for board layout, refer to *Stratix IV GX and Stratix IV E Device Family Pin Connection Guidelines*.

Resource Section

Expand the **Resource Section** option under the **Fitter** tab to view the following tabs:

- The **GXB Transmitter channel** tab—Provides generated settings for all the transmitter channels instantiated in your design.
- The **GXB Transmitter PLL** tab—Provides generated settings for all the transmitter PLLs instantiated in your design.
- The **GXB Receiver channel** tab—Provides generated settings for all the receiver channels instantiated in your design.
- The **Global and other fast signals** tab—Displays the list of clock and other signals in your design that are assigned to the global and regional clock resources.

You can use the report file to verify whether the transceiver settings (for example, data rate), are generated per your settings in the ALTGX MegaWizard Plug-In Manager.

Verification

The SignalTap® Logic Analyzer allows you to verify design functionality using the on-chip logic analyzer. SignalTap provides options to create multiple sets of signals that can be sampled using different trigger clocks. You can add the signals to the SignalTap Logic Analyzer and save the file as an STP file (**.stp)**. When you include this **.stp** along with the design files and compile the design, the Quartus II software creates an **.sof** that allows you to verify the functionality of the signals that you added in the SignalTap Logic Analyzer file.

You can run the **.stp** that connects to the device through the JTAG port and displays the signal transitions using the Quartus II software. Because the JTAG port is required to run SignalTap, consider designing the board with the JTAG interface for debugging your system.

For more information about using SignalTap, refer to the *Design Debugging Using the SignalTap II Embedded Logic Analyzer* section in volume 3 of the *Quartus II Development Software Handbook*.

To verify the functionality of the PCS and PMA blocks, the Stratix IV GX transceiver provides diagnostic loopback features between the transmitter and the receiver channels.

For more information, refer to the "Loopback Modes" section in the *Transceiver Clocking in Stratix IV Devices* chapter.

Functional Simulation

Use the ALTGX MegaWizard Plug-In Manager-generated wrapper file to simulate the instantiated transceiver configuration in third-party simulation software such as ModelSim. For simulation, specific Altera® simulation library files are required (listed in Table 2–1). The following library files are available in VHDL and Verilog versions:

- 220pack
- 220model
- altera_mf_components
- altera_mf
- sgate_pack
- sgate
- stratixiv_hssi_component
- stratixiv_hssi_atoms

These simulation files are available under the following folder in the Quartus II installation directory: **<*Quartus II installation folder*>/eda/sim_lib**

The stratixiv_hssi_component library file is only applicable if the transceiver instance is created using VHDL.

For VHDL simulation using ModelSim, create the following libraries in your ModelSim project:

- lpm
- sgate
- altera_mf
- stratixiv_hssi

These simulation files are available under **<*Quartus II installation folder**quartus**eda**sim_lib*>**.

Compile the simulation files into the libraries specified in Table 2–1.

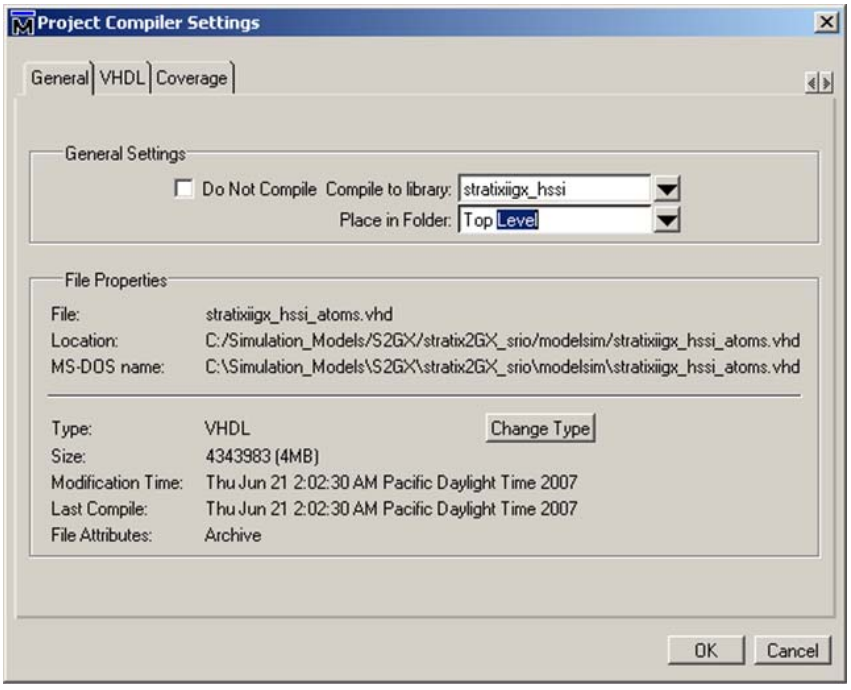
Table 2–1. Library to Compile Simulation Files

Altera Simulation Files	Library
220pack	lpm
220model	lpm
sgate pack	sgate
sgate	sgate
altera_mf_components	altera_mf
altera_mf	altera_mf
stratixiv_hssi_component	stratixiv_hssi
stratixiv_hssi_atoms	stratixiv_hssi
user design files	work

For example, to compile a file into a specific library using ModelSim, right click on the file, select **Properties**, then click the **General** tab.

In the **Compile to library** option, select the corresponding library for the file selected. Figure 2–2 shows the ModelSim window compilation of files in a specific library for the Stratix II GX device.

Figure 2–2. ModelSim Option to Compile Files in a Specific Library



Include all the libraries in the search path. Add the ALTGX and ALTGX_RECONFIG MegaWizard Plug-In Manager-generated wrapper files (**.v** or **.vhd**) and all of the design files to the library. Compile all the library files first, then the design files, and lastly run the simulation.

For Verilog simulation, add the ALTGX and ALTGX_RECONFIG MegaWizard Plug-In Manager-generated Verilog wrapper files (**.v**), the Altera library files, and all of the design files. Compile all the library files first, then the simulation model file, followed by the design files. Lastly, run the simulation.

These guidelines are further described in "Example 1: Fibre Channel Protocol Application" below.

For more information about functional register transfer level (RTL) simulation or post-fit simulation, refer to the *Simulation* chapter in volume 3 of the *Quartus II Handbook*.

Guidelines to Debug Transceiver-Based Designs

This section provides guidelines to debug transceiver-based designs. If a system failure occurs, the first step is to ensure the functionality of the logic within the FPGA. Use the following information when you observe a system failure.

Guidelines to Debug the FPGA Logic and the Transceiver Interface

Before checking the functionality in silicon, perform functional simulation to ensure the basic functionality of the RTL and the transceiver-FPGA fabric interface.

- Understand the limitations of functional simulation. If you intend to simulate timing parameters, consider post-fit simulation. The functional simulation model for transceivers does not model timing-related parameters or uncertainties in the transceiver data path. For example, the PPM difference in the rate matcher clocks (clock rate compensation) or the phase differences between the read and write side of the phase compensation FIFO are not modeled.

  For information about functional RTL simulation or post-fit simulation, refer to the *Simulation* chapter in volume 3 of the *Quartus II Handbook*.

- Check whether the compiled design has timing violations in the TimeQuest Timing Analyzer report. Set the appropriate timing constraints on the failing paths.

  For information about using the TimeQuest Timing Analyzer, refer to the *The Quartus II TimeQuest Timing Analyzer* chapter in volume 3 of the *Quartus II Handbook*.

- Verify the functionality of the transmitter and receiver data path with serial loopback. Dynamically control the serial loopback through the `rx_seriallpbken` port. When this signal is asserted, data from the transmitter serializer is looped back to the receiver CDR of the channel.

- Use SignalTap to verify the behavior of the user logic and the transceiver interface signals. If you have FPGA I/O pins available for debug, you can also use the external logic analyzer to debug the functionality of the device.

  For more information, refer to the *In-System Debugging Using External Logic Analyzers* chapter in volume 3 of the *Quartus II Handbook*.

  To use these features, you must connect the JTAG configuration pins in the FPGA.

- Verify the interconnect on the receive side by configuring the transceiver in reverse serial loopback mode. In this case, the recovered data from the receiver channel is sent to the transmitter buffer. To configure a transceiver channel operating in a different configuration to reverse serial loopback mode, use the dynamic reconfiguration controller.
- Check whether the transceiver FPGA fabric interface clocking schemes follow the recommendations provided in the "FPGA Fabric-Transceiver Interface Clocking" section in the *Transceiver Clocking in Stratix IV Devices* chapter.
- Ensure that you have used the recommended transceiver reset sequence.

Guidelines to Debug System Level Issues

If you have determined that the logic in the FPGA fabric is functionally correct, check for system level issues:

- Check the voltage ripple across the 2 kΩ resistor that is connected to the RREF pin. The voltage ripple must be less than 60 mv.
- Measure the eye on the near-end and far-end of the transmitter to understand the jitter added by the transmitter and interconnect.
  - Ensure that the high-speed scopes you use for measurement have sufficient bandwidth (the bandwidth rating on the scope and cables must be at least three times the serial data rate).
  - Check whether the eye meets the eye-mask requirements if specified by the protocol application.
  - Use scopes that provide information on the different jitter components to understand the possible source of the increased jitter. For example, increased intersymbol interface (ISI) indicates potential bandwidth limitations on the interconnect.

    Some scopes, such as Agilent 86100C DCA, require pre-defined patterns (for example, PRBS7 or PRBS23) to provide jitter components.

- Measure signals on the traces (no connector) using a high-impedance differential probe with short leads.

- Ensure that characteristic impedance on the interconnect matches the source and load systems.
  - Check for impedance discontinuities on the trace by Time Domain Reflectometry (TDR).
  - Revisit the board design, layout, and routing for any inconsistencies that can cause impedance discontinuities.
  - Check whether the termination schemes on the Stratix IV GX device and on the upstream system are matched. Altera recommends using OCT in the Stratix IV GX device instead of external termination to improve signal integrity.
  - Change the transmit output differential voltage to improve eye amplitude.
- Compensate for high frequency losses in the interconnect by changing the equalization settings of the Stratix IV GX device and check for improvement of the bit error rate. If the upstream system does not have an equalization feature, increase the pre-emphasis (1st post tap) of the Stratix IV GX transmitter. In cases where there are multiple interconnects between the Stratix IV GX device and the upstream system, use the pre-tap and 2nd post tap. Altera provides tools to select the pre-emphasis.
- Measure the increase in jitter at the near end and far end with one channel turned on at a time if you have multiple transceiver channels connected to the upstream system. This helps to observe the effect of cross talk from adjacent channels on the victim channel.
  - Check the board layout and routing to ensure that you have implemented the design practices to mitigate cross talk.
- Ensure that the input voltage and duty cycle of the input reference clock source provided to the transmitter PLLs meet the input reference clock requirements.
- Check whether the voltage drop on the power supplies is within the specified tolerance range.
  - Measure the voltage at the via beneath the power supply pin using a high-impedance probe.
  - Check whether the voltage regulator specifications meet the Stratix IV GX power supply requirements.
  - Revisit the power distribution scheme for the supply voltage to ensure that it is designed to handle the transient current requirements of the transceiver.

  For the tolerance values of the different power supplies, refer to the *DC and Switching Characteristics for Stratix IV Devices* chapter.
- Check for periodic modulation of other frequency components on the transmit data. Send a high-frequency pattern (1010) from the transmitter side and connect the transmitter serial output to a spectrum analyzer.

For more information about debugging Stratix IV GX transceivers, refer to *AN 553: Debugging Transceivers*.

Example 1: Fibre Channel Protocol Application

Assume that you want to implement a fibre channel protocol application using three transceiver channels. Consider the following system requirements:

- You need three transceiver channels
- All the channels need to be placed in the same transceiver block
- All the channels need to have independent control to reset their PCS and PMA functional blocks

Table 2–2 lists the transceiver channel configuration for Example 1.

Table 2–2. Transceiver Channel Configuration for Example 1

Channels	Mode of Operation	Data Rate	Input Reference Clock Frequency (MHz)
0	**Receiver and Transmitter**	FC4G (4.25 Gbps)	106.25
1	**Receiver and Transmitter**	FC1G (1.0625 Gbps)	53.125
2	**Transmitter Only**	FC4G (4.25 Gbps)	106.25

Phase 1—Architecture

In this phase, check whether the Stratix IV GX device supports or meets your design requirements.

Device Specification

Consider the questions listed in Table 2–3 before setting device-specific parameters.

Table 2–3. Device Specific Parameters

Questions	Answer
Do the parameters meet the fibre channel protocol electrical requirements?	Yes For more information, refer to the "Transceiver Performance Characteristics" section in the *DC and Switching Characteristics for Stratix IV Devices* chapter
Are three transceiver channels available?	Yes
Is there support for 4.25 Gbps and 1.0625 Gbps data rates?	Yes Two CMU PLLs are available within each transceiver block to support two different transmitter data rates. Each receiver channel contains a dedicated receiver CDR that supports 4.25 Gbps and 1.0625 Gbps data rates.

For the maximum data rates supported, refer to the "Transceiver Performance Specifications" section in the *DC and Switching Characteristics for Stratix IV Devices* chapter.

Transceiver Configuration

The fibre channel protocol uses an 8B/10B encoder and requires clock rate compensation.

Functional Blocks

Consider the questions listed in Table 2–4 before configuring the transceiver.

Table 2–4. Configuring the Transceiver

Questions	Answer
Is the 8B/10B encoder in the PCS block fibre channel compliant?	No The fibre channel protocol consists of two different End-of-Frame (EOFt) ordered sets. The correct EOFt ordered set sent by the user logic depends on the ending disparity of the word preceeding the EOFt. The Stratix IV GX transceiver does not provide running disparity flags to the user logic. Therefore, the user logic might not be able to select the correct EOFt ordered set.
Is there a workaround?	Yes Implement the 8B/10B encoder in the FPGA fabric.
Is the clock rate compensation block in the PCS available without an 8B/10B encoder?	No You can implement this in the FPGA fabric.

The design requires a **Transmitter and Receiver** configuration for two channels and a **Transmitter Only** configuration for one channel (Table 2–5).

Table 2–5. Multiple Channels

Questions	Answer
Does the Stratix IV GX transceiver support these two configurations and allow you to combine them within the same transceiver block	Yes The available FPGA fabric interface width is 20 or 40 bits to support 4.25 Gbps and 1.0625 Gbps data rates, respectively. This FPGA fabric interface facilitates 8B/10B encoding and decoding in the FPGA fabric without additional re-arrangement of the received parallel data to a 10-bit boundary.

Dynamic Reconfiguration

If your application requires you to dynamically reconfigure the transceiver PMA controls, ensure that you understand the settings, options, and user logic required to enable this feature.

For more information, refer to the "Interfacing ALTGX and ALTGX_RECONFIG Instances" section in the *Dynamic Reconfiguration in Stratix IV Devices* chapter.

For more information about initiating read and write transactions, refer to the "Dynamically Reconfiguring PMA Controls" section in the *Dynamic Reconfiguration in Stratix IV Devices* chapter.

If you are using the channel reconfiguration feature, enable the appropriate options in the ALTGX and ALTGX_RECONFIG MegaWizard Plug-In Managers.

You can dynamically use the reconfiguration modes to reconfigure different functional blocks in a transceiver channel using **.mifs**. For information about generating **.mif**s, refer to the "Channel and CMU PLL Reconfiguration Mode Details" section in the *Dynamic Reconfiguration in Stratix IV Devices* chapter.

Clocking

Consider the questions listed in Table 2–6 before configuring clocking.

Table 2–6. Configuring Clocking

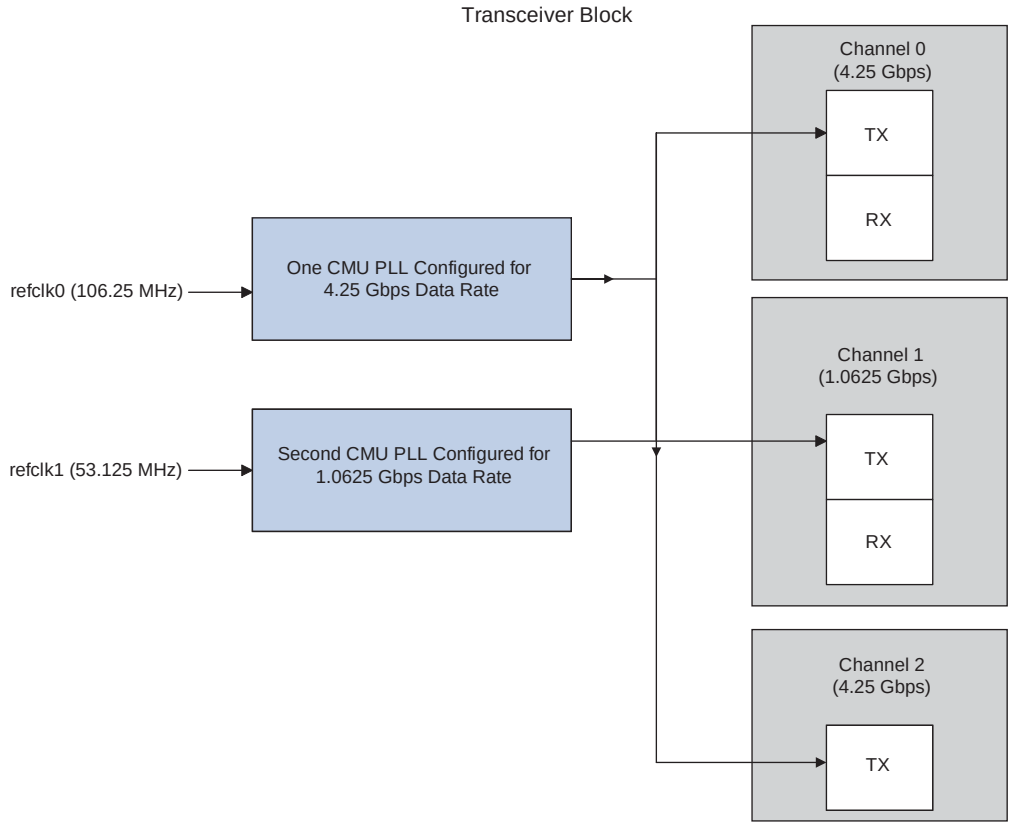
Questions	Answer
Is there support for two different input reference clocks?	Yes The Stratix IV GX transceiver has two `refclk` pins for each transceiver block.
Do the `refclk` pins support the required frequency range?	Yes The minimum frequency range of `refclk` is 50 MHz; the maximum frequency range is 622.08 MHz.
Can transceiver-FPGA fabric interface clocking be shared?	No The design requires independent control on all channels, so you must not share the transceiver-FPGA fabric interface clock of one channel with another channel. Each of the channels must use its own `tx_clkout` and `rx_clkout` signals to clock the data between the transceiver channels and the FPGA fabric.
Does the Stratix IV GX transceiver support this feature?	Yes

For more information about clocking the transmitter and receiver channel data path for this type of configuration, refer to the "Transmitter Channel Datapath Clocking" section of the *Transceiver Clocking in Stratix IV Devices* chapter.

Figure 2–3 shows the transmitter side of the transceiver setup for Example 1.

The transmitter side receives its clocks from the clock multiplier unit (CMU) PLLs. The receiver side contains its dedicated CDR that provides the high-speed serial and low-speed parallel clocks to its PMA and PCS blocks, respectively.

Figure 2–3. Top-Level Transceiver Setup—Transmitter-Side Only



Phase 2—Implementation

Create the transceiver instance using the ALTGX MegaWizard Plug-In Manager.

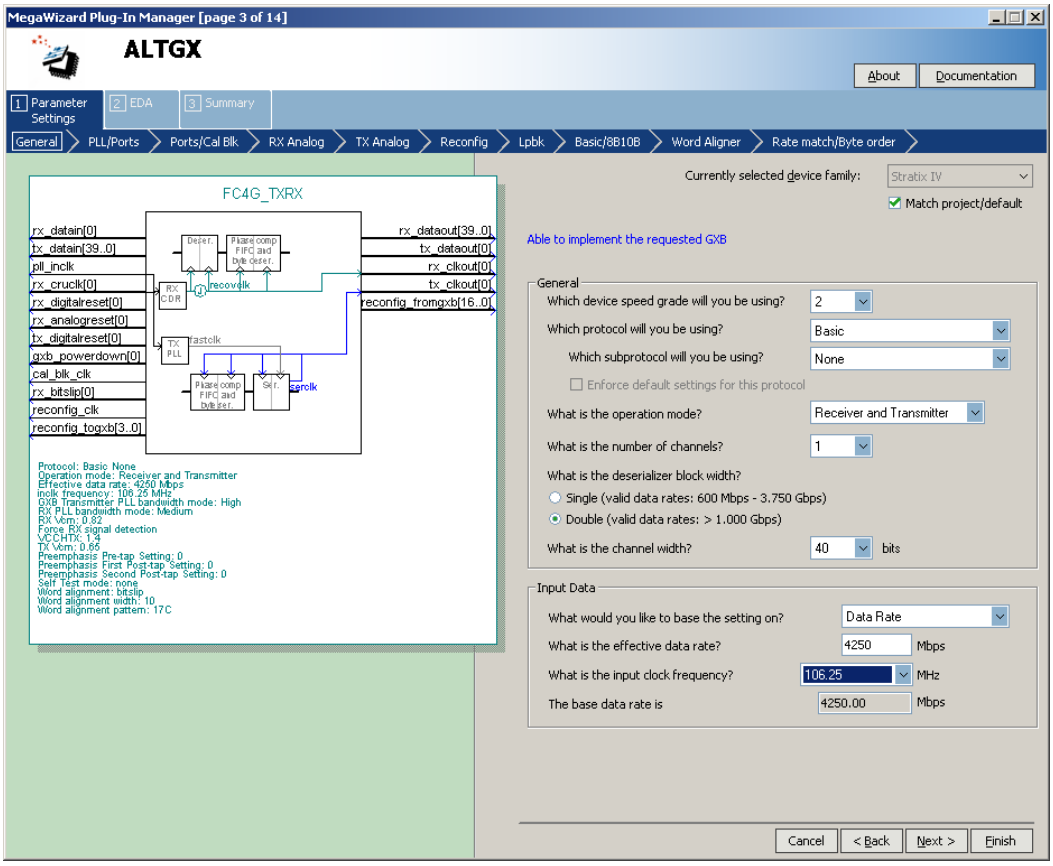
For a description of the individual options, refer to the *ALTGX Transceiver Setup Guide for Stratix IV Devices* chapter.

Create the Transceiver Instance for an FC4G Configuration (Channel 0)

Figure 2–4 through Figure 2–14 show the different options available in the ALTGX MegaWizard Plug-In Manager to create the transceiver channel instance for the FC4G data rate. Use this instance for channel 0, with the following settings:

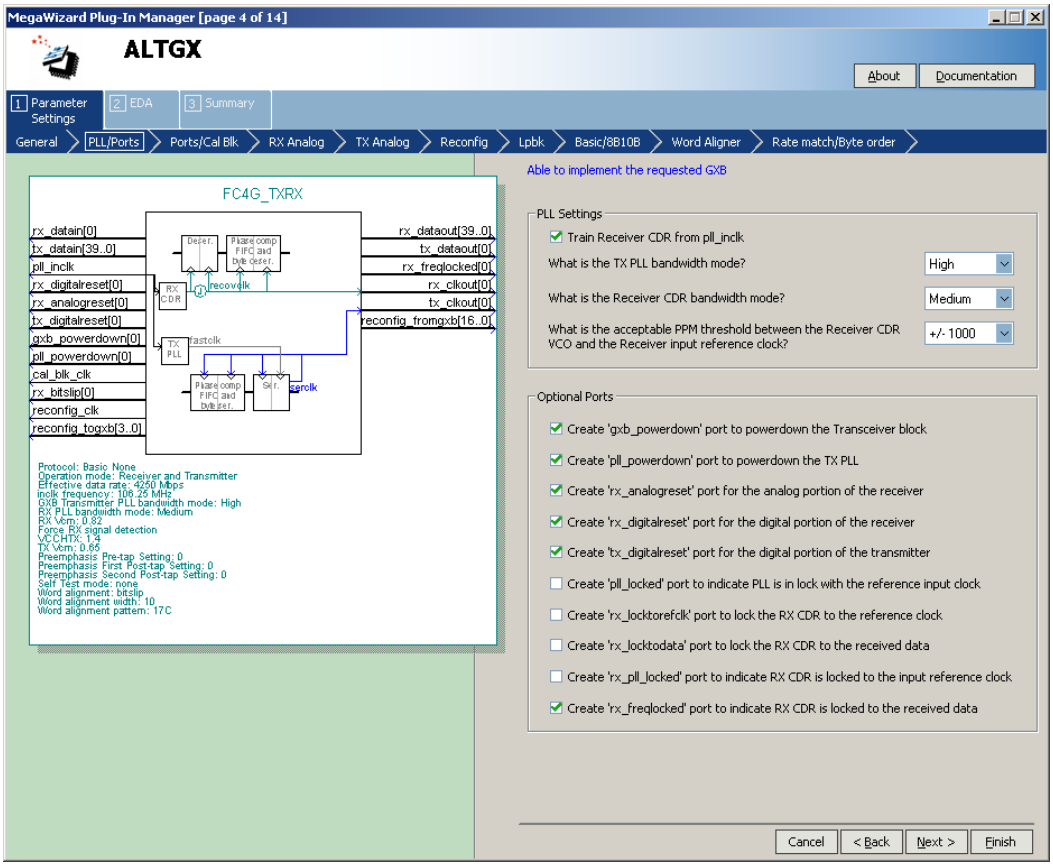
- **General** screen—You can configure the Stratix IV GX transceiver for fibre channel protocol using Basic mode. Set the options with the values shown in Figure 2–4.

Figure 2–4. FC4G Instance Settings (General Screen)



- **PLL/Ports** screen—Check the **Train Receiver CDR from PLL inclk** option, as shown in Figure 2–5. When you select this option, the same input reference clock used for the CMU PLL is provided as a training clock to the receiver CDR.

Figure 2–5. FC4G Instance Settings (PLL/Ports Screen)

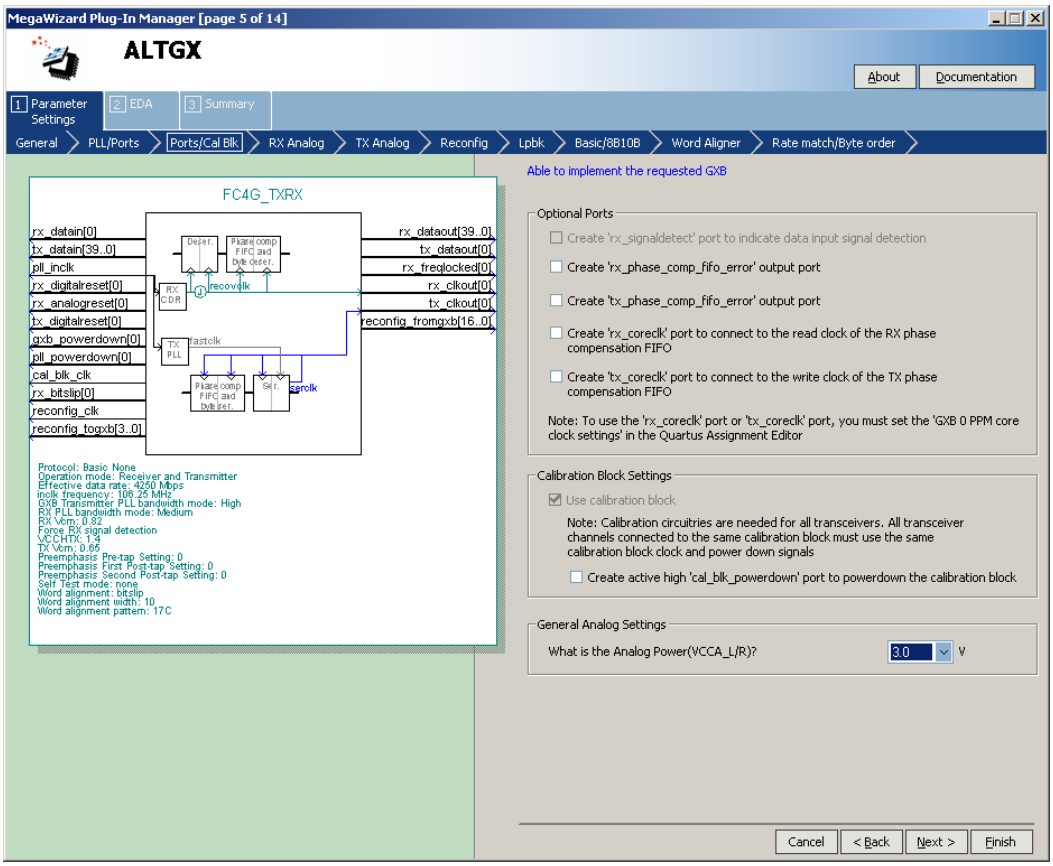


- Check the `pll_powerdown` signal. This signal allows you to power down the CMU PLL. Use this signal as part of your reset sequence.
- Check the `pll_locked` signal. This signal indicates whether the CMU PLL is locked to the input reference clock. The user logic waits until the `pll_locked` signal goes high before transmitting data.
- Check the `rx_freqlocked` signal. This signal indicates whether the receiver CDR is locked to data. When the receiver CDR is configured in automatic lock mode, assert the `rx_digitalreset` signal if the `rx_freqlocked` signal goes low to keep the receiver PCS under reset. Altera recommends specific transceiver reset sequences to ensure proper device operation.

For more information about receiver CDR and lock modes, refer to the "Receiver Channel Datapath" section of the *Transceiver Architecture in Stratix IV Devices* chapter.

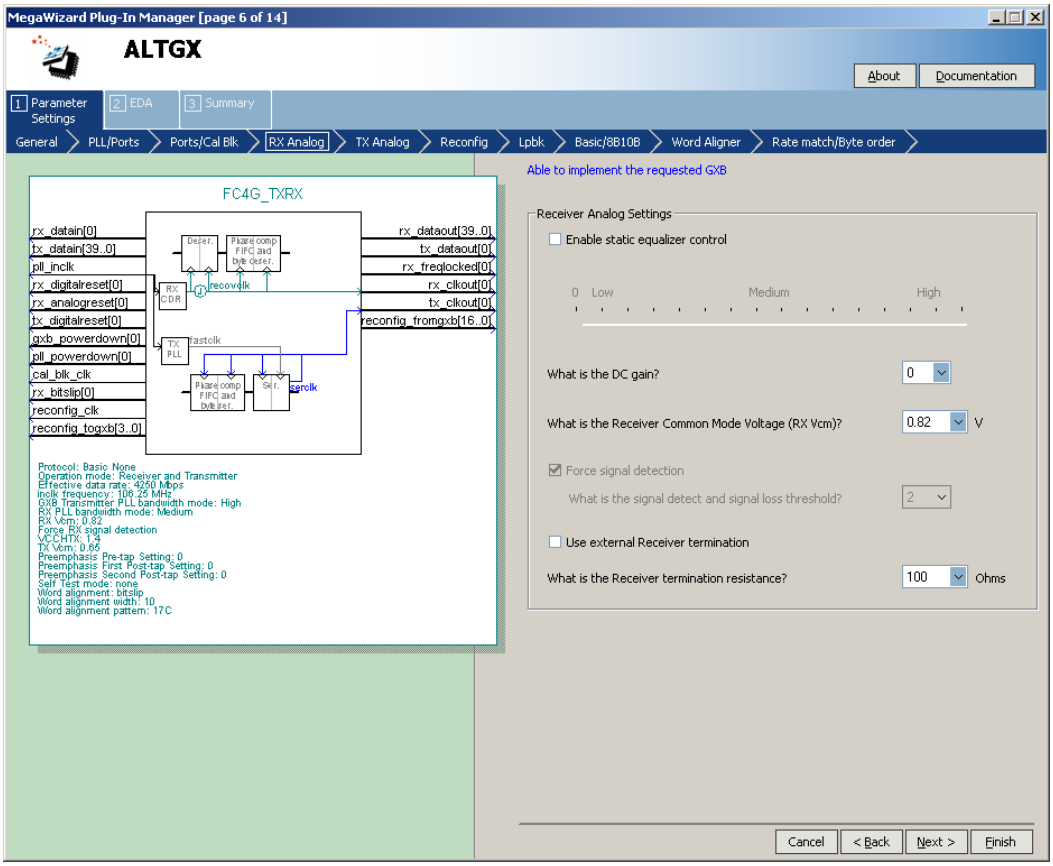
- **Ports /Cal Blk** screen—The calibration block is required so it is always enabled. Select the options shown in Figure 2–6.

Figure 2–6. FC4G Instance Settings (Ports/Cal Blk Screen)



- **RX Analog** screen—Select the options shown in Figure 2–7.

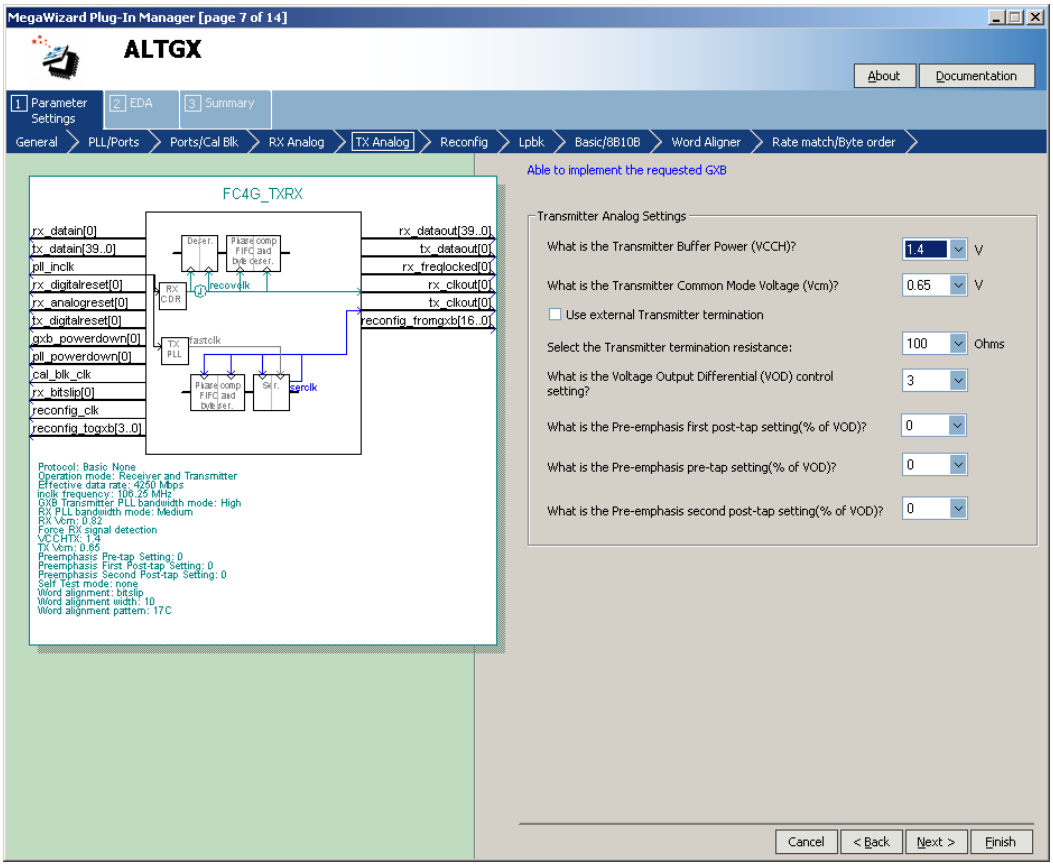
Figure 2–7. FC4G Instance Settings (RxAnalog Screen)



For a description of the individual options, refer to the *ALTGX_RECONFIG Megafunction User Guide for Stratix IV Devices* chapter.

- **TX Analog** screen—Select the output differential voltage and common mode voltage values that meet the fibre channel protocol specification. If you intend to transmit data through faulty interconnects, select the pre-emphasis settings shown in Figure 2–8.

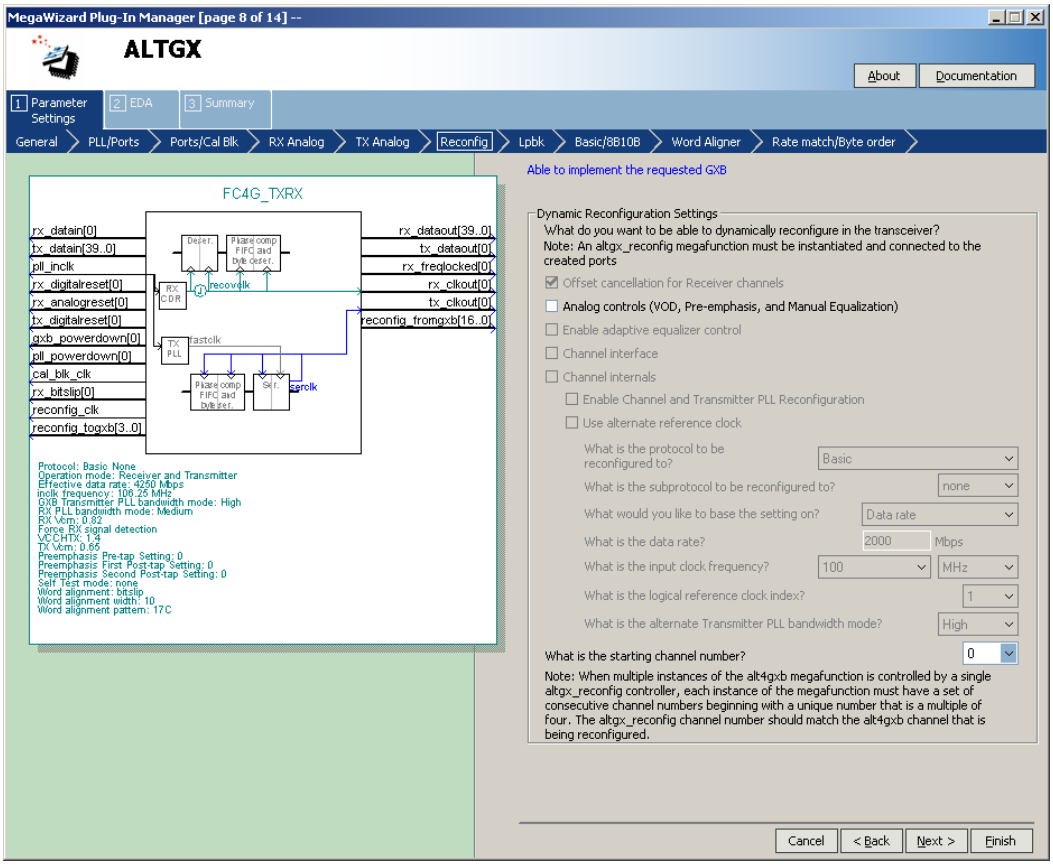
Figure 2–8. FC4G Instance Settings (TX Analog Screen)



For more information about pre-emphasis settings, refer to the *DC and Switching Characteristics for Stratix IV Devices* chapter.

- **Reconfig** screen—Set the starting channel number to **0**. Because offset cancellation is required for receiver channels, the **Offset Cancellation for Receiver Channels** option is automatically enabled. Ensure that you connect the `reconfig_fromgxb` and `reconfig_togxb` ports with the dynamic reconfiguration controller (Figure 2–9).

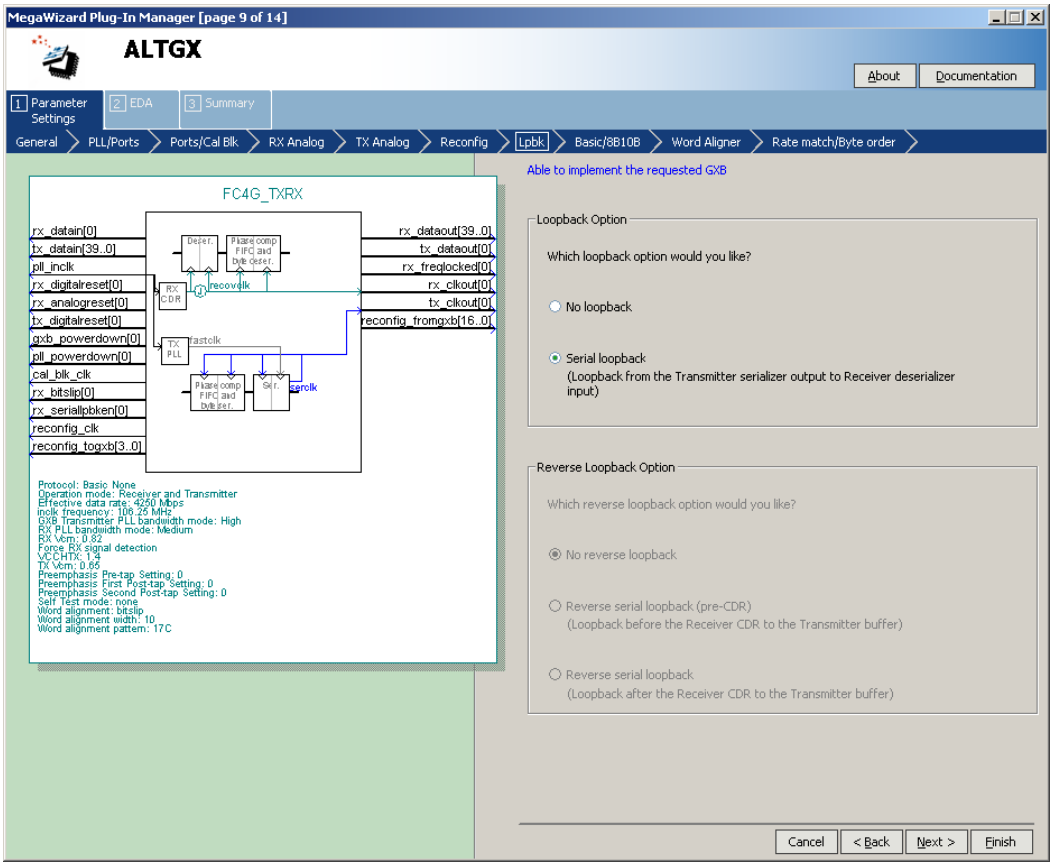
Figure 2–9. FC4G Instance Settings (Reconfig Screen)



For more information about the starting channel numbers, refer to the "Logical Channel Addressing" section of the *Dynamic Reconfiguration in Stratix IV Devices* chapter.

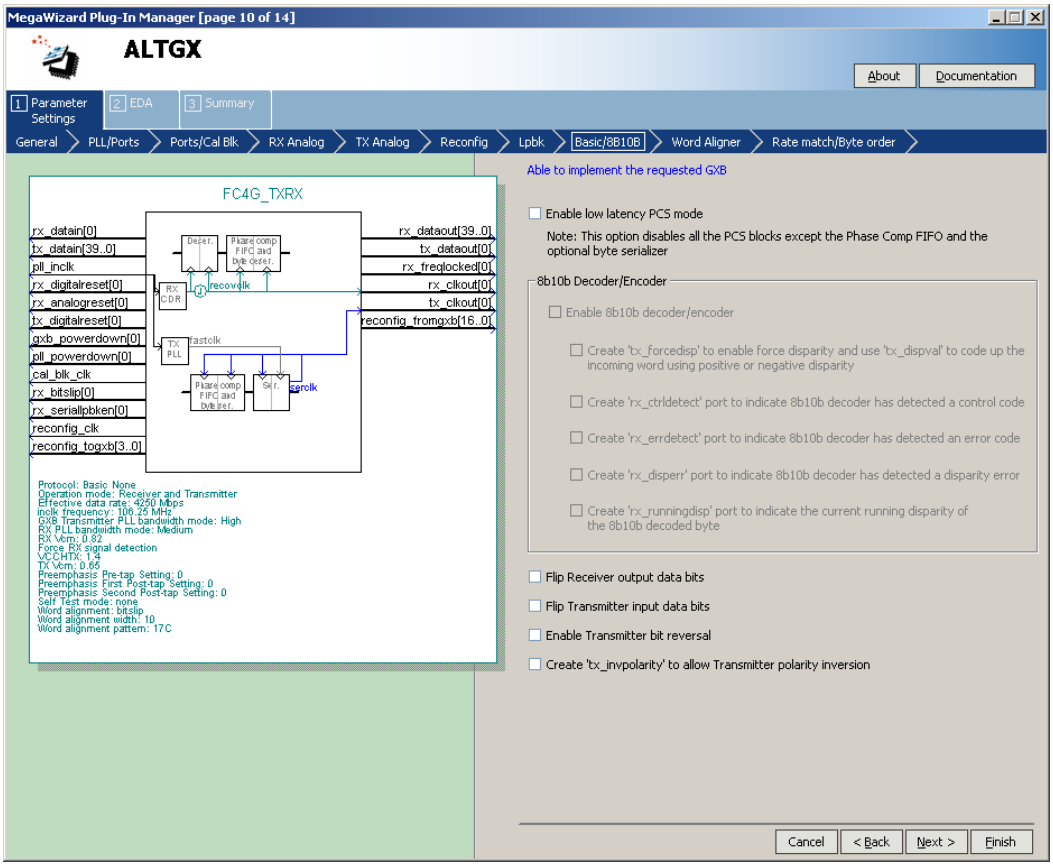
- **Lpbk** screen—The serial loopback option is enabled, as shown in Figure 2–10.

Figure 2–10. FC4G Instance Settings (Lpbk Screen)



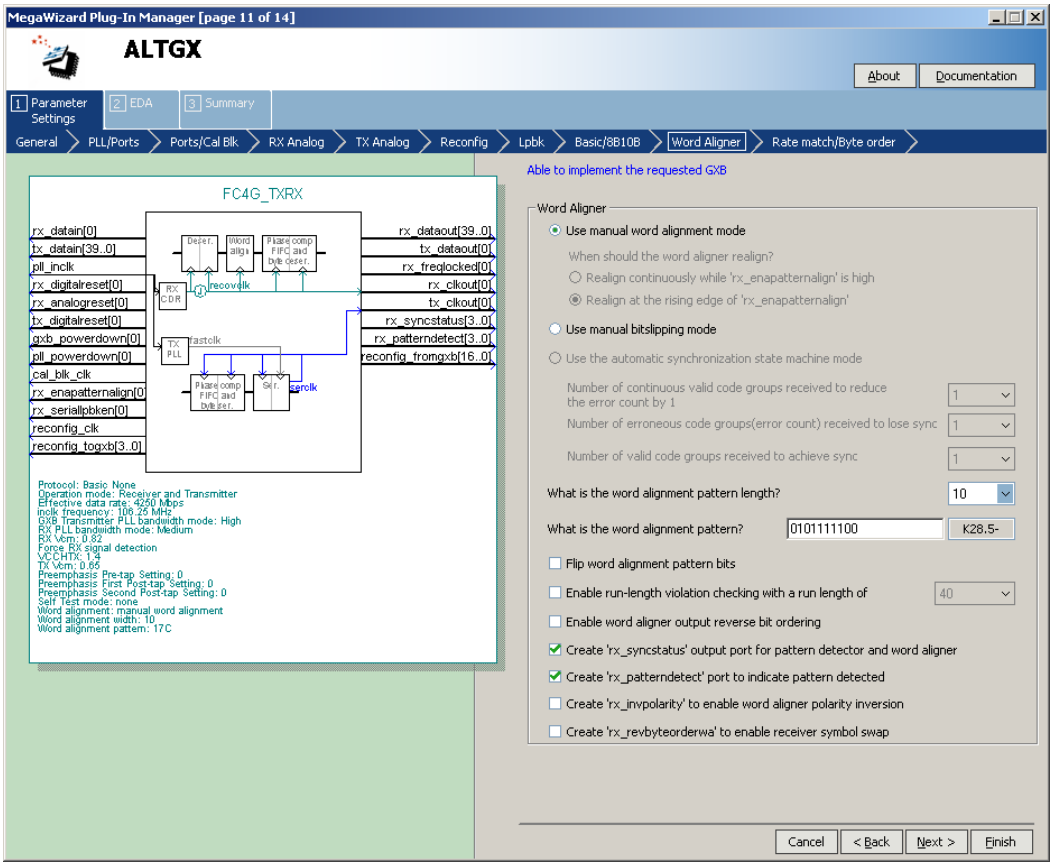
- **Basic/8B10B** screen—The Basic/8B10B screen is shown in Figure 2–11. The 8B/10B encoder is not compatible with the fibre channel protocol application; therefore, this option is unchecked.

Figure 2–11. FC4G Instance Settings (Basic 8B/10B)



- **Word Aligner** screen—The fibre channel protocol requires that you use K28.5 to align the byte boundary. In the **What is the word alignment pattern?** option, set one of the 10-bit disparity values to **K28.5**. The word aligner automatically detects when the other disparity value is received.

Figure 2–12. FC4G Instance Settings (Word Aligner Screen)



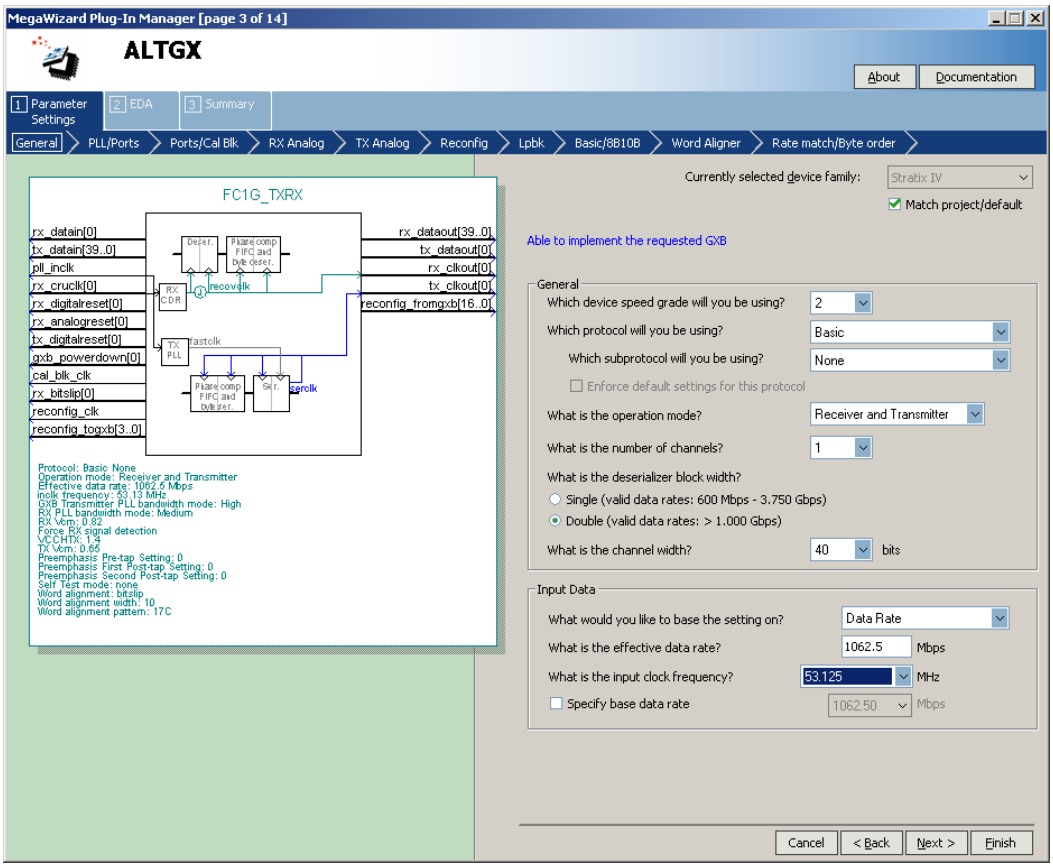
- Select the `rx_patterndetect` and `rx_syncstatus` signals. The `rx_patterndetect` signal indicates whenever the word alignment pattern is detected in the word boundary.
- Click **Finish** to exit the ALTGX MegaWizard Plug-In Manager.

Create the Transceiver Instance for an FC1G Configuration (Channel 1)

Creating the instance for FC1G is very similar to that of the FC4G configuration, with the following changes:

- **General** screen—Set the values shown in Figure 2–13.

Figure 2–13. FC1G Instance (Channel 1) Settings (General Screen)



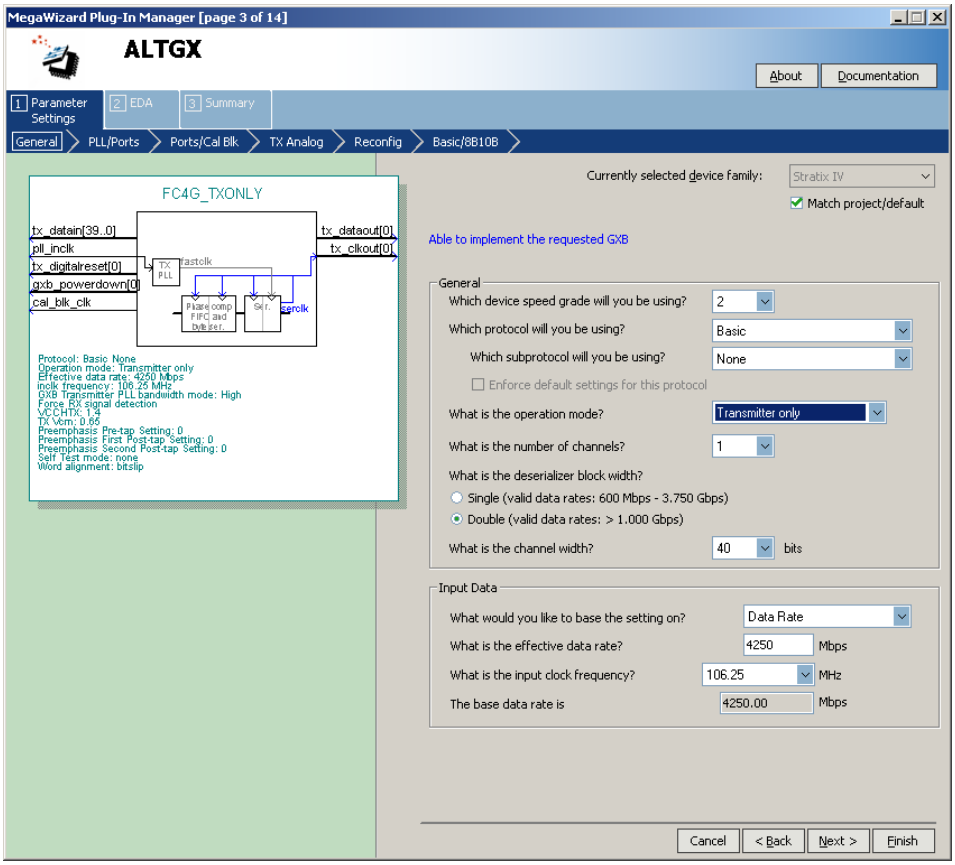
- **Reconfig** screen—Set the starting channel number to **4**.

Create the Instance for an FC4G Configuration—Transmitter Only Mode (Channel 2)

This configuration is similar to the channel 0 configuration, with the following changes:

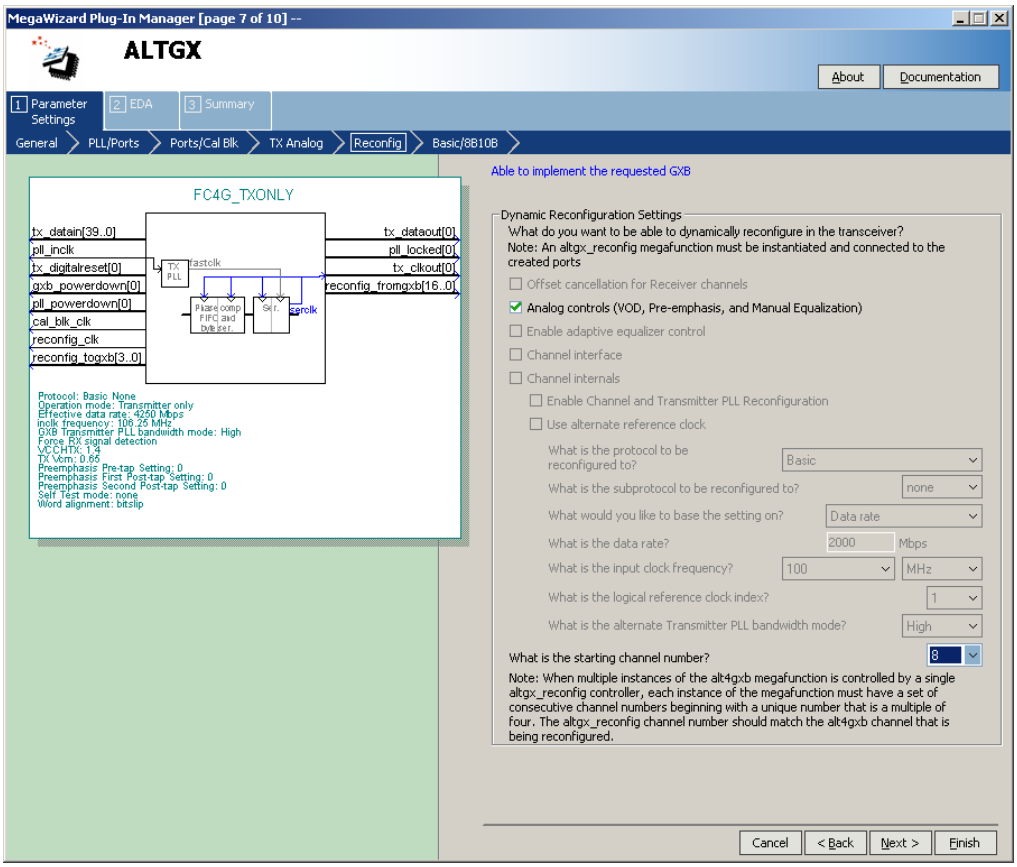
- Set the operation mode to **Transmitter Only**, as shown in Figure 2–14. Because this is a **Transmitter Only** instance, all the options relevant to the receiver are not available in the ALTGX MegaWizard Plug-In Manager.

Figure 2–14. FC4G_TXONLY Instance (Channel 1) Settings (General Screen)



- **Reconfig** screen—Set the starting channel number to **8**. Select the **Analog controls** option even if you do not intend to dynamically reconfigure the PMA controls, as shown in Figure 2–15. Selecting this option is required for this example scenario because:
  - For a **Transmitter Only** instance, offset cancellation is not available; therefore, the `reconfig_fromgxb` and `reconfig_togxb` ports are not available.
  - The other two instances (containing a receiver channel) have these ports available because offset cancellation is automatically enabled.
  - If one transceiver instance has the `reconfig_fromgxb` and `reconfig_togxb` ports enabled, the Quartus II software requires the other transceiver instances to have these ports enabled to combine them in the same transceiver block. Therefore, for this **Transmitter Only** instance, the **Analog options...** must be selected.

Figure 2–15. FC4G_TXONLY Instance (Reconfig) Screen

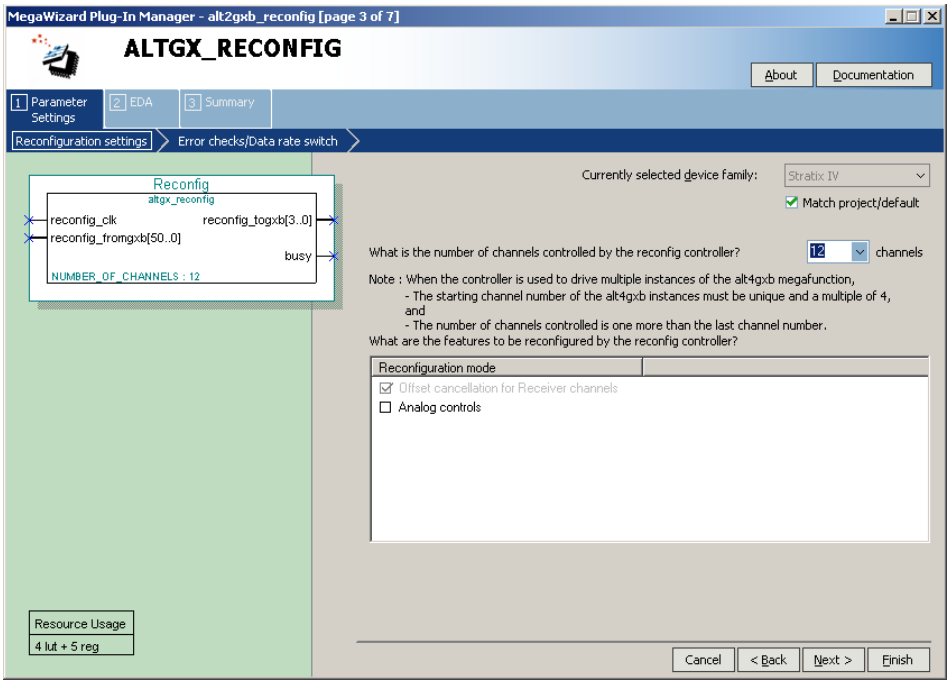


For more information about the requirements to combine multiple transceiver instances, refer to the "Combining Transceiver Instances in Multiple Transceiver Blocks" section in the *Configuring Multiple Protocols and Data Rates in Stratix IV Devices* chapter.

Create the Dynamic Reconfiguration Controller (ALTGX_Reconfig) Instance

This section only describes the relevant options that must be set to implement the application.

Figure 2–16. ALTGX_Reconfig Settings (Reconfiguration Settings Screen)



For more information, refer to the *Dynamic Reconfiguration in Stratix IV Devices* chapter.

Figure 2–16 shows the options that you must set (assuming that you do not require dynamic reconfiguration of the PMA controls in the transceiver channels).

For more information about selecting the **Number of Channels** option, refer to the "Total Number of Channels Option in the ALTGX_RECONFIG Instance" section in the *Dynamic Reconfiguration in Stratix IV Devices* chapter.

Connect the following:

- `reconfig_fromgxb[16:0]` of the ALTGX_RECONFIG instance to the FC4G instance (channel0)
- `reconfig_fromgxb[33:17]` to the FC1G instance (channel1)
- `reconfig_fromgxb[50:34]` to the FC4G **Transmitter Only** instance (channel2)
- `reconfig_togxb[3:0]` of the ALTGX_RECONFIG instance to all three transceiver instances

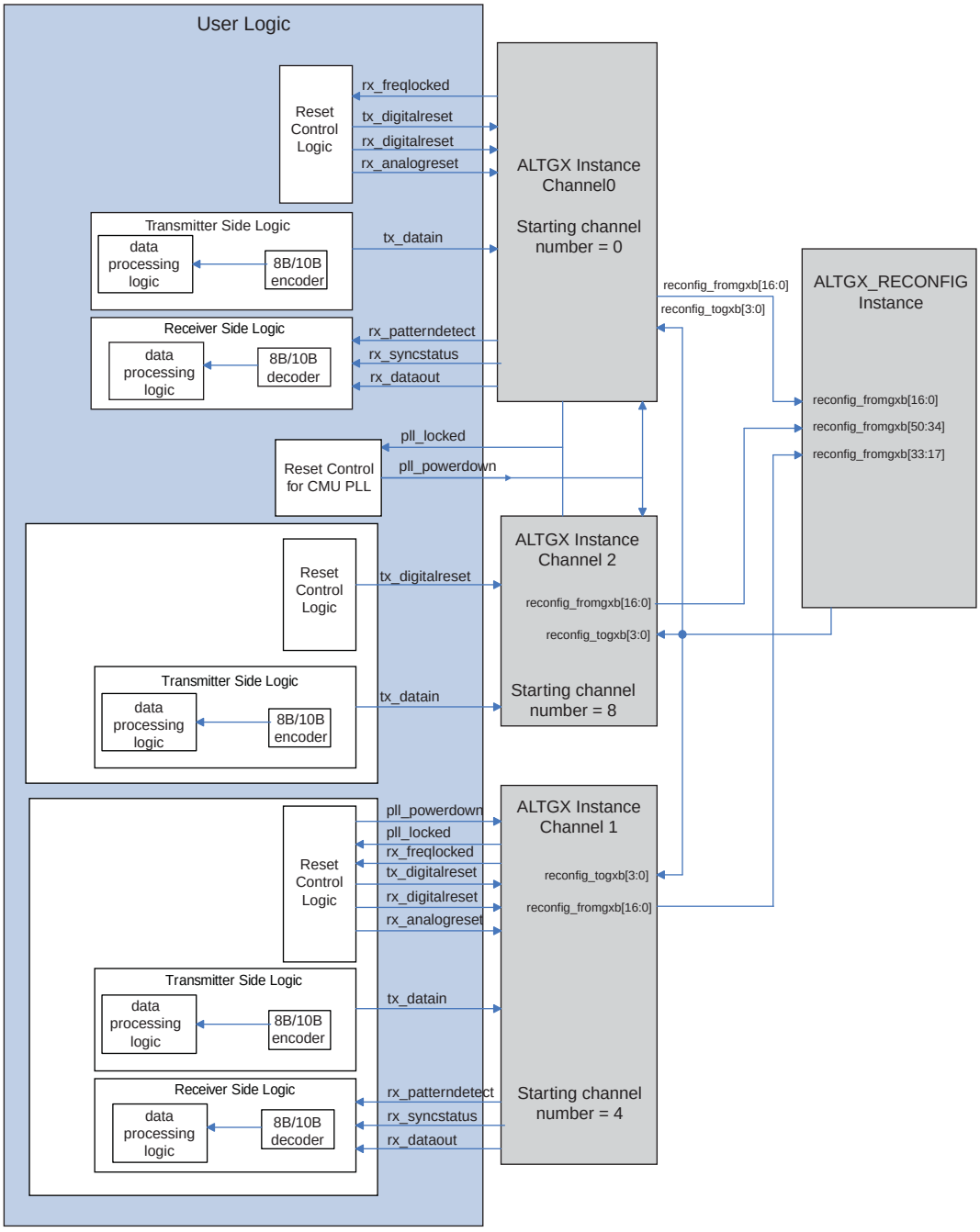
Create Reset Logic to Control the FPGA Fabric and Transceivers

The design requires independent control on each channel. Altera recommends creating independent reset control logic for each channel.

In this design, channel 0 and channel 2 share the same CMU PLL (because they are configured at the same data rate) and channel 1 uses the second CMU PLL. When you create a **Transmitter Only** or **Receiver and Transmitter** instance, the ALTGX MegaWizard Plug-In Manager provides a `pll_powerdown` signal to reset the CMU PLL that provides clocks to the transmitter channel. In this design example, because channels 0 and 2 share the same CMU PLL, drive the `pll_powerdown` port of channel 0 and channel 2 in the ALTGX instance from the same logic.

Channels 0, 1, and 2 have separate `rx_digitalreset`, `rx_analogreset`, and `tx_digitalreset` signals. Figure 2–17 shows the interface between the three transceiver instances and the FPGA fabric.

Figure 2–17. Transceiver—FPGA Fabric Interface



Create Data Processing and Other User Logic

For this example, you must implement the 8B/10B encoder and decoder in the FPGA fabric. Figure 2–17 on page 2–35 shows the logic on the transmitter and receiver side and the system logic controls for all channels in the FPGA fabric. This block diagram is a representation of a typical system and may not exactly show the different blocks in a practical application. Interface all the logic blocks with the transceiver.

If you would like to add SignalTap for verification, first complete synthesis, then add the transceiver-FPGA fabric or other user logic signals in SignalTap. Lastly, compile the design to generate the **.sof**.

Phase 3—Compilation

Assign pins for the input and output signals in your design. The Quartus II software versions 8.1 and earlier do not allow pin assignments for the Stratix IV GX device.

Set the OCT values for the transceiver serial pins, add timing constraints for the clocks and data paths in your logic, then compile the design.

Phase 4—Simulating the Design

To simulate the design, follow the steps outlined in "Functional Simulation" on page 2–12.

Document Revision History

Table 2–7 lists the revision history for this chapter.

Table 2–7. Document Revision History (Part 1 of 2)

Date	Version	Changes
February 2011	4.1	■ Applied new template. ■ Updated chapter title. ■ Minor text edits
November 2009	4.0	■ Added Table 2–3, Table 2–4, Table 2–5, and Table 2–6. ■ Minor text edits.
June 2009	3.1	■ Updated the "Introduction", "Power Supplies", "Transceiver Configuration", "Clocking", "Create Transceiver Instances", "Create Dynamic Reconfiguration Controller Instances", "Create Data Processing and Other User Logic", "Functional Simulation" sections. ■ Added the "Board Design Requirements", "Gear Boxing Logic", "Guidelines to Debug the FPGA Logic and the Transceiver Interface", and "Guidelines to Debug System Level Issues" sections. ■ Added introductory sentences to improve search ability.
March 2009	3.0	■ Add "Power Supplies" on page 2–6 ■ Updated "Dynamic Reconfiguration" on page 2–4 ■ Text edits

Table 2–7. Document Revision History (Part 2 of 2)

Date	Version	Changes
November 2008	2.0	■ Added "Transceiver Configuration" on page 2–3 ■ Added "Create Dynamic Reconfiguration Controller Instances" on page 2–8 ■ "Dynamic Reconfiguration" on page 2–15 ■ Updated "Create the Instance for an FC4G Configuration—Transmitter Only Mode (Channel 2)" on page 2–28 ■ Added "Create the Dynamic Reconfiguration Controller (ALTGX_Reconfig) Instance" on page 2–30 ■ Updated Figure 2–1, Figure 2–4, Figure 2–5, Figure 2–6, Figure 2–7, Figure 2–8, Figure 2–10, Figure 2–11, Figure 2–12, Figure 2–13, and Figure 2–14 ■ Added Figure 2–9, Figure 2–15, and Figure 2–16
May 2008	1.0	Initial release.

3. ALTGX_RECONFIG Megafunction User Guide for Stratix IV Devices

SIV53004-3.1

You can use the ALTGX_RECONFIG MegaWizard™ Plug-In Manager in the Quartus® II software to create and modify design files for the Stratix® IV device family. This chapter describes the different Quartus II settings for dynamic reconfiguration in the ALTGX_RECONFIG MegaWizard Plug-In Manager.

The MegaWizard Plug-In Manager helps you create or modify design files that contain custom megafunction variations. These auto-generated MegaWizard files can then be instantiated in a design file. The MegaWizard Plug-In Manager allows you to specify options for the ALTGX_RECONFIG megafunction.

Start the MegaWizard Plug-In Manager using one of the following methods:

- Choose the **MegaWizard Plug-In Manager** command (Tools menu).
- When working in the **Block Editor** (schematic symbol), open the Edit menu and choose **Insert Symbol**. The **Symbol** dialog box appears. In the **Symbol** dialog box, click **MegaWizard Plug-In Manager**.
- Start the stand-alone version of the MegaWizard Plug-In Manager by typing the following command at the command prompt: `qmegawiz`.

Dynamic Reconfiguration

This section describes the options available on the individual pages of the ALTGX_RECONFIG MegaWizard Plug-In Manager.

The MegaWizard Plug-In Manager provides a warning if any of the settings you choose are illegal.

Figure 3–1 shows the first page of the MegaWizard Plug-In Manager. To generate an ALTGX_RECONFIG custom megafunction variation, select **Create a new custom megafunction variation**. Click **Next**.

Figure 3–1. MegaWizard Plug-In Manager (Page 1)

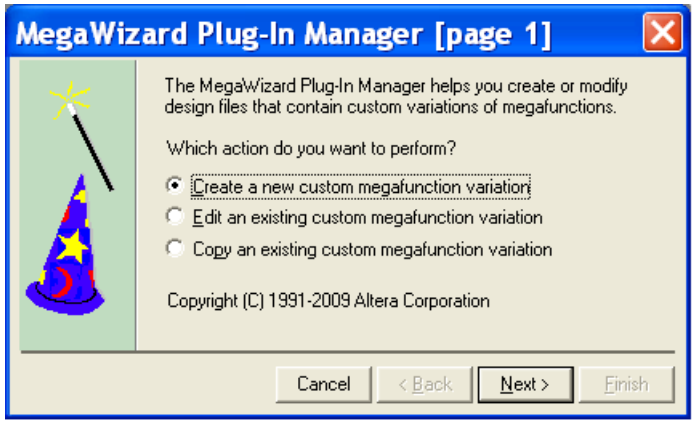


Figure 3–2 shows the second page of the MegaWizard Plug-In Manager. Select the following options (click **Next** when you are done):

1. In the list of megafunctions on the left, click the "+" icon beside the I/O item. From the options presented, choose **ALTGX_RECONFIG megafunction**.
2. From the drop-down menu beside **Which device family will you be using?**, select **Stratix IV**.
3. From the radio buttons under **Which type of output file do you want to create?**, choose your output file format (**AHDL**, **VHDL**, or **Verilog HDL**).
4. In the box beneath **What name do you want for the output file?**, enter the file name or click the **Browse** button to search for it.

☞ For the design to compile successfully, always enable the dynamic reconfiguration controller for all the ALTGX instances in the design.

Figure 3–2. MegaWizard Plug-In Manager—ALTGX_RECONFIG (Page 2)

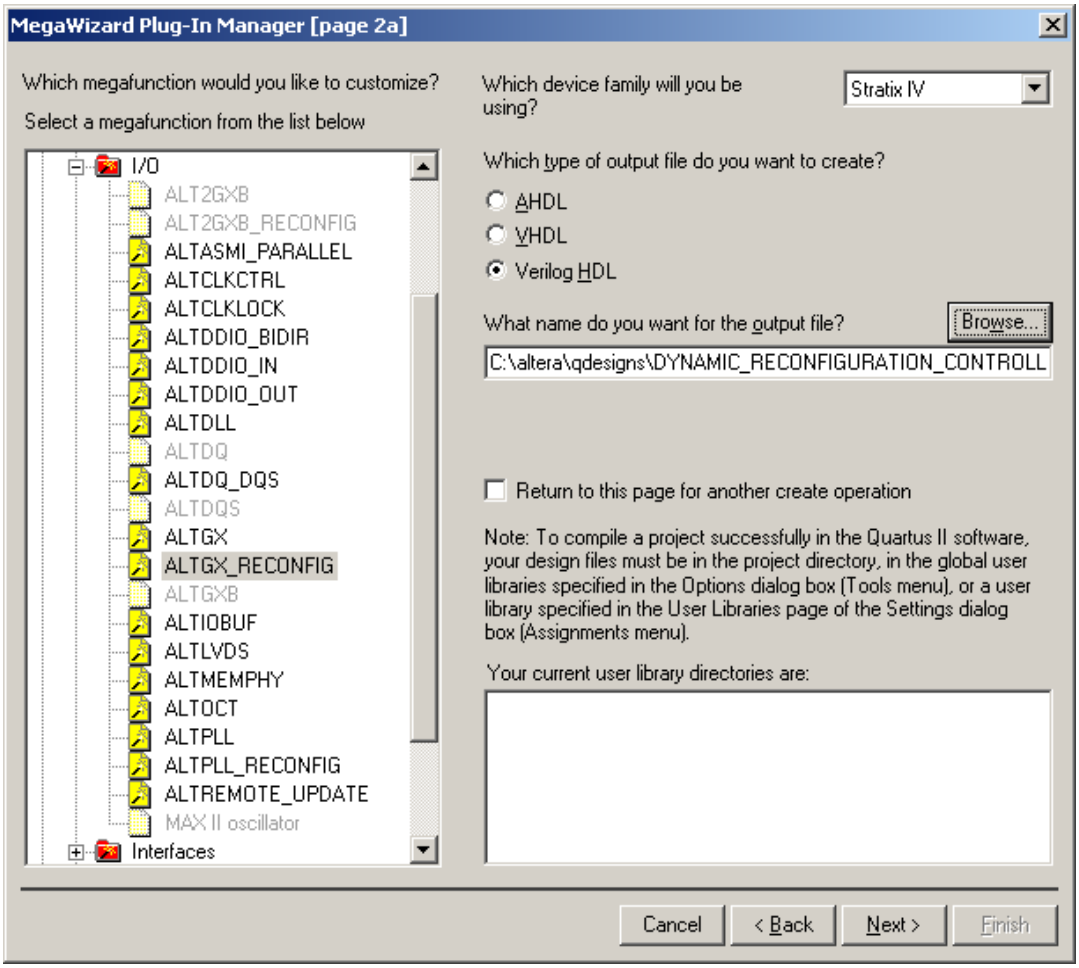


Figure 3–3 shows page 3 of the ALTGX_RECONFIG MegaWizard Plug-In Manager. From the drop-down menu, select the number of channels controlled by the dynamic reconfiguration controller.

Figure 3–3. MegaWizard Plug-In Manager—ALTGX_RECONFIG (Reconfiguration Settings)

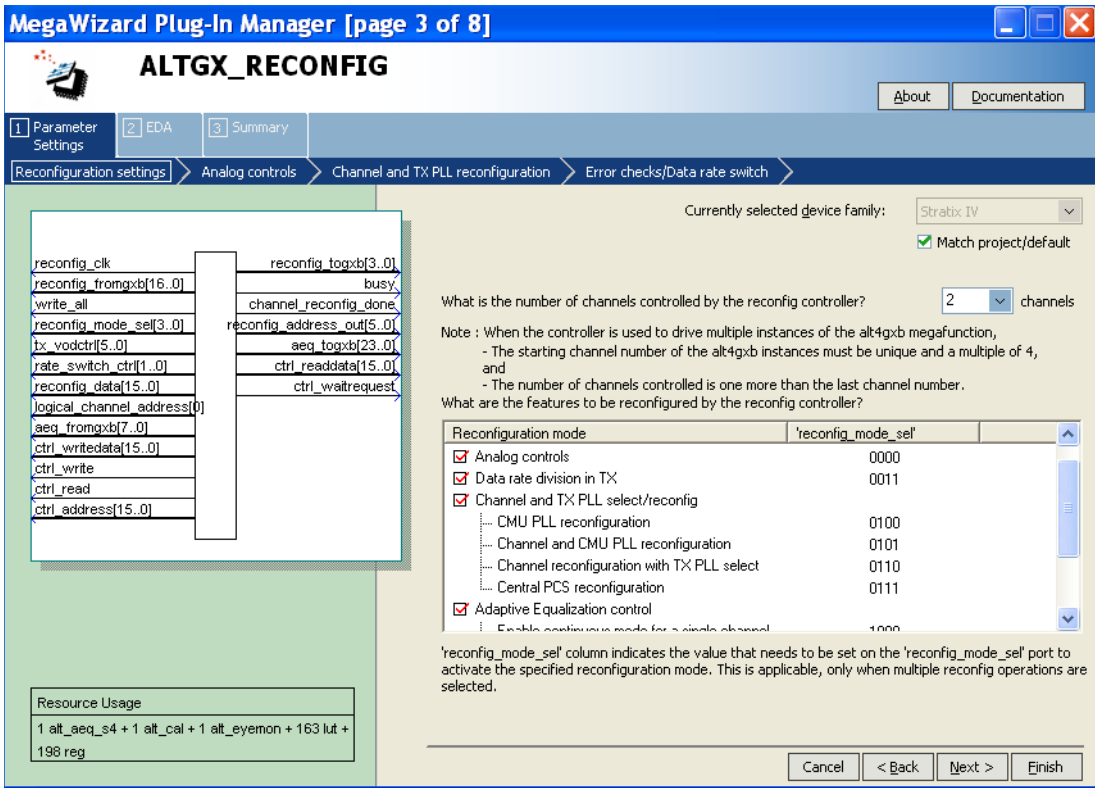


Table 3–1 lists the available options on page 3 of the MegaWizard Plug-In Manager for your ALTGX_RECONFIG custom megafunction variation. Select the **Match project/default** option if you want to change the device **Currently selected device family** options.

Make your selections on page 3, then click **Next**.

Table 3–1. MegaWizard Plug-In Manager Options (Page 3) (Part 1 of 2)

ALTGX_RECONFIG Setting	Description	Reference
What is the number of channels controlled by the reconfig controller?	Determine the highest logical channel address among all the ALTGX instances connected to the ALTGX_RECONFIG instance. Round it up to the next multiple of four and set that number in this option. Depending on this setting, the ALTGX_RECONFIG MegaWizard Plug-in Manager generates the appropriate signal width for the interface signal (`reconfig_fromgxb`) between the ALTGX_RECONFIG and the ALTGX instances. It also gives the necessary bus width for all the selected physical media attachment (PMA) signals. Depending on the number of channels set, the resource estimate changes because this is a soft implementation that uses fabric logic resources. The resource estimate is shown in the bottom left of Page 3 of the MegaWizard Plug-in Manager.	"Total Number of Channels Controlled by the ALTGX_RECONFIG Instance" section of the *Dynamic Reconfiguration in Stratix IV Devices* chapter.

Table 3–1. MegaWizard Plug-In Manager Options (Page 3) (Part 2 of 2)

ALTGX_RECONFIG Setting	Description	Reference
What are the features to be reconfigured by the reconfig controller?	This feature is always enabled by default: ■ **Offset Cancellation for Receiver Channels**—After the device powers up, the dynamic reconfiguration controller performs offset cancellation on the receiver portion of all the transceiver channels controlled by it.	The "Offset Cancellation" section of the *Dynamic Reconfiguration in Stratix IV Devices* chapter.
	These features are available for selection: ■ **Analog Controls**—Allows dynamic reconfiguration of PMA controls such as Equalization, Pre-emphasis, DC Gain, and voltage offset differential (VOD). ■ **Data rate division in TX**—Allows dynamic reconfiguration of the transmitter local divider settings to 1, 2, or 4. The transmitter channel data rate is reconfigured based on the local divider settings. ■ **Channel and TX PLL select/reconfig**—The following features are available under this option: ■ **CMU PLL Reconfiguration**—Allows you to dynamically reconfigure the clock multiplier unit (CMU) phase-locked loop (PLL) to a different data rate. ■ **Channel and CMU PLL reconfiguration**—Allows the dynamic reconfiguration of the transceiver channel from one functional mode to another and also the CMU PLL reconfiguration. ■ **Channel reconfiguration with TX PLL select**—Allows you to select additional transmitter PLLs for the transceiver channel and reconfigure the functional mode of the channel. ■ **Central Control Unit reconfiguration**—Allows you to reconfigure bonded mode configurations from one to another. ■ **Adaptive Equalization Control** —Allows you to reconfigure the adaptive equalization hardware (AEQ) in the receiver portion of the transceivers. **Enable one time mode for a single channel** mode is a single stable equalization value is set up and locked for the specified channel by the AEQ hardware.	The "PMA Controls Reconfiguration Mode Details" section, "Data Rate Division in Transmitter Mode Details" section, "CMU PLL Reconfiguration Mode Details'" section, "Channel and CMU PLL Reconfiguration Mode Details" section, "Channel reconfiguration with TX PLL Select Mode Details" section, and the "Adaptive Equalization (AEQ)" section in the *Dynamic Reconfiguration in Stratix IV Devices* chapter.
What are the features to be reconfigured by the reconfig controller?	■ **EyeQ control**—Allows you to reconfigure the EyeQ hardware in the receiver portion of the transceivers.	"EyeQ" section in the *Dynamic Reconfiguration in Stratix IV Devices* chapter.

Figure 3–4 shows page 4 of the ALTGX_RECONFIG MegaWizard Plug-In Manager.

Figure 3–4. MegaWizard Plug-In Manager—ALTGX_RECONFIG (Analog Controls)

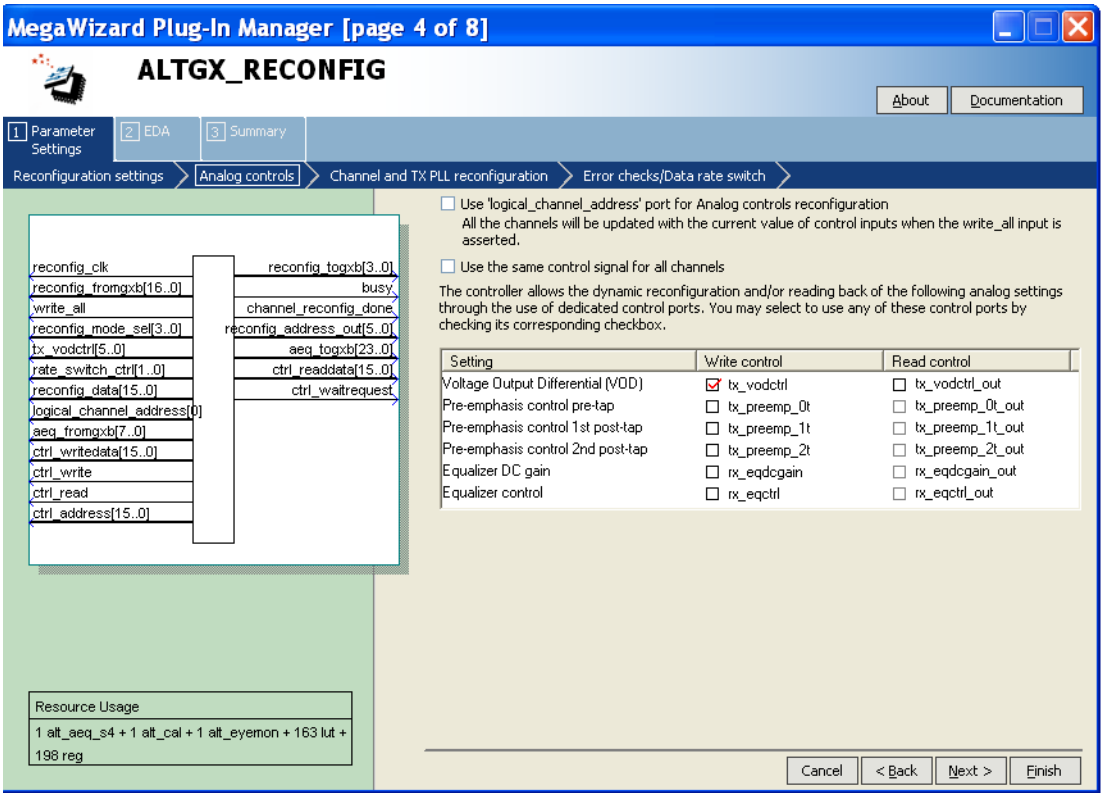


Table 3–2 lists the available options on page 4 of the MegaWizard Plug-In Manager for your ALTGX_RECONFIG custom megafunction variation.

Make your selections on page 4, then click **Next**.

Table 3–2. MegaWizard Plug-In Manager Options (Page 4) (Part 1 of 2)

ALTGX_RECONFIG Setting	Description	Reference
Use '`logical_channel_address`' port for Analog controls reconfiguration	This option is applicable only for Analog controls reconfiguration and is available for selection when the number of channels controlled by the ALTGX_RECONFIG instance is more than one. The dynamic reconfiguration controller reconfigures only the channel whose logical channel address is specified at the `logical_channel_address` port. The width of this port is selected by the ALTGX_RECONFIG MegaWizard Plug-In Manager depending on the number of channels controlled by the dynamic reconfiguration controller. The maximum width of the `logical_channel_address` port is 9 bits.	"Dynamic Reconfiguration Controller Port List" and "Method 1—Using the logical_channel_address Port" sections of the *Dynamic Reconfiguration in Stratix IV Devices* chapter.
Use the same control signal for all channels	This option is available for selection when the number of channels controlled by the ALTGX_RECONFIG instance is more than one. When you enable this option, the dynamic reconfiguration controller writes the same control signals to all the channels connected to it. You cannot select this option if you enable the **Use 'logical_channel_address' port for Analog controls reconfiguration** option.	Method 2 and Method 3 of the "PMA Controls Reconfiguration Mode Details" section of *Dynamic Reconfiguration in Stratix IV Devices* chapter.

Table 3–2. MegaWizard Plug-In Manager Options (Page 4) (Part 2 of 2)

ALTGX_RECONFIG Setting	Description	Reference
Write Control	The PMA control ports available to write various analog settings to the transceiver channels controlled by the dynamic reconfiguration controller are as follows: ■ `tx_vodctrl`—V_{OD}; 3 bits per channel ■ `tx_preemp_0t`—Pre-emphasis control pre-tap; 5 bits per channel ■ `tx_preemp_1t`—Pre-emphasis control 1st post-tap; 5 bits per channel ■ `tx_preemp_2t`—Pre-emphasis control 2nd post-tap; 5 bits per channel ■ `rx_eqdcgain`—Equalizer DC gain; 3 bits per channel ■ `rx_eqctrl`—Equalizer control; 4 bits per channel These are optional signals. The signal widths are based on the setting you entered for the **What is the number of channels controlled by the reconfig controller?** option and whether you enabled the **Use 'logical_channel_address' port for Analog controls reconfiguration** option. The port width is also determined by the **Use the same control signal for all channels** option. At least one of these PMA control ports must be enabled to configure and use the dynamic reconfiguration controller.	"Dynamically Reconfiguring PMA Controls" section of the *Dynamic Reconfiguration in Stratix IV Devices* chapter.
Read Control	The PMA control ports available to read the existing values from the transceiver channels controlled by the dynamic reconfiguration controller are as follows: ■ `tx_vodctrl_out`—V_{OD}; 3 bits per channel ■ `tx_preemp_0t_out`—Pre-emphasis control pre-tap; 5 bits per channel ■ `tx_preemp1t_out`—Pre-emphasis control 1st post-tap; 5 bits per channel ■ `tx_preemp_2t_out`—Pre-emphasis control 2nd post-tap; 5 bits per channel ■ `rx_eqdcgain_out`—Equalizer DC gain; 3 bits per channel ■ `rx_eqctrl_out`—Equalizer control; 4 bits per channel These are optional signals. The signal widths are based on the setting you entered for the **What is the number of channels controlled by the reconfig controller?** option and whether you enabled the **Use 'logical_channel_address' port for Analog controls reconfiguration** option. The PMA controls are available for selection only if you select the corresponding write control. Read and write transactions cannot be performed simultaneously.	

Figure 3–5 shows page 5 of the ALTGX_RECONFIG MegaWizard Plug-In Manager.

Figure 3–5. MegaWizard Plug-In Manager—ALTGX_RECONFIG (Channel and TX/PLL Reconfiguration)

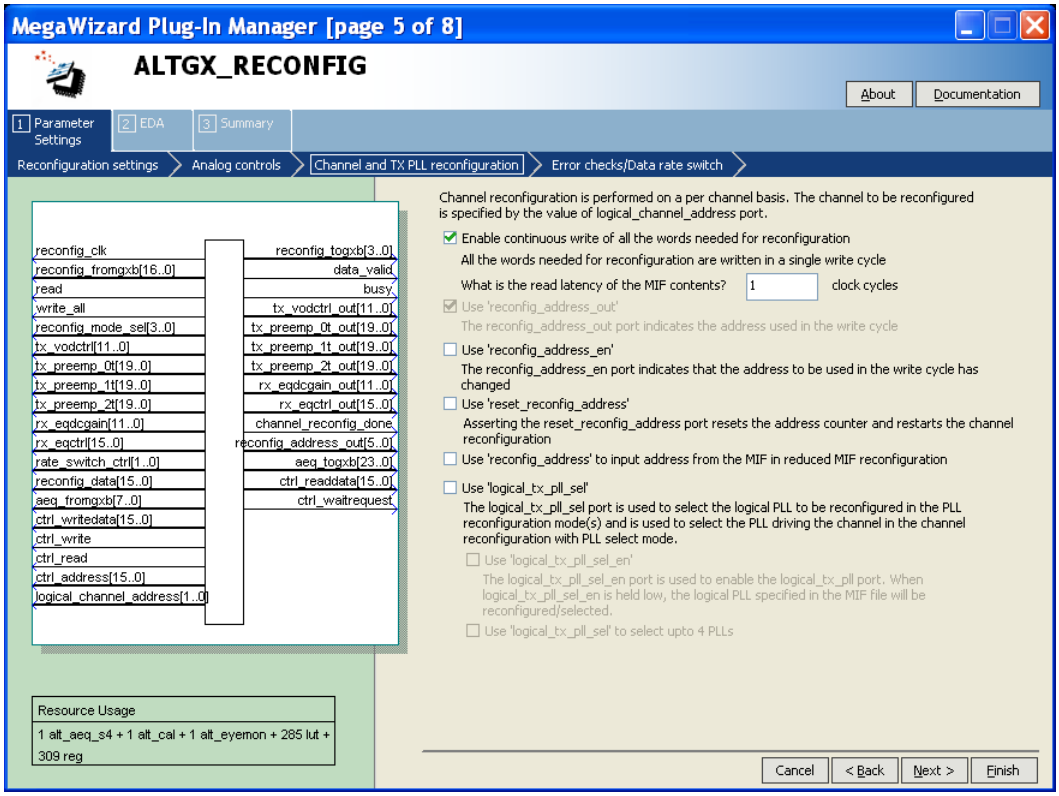


Table 3–4 lists the available options on page 5 of the MegaWizard Plug-In Manager for your ALTGX_RECONFIG custom megafunction variation.

Table 3–3. MegaWizard Plug-In Manager Options (Page 5) (Part 1 of 2)

ALTGX_RECONFIG Setting	Description	Reference
Enable continuous write of all the words needed for reconfiguration.	For a continuous write operation, select the **Enable continuous write of all the words needed for reconfiguration** option to pulse the `write_all signal` once to write an entire memory initialization file (**.mif**).	"Dynamic Reconfiguration Controller Port List" section in the *Dynamic Reconfiguration in Stratix IV Devices* chapter.
What is the read latency of the MIF contents?	This option is available only if you have selected the **Enable continuous write of all the words needed for reconfiguration** option. Enter the desired latency in terms of the `reconfig_clk` cycles it takes for each **.mif** word to be present at the `reconfig_data` port. For more information, refer to Figure 3–6.	"Dynamic Reconfiguration Controller Port List" section in the *Dynamic Reconfiguration in Stratix IV Devices* chapter.

Table 3–3. MegaWizard Plug-In Manager Options (Page 5) (Part 2 of 2)

ALTGX_RECONFIG Setting	Description	Reference
Use 'reconfig_address_out'	This option is enabled by default when you select the **Channel and TX PLL select/reconfig** option. The value on `reconfig_address_out[5:0]` indicates the address associated with the words in the **.mif**, which contains the dynamic reconfiguration instructions. The dynamic reconfiguration controller automatically increments the address at the end of each **.mif** write transaction.	"Dynamic Reconfiguration Controller Port List" section in the *Dynamic Reconfiguration in Stratix IV Devices* chapter.
Use 'reconfig_address_en'	When high, this optional output status signal indicates that the address used in the **.mif** write transaction cycle has changed. This signal is asserted when the **.mif** write transaction is completed (when the `busy` signal is de-asserted).	"Dynamic Reconfiguration Controller Port List" section in the *Dynamic Reconfiguration in Stratix IV Devices* chapter.
Use 'reset_reconfig_address'	When asserted, this optional control signal resets `reconfig_address_out` (the current reconfiguration address) to **0**.	"Dynamic Reconfiguration Controller Port List" section in the *Dynamic Reconfiguration in Stratix IV Devices* chapter.
Use 'logical_tx_pll_sel'	This is an optional control signal. The `logical_tx_pll_sel[1:0]` signal refers to the logical reference index of the CMU PLL. The functionality of the signal depends on the feature activated, as shown below: ■ **CMU PLL reconfiguration**—The corresponding CMU PLL is reconfigured based on the value at `logical_tx_pll_sel[1:0]`. ■ **Channel and CMU PLL reconfiguration**—The corresponding CMU PLL is reconfigured based on the value at this signal. The transceiver channel listens to the CMU PLL selected by `logical_tx_pll_sel[1:0]`. ■ **Channel reconfiguration with TX PLL select**—The transceiver channel listens to the TX PLL selected by `logical_tx_pll_sel[1:0]`.	"Guidelines for logical_tx_pll_sel and logical_tx_pll_sel_en Ports" section in the *Dynamic Reconfiguration in Stratix IV Devices* chapter.
Use 'logical_tx_pll_sel_en'	This is an optional control signal. When you enable this signal, the value set on the `logical_tx_pll_sel[1:0]` signal is valid only if the `logical_tx_pll_sel_en` is set to **1**.	"Guidelines for logical_tx_pll_sel and logical_tx_pll_sel_en Ports" section in the *Dynamic Reconfiguration in Stratix IV Devices* chapter.

Figure 3–6 shows that the read latency of the **.mif** contents is 2, as it takes two `reconfig_clk` cycles for the **.mif** data to become available on the `reconfig_data` port after providing address on the `reconfig_address_out` port.

Figure 3–6. Read Latency

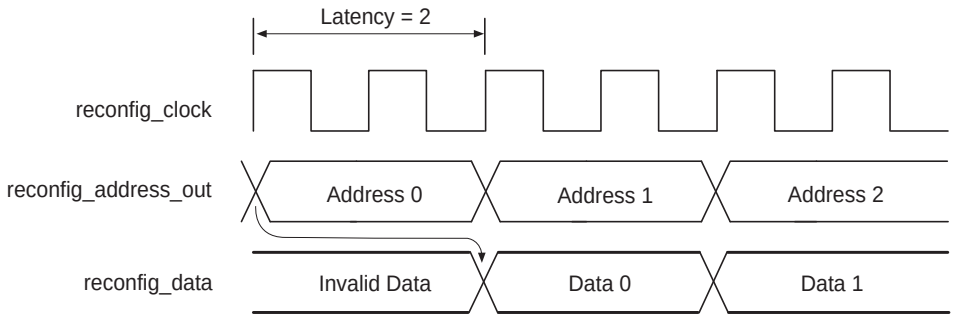


Figure 3–7 shows page 6 of the ALTGX_RECONFIG MegaWizard Plug-In Manager.

Figure 3–7. MegaWizard Plug-In Manager—ALTGX_RECONFIG (Error Checks/Data Rate Switch)

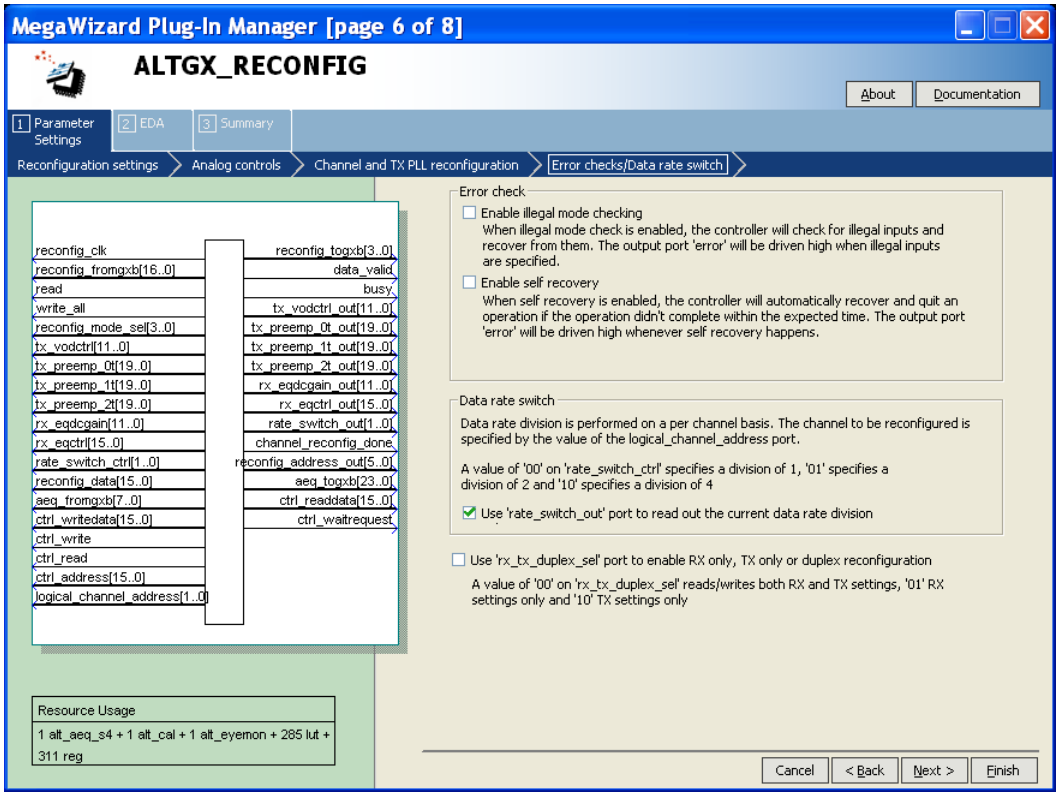


Table 3–4 lists the available options on page 6 of the MegaWizard Plug-In Manager for your ALTGX_RECONFIG custom megafunction variation.

Make your selections on page 6, then click **Next**.

Table 3–4. MegaWizard Plug-In Manager Options (Page 6)

ALTGX_RECONFIG Setting	Description	Reference
Enable illegal mode checking	When you select this option, the ALTGX_RECONFIG MegaWizard Plug-In Manager provides the `error` output port. The dynamic reconfiguration controller detects the error conditions within two `reconfig_clk cycles`, de-asserts the busy signal, and asserts the error signal for two `reconfig_clk cycles`.	The "Error Indication During Dynamic Reconfiguration" section of the *Dynamic Reconfiguration in Stratix IV Devices* chapter.
Enable self recovery	When you select this option, the controller automatically recovers if the operation did not complete within the expected time. The error signal is driven high whenever the controller performs a self recovery.	The "Error Indication During Dynamic Reconfiguration" section of the *Dynamic Reconfiguration in Stratix IV Devices* chapter.
Use `rate_switch_out` port to read out the current data rate division	The `rate_switch_out[1:0]` signal is available when you select **Data Rate Division in TX** mode. You can read the existing local divider settings of a transmitter channel at this port. The decoding for this signal is listed below: 2'b00—Division of 1 2'b01—Division of 2 2'b10—Division of 4 2'b11—Not supported	The "Data Rate Division in Transmitter Mode Details" mode section in the *Dynamic Reconfiguration in Stratix IV Devices* chapter.
Use the `rx_tx_duplex_sel` port to enable RX only, TX only or duplex configuration	You can read or write the receiver and transmitter settings, only the receiver settings, or only the transmitter settings, based on the value you set at the `rx_tx_duplex_sel[1:0]` port; ■ 2'b00—Duplex mode ■ 2'b01—RX only mode ■ 2'b10—TX only mode ■ 2'b11—unsupported value (do not use this value) If you disable the `rx_tx_duplex_sel[1:0]` port, the dynamic reconfiguration controller reads or writes both the receiver and transmitter settings.	"Dynamically Reconfiguring PMA Controls" section of the *Dynamic Reconfiguration in Stratix IV Devices* chapter.

Figure 3–8 shows page 7 (the Simulation Libraries page) of the MegaWizard Plug-In Manager, which is used for dynamic reconfiguration selection.

Make your selections, then click **Next**.

Figure 3–8. MegaWizard Plug-In Manager—ALTGX_RECONFIG (Simulation Libraries)

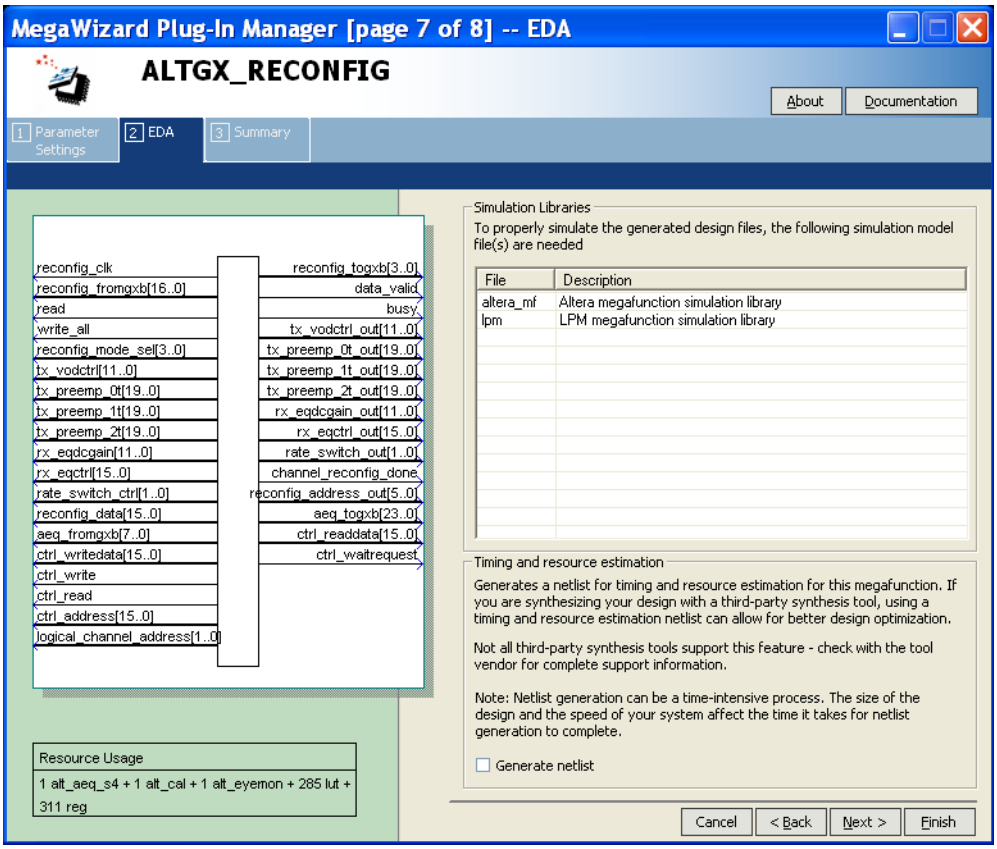


Table 3–5 lists the available option on page 7 of the MegaWizard Plug-In Manager for your ALTGX_RECONFIG custom Megafunction variation.

Make your selections on page 7, then click **Next**.

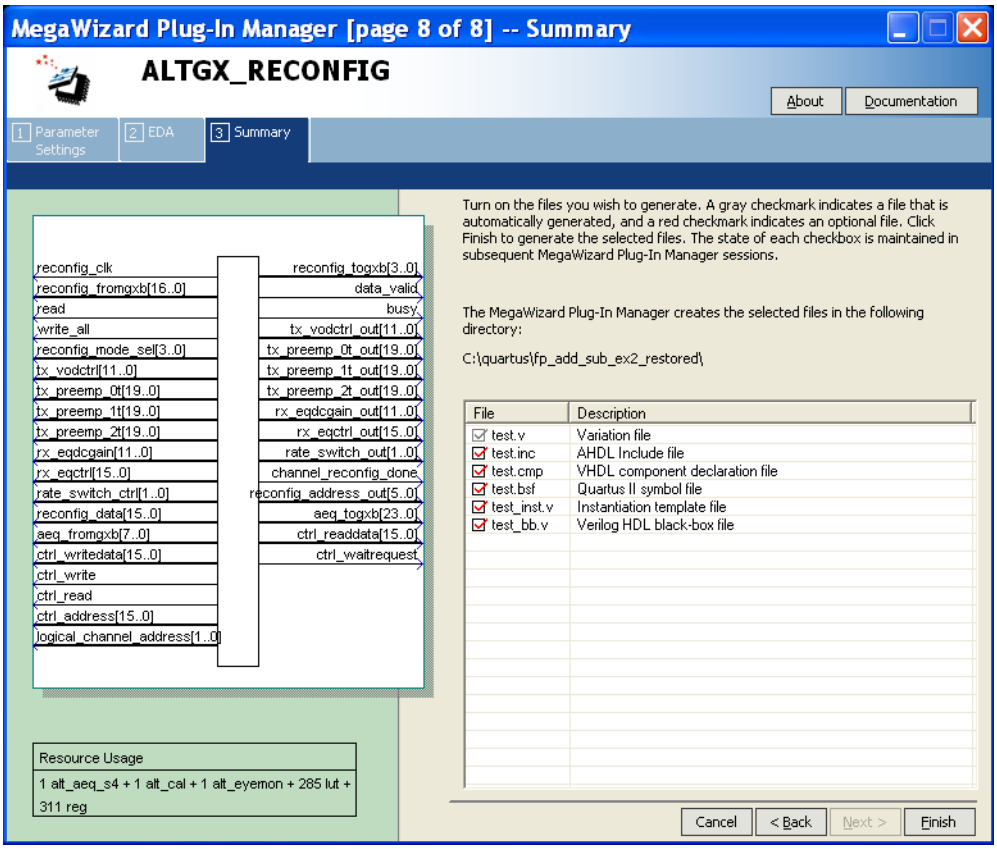
Table 3–5. MegaWizard Plug-In Manager Options (Page 7)

ALTGX_RECONFIG Setting	Description	Reference
Generate a netlist for synthesis area and timing estimation	Selecting this option generates a netlist file that third-party synthesis tools can use to estimate the timing and resource usage.	—

Figure 3–9 shows page 8 (the last page) of the MegaWizard Plug-In Manager for the dynamic reconfiguration protocol set up. You can select optional files on this page.

After you make your selections, click **Finish** to generate the files.

Figure 3–9. MegaWizard Plug-In Manager—ALTGX_RECONFIG (Summary)



Document Revision History

Table 3–6 lists the revision history for this chapter.

Table 3–6. Document Revision History (Part 1 of 2)

Date	Version	Changes
February 2011	3.1	■ Updated Table 3–1. ■ Applied new template. ■ Updated chapter title. ■ Minor text edits.
November 2009	3.0	■ Updated Table 3–1. ■ Updated Table 3–3. ■ Added Figure 3–6. ■ Made minor text edits.

Table 3–6. Document Revision History (Part 2 of 2)

Date	Version	Changes
June 2009	2.1	■ Updated Table 3–3. ■ Added introductory sentences to improve search ability. ■ Minor text edits.
March 2009	2.0	Updated screen shots.
November 2008	1.0	Added chapter to the Stratix IV Device Handbook

This chapter provides additional information about the document and Altera.

How to Contact Altera

To locate the most up-to-date information about Altera products, refer to the following table.

Contact	Contact Method	Address
Technical support	Website	www.altera.com/support
Technical training	Website	www.altera.com/training
	Email	custrain@altera.com
Product literature	Website	www.altera.com/literature
Nontechnical support (general)	Email	nacomp@altera.com
(software licensing)	Email	authorization@altera.com

Note to Table:

(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

The following table shows the typographic conventions this document uses.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Indicate command names, dialog box titles, dialog box options, and other GUI labels. For example, **Save As** dialog box. For GUI elements, capitalization matches the GUI.
bold type	Indicates directory names, project names, disk drive names, file names, file name extensions, software utility names, and GUI labels. For example, **\qdesigns** directory, **D:** drive, and **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Indicate document titles. For example, *Stratix IV Design Guidelines*.
italic type	Indicates variables. For example, *n* + 1. Variable names are enclosed in angle brackets (< >). For example, *<file name>* and *<project name>***.pof** file.
Initial Capital Letters	Indicate keyboard keys and menu names. For example, the Delete key and the Options menu.
"Subheading Title"	Quotation marks indicate references to sections in a document and titles of Quartus II Help topics. For example, "Typographic Conventions."

Visual Cue	Meaning
`Courier type`	Indicates signal, port, register, bit, block, and primitive names. For example, `data1`, `tdi`, and `input`. The suffix n denotes an active-low signal. For example, `resetn`. Indicates command line commands and anything that must be typed exactly as it appears. For example, `c:\qdesigns\tutorial\chiptrip.gdf`. Also indicates sections of an actual file, such as a Report File, references to parts of files (for example, the AHDL keyword `SUBDESIGN`), and logic function names (for example, `TRI`).
↵	An angled arrow instructs you to press the Enter key.
1., 2., 3., and a., b., c., and so on	Numbered steps indicate a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ■ ■	Bullets indicate a list of items when the sequence of the items is not important.
	The hand points to information that requires special attention.
	The question mark directs you to a software help system with related information.
	The feet direct you to another document or website with related information.
	The multimedia icon directs you to a related multimedia presentation.
	A caution calls attention to a condition or possible situation that can damage or destroy the product or your work.
	A warning calls attention to a condition or possible situation that can cause you injury.
	The envelope links to the Email Subscription Management Center page of the Altera website, where you can sign up to receive update notifications for Altera documents.