16. Understanding Timing in MAX II Devices

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Introduction

Altera® devices provide predictable device performance that is consistent from simulation to application. Before programming a device, you can determine the worst-case timing delays for any design. You can approximate propagation delays with either the Quartus® II Timing Analyzer or the timing models given in this chapter and the timing parameters listed in individual device data sheets.

For the most precise timing results, you should use the Quartus II Timing Analyzer, which accounts for the effects of the secondary factors as mentioned later in this chapter.

This chapter defines external and internal timing parameters, and illustrates the timing models for the MAX® II device family.

Familiarity with device architecture and characteristics is assumed. Refer to specific device or device family data sheets in this handbook for a complete description of the architecture, and for the specific values of the timing parameters listed in this chapter.

This chapter contains the following sections:

External Timing Parameters

External timing parameters represent actual pin-to-pin timing characteristics. Each external timing parameter consists of a combination of internal timing parameters. You can find the values of the external timing parameters in the *DC and Switching Characteristics* chapter in the *MAX II Device Handbook*. These external timing parameters are worst-case values, derived from extensive performance measurements and ensured by testing. All external timing parameters are shown in bold type. Table 16–1 defines external timing parameters for the MAX II family.

Table 16–1. External Timing Parameters

Parameter	Description
t_{PD1}	Pin-to-pin delay for the worst case I/O placement with full a diagonal path across the device with combinational logic implemented in a single look-up table (LUT) in a logic array block (LAB) adjacent to output pin. Fast I/O Connection is used from the adjacent logic element (LE) to the output pin.
t_{PD2}	Pin-to-pin delay for the best case I/O placement with combinational logic (2-input AND gate) implemented in a single edge LE adjacent to the input pin. The longest pin path of the two inputs is shown. Fast I/O Connection is used from the adjacent LE to the output pin.
t_{CLR}	Time to clear register delay. The time required for a low signal to appear at the external output, measured from the input transition.
t_{SU}	Global clock setup time. The time that data must be present at the input pin before the global (synchronous) clock signal is asserted at the clock pin.
t_{H}	Global clock hold time. The time that data must be present at the input pin after the global clock signal is asserted at the clock pin.
t_{CO}	Global clock to output delay. The time required to obtain a valid output after the global clock is asserted at the clock pin.
t_{CNT}	Minimum global clock period. The minimum period maintained by a globally clocked counter.

Internal Timing Parameters

Within a device, the timing delays contributed by individual architectural elements are called internal timing parameters, which cannot be measured explicitly. All internal parameters are shown in italic type. Table 16–2 defines the internal timing microparameters for the MAX II device family.

Table 16–2. Internal Timing Microparameters (Part 1 of 2)

Parameter	Description
t_{LUT}	LE combinational LUT delay for data-in to data-out.
t_{COMB}	Combinational path delay. The delay from the time when a combinational logic signal from the LUT bypasses the LE register to the time it becomes available at the LE output.
t_{CLR}	LE register clear delay. The delay from the assertion of the register's asynchronous clear input to the time the register output stabilizes at logical low.
t_{PRE}	LE register preset delay. The delay from the assertion of the register's asynchronous preset input to the time the register output stabilizes at logical high.
t_{SU}	LE register setup time before clock. The time required for a signal to be stable at the register's data and enable inputs before the register clock rising edge to ensure that the register correctly stores the input data.
t_{H}	LE register hold time after clock. The time required for a signal to be stable at the register's data and enable inputs after the register clock's rising edge to ensure that the register correctly stores the input data.
t_{CO}	LE register clock-to-output delay. The delay from the rising edge of the register's clock to the time the data appears at the register output.
t_{C}	Register control delay. The time required for a signal to be routed to the clock, preset, or clear input of an LE register.
t_{FASTIO}	Combinational output delay. t_{FASTIO} is the time required for a combinational signal from the LE adjacent to the I/O block using the fast I/O connection.
t_{IN}	I/O input pad and buffer delay. The t_{IN} applies to I/O pins used as inputs.
t_{GLOB}	t_{GLOB} applies to GCLK pins when used for global signals. t_{GLOB} is the delay required for a global signal to be routed from the GCLK pins to the LAB column clocks through the global clock network.

Table 16–2. Internal Timing Microparameters (Part 2 of 2)

Parameter	Description
t_{IOE}	Internal generated output enable delay. The delay from an internally generated signal on the interconnect to the output enable of the tri-state buffer.
t_{DL}	Input routing delay. The delay incurred from the row I/O pin used as input to the LE adjacent to it.
t_{IODR}	Output data delay for the row interconnect. The delay incurred by signals routed from an interconnect to an I/O cell.
t_{OD}	Output delay buffer and pad delay. Refer to *Timing Model and Specifications* section in the *DC and Switching Characteristics* chapter in the *MAX II Device Handbook* for delay adders associated with different I/O standards, drive strengths, and slew rates.
t_{XZ}	Output buffer disable delay. The delay required for high impedance to appear at the output pin after the output buffer's enable control is disabled. Refer to *Timing Model and Specifications* section in the *DC and Switching Characteristics* chapter in the *MAX II Device Handbook* for delay adders associated with different I/O standards, drive strengths, and slew rates.
t_{ZX}	Output buffer enable delay required for the output signal to appear at the output pin after the tri-state buffer's enable control is enabled. Refer to *Timing Model and Specifications* section in the *DC and Switching Characteristics* chapter in the *MAX II Device Handbook* for delay adders associated with different I/O standards, drive strengths, and slew rates.
t_{C4}	Delay for a column interconnect with average loading. The t_{C4} covers a distance of four LAB rows.
t_{R4}	Delay for a row interconnect with average loading. The t_{R4} covers a distance of four LAB columns.
t_{LOCAL}	Local interconnect delay.

Internal Timing Parameters for MAX II UFM

Timing parameters for MAX II user flash memory (UFM) are the timing delays contributed by the UFM architectural elements, which cannot be measured explicitly. All timing parameters are shown in italic type. Table 16–3 defines the timing microparameters for MAX II UFM.

Table 16–3. Internal Timing Microparameters for MAX II UFM (Part 1 of 2)

Parameter	Description
t_{ASU}	Address register shift signal setup to address register clock.
t_{AH}	Address register shift signal hold from address register clock.
t_{ADS}	Address register data in setup to address register clock.
t_{ADH}	Address register data in hold from address register clock.
t_{DSS}	Data register shift signal setup to data register clock.
t_{DSH}	Data register shift signal hold from data register clock.
t_{DDS}	Data register data in setup to data register clock.
t_{DDH}	Data register data in hold from data register clock.
t_{DCO}	Delay incurred from the data register clock to data register output when shifting the data out.
t_{DP}	`PROGRAM` signal to data clock hold time.
t_{PB}	Maximum delay between `PROGRAM` rising edge to UFM `BUSY` signal rising edge.
t_{BP}	Minimum delay allowed from UFM `BUSY` signal going low to `PROGRAM` signal going low.
t_{PPMX}	Maximum length of busy pulse during a program.
t_{AE}	Minimum `ERASE` signal to address clock hold time.

Table 16–3. Internal Timing Microparameters for MAX II UFM (Part 2 of 2)

Parameter	Description
t_{EB}	Maximum delay between ERASE rising edge to UFM BUSY signal rising edge.
t_{BE}	Minimum delay allowed from UFM BUSY signal going low to ERASE signal going low.
t_{EPMX}	Maximum length of busy pulse during an erase.
t_{RA}	Maximum read access time. The delay incurred between the DRSHFT signal going low to the first bit of data observed at the data register output.
t_{OE}	Delay from OSC_ENA signal reaching UFM to rising clock of OSC leaving the UFM.
t_{OSCS}	Maximum delay between the OSC_ENA rising edge to the ERASE/PROGRAM signal rising edge.
t_{OSCH}	Minimum delay allowed from the ERASE/PROGRAM signal going low to the OSC_ENA signal going low.

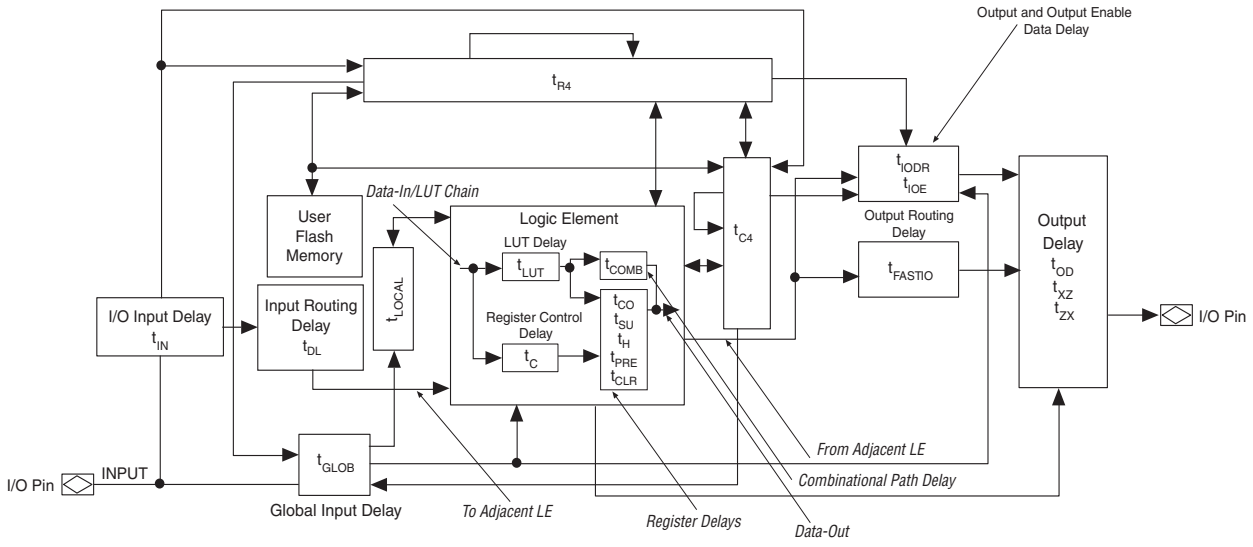
Timing Models

Timing models are simplified block diagrams that illustrate the delays through Altera devices. Logic can be implemented on different paths. You can trace the actual paths used in your design by examining the equations listed in the Quartus II Report File (**.rpt**) for the project. You can then add up the appropriate internal timing parameters to estimate the delays through the device.

The MAX II architecture has a globally routed clock. The MultiTrack interconnect ensures predictable performance, accurate simulation, and accurate timing analysis across all MAX II device densities and speed grades.

Figure 16–1 shows the timing model for MAX II devices. The timing model is the preliminary version which is subject to change. The final version of the timing model will be released once available.

Figure 16–1. MAX II Device Timing Model

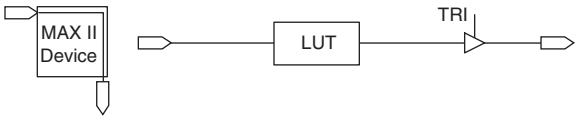


Calculating Timing Delays

You can calculate approximate pin-to-pin timing delays for MAX II devices with the timing model shown in Figure 16–1 and by referring to the *DC and Switching Characteristics* chapter in the *MAX II Device Handbook*. Each external timing parameter is calculated from a combination of internal timing parameters. Figure 16–2 through Figure 16–6 show the external timing parameters for the MAX II device family. To calculate the delay for a signal that follows a different path through the MAX II device, refer to the timing model to determine which internal timing parameters to add together.

For the most precise timing results, use the Quartus II Timing Analyzer, which accounts for the effects of secondary factors such as placement and fan-out.

Figure 16–2. External Timing Parameter (t_{PD1}) *Note (1)*



Note to Figure 16–2:

(1) $t_{PD1} = t_{IN} + N \times t_{R4}/4 + M \times t_{C4}/4 + t_{LUT} + t_{COMB} + t_{FASTIO} + (t_{OD} + \Delta t_{OD})$

Table 16–4 lists the numbers of LABs according to device density.

Table 16–4. Numbers of LABs According to Device Density

Device Density	N LAB Rows	M LAB Columns
EPM240	4	6
EPM570	7	12
EPM1270	10	16
EPM2210	13	20

Dt_{OD} is the adder delay (see note to Figure 16–2) for the t_{OD} microparameter when using an I/O standard other than 3.3-V LVTTL with 16 mA current strength.

Refer to the *DC and Switching Characteristics* chapter in the *MAX II Device Handbook* for adder delay values.

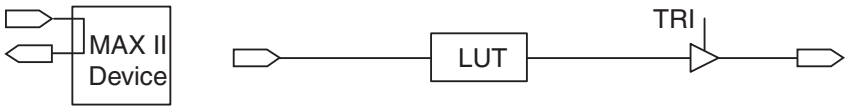
The following is an example:

t_{PD1} for the EPM240 device using an I/O standard of 3.3-V LVTTL fast slew rate with a drive strength of 16 mA:

$t_{PD1} = t_{IN} + 4 \times t_{R4}/4 + 6 \times t_{C4}/4 + t_{LUT} + t_{COMB} + t_{FASTIO} + t_{OD}$……(a)

t_{PD1} for the EPM240 device using an I/O standard of 2.5-V LVTTL fast slew rate with a drive strength of 7 mA: t_{PD1} = (a) + (Dt_{OD} of 2.5-V LVTTL fast slew 7 mA)

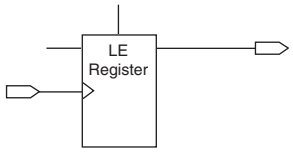
Figure 16–3. External Timing Parameter (t_{PD2}) *Note (1)*



Note to Figure 16–3:

(1) $t_{PD2} = t_{IN} + t_{DL} + t_{LUT} + t_{COMB} + t_{FASTIO} + (t_{OD} + \Delta t_{OD})$

Figure 16–4. External Timing Parameter (t_{CO}) *Note (1), (2)*

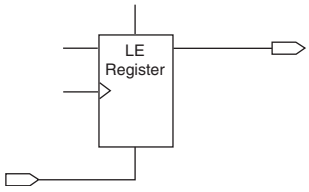


Notes to Figure 16–4:

(1) $t_{CO} = t_{GLOB} + t_C + t_{CO} + (N \times t_{R4}/4 + M \times t_{C4}/4) + (t_{IODC} \text{ or } t_{IODR}) + (t_{OD} + \Delta t_{OD})$

(2) The constants N and M are subject to change according to the position of the LAB in the entire device.

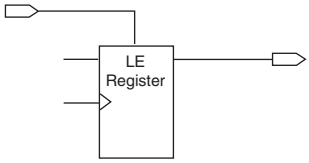
Figure 16–5. LE Register Clear and Preset Time (t_{CLR}) *Note (1)*



Note to Figure 16–5:

(1) $t_{CLR} = t_{GLOB} + t_C + t_{CLR} + (N \times t_{R4}/4 + M \times t_{C4}/4) + (t_{IODC} \text{ or } t_{IODR}) + (t_{OD} + \Delta t_{OD})$

Figure 16–6. LE Register Clear and Preset Time (t_{PRE}) *Note (1)*



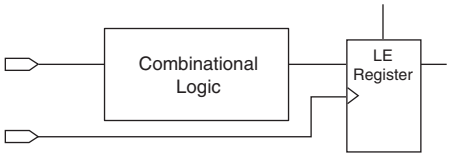
Note to Figure 16–6:

(1) $t_{PRE} = t_{GLOB} + t_{LOCAL} + t_C + t_{PRE} + (N \times t_{R4}/4 + M \times t_{C4}/4) + (t_{IODC} \text{ or } t_{IODR}) + (t_{OD} + \Delta t_{OD})$

Setup and Hold Time from an I/O Data and Clock Input

The Quartus II software might insert additional routing delays from the input pin to the register input to ensure a zero hold time for the LE register. Altera recommends that you use the Quartus II Timing Analyzer to obtain the setup time and hold time. See Figure 16–7 and Figure 16–8.

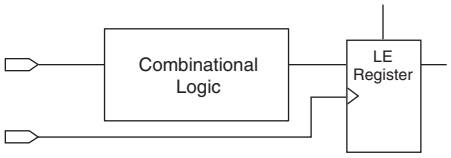
Figure 16–7. Setup and Hold Time (t_{SU}) *Note (1)*



Note to Figure 16–7:

(1) $t_{SU} = (t_{IN} + N \times t_{R4}/4 + M \times t_{C4}/4 + t_{LUT}) - (t_{GLOB} + t_C) + t_{SU}$

Figure 16–8. Setup and Hold Time (t_H) *Note (1)*



Note to Figure 16–8:

(1) $t_H = (t_{GLOB} + t_C) - (t_{IN} + N \times t_{R4}/4 + M \times t_{C4}/4 + t_{LUT}) + t_H$

For Figure 16–4 through Figure 16–8, the constants N and M are subject to change according to the position of LAB in the entire device for combinational logic implementation.

Programmable Input Delay

The programmable input delay provides an option to add a delay to the input pin, guaranteeing a zero hold time. You can set this option in the Assignment Editor (Assignments menu) on a pin-by-pin basis. The following procedure shows how to turn on the input delay for the selected input pin in the Quartus II software:

1. Select input pin name in the design file.
2. Right-click and select **Locate** in the Assignment Editor.
3. Double-click the cell under Assignment Name and select **Input Delay from Pin to Internal Cells** in the pull-down list.
4. Double-click the **Value** cell to the right of the assignment name just made and enter 1.
5. On the File menu, click **Save**.

Timing Model versus Quartus II Timing Analyzer

Hand calculations based on the timing model provide a good estimate of a design's performance. However, the Quartus II Timing Analyzer always provides the most accurate information on design performance because it takes into account secondary factors that influence the routing microparameters such as:

- Fan-out for each signal in the delay path
- Positions of other loads relative to the signal source and destination

- Distance between the signal source and destination
- Various interconnect lengths where some interconnects are truncated at the edge of the device

Conclusion

The MAX II device architecture has predictable internal timing delays that can be estimated based on signal synthesis and placement. The Quartus II Timing Analyzer provides the most accurate timing information. However, you can use the timing model along with the timing parameters listed in the *DC and Switching Characteristics* chapter in the *MAX II Device Handbook* to estimate a design's performance before compilation. Both methods enable you to accurately predict your design's in-system timing performance.

Referenced Documents

This chapter references the following document:

- *DC and Switching Characteristics* chapter in the *MAX II Device Handbook*

Document Revision History

Table 16–5 shows the revision history for this chapter.

Table 16–5. Document Revision History

Date and Revision	Changes Made	Summary of Changes
October 2008, version 2.1	■ Updated New Document Format.	—
December 2007, version 2.0	■ Updated t_{PD2} information in Table 16–1. ■ Added t_{COMB} information in Table 16–2. ■ Updated Figure 16–1. ■ Updated *Note (1)* to Figure 16–2. ■ Updated "Calculating Timing Delays" section. ■ Added "Referenced Documents" section.	—
December 2006, version 1.4	■ Added document revision history.	—
January 2005, version 1.3	■ Previously published as Chapter 17. No changes to content.	—
December 2004, version 1.2	■ Added section Programmable Input Delay.	—
June 2004, version 1.1	■ Updated Table 16–1. Various parameter naming updates.	—