6. I/O Features in Stratix IV Devices

SIV51006-3.4

This chapter describes how Stratix® IV devices provide I/O capabilities that allow you to work in compliance with current and emerging I/O standards and requirements. With these device features, you can reduce board design interface costs and increase development flexibility.

Altera® Stratix IV FPGAs deliver a breakthrough level of system bandwidth and power efficiency for high-end applications, allowing you to innovate without compromise. Stratix IV I/Os are specifically designed for ease-of-use and rapid system integration while simultaneously providing the high bandwidth required to maximize internal logic capabilities and produce system-level performance.

Stratix IV device I/O capability far exceeds the I/O bandwidth available from previous generation FPGAs. Independent modular I/O banks with a common bank structure for vertical migration lend efficiency and flexibility to the high-speed I/O.

Package and die enhancements with dynamic termination and output control provide best-in-class signal integrity. Numerous I/O features assist high-speed data transfer into and out of the device, including:

- Up to 32 full-duplex clock data recovery (CDR)-based transceivers supporting data rates between 600 Mbps and 8.5 Gbps
- Dedicated circuitry to support physical layer functionality for popular serial protocols, such as PCI Express® (PIPE) (PCIe) Gen1 and Gen2, Gigabit Ethernet (GbE), Serial RapidIO®, SONET/SDH, XAUI/HiGig, (OIF) CEI-6G, SD/HD/3G-SDI, Fibre Channel, SFI-5, and Interlaken
- Complete PCIe protocol solution with embedded PCIe hard IP blocks that implement PHY-MAC layer, data link layer, and transaction layer functionality
- Single-ended, non-voltage-referenced, and voltage-referenced I/O standards
- Low-voltage differential signaling (LVDS), reduced swing differential signaling (RSDS), mini-LVDS, high-speed transceiver logic (HSTL), and SSTL
- Single data rate (SDR) and half data rate (HDR—half frequency and twice data width of SDR) input and output options
- Up to 132 full duplex 1.6 Gbps true LVDS channels (132 Tx + 132 Rx) on the row I/O banks
- Hard dynamic phase alignment (DPA) block with serializer/deserializer (SERDES)
- Deskew, read and write leveling, and clock-domain crossing functionality
- Programmable output current strength
- Programmable slew rate

- Programmable delay
- Programmable bus-hold circuit
- Programmable pull-up resistor
- Open-drain output
- Serial, parallel, and dynamic on-chip termination (OCT)
- Differential OCT
- Programmable pre-emphasis
- Programmable equalization
- Programmable differential output voltage (V_{OD})

This chapter contains the following sections:

I/O Standards Support

Stratix IV devices support a wide range of industry I/O standards. Table 6–1 lists the I/O standards Stratix IV devices support, as well as the typical applications. These devices support V_{CCIO} voltage levels of 3.0, 2.5, 1.8, 1.5, and 1.2 V.

Table 6–1. I/O Standards and Applications for Stratix IV Devices (Part 1 of 2)

I/O Standard	Application
3.3-V LVTTL/LVCMOS (1), (2)	General purpose
2.5-V LVCMOS	General purpose
1.8-V LVCMOS	General purpose
1.5-V LVCMOS	General purpose
1.2-V LVCMOS	General purpose
3.0-V PCI/PCI-X	PC and embedded system
SSTL-2 Class I and II	DDR SDRAM
SSTL-18 Class I and II	DDR2 SDRAM
SSTL-15 Class I and II	DDR3 SDRAM
HSTL-18 Class I and II	QDRII/RLDRAM II
HSTL-15 Class I and II	QDRII/QDRII+/RLDRAM II
HSTL-12 Class I and II	General purpose
Differential SSTL-2 Class I and II	DDR SDRAM
Differential SSTL-18 Class I and II	DDR2 SDRAM

Table 6–1. I/O Standards and Applications for Stratix IV Devices (Part 2 of 2)

I/O Standard	Application
Differential SSTL-15 Class I and II	DDR3 SDRAM
Differential HSTL-18 Class I and II	Clock interfaces
Differential HSTL-15 Class I and II	Clock interfaces
Differential HSTL-12 Class I and II	Clock interfaces
LVDS	High-speed communications
RSDS	Flat panel display
mini-LVDS	Flat panel display
LVPECL	Video graphics and clock distribution

Notes to Table 6–1:

(1) The 3.3-V LVTTL/LVCMOS standard is supported using V_{CCIO} at 3.0 V.

(2) For more information about the 3.3-V LVTTL/LVCMOS standard supported in Stratix IV devices, refer to "3.3-V I/O Interface" on page 6–19.

For more information about transceiver supported I/O standards, refer to the *Transceiver Architecture in Stratix IV Devices* chapter.

I/O Standards and Voltage Levels

Stratix IV devices support a wide range of industry I/O standards, including single-ended, voltage-referenced single-ended, and differential I/O standards.

Table 6–2 lists the supported I/O standards and typical values for input and output V_{CCIO}, V_{CCPD}, V_{REF}, and board V_{TT}.

Table 6–2. I/O Standards and Voltage Levels for Stratix IV Devices (1) (Part 1 of 3)

I/O Standard	Standard Support	V_{CCIO} (V)				V_{CCPD} (V) (Pre-Driver Voltage)	V_{REF} (V) (Input Ref Voltage)	V_{TT} (V) (Board Termination Voltage)
		Input Operation		Output Operation				
		Column I/O Banks	Row I/O Banks	Column I/O Banks	Row I/O Banks			
3.3-V LVTTL	JESD8-B	3.0/2.5	3.0/2.5	3.0	3.0	3.0	—	—
3.3-V LVCMOS (3)	JESD8-B	3.0/2.5	3.0/2.5	3.0	3.0	3.0	—	—
2.5-V LVCMOS	JESD8-5	3.0/2.5	3.0/2.5	2.5	2.5	2.5	—	—
1.8-V LVCMOS	JESD8-7	1.8/1.5	1.8/1.5	1.8	1.8	2.5	—	—
1.5-V LVCMOS	JESD8-11	1.8/1.5	1.8/1.5	1.5	1.5	2.5	—	—
1.2-V LVCMOS	JESD8-12	1.2	1.2	1.2	1.2	2.5	—	—
3.0-V PCI	PCI Rev 2.1	3.0	3.0	3.0	3.0	3.0	—	—
3.0-V PCI-X	PCI-X Rev 1.0	3.0	3.0	3.0	3.0	3.0	—	—
SSTL-2 Class I	JESD8-9B	(2)	(2)	2.5	2.5	2.5	1.25	1.25
SSTL-2 Class II	JESD8-9B	(2)	(2)	2.5	2.5	2.5	1.25	1.25
SSTL-18 Class I	JESD8-15	(2)	(2)	1.8	1.8	2.5	0.90	0.90
SSTL-18 Class II	JESD8-15	(2)	(2)	1.8	1.8	2.5	0.90	0.90

Table 6–2. I/O Standards and Voltage Levels for Stratix IV Devices (1) (Part 2 of 3)

I/O Standard	Standard Support	V_{CCIO} (V)				V_{CCPD} (V) (Pre-Driver Voltage)	V_{REF} (V) (Input Ref Voltage)	V_{TT} (V) (Board Termination Voltage)
		Input Operation		Output Operation				
		Column I/O Banks	Row I/O Banks	Column I/O Banks	Row I/O Banks			
SSTL-15 Class I	—	(2)	(2)	1.5	1.5	2.5	0.75	0.75
SSTL-15 Class II	—	(2)	(2)	1.5	—	2.5	0.75	0.75
HSTL-18 Class I	JESD8-6	(2)	(2)	1.8	1.8	2.5	0.90	0.90
HSTL-18 Class II	JESD8-6	(2)	(2)	1.8	1.8	2.5	0.90	0.90
HSTL-15 Class I	JESD8-6	(2)	(2)	1.5	1.5	2.5	0.75	0.75
HSTL-15 Class II	JESD8-6	(2)	(2)	1.5	—	2.5	0.75	0.75
HSTL-12 Class I	JESD8-16A	(2)	(2)	1.2	1.2	2.5	0.6	0.6
HSTL-12 Class II	JESD8-16A	(2)	(2)	1.2	—	2.5	0.6	0.6
Differential SSTL-2 Class I	JESD8-9B	(2)	(2)	2.5	2.5	2.5	—	1.25
Differential SSTL-2 Class II	JESD8-9B	(2)	(2)	2.5	2.5	2.5	—	1.25
Differential SSTL-18 Class I	JESD8-15	(2)	(2)	1.8	1.8	2.5	—	0.90
Differential SSTL-18 Class II	JESD8-15	(2)	(2)	1.8	1.8	2.5	—	0.90
Differential SSTL-15 Class I	—	(2)	(2)	1.5	1.5	2.5	—	0.75
Differential SSTL-15 Class II	—	(2)	(2)	1.5	—	2.5	—	0.75
Differential HSTL-18 Class I	JESD8-6	(2)	(2)	1.8	1.8	2.5	—	0.90
Differential HSTL-18 Class II	JESD8-6	(2)	(2)	1.8	1.8	2.5	—	0.90
Differential HSTL-15 Class I	JESD8-6	(2)	(2)	1.5	1.5	2.5	—	0.75
Differential HSTL-15 Class II	JESD8-6	(2)	(2)	1.5	—	2.5	—	0.75
Differential HSTL-12 Class I	JESD8-16A	(2)	(2)	1.2	1.2	2.5	—	0.60
Differential HSTL-12 Class II	JESD8-16A	(2)	(2)	1.2	—	2.5	—	0.60
LVDS (4), (5), (8)	ANSI/TIA/EIA-644	(2)	(2)	2.5	2.5	2.5	—	—
RSDS (6), (7), (8)	—	(2)	(2)	2.5	2.5	2.5	—	—
mini-LVDS (6), (7), (8)	—	(2)	(2)	2.5	2.5	2.5	—	—

Table 6–2. I/O Standards and Voltage Levels for Stratix IV Devices (1) (Part 3 of 3)

I/O Standard	Standard Support	V_{CCIO} (V)				V_{CCPD} (V) (Pre-Driver Voltage)	V_{REF} (V) (Input Ref Voltage)	V_{TT} (V) (Board Termination Voltage)
		Input Operation		Output Operation				
		Column I/O Banks	Row I/O Banks	Column I/O Banks	Row I/O Banks			
LVPECL	—	(4)	2.5	—	—	2.5	—	—

Notes to Table 6–2:

(1) V_{CCPD} is either 2.5 or 3.0 V. For V_{CCIO} = 3.0 V, V_{CCPD} = 3.0 V. For V_{CCIO} = 2.5 V or less, V_{CCPD} = 2.5 V.

(2) Single-ended HSTL/SSTL, differential SSTL/HSTL, and LVDS input buffers are powered by V_{CCPD}. Row I/O banks support both true differential input buffers and true differential output buffers. Column I/O banks support true differential input buffers, but not true differential output buffers. I/O pins are organized in pairs to support differential standards. Column I/O differential HSTL and SSTL inputs use LVDS differential input buffers without on-chip R_D support.

(3) For more information about the 3.3-V LVTTL/LVCMOS standard supported in Stratix IV devices, refer to "3.3-V I/O Interface" on page 6–19.

(4) Column I/O banks support LVPECL I/O standards for input clock operation. Clock inputs on column I/Os are powered by $V_{CCCLKIN}$ when configured as differential clock inputs. They are powered by V_{CCIO} when configured as single-ended clock inputs. Differential clock inputs in row I/Os are powered by V_{CCPD}.

(5) Column and row I/O banks support LVDS outputs using two single-ended output buffers, an external one-resistor (LVDS_E_1R), and a three-resistor (LVDS_E_3R) network.

(6) Row I/O banks support RSDS and mini-LVDS I/O standards using a true LVDS output buffer without a resistor network.

(7) Column and row I/O banks support RSDS and mini-LVDS I/O standards using two single-ended output buffers with one-resistor (RSDS_E_1R and mini-LVDS_E_1R) and three-resistor (RSDS_E_3R and mini-LVDS_E_3R) networks.

(8) The emulated differential output standard that supports the tri-state feature includes: LVDS_E_1R, LVDS_E_3R, RSDS_E_1R, RSDS_E_3R, Mini_LVDS_E_1R, and Mini_LVDS_E_3R. For more information, refer to the *I/O Buffer (ALTIOBUF) Megafunction User Guide*.

For more information about the electrical characteristics of each I/O standard, refer to the *DC and Switching Characteristics for Stratix IV Devices* chapter.

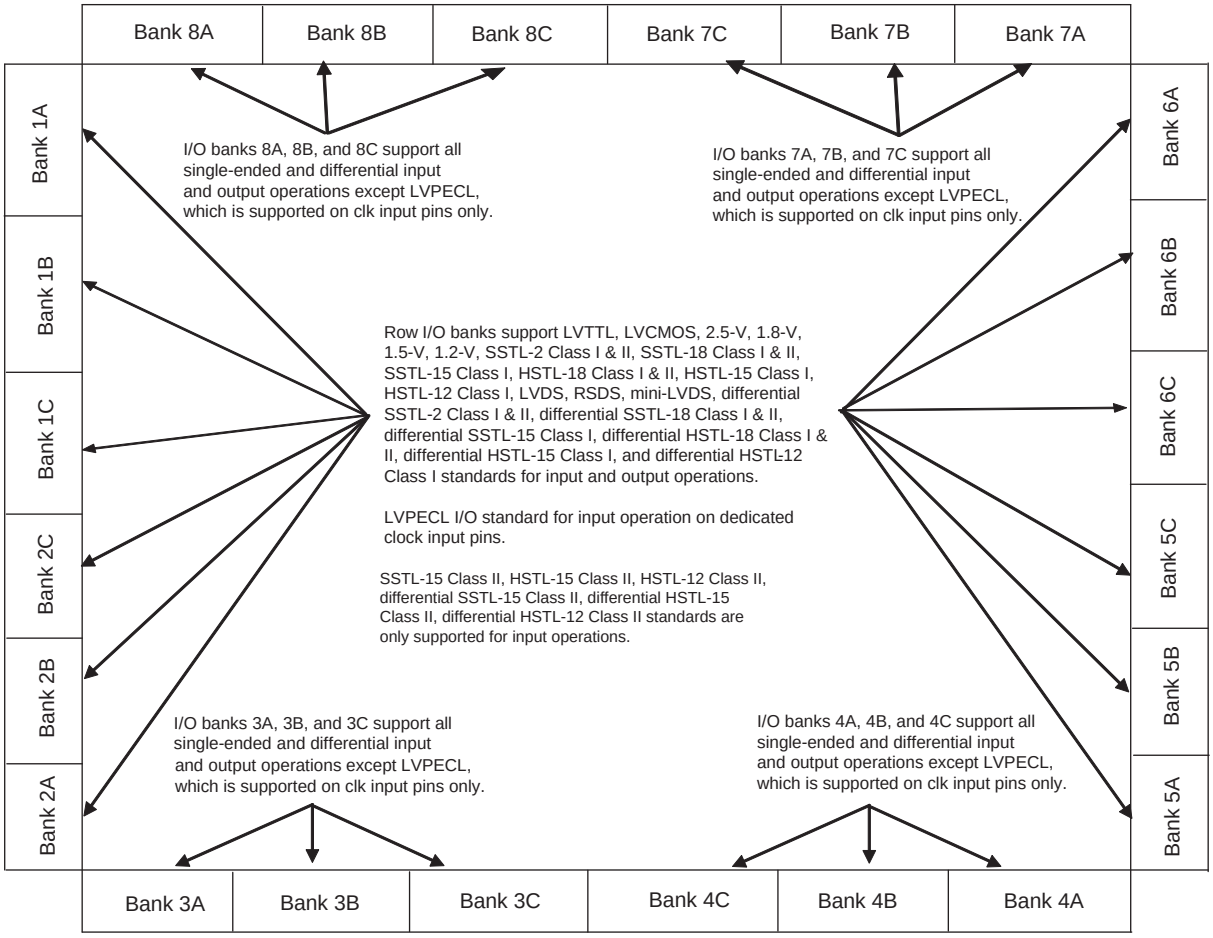
I/O Banks

Stratix IV devices contain up to 24 I/O banks, as shown in Figure 6–1 and Figure 6–2. The row I/O banks contain true differential input and output buffers and dedicated circuitry to support differential standards at speeds up to 1.6 Gbps.

Each I/O bank in Stratix IV devices can support high-performance external memory interfaces with dedicated circuitry. The I/O pins are organized in pairs to support differential standards. Each I/O pin pair can support both differential input and output buffers. The only exceptions are the `clk[1,3,8,10]`, `PLL_L[1,4]_clk`, and `PLL_R[1,4]_clk` pins, which support differential input operations only.

For information about the number of channels available for the LVDS I/O standard, refer to the *High-Speed Differential I/O Interface and DPA in Stratix IV Devices* chapter. For more information about transceiver-bank-related features, refer to the *Transceiver Architecture in Stratix IV Devices* chapter.

Figure 6–1. Stratix IV E Devices I/O Banks *(1), (2), (3), (4), (5), (6), (7), (8)*



Notes to Figure 6–1:

(1) Differential HSTL and SSTL outputs are not true differential outputs. They use two single-ended outputs with the second output programmed as inverted.

(2) Column I/O differential HSTL and SSTL inputs use LVDS differential input buffers without differential OCT support.

(3) Column I/O supports LVDS outputs using single-ended buffers and external resistor networks.

(4) Column I/O supports PCI/PCI-X with on-chip clamp diode. Row I/O supports PCI/PCI-X with external clamp diode.

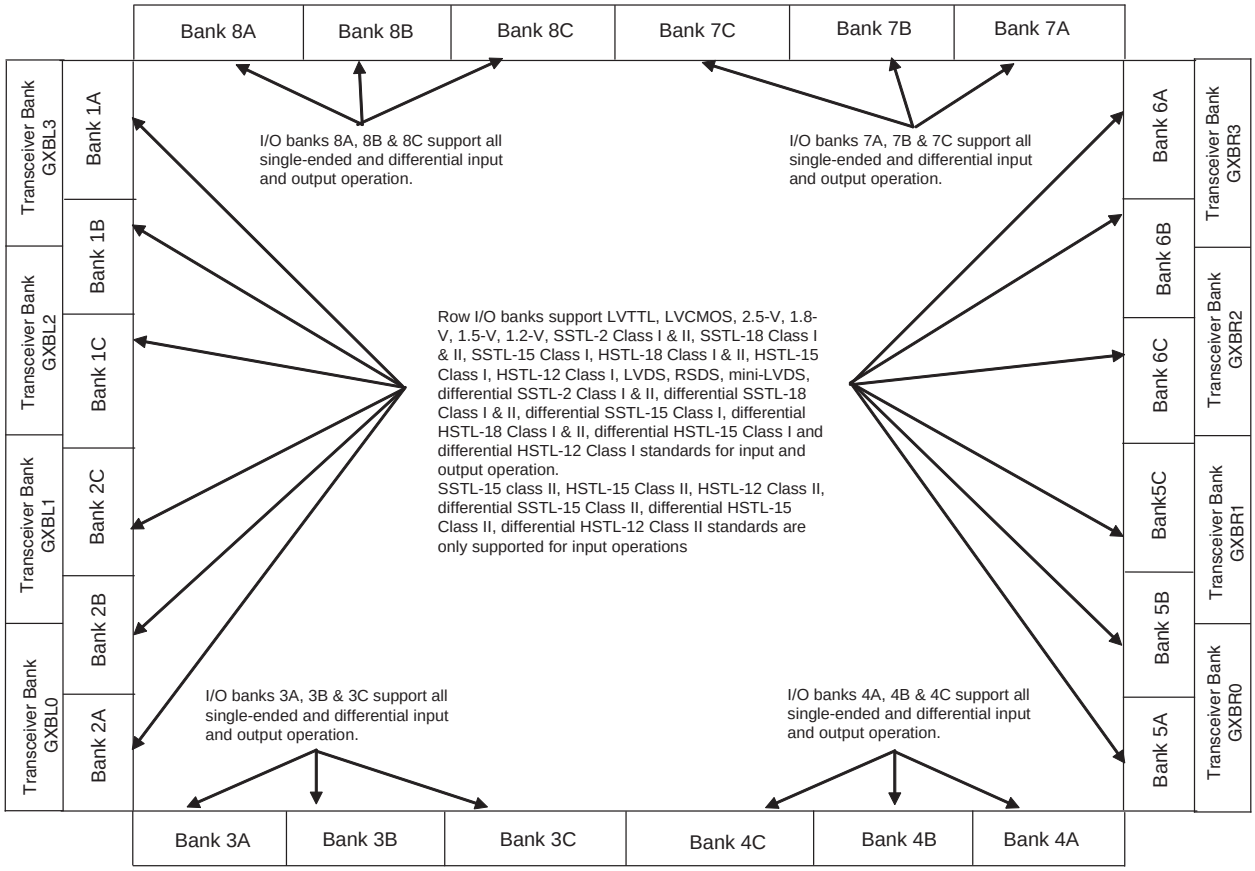
(5) Clock inputs on column I/Os are powered by $V_{CCCLKIN}$ when configured as differential clock inputs. They are powered by V_{CCIO} when configured as single-ended clock inputs. All outputs use the corresponding bank V_{CCIO}.

(6) Row I/O supports the true LVDS output buffer.

(7) Column and row I/O banks support LVPECL standards for input clock operation.

(8) Figure 6–1 is a top view of the silicon die that corresponds to a reverse view for flip chip packages. It is a graphical representation only.

Figure 6–2. Stratix IV GX Devices I/O Banks *(1), (2), (3), (4), (5), (6), (7), (8), (9)*



Notes to Figure 6–2:

(1) Differential HSTL and SSTL outputs are not true differential outputs. They use two single-ended outputs with the second output programmed as inverted.

(2) Column I/O differential HSTL and SSTL inputs use LVDS differential input buffers without differential OCT support.

(3) Column I/O supports LVDS outputs using single-ended buffers and external resistor networks.

(4) Column I/O supports PCI/PCI-X with an on-chip clamp diode. Row I/O supports PCI/PCI-X with an external clamp diode.

(5) Clock inputs on column I/Os are powered by $V_{CCCLKIN}$ when configured as differential clock inputs. They are powered by V_{CCIO} when configured as single-ended clock inputs. All outputs use the corresponding bank V_{CCIO}.

(6) Row I/O supports the true LVDS output buffer.

(7) Column and row I/O banks support LVPECL standards for input clock operation.

(8) Figure 6–2 is a top view of the silicon die that corresponds to a reverse view for flip chip packages. It is a graphical representation only.

(9) Stratix IV devices do not support the PCI clamp diode when V_{CCIO} is 1.2 V, 1.5 V, or 1.8 V.

Modular I/O Banks

The I/O pins in Stratix IV devices are arranged in groups called modular I/O banks. Depending on device densities, the number of Stratix IV device I/O banks range from 16 to 24. The number of I/O pins on each bank is 24, 32, 36, 40, or 48. Figure 6–4 through Figure 6–16 show the number of I/O pins available in each I/O bank.

In Stratix IV devices, the maximum number of I/O banks per side is either four or six, depending on the device density. When migrating between devices with a different number of I/O banks per side, it is the middle or "B" bank that is removed or inserted. For example, when moving from a 24-bank device to a 16-bank device, the banks that are dropped are "B" banks, namely: 1B, 2B, 3B, 4B, 5B, 6B, 7B, and 8B. Similarly, when moving from a 16-bank device to a 24-bank device, the banks that are added are the same "B" banks.

After migration from a smaller device to a larger device, the bank size increases or remains the same, but never decreases. For example, the number of I/O pins to a bank may increase from 24 to 26, 32, 36, 40, 42, or 48, but will never decrease. This is shown in Figure 6–3.

Figure 6–3. Bank Migration Path with Increasing Device Size

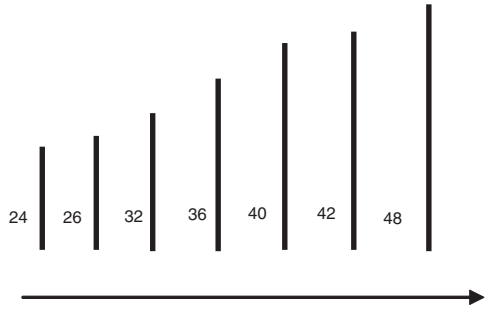


Figure 6–4 through Figure 6–16 show the number of I/O pins and packaging information for different sets of available devices. They show the top view of the silicon die that corresponds to a reverse view for flip chip packages. They are graphical representations only.

For Figure 6–4 through Figure 6–16, the pin count includes all general purpose I/Os, dedicated clock pins, and dual purpose configuration pins. Transceiver pins and dedicated configuration pins are not included in the pin count.

Figure 6–4. Number of I/Os in Each Bank in EP4SE230 and EP4SE360 Devices in the 780-Pin FineLine BGA Package

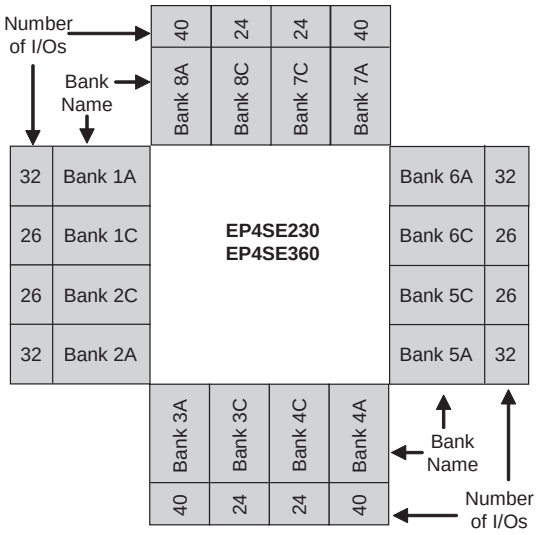


Figure 6–5. Number of I/Os in Each Bank in EP4SE360, EP4SE530, and EP4SE820 Devices in the 1152-Pin FineLine BGA Package

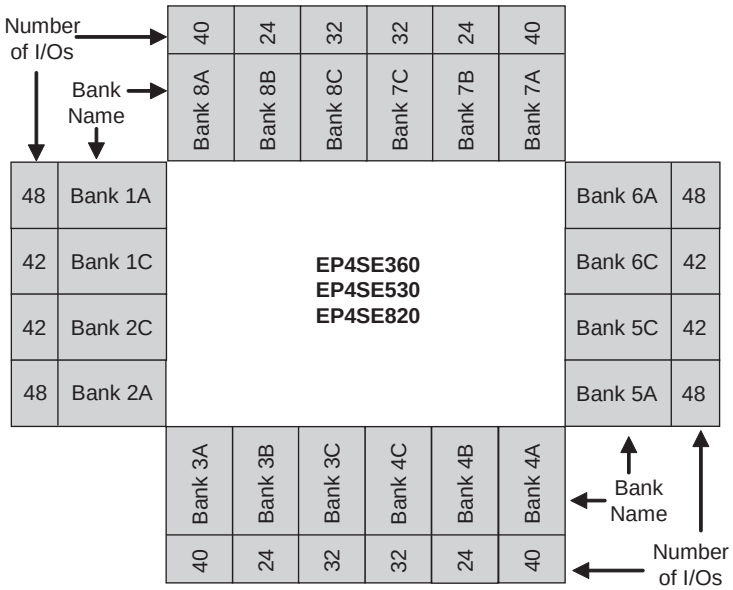


Figure 6–6. Number of I/Os in Each Bank in EP4SE530 and EP4SE820 Devices in the 1517-Pin FineLine BGA Package

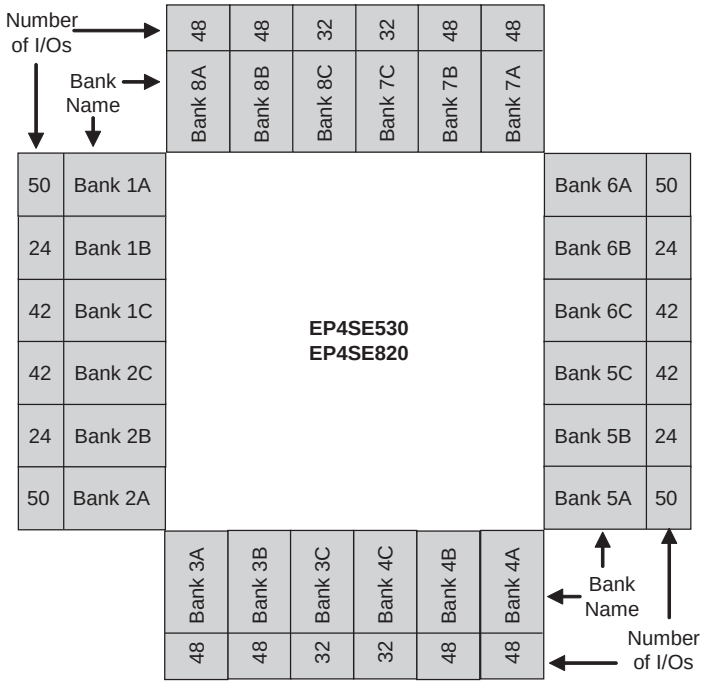


Figure 6–7. Number of I/Os in Each Bank in EP4SE530 and EP4SE820 Devices in the 1760-Pin Fineline BGA Package

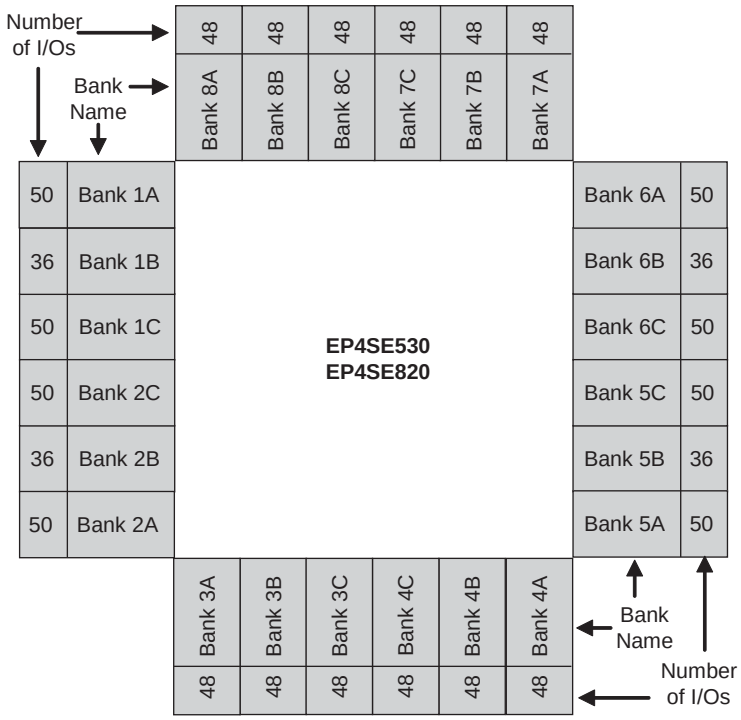


Figure 6–8. Number of I/Os in Each Bank in EP4SGX70, EP4SGX110, EP4SGX180, and EP4SGX230 Devices in the 780-Pin FineLine BGA Package

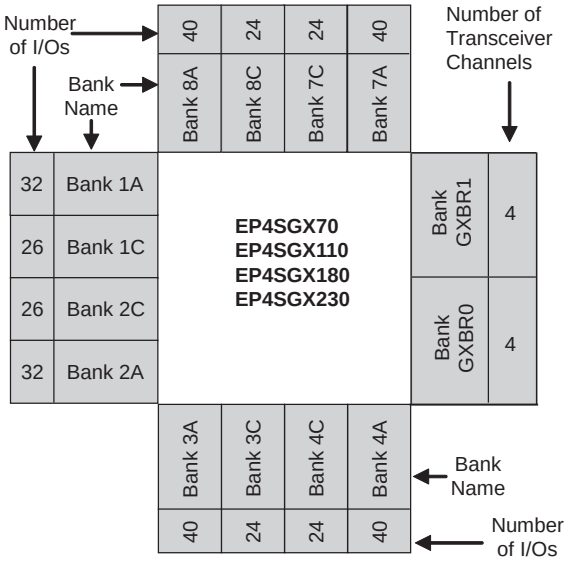


Figure 6–9. Number of I/Os in Each Bank in EP4SGX290 and EP4SGX360 Devices in the 780-Pin FineLine BGA Package

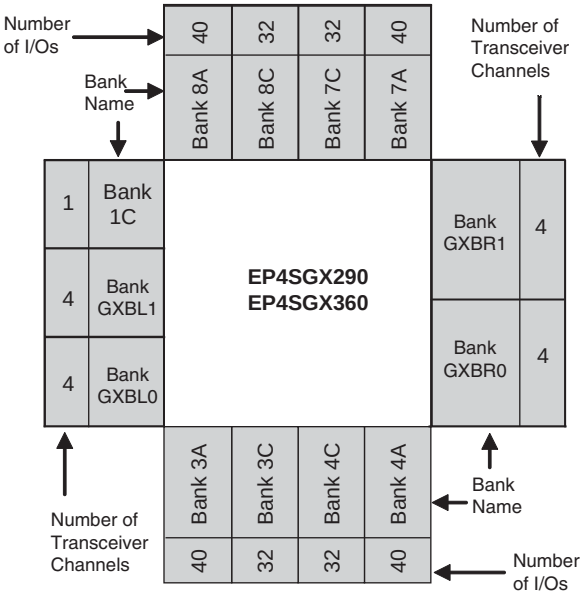


Figure 6–10. Number of I/Os in Each Bank in EP4SGX70 and EP4SGX110 Devices in the 1152-Pin FineLine BGA Package

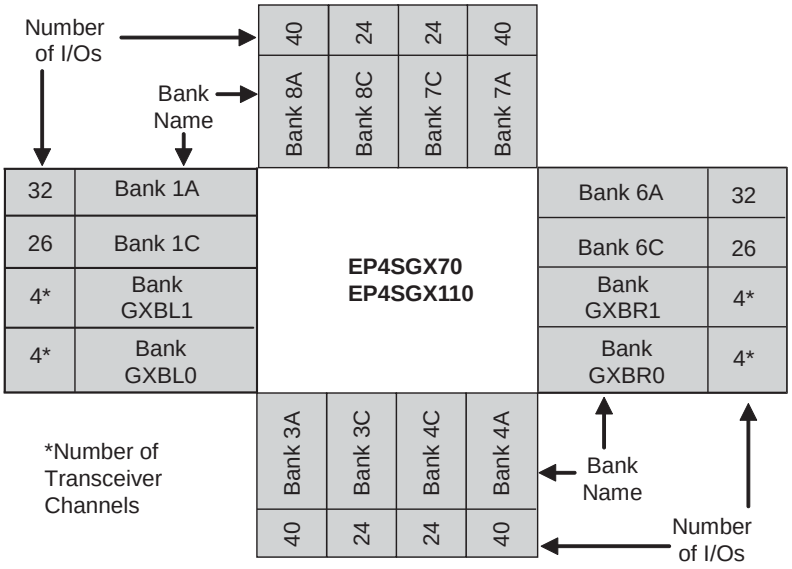
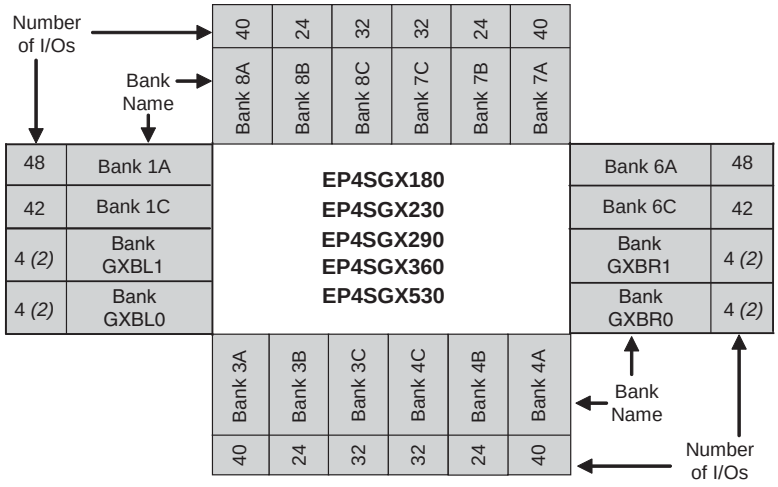


Figure 6–11. Number of I/Os in Each Bank in EP4SGX180, EP4SGX230, EP4SGX290, EP4SGX360, and EP4SGX530 Devices in the 1152-Pin FineLine BGA Package *(1)*, *(2)*

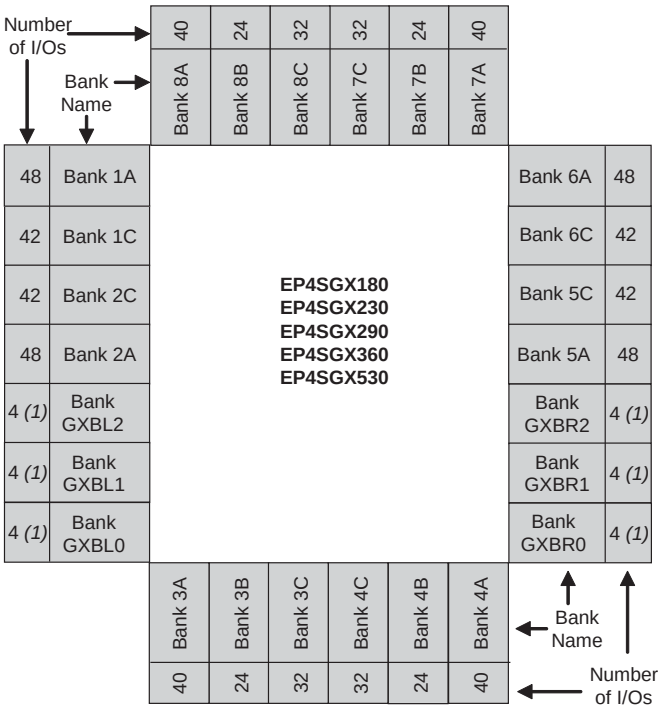


Notes to Figure 6–11:

(1) Except for the EP4SGX530 device, all listed devices have two variants in the F1152 package option—one with no PMA-only transceiver channels and the other with two PMA-only transceiver channels for each transceiver bank. The EP4SGX530 device is only offered with two PMA-only transceiver channels for each transceiver bank in the F1152 package option.

(2) There are two additional PMA-only transceiver channels in each transceiver bank for devices with the PMA-only transceiver package option.

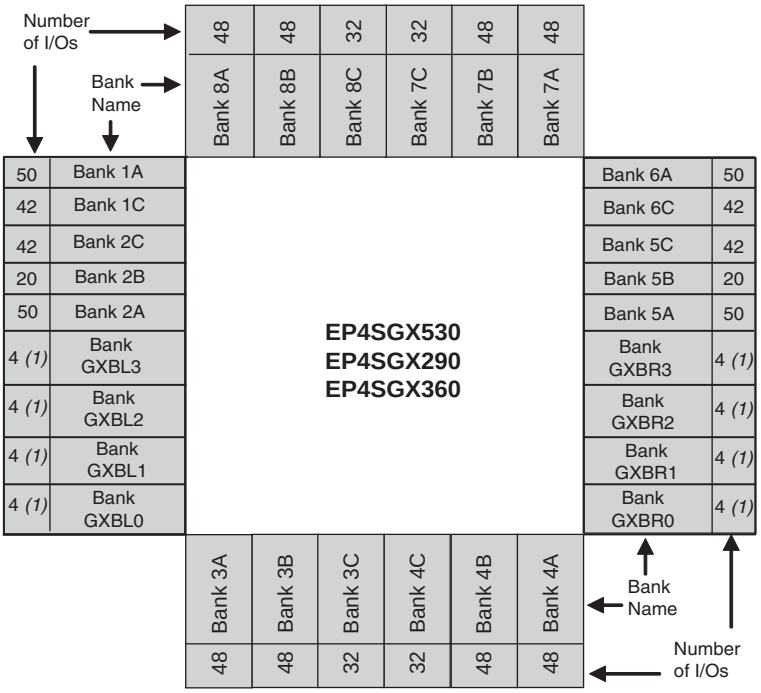
Figure 6–12. Number of I/Os in Each Bank in EP4SGX180, EP4SGX230, EP4SGX290, EP4SGX360, and EP4SGX530 Devices in the 1517-Pin FineLine BGA Package *(1)*



Note to Figure 6–12:

(1) There are two additional PMA-only transceiver channels in each transceiver bank.

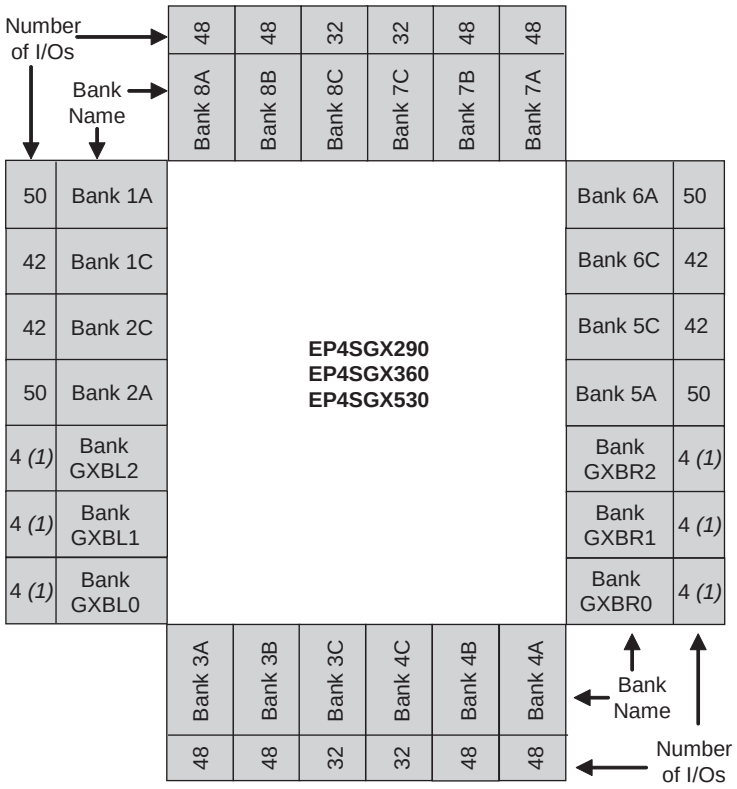
Figure 6–13. Number of I/Os in Each Bank in EP4SGX290, EP4SGX360, and EP4SGX530 Devices in the 1932-Pin FineLine BGA Package *(1)*



Note to Figure 6–13:

(1) There are two additional PMA-only transceiver channels in each transceiver bank.

Figure 6–14. Number of I/Os in Each Bank in EP4SGX290, EP4SGX360, and EP4SGX530 Devices in the 1760-Pin FineLine BGA Package *(1)*

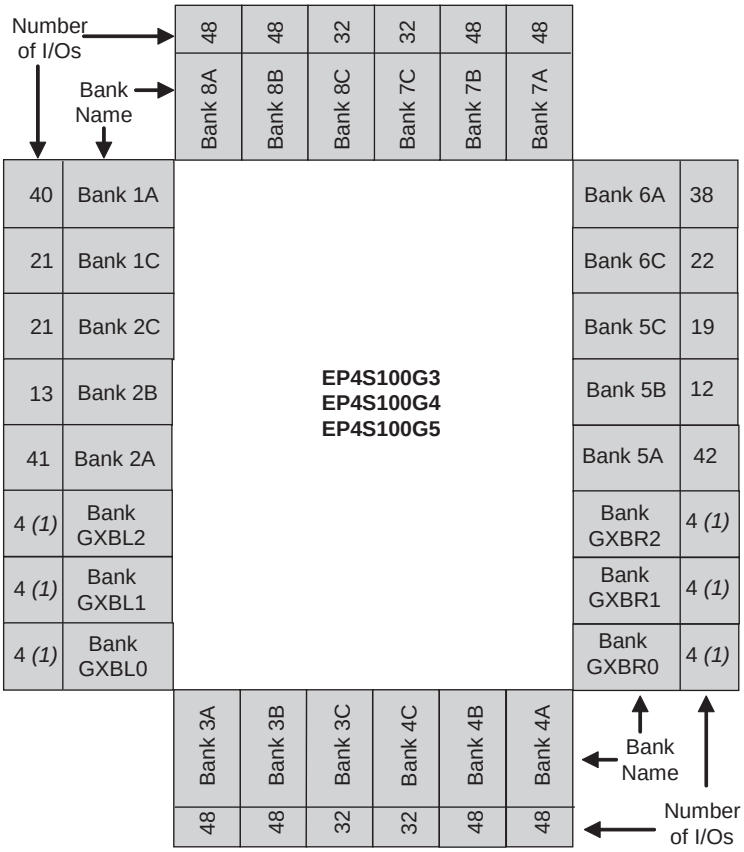


Note to Figure 6–14:

(1) There are two additional PMA-only transceiver channels in each transceiver bank.

The information in Figure 6–15 and Figure 6–16 applies to Stratix IV GX and GT devices.

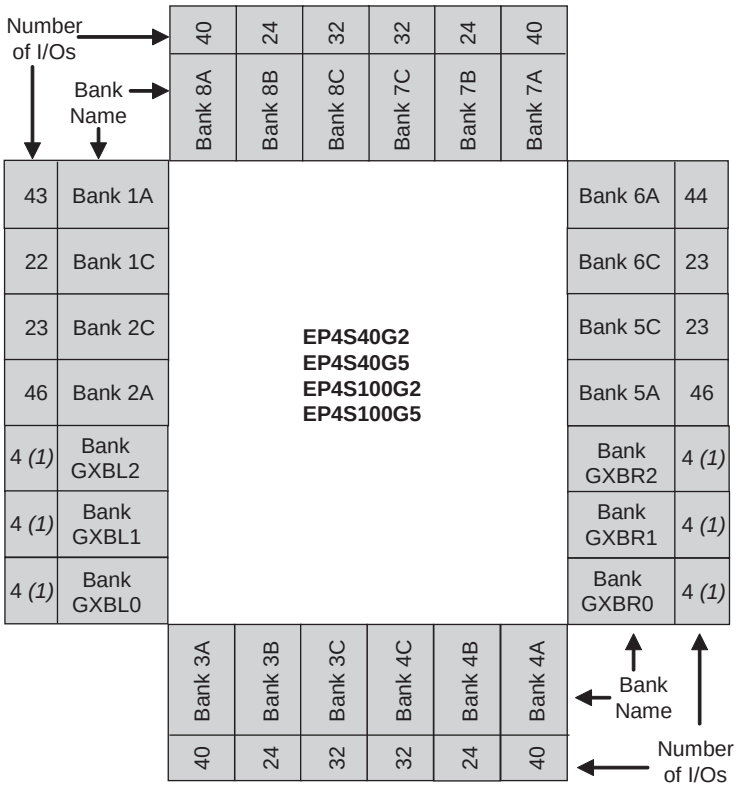
Figure 6–15. Number of I/Os in Each Bank in EP4S100G3, EP4S100G4, and EP4S100G5 Devices in the 1932-Pin FineLine BGA Package *(1)*



Note to Figure 6–15:

(1) There are two additional PMA-only transceiver channels in each transceiver bank.

Figure 6–16. Number of I/Os in Each Bank in EP4S40G2, EP4S40G5, EP4S100G2, and EP4S100G5 Devices in the 1517-Pin FineLine BGA Package *(1)*



Note to Figure 6–16:

(1) There are two additional PMA-only transceiver channels in each transceiver bank.

I/O Structure

The I/O element (IOE) in Stratix IV devices contain a bidirectional I/O buffer and I/O registers to support a complete embedded bidirectional single data rate or DDR transfer. The IOEs are located in I/O blocks around the periphery of the Stratix IV device. There are up to four IOEs per row I/O block and four IOEs per column I/O block. The row IOEs drive row, column, or direct link interconnects. The column IOEs drive column interconnects.

The Stratix IV bidirectional IOE also supports the following features:

- Programmable input delay
- Programmable output-current strength
- Programmable slew rate
- Programmable output delay
- Programmable bus-hold
- Programmable pull-up resistor
- Open-drain output
- On-chip series termination with calibration

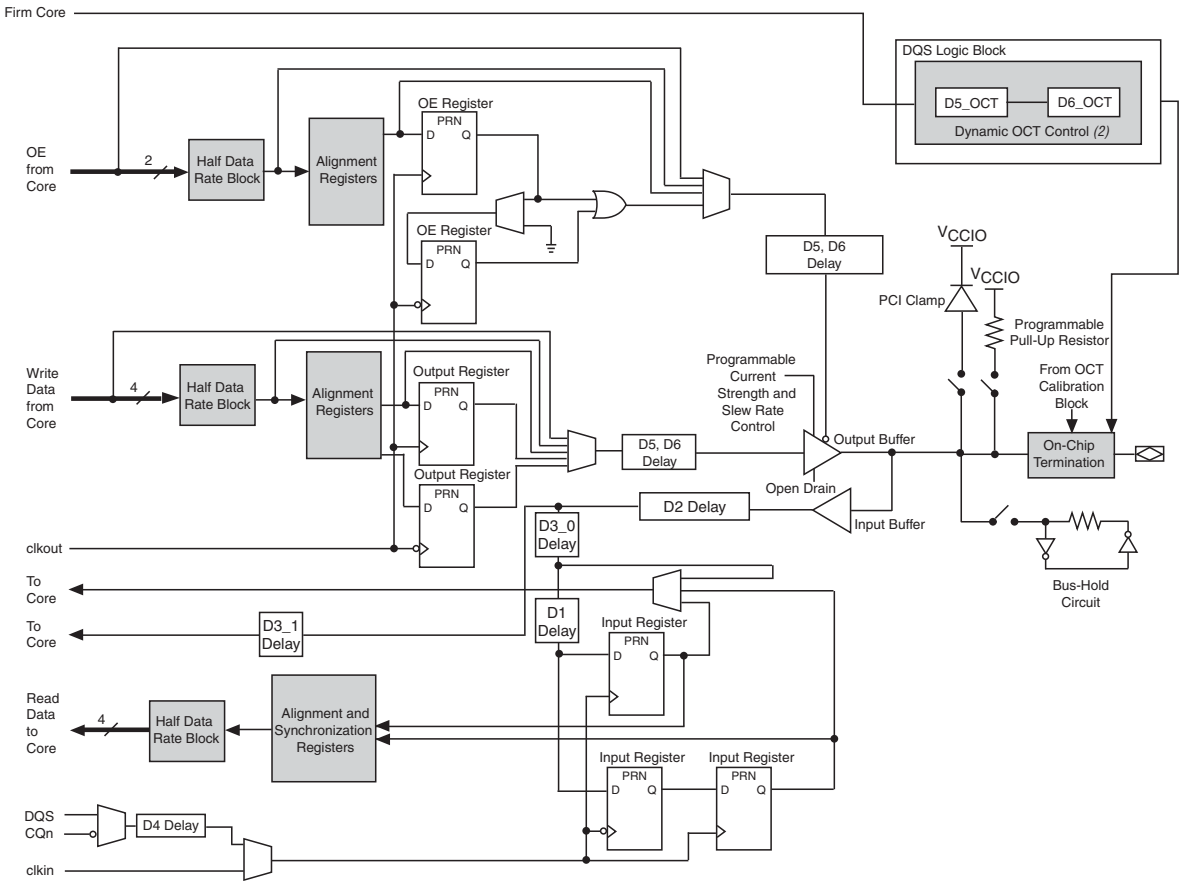
- On-chip series termination without calibration
- On-chip parallel termination with calibration
- On-chip differential termination
- PCI clamping diode

I/O registers are composed of the input path for handling data from the pin to the core, the output path for handling data from the core to the pin, and the output-enable (OE) path for handling the OE signal to the output buffer. These registers allow faster source-synchronous register-to-register transfers and resynchronization. The input path consists of the DDR input registers, alignment and synchronization registers, and HDR. You can bypass each block of the input path.

The output and OE paths are divided into output or OE registers, alignment registers, and HDR blocks. You can bypass each block of the output and OE paths.

Figure 6–17 shows the Stratix IV IOE structure.

Figure 6–17. IOE Structure in Stratix IV Devices *(1)*, *(2)*, *(3)*, *(4)*



Notes to Figure 6–17:

(1) The following features are not supported by true differential standards: open drain or tri-state output,; programmable current strength and slew rate control; PCI Clamp; programmable pull-up resistor; bus-hold circuit.

(2) The `D3_0` and `D3_1` delays have the same available settings in the Quartus® II software

(3) One dynamic OCT control is available per DQ/DQS group.

(4) Column I/O supports PCI/PCI-X with an on-chip clamp diode. Row I/O supports PCI/PCI-X with an external clamp diode.

For more information about I/O registers and how they are used for memory applications, refer to the *External Memory Interfaces in Stratix IV Devices* chapter.

3.3-V I/O Interface

Stratix IV I/O buffers support 3.3-V I/O standards. You can use them as transmitters or receivers in your system. The output high voltage (V_{OH}), output low voltage (V_{OL}), input high voltage (V_{IH}), and input low voltage (V_{IL}) levels meet the 3.3-V I/O standards specifications defined by EIA/JEDEC Standard JESD8-B with margin when the Stratix IV V_{CCIO} voltage is powered by 3.0 V.

To ensure device reliability and proper operation, when interfacing with a 3.3-V I/O system using Stratix IV devices, ensure that you do not violate the absolute maximum ratings of the devices. Altera recommends performing IBIS simulation to determine that the overshoot and undershoot voltages are within the guidelines.

When using the Stratix IV device as a transmitter, you can use slow slew rate and series termination to limit overshoot and undershoot at the I/O pins, but they are not required. Transmission line effects that cause large voltage deviations at the receiver are associated with an impedance mismatch between the driver and the transmission lines. By matching the impedance of the driver to the characteristic impedance of the transmission line, you can significantly reduce overshoot voltage. You can use a series termination resistor placed physically close to the driver to match the total driver impedance to the transmission line impedance. Stratix IV devices support series OCT for all LVTTL and LVCMOS I/O standards in all I/O banks.

When using the Stratix IV device as a receiver, you can use a clamping diode (on-chip or off-chip) to limit overshoot, though this is not required. Stratix IV devices provide an optional on-chip PCI-clamping diode for column I/O pins. You can use this diode to protect the I/O pins against overshoot voltage.

The 3.3-V I/O standard is supported using bank supply voltage (V_{CCIO}) at 3.0 V. In this method, the clamping diode (on-chip or off-chip), when enabled, can sufficiently clamp overshoot voltage to within the DC and AC input voltage specifications. The clamped voltage can be expressed as the sum of the supply voltage (V_{CCIO}) and the diode forward voltage.

For more information about the absolute maximum rating and maximum allowed overshoot during transitions, refer to the *DC and Switching Characteristics for Stratix IV Devices* chapter.

External Memory Interfaces

In addition to the I/O registers in each IOE, Stratix IV devices also have dedicated registers and phase-shift circuitry on all I/O banks for interfacing with external memory interfaces.

For more information about external memory interfaces, refer to the *External Memory Interfaces in Stratix IV Devices* chapter.

High-Speed Differential I/O with DPA Support

Stratix IV devices have the following dedicated circuitry for high-speed differential I/O support:

- Differential I/O buffer
- Transmitter serializer
- Receiver deserializer
- Data realignment
- Dynamic phase aligner (DPA)
- Synchronizer (FIFO buffer)
- Phase-locked loops (PLLs)

For more information about DPA support, refer to the *High-Speed Differential I/O Interfaces and DPA in Stratix IV Devices* chapter.

Programmable Current Strength

The output buffer for each Stratix IV device I/O pin has a programmable current strength control for certain I/O standards. Use programmable current strength to mitigate the effects of high signal attenuation due to a long transmission line or a legacy backplane. The LVTTL, LVCMOS, SSTL, and HSTL standards have several levels of current strength that you can control. Table 6–3 lists the programmable current strength for Stratix IV devices.

Table 6–3. Programmable Current Strength (Part 1 of 2) (1), (2)

I/O Standard	I_{OH} / I_{OL} Current Strength Setting (mA) for Column I/O Pins	I_{OH} / I_{OL} Current Strength Setting (mA) for Row I/O Pins
3.3-V LVTTL	16, 12, 8, 4	12, 8, 4
3.3-V LVCMOS	16, 12, 8, 4	8, 4
2.5-V LVCMOS	16, 12, 8, 4	12, 8, 4
1.8-V LVCMOS	12, 10, 8, 6, 4, 2	8, 6, 4, 2
1.5-V LVCMOS	12, 10, 8, 6, 4, 2	8, 6, 4, 2
1.2-V LVCMOS	8, 6, 4, 2	4, 2
SSTL-2 Class I	12, 10, 8	12, 8
SSTL-2 Class II	16	16
SSTL-18 Class I	12, 10, 8, 6, 4	12, 10, 8, 6, 4
SSTL-18 Class II	16, 8	16, 8
SSTL-15 Class I	12, 10, 8, 6, 4	8, 6, 4
SSTL-15 Class II	16, 8	—
HSTL-18 Class I	12, 10, 8, 6, 4	12, 10, 8, 6, 4
HSTL-18 Class II	16	16
HSTL-15 Class I	12, 10, 8, 6, 4	8, 6, 4
HSTL-15 Class II	16	—

Table 6–3. Programmable Current Strength (Part 2 of 2) (1), (2)

I/O Standard	I_{OH} / I_{OL} Current Strength Setting (mA) for Column I/O Pins	I_{OH} / I_{OL} Current Strength Setting (mA) for Row I/O Pins
HSTL-12 Class I	12, 10, 8, 6, 4	8, 6, 4
HSTL-12 Class II	16	—

Notes to Table 6–3:

(1) The default setting in the Quartus II software is 50-Ω OCT R_S without calibration for all non-voltage reference and HSTL and SSTL Class I I/O standards. The default setting is 25-Ω OCT R_S without calibration for HSTL and SSTL Class II I/O standards.

(2) The 3.3-V LVTTL and 3.3-V LVCMOS are supported using V_{CCIO} and V_{CCPD} at 3.0 V.

Altera recommends performing IBIS or SPICE simulations to determine the best current strength setting for your specific application.

Programmable Slew Rate Control

The output buffer for each Stratix IV device regular- and dual-function I/O pin has a programmable output slew-rate control that you can configure for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. A slower slew rate can help reduce system noise, but adds a nominal delay to the rising and falling edges. Each I/O pin has an individual slew-rate control, allowing you to specify the slew rate on a pin-by-pin basis.

You cannot use the programmable slew rate feature when using OCT.

The Quartus II software allows four settings for programmable slew rate control—0, 1, 2, and 3—where 0 is slow slew rate and 3 is fast slew rate. Figure 6–4 lists the default slew rate settings from the Quartus II software.

Table 6–4. Default Slew Rate Settings

I/O Standard	Slew Rate Option	Default Slew Rate
1.2-V, 1.5-V, 1.8-V, 2.5-V LVCMOS, and 3.3-V LVTTL/LVCMOS	0, 1, 2, 3	3
SSTL-2, SSTL-18, SSTL-15, HSTL-18, HSTL-15, and HSTL-12	0, 1, 2, 3	3
3.0-V PCI/PCI-X	0, 1, 2, 3	3
LVDS_E_1R, mini-LVDS_E_1R, and RSDS_E_1R	0, 1, 2, 3	3
LVDS_E_3R, mini-LVDS_E_3R, and RSDS_E_3R	0, 1, 2, 3	3

You can use faster slew rates to improve the available timing margin in memory-interface applications or when the output pin has high-capacitive loading.

Altera recommends performing IBIS or SPICE simulations to determine the best slew rate setting for your specific application.

Programmable I/O Delay

The following sections describe programmable IOE delay and programmable output buffer delay.

Programmable IOE Delay

The Stratix IV device IOE includes programmable delays, shown in Figure 6–17 on page 6–18, that you can activate to ensure zero hold times, minimize setup times, or increase clock-to-output times. Each pin can have a different input delay from pin-to-input register or a delay from output register-to-output pin values to ensure that the bus has the same delay going into or out of the device. This feature helps read and time margins because it minimizes the uncertainties between signals in the bus.

For more information about programmable IOE delay specifications, refer to the *High-Speed Differential I/O Interfaces and DPA in Stratix IV Devices* chapter.

Programmable Output Buffer Delay

Stratix IV devices support delay chains built inside the single-ended output buffer, as shown in Figure 6–17 on page 6–18. The delay chains can independently control the rising and falling edge delays of the output buffer, providing the ability to adjust the output-buffer duty cycle, compensate channel-to-channel skew, reduce simultaneous switching output (SSO) noise by deliberately introducing channel-to-channel skew, and improve high-speed memory-interface timing margins. Stratix IV devices support four levels of output buffer delay settings. The default setting is **No Delay**.

For more information about programmable output buffer delay specifications, refer to the *High-Speed Differential I/O Interfaces and DPA in Stratix IV Devices* chapter.

Open-Drain Output

Stratix IV devices provide an optional open-drain output (equivalent to an open collector output) for each I/O pin. When configured as open drain, the logic value of the output is either high-Z or 0. Typically, an external pull-up resistor is required to provide logic high.

Bus Hold

Each Stratix IV device I/O pin provides an optional bus-hold feature. Bus-hold circuitry can weakly hold the signal on an I/O pin at its last-driven state. Because the bus-hold feature holds the last-driven state of the pin until the next input signal is present, you do not need an external pull-up or pull-down resistor to hold a signal level when the bus is tri-stated.

Bus-hold circuitry also pulls non-driven pins away from the input threshold voltage where noise can cause unintended high-frequency switching. You can select this feature individually for each I/O pin. The bus-hold output drives no higher than V_{CCIO} to prevent over-driving signals. If you enable the bus-hold feature, you cannot use the programmable pull-up option. Disable the bus-hold feature if the I/O pin is configured for differential signals.

Bus-hold circuitry uses a resistor with a nominal resistance (R_{BH}) of approximately 7 kΩ to weakly pull the signal level to the last-driven state.

For more information about the specific sustaining current driven through this resistor and the overdrive current used to identify the next-driven input level, refer to the *High-Speed Differential I/O Interfaces and DPA in Stratix IV Devices* chapter.

Bus-hold circuitry is active only after configuration. When going into user mode, the bus-hold circuit captures the value on the pin present at the end of configuration.

Programmable Pull-Up Resistor

Each Stratix IV device I/O pin provides an optional programmable pull-up resistor during user mode. If you enable this feature for an I/O pin, the pull-up resistor (typically 25 K) weakly holds the I/O to the V_{CCIO} level.

Programmable pull-up resistors are only supported on user I/O pins and are not supported on dedicated configuration pins, JTAG pins, or dedicated clock pins. If you enable the programmable pull-up option, you cannot use the bus-hold feature.

When the optional DEV_OE signal drives low, all the I/O pins remain tri-stated even with the programmable pull-up option enabled.

Programmable Pre-Emphasis

Stratix IV LVDS transmitters support programmable pre-emphasis to compensate for the frequency dependent attenuation of the transmission line. The Quartus II software allows four settings for programmable pre-emphasis.

For more information about programmable pre-emphasis, refer to the *High-Speed Differential I/O Interfaces and DPA in Stratix IV Devices* chapter.

Programmable Differential Output Voltage

Stratix IV LVDS transmitters support programmable V_{OD}. The programmable V_{OD} settings allow you to adjust output eye height to optimize trace length and power consumption. A higher V_{OD} swing improves voltage margins at the receiver end; a smaller V_{OD} swing reduces power consumption. The Quartus II software allows four settings for programmable V_{OD}.

For more information about programmable V_{OD}, refer to the *High-Speed Differential I/O Interfaces and DPA in Stratix IV Devices* chapter.

MultiVolt I/O Interface

The Stratix IV architecture supports the MultiVolt I/O interface feature that allows the Stratix IV devices in all packages to interface with systems of different supply voltages.

You can connect the VCCIO pins to a 1.2-, 1.5-, 1.8-, 2.5-, or 3.0-V power supply, depending on the output requirements. The output levels are compatible with systems of the same voltage as the power supply. (For example, when VCCIO pins are connected to a 1.5-V power supply, the output levels are compatible with 1.5-V systems.)

For more information about pin connection guidelines, refer to the *Stratix IV GX and Stratix IV E Device Family Pin Connection Guidelines*.

The Stratix IV VCCPD power pins must be connected to a 2.5- or 3.0-V power supply. Using these power pins to supply the pre-driver power to the output buffers increases the performance of the output pins. Table 6–5 lists Stratix IV MultiVolt I/O support.

Table 6–5. Stratix IV MultiVolt I/O Support *(1)*

V_{CCIO} (V) *(3)*	Input Signal (V)						Output Signal (V)					
	1.2	1.5	1.8	2.5	3.0	3.3	1.2	1.5	1.8	2.5	3.0	3.3
1.2	Y	—	—	—	—	—	Y	—	—	—	—	—
1.5	—	Y	Y	—	—	—	—	Y	—	—	—	—
1.8	—	Y	Y	—	—	—	—	—	Y	—	—	—
2.5	—	—	—	Y	Y *(2)*	Y *(2)*	—	—	—	Y	—	—
3.0	—	—	—	Y	Y	Y	—	—	—	—	Y	—

Notes to Table 6–5:

(1) The pin current may be slightly higher than the default value. You must verify that the driving device's V_{OL} maximum and V_{OH} minimum voltages do not violate the applicable Stratix IV V_{IL} maximum and V_{IH} minimum voltage specifications.

(2) Altera recommends that you use an external clamping diode on the I/O pins when the input signal is 3.0 V or 3.3 V. You have the option to use an internal clamping diode for column I/O pins.

(3) Each I/O bank of a Stratix IV device has its own VCCIO pins and supports only one V_{CCIO}, either 1.2, 1.5, 1.8, or 3.0 V. The LVDS I/O standard is not supported when V_{CCIO} is 3.0 V. The LVDS input operations are supported when V_{CCIO} is 1.2 V, 1.5 V, 1.8 V, or 2.5 V. The LVDS output operations are only supported when V_{CCIO} is 2.5 V.

On-Chip Termination Support and I/O Termination Schemes

Stratix IV devices feature dynamic series and parallel OCT to provide I/O impedance matching and termination capabilities. OCT maintains signal quality, saves board space, and reduces external component costs.

Stratix IV devices support:

- On-chip series termination (R_S) with calibration
- On-chip series termination (R_S) without calibration
- On-chip Parallel termination (R_T) with calibration
- Dynamic series termination for single-ended I/O standards
- Dynamic Parallel termination for single-ended I/O standards
- On-chip differential termination (R_D) for differential LVDS I/O standards

Stratix IV devices support OCT in all I/O banks by selecting one of the OCT I/O standards.

These devices also support OCT R_S and R_T in the same I/O bank for different I/O standards if they use the same V_{CCIO} supply voltage. You can independently configure each I/O in an I/O bank to support OCT R_S, programmable current strength, or OCT R_T.

You cannot configure both OCT R_S and programmable current strength for the same I/O buffer.

A pair of RUP and RDN pins are available in a given I/O bank and are shared for series- and parallel-calibrated termination. The RUP and RDN pins share the same V_{CCIO} and GND, respectively, with the I/O bank where they are located. The RUP and RDN pins are dual-purpose I/Os and function as regular I/Os if you do not use the calibration circuit.

For calibration, the connections are as follows:

- The RUP pin is connected to V_{CCIO} through an external 25-Ω ±1% or 50-Ω ±1% resistor for an on-chip series termination value of 25-Ω or 50-Ω, respectively.
- The RDN pin is connected to GND through an external 25-Ω ±1% or 50-Ω ±1% resistor for an on-chip series termination value of 25-Ω or 50-Ω, respectively.

For on-chip parallel termination, the connections are as follows:

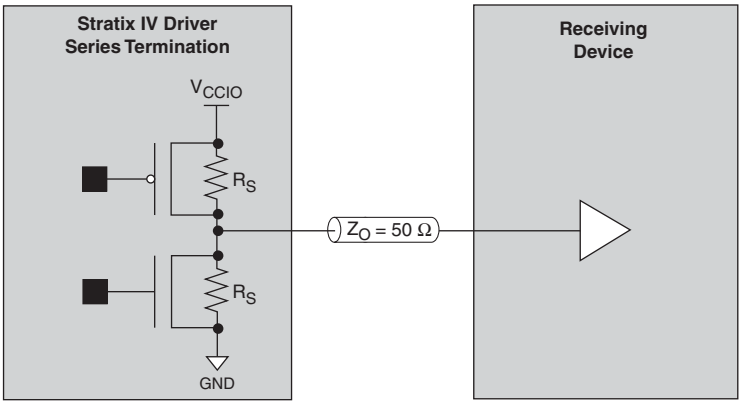
- The RUP pin is connected to V_{CCIO} through an external 50-Ω ±1% resistor.
- The RDN pin is connected to GND through an external 50-Ω ±1% resistor.

On-Chip Series (R_S) Termination Without Calibration

Stratix IV devices support driver-impedance matching to provide the I/O driver with controlled output impedance that closely matches the impedance of the transmission line. As a result, you can significantly reduce reflections. Stratix IV devices support on-chip series termination for single-ended I/O standards (Figure 6–18).

The R_S shown in Figure 6–18 is the intrinsic impedance of the output transistors. Typical R_S values are 25 Ω and 50 Ω. When you select matching impedance, current strength is no longer selectable.

Figure 6–18. On-Chip Series Termination Without Calibration



To use on-chip termination for the SSTL Class I standard, you must select the **50-Ω on-chip series termination** setting, thus eliminating the external 25-Ω R_S (to match the 50-Ω transmission line). For the SSTL Class II standard, you must select the **25-Ω on-chip series termination** setting (to match the 50-Ω transmission line and the near-end external 50-Ω pull-up to V_{TT}).

On-Chip Series Termination with Calibration

Stratix IV devices support on-chip series termination with calibration in all banks. The on-chip series termination calibration circuit compares the total impedance of the I/O buffer to the external 25-Ω ±1% or 50-Ω ±1% resistors connected to the RUP and RDN pins and dynamically enables or disables the transistors until they match.

The R_S shown in Figure 6–19 is the intrinsic impedance of the transistors. Calibration occurs at the end of device configuration. When the calibration circuit finds the correct impedance, it powers down and stops changing the characteristics of the drivers.

Figure 6–19. On-Chip Series Termination with Calibration

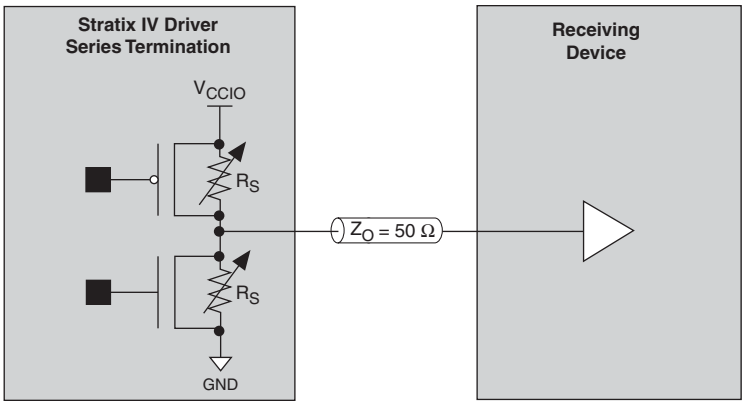


Table 6–6 lists the I/O standards that support on-chip series termination with and without calibration.

Table 6–6. Selectable I/O Standards for On-Chip Series Termination with and Without Calibration (Part 1 of 2)

I/O Standard	On-Chip Series Termination Setting	
	Row I/O (Ω)	Column I/O (Ω)
3.3-V LVTTL/LVCMOS	50	50
	25	25
2.5-V LVCMOS	50	50
	25	25
1.8-V LVCMOS	50	50
	25	25
1.5-V LVCMOS	50	50
		25
1.2-V LVCMOS	50	50
		25
SSTL-2 Class I	50	50
SSTL-2 Class II	25	25
SSTL-18 Class I	50	50
SSTL-18 Class II	25	25

Table 6–6. Selectable I/O Standards for On-Chip Series Termination with and Without Calibration (Part 2 of 2)

I/O Standard	On-Chip Series Termination Setting	
	Row I/O (Ω)	Column I/O (Ω)
SSTL-15 Class I	50	50
SSTL-15 Class II	—	25
HSTL-18 Class I	50	50
HSTL-18 Class II	25	25
HSTL-15 Class I	50	50
HSTL-15 Class II	—	25
HSTL-12 Class I	50	50
HSTL-12 Class II	—	25

Left-Shift Series Termination Control

Stratix IV devices support left-shift series termination control. You can use left-shift series termination control to get the calibrated OCT R_S with half of the impedance value of the external reference resistors connected to the RUP and RDN pins. This feature is useful in applications that require both 25-Ω and 50-Ω calibrated OCT R_S at the same V_{CCIO}. For example, if your application requires 25-Ω and 50-Ω calibrated OCT R_S for SSTL-2 Class I and Class II I/O standards, you only need one OCT calibration block with 50-Ω external reference resistors.

You can enable the left-shift series termination control feature in the ALTIOBUF megafunction in the Quartus II software. The Quartus II software only allows left-shift series termination control for 25-Ω calibrated OCT R_S with 50-Ω external reference resistors connected to the RUP and RDN pins. You can only use left-shift series termination control for the I/O standards that support 25-Ω calibrated OCT R_S .

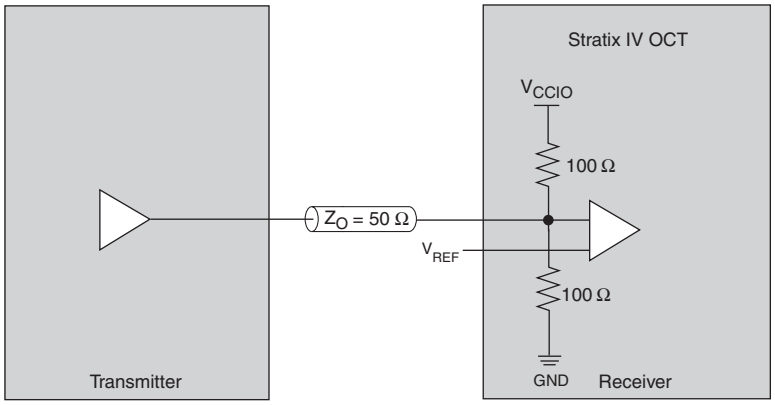
This feature is automatically enabled if you are using a bidirectional I/O with 25-Ω calibrated OCT R_S and 50-Ω parallel OCT.

For more information about how to enable the left-shift series termination feature in the ALTIOBUF megafunction, refer to the *I/O Buffer (ALTIOBUF) Megafunction User Guide*.

On-Chip Parallel Termination with Calibration

Stratix IV devices support on-chip parallel termination with calibration in all banks. On-chip parallel termination with calibration is only supported for input configuration of input and bidirectional pins. Output pin configurations do not support on-chip parallel termination with calibration. Figure 6–20 shows on-chip parallel termination with calibration. When you use parallel OCT, the V_{CCIO} of the bank must match the I/O standard of the pin where the parallel OCT is enabled.

Figure 6–20. On-Chip Parallel Termination with Calibration



The on-chip parallel termination calibration circuit compares the total impedance of the I/O buffer to the external 50-Ω ±1% resistors connected to the RUP and RDN pins and dynamically enables or disables the transistors until they match. Calibration occurs at the end of device configuration. When the calibration circuit finds the correct impedance, it powers down and stops changing the characteristics of the drivers. Table 6–7 lists the I/O standards that support on-chip parallel termination with calibration.

Table 6–7. Selectable I/O Standards with On-Chip Parallel Termination with Calibration

I/O Standard	On-Chip Parallel Termination Setting (Column I/O) (Ω)	On-Chip Parallel Termination Setting (Row I/O) (Ω)
SSTL-2 Class I, II	50	50
SSTL-18 Class I, II	50	50
SSTL-15 Class I, II	50	50
HSTL-18 Class I, II	50	50
HSTL-15 Class I, II	50	50
HSTL-12 Class I, II	50	50
Differential SSTL-2 Class I, II	50	50
Differential SSTL-18 Class I, II	50	50
Differential SSTL-15 Class I, II	50	50
Differential HSTL-18 Class I, II	50	50
Differential HSTL-15 Class I, II	50	50
Differential HSTL-12 Class I, II	50	50

Expanded On-Chip Series Termination with Calibration

OCT calibration circuits always adjust OCT R_S to match the external resistors connected to the RUP and RDN pin; however, it is possible to achieve OCT R_S values other than the 25-Ω and 50-Ω resistors. Theoretically, if you need a different OCT R_S value, you can change the resistance connected to the RUP and RDN pins accordingly. Practically, the OCT R_S range that Stratix IV devices support is limited because of output buffer size and granularity limitations.

The Quartus II software only allows discrete OCT R_S calibration settings of 25, 40, 50, and 60 Ω . You can select the closest discrete value of OCT R_S with calibration settings in the Quartus II software to your system to achieve the closest timing. For example, if you are using 20-Ω OCT R_S with calibration in your system, you can select the **25-Ω OCT R_S with calibration** setting in the Quartus II software to achieve the closest timing.

Table 6–8 lists expanded OCT R_S with calibration supported in Stratix IV devices. Use expanded on-chip series termination with calibration of SSTL and HSTL for impedance matching to improve signal integrity but do not use it to meet the JEDEC standard.

Table 6–8. Selectable I/O Standards with Expanded On-Chip Series Termination with Calibration Range

I/O Standard	Expanded OCT R_S Range	
	Row I/O (Ω)	Column I/O (Ω)
3.3-V LVTTL/LVCMOS	20–60	20–60
2.5-V LVTTL/LVCMOS	20–60	20–60
1.8-V LVTTL/LVCMOS	20–60	20–60
1.5-V LVTTL/LVCMOS	40–60	20–60
1.2-V LVTTL/LVCMOS	40–60	20–60
SSTL-2	20–60	20–60
SSTL-18	20–60	20–60
SSTL-15	40–60	20–60
HSTL-18	20–60	20–60
HSTL-15	40–60	20–60
HSTL-12	40–60	20–60

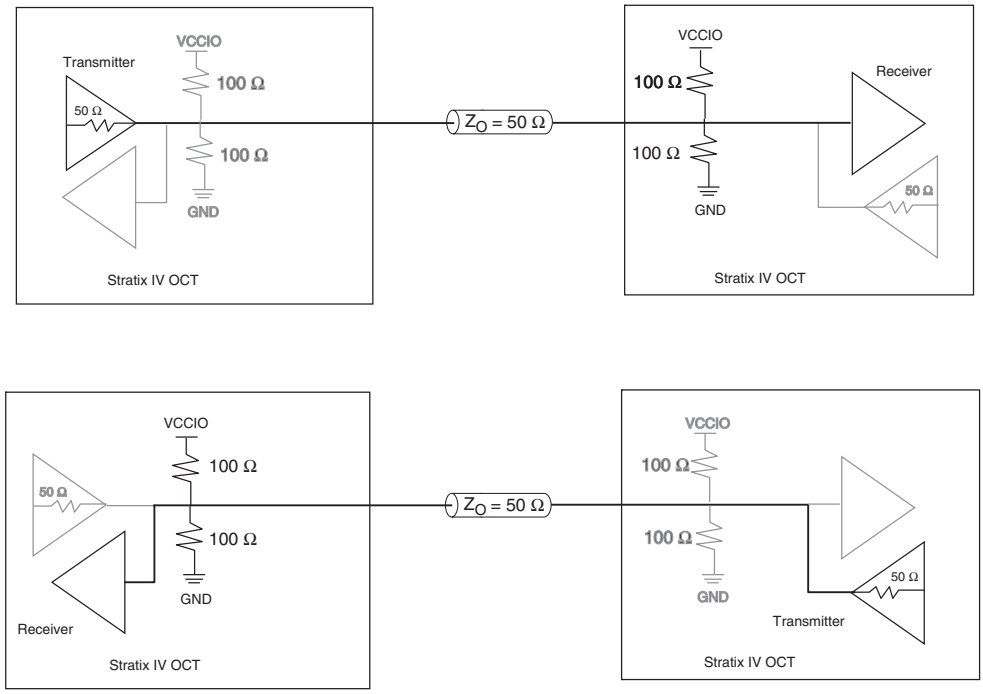
Dynamic On-Chip Termination

Stratix IV devices support on and off dynamic termination, both series and parallel, for a bidirectional I/O in all I/O banks. Figure 6–21 shows the termination schemes supported in Stratix IV devices. Dynamic parallel termination is enabled only when the bidirectional I/O acts as a receiver and is disabled when it acts as a driver. Similarly, dynamic series termination is enabled only when the bidirectional I/O acts as a driver and is disabled when it acts as a receiver. This feature is useful for terminating any high-performance bidirectional path because signal integrity is optimized depending on the direction of the data.

Using dynamic OCT helps save power because device termination is internal instead of external. Termination only switches on during input operation, thus drawing less static power.

When using calibrated input parallel and calibrated output series termination on bidirectional pins, they must use the same termination value because each I/O pin can only reference one OCT calibration block. The only exception is when using 50 Ω parallel OCT and 25 Ω series OCT using the left shift series termination control. For example, you cannot use calibrated 50 Ω parallel OCT on the input buffer of a bidirectional pin and calibrated 40 Ω series OCT on the output buffer because these would require two separate calibration blocks with different RUP and RDN resistor values.

Figure 6–21. Dynamic Parallel OCT in Stratix IV Devices

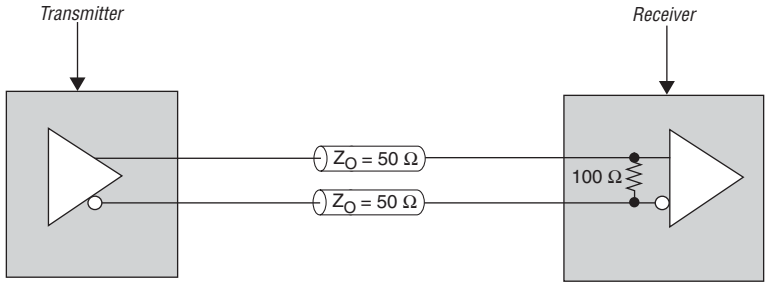


For more information about tolerance specifications for OCT with calibration, refer to the *DC and Switching Characteristics for Stratix IV Devices* chapter.

LVDS Input OCT (R_D)

Stratix IV devices support OCT for differential LVDS input buffers with a nominal resistance value of 100 Ω, as shown in Figure 6–22. Differential OCT R_D can be enabled in row I/O banks when both the V_{CCIO} and V_{CCPD} is set to **2.5 V**. Column I/O banks do not support OCT R_D. Dedicated clock input pairs `CLK[1,3,8,10][p,n]`, `PLL_L[1,4]_CLK[p,n]`, and `PLL_R[1,4]_CLK[p,n]` on the row I/O banks of Stratix IV devices do not support R_D termination.

Figure 6–22. Differential Input OCT



For more information about differential on-chip termination, refer to the *High-Speed Differential I/O Interfaces and DPA in Stratix IV Devices* chapter.

Summary of OCT Assignments

Table 6–9 lists the OCT assignments for the Quartus II software version 9.1 and later.

Table 6–9. Summary of OCT Assignments in the Quartus II Software

Assignment Name	Value	Applies To
Input Termination	Parallel 50 Ω with calibration	Input buffers for single-ended and differential HSTL/SSTL standards
	Differential	Input buffers for LVDS receivers on row I/O banks (1)
Output Termination	Series 25 Ω without calibration	Output buffers for single-ended LVTTL/LVCMOS and HSTL/SSTL standards as well as differential HSTL/SSTL standards
	Series 50 Ω without calibration	
	Series 25 Ω with calibration	
	Series 40 Ω with calibration	
	Series 50 Ω with calibration	
	Series 60 Ω with calibration	

Note to Table 6–9:

(1) You can enable differential OCT R_D in row I/O banks when both V_{CCIO} and V_{CCPD} are set to **2.5 V**.

OCT Calibration

Stratix IV devices support calibrated on-chip series termination (R_S) and calibrated on-chip parallel termination (R_T) on all I/O pins. You can calibrate the device's I/O bank with any of the OCT calibration blocks available in the device provided the V_{CCIO} of the I/O bank with the pins using calibrated OCT matches the V_{CCIO} of the I/O bank with the calibration block and its associated RUP and RDN pins.

OCT Calibration Block Location

Table 6–10 and Table 6–11 list the location of OCT calibration blocks in Stratix IV devices. For both tables, the following legend applies:

- "Y" indicates I/O banks with OCT calibration block
- "N" indicates I/O banks without OCT calibration block
- "—" indicates I/O banks that are not available in the device

Table 6–10 and Table 6–11 do not show transceiver banks and transceiver calibration blocks.

Table 6–10 lists the OCT calibration blocks in Banks 1A through 4C.

Table 6–10. OCT Calibration Block Counts and Placement in Stratix IV Devices (1A through 4C) (Part 1 of 2)

Device	Pin	Number of OCT Blocks	Bank											
			1A	1B	1C	2A	2B	2C	3A	3B	3C	4A	4B	4C
EP4SE230	780	8	Y	—	N	Y	—	N	Y	—	N	Y	—	N
EP4SE360	780	8	Y	—	N	Y	—	N	Y	—	N	Y	—	N
	1152	8	Y	—	N	Y	—	N	Y	N	N	Y	N	N
EP4SE530	1152	8	Y	—	N	Y	—	N	Y	N	N	Y	N	N
	1517	10	Y	N	N	Y	N	N	Y	N	Y	Y	N	N
	1760	10	Y	N	N	Y	N	N	Y	N	Y	Y	N	N
EP4SE820	1152	8	Y	—	N	Y	—	N	Y	N	N	Y	N	N
	1517	10	Y	N	N	Y	N	N	Y	N	Y	Y	N	N
	1760	10	Y	N	N	Y	N	N	Y	N	Y	Y	N	N
EP4SGX70	780	8	Y	—	N	Y	—	N	Y	—	N	Y	—	N
EP4SGX110	780	8	Y	—	N	Y	—	N	Y	—	N	Y	—	N
	1152	8	Y	—	N	—	—	—	Y	—	N	Y	—	N
EP4SGX180	780	8	Y	—	N	Y	—	N	Y	—	N	Y	—	N
	1152	8	Y	—	N	—	—	—	Y	N	N	Y	N	N
	1517	8	Y	—	N	Y	—	N	Y	N	N	Y	N	N
EP4SGX230	780	8	Y	—	N	Y	—	N	Y	—	N	Y	—	N
	1152	8	Y	—	N	—	—	—	Y	N	N	Y	N	N
	1517	8	Y	—	N	Y	—	N	Y	N	N	Y	N	N

Table 6–10. OCT Calibration Block Counts and Placement in Stratix IV Devices (1A through 4C) (Part 2 of 2)

Device	Pin	Number of OCT Blocks	Bank											
			1A	1B	1C	2A	2B	2C	3A	3B	3C	4A	4B	4C
EP4SGX290	780	8	—	—	—	—	—	—	Y	—	N	Y	—	N
	1152	8	Y	—	N	—	—	—	Y	N	N	Y	N	N
	1517	8	Y	—	N	Y	—	N	Y	N	N	Y	N	N
	1760	8	Y	—	N	Y	—	N	Y	N	N	Y	N	N
	1932	10	Y	N	N	Y	—	N	Y	N	Y	Y	N	N
EP4SGX360	780	8	—	—	—	—	—	—	Y	—	N	Y	—	N
	1152	8	Y	—	N	—	—	—	Y	N	N	Y	N	N
	1517	8	Y	—	N	Y	—	N	Y	N	N	Y	N	N
	1760	8	Y	—	N	Y	—	N	Y	N	N	Y	N	N
	1932	10	Y	N	N	Y	—	N	Y	N	Y	Y	N	N
EP4SGX530	1152	8	Y	—	N	—	—	—	Y	N	Y	Y	N	N
	1517	10	Y	—	N	Y	—	N	Y	N	Y	Y	N	N
	1760	10	Y	—	N	Y	—	N	Y	N	Y	Y	N	N
	1932	10	Y	—	N	Y	N	N	Y	N	Y	Y	N	N
EP4S40G2	1517	8	Y	—	N	Y	—	N	Y	N	N	Y	N	N
EP4S40G5	1517	10	Y	—	N	Y	—	N	Y	N	Y	Y	N	N
EP4S100G2	1517	8	Y	—	N	Y	—	N	Y	N	N	Y	N	N
EP4S100G3	1932	10	Y	—	N	Y	N	N	Y	N	Y	Y	N	N
EP4S100G4	1932	10	Y	—	N	Y	N	N	Y	N	Y	Y	N	N
EP4S100G5	1517	10	Y	—	N	Y	—	N	Y	N	Y	Y	N	N
	1932	10	Y	—	N	Y	N	N	Y	N	Y	Y	N	N

Table 6–11 lists the OCT calibration blocks in Banks 5A through 8C.

Table 6–11. OCT Calibration Block Counts and Placement in Stratix IV Devices (5A through 8C) (Part 1 of 2)

Device	Pin	Number of OCT Blocks	Bank											
			5A	5B	5C	6A	6B	6C	7A	7B	7C	8A	8B	8C
EP4SE230	780	8	Y	—	N	Y	—	N	Y	—	N	Y	—	N
EP4SE360	780	8	Y	—	N	Y	—	N	Y	—	N	Y	—	N
	1152	8	Y	—	N	Y	—	N	Y	N	N	Y	N	N
EP4SE530	1152	8	Y	—	N	Y	—	N	Y	N	N	Y	N	N
	1517	10	Y	N	N	Y	N	N	Y	N	N	Y	N	Y
	1760	10	Y	N	N	Y	N	N	Y	N	N	Y	N	Y
EP4SE820	1152	8	Y	—	N	Y	—	N	Y	N	N	Y	N	N
	1517	10	Y	N	N	Y	N	N	Y	N	N	Y	N	Y
	1760	10	Y	N	N	Y	N	N	Y	N	N	Y	N	Y
EP4SGX70	780	8	—	—	—	—	—	—	Y	—	N	Y	—	N

Table 6–11. OCT Calibration Block Counts and Placement in Stratix IV Devices (5A through 8C) (Part 2 of 2)

Device	Pin	Number of OCT Blocks	Bank											
			5A	5B	5C	6A	6B	6C	7A	7B	7C	8A	8B	8C
EP4SGX110	780	8	—	—	—	—	—	—	Y	—	N	Y	—	N
	1152	8	—	—	—	Y	—	N	Y	—	N	Y	—	N
EP4SGX180	780	8	—	—	—	—	—	—	Y	—	N	Y	—	N
	1152	8	—	—	—	Y	—	N	Y	N	N	Y	Y	N
	1517	8	Y	—	N	Y	—	N	Y	N	N	Y	N	N
EP4SGX230	780	8	—	—	—	—	—	—	Y	—	N	Y	—	N
	1152	8	—	—	—	Y	—	N	Y	N	N	Y	Y	N
	1517	8	Y	—	N	Y	—	N	Y	N	N	Y	N	N
EP4SGX290	780	8	—	—	—	—	—	—	Y	—	N	Y	—	N
	1152	8	—	—	—	Y	—	N	Y	N	N	Y	N	N
	1517	8	Y	—	N	Y	—	N	Y	N	N	Y	N	N
	1760	8	Y	—	N	Y	—	N	Y	N	N	Y	N	N
	1932	10	Y	—	N	Y	N	N	Y	N	N	Y	N	Y
EP4SGX360	780	8	—	—	—	—	—	—	Y	—	N	Y	—	N
	1152	8	—	—	—	Y	—	N	Y	N	N	Y	N	N
	1517	8	Y	—	N	Y	—	N	Y	N	N	Y	N	N
	1760	8	Y	—	N	Y	—	N	Y	N	N	Y	N	N
	1932	10	Y	—	N	Y	N	N	Y	N	N	Y	N	Y
EP4SGX530	1152	8	—	—	—	Y	—	N	Y	N	N	Y	N	Y
	1517	10	Y	—	N	Y	—	N	Y	N	N	Y	N	Y
	1760	10	Y	—	N	Y	—	N	Y	N	N	Y	N	Y
	1932	10	Y	N	N	Y	—	N	Y	N	N	Y	N	Y
EP4S40G2	1517	8	Y	—	N	Y	—	N	Y	N	N	Y	N	N
EP4S40G5	1517	10	Y	—	N	Y	—	N	Y	N	N	Y	N	Y
EP4S100G2	1517	8	Y	—	N	Y	—	N	Y	N	N	Y	N	N
EP4S100G3	1932	10	Y	N	N	Y	—	N	Y	N	N	Y	N	Y
EP4S100G4	1932	10	Y	N	N	Y	—	N	Y	N	N	Y	N	Y
EP4S100G5	1517	10	Y	—	N	Y	—	N	Y	N	N	Y	N	Y
	1932	10	Y	N	N	Y	—	N	Y	N	N	Y	N	Y

Sharing an OCT Calibration Block on Multiple I/O Banks

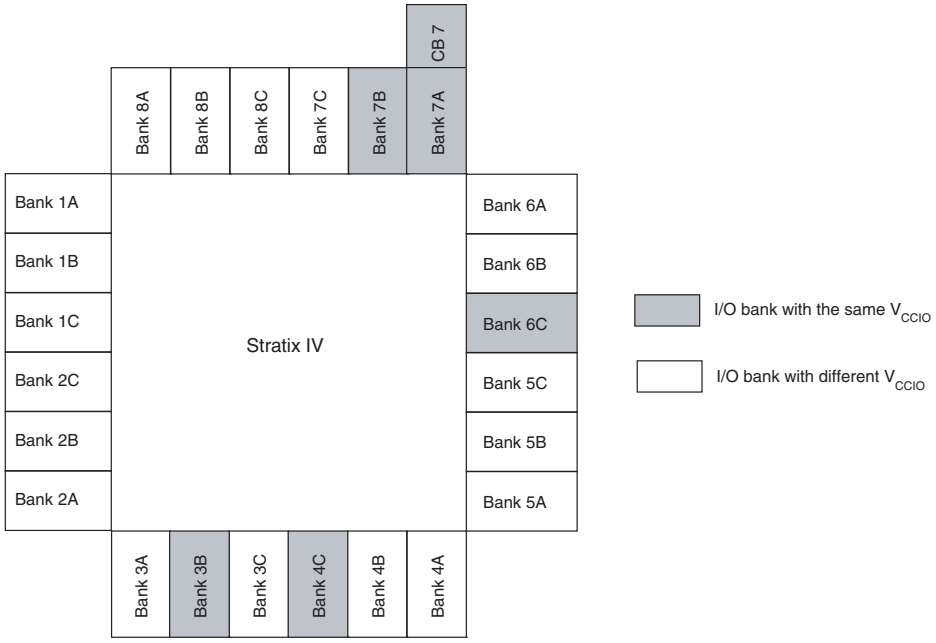
An OCT calibration block has the same V_{CCIO} as the I/O bank that contains the block. OCT R_S calibration is supported on all I/O banks with different V_{CCIO} voltage standards, up to the number of available OCT calibration blocks. You can configure the I/O banks to receive calibration codes from any OCT calibration block with the same V_{CCIO}. All I/O banks with the same V_{CCIO} can share one OCT calibration block, even if that particular I/O bank has an OCT calibration block.

For example, Figure 6–23 shows a group of I/O banks that has the same V_{CCIO} voltage. If a group of I/O banks has the same V_{CCIO} voltage, you can use one OCT calibration block to calibrate the group of I/O banks placed around the periphery. Because 3B, 4C, 6C, and 7B have the same V_{CCIO} as bank 7A, you can calibrate all four I/O banks (3B, 4C, 6C, and 7B) with the OCT calibration block (CB7) located in bank 7A. You can enable this by serially shifting out OCT R_S calibration codes from the OCT calibration block located in bank 7A to the I/O banks located around the periphery.

I/O banks that do not contain calibration blocks share calibration blocks with I/O banks that do contain calibration blocks.

Figure 6–23 is a top view of the silicon die that corresponds to a reverse view for flip chip packages. It is a graphical representation only. This figure does not show transceiver banks and transceiver calibration blocks.

Figure 6–23. Example of Calibrating Multiple I/O Banks with One Shared OCT Calibration Block



OCT Calibration Block Modes of Operation

Stratix IV devices support OCT R_S and OCT R_T on all I/O banks. The calibration can occur in either power-up or user mode.

Power-Up Mode

In power-up mode, OCT calibration is automatically performed at power up. Calibration codes are shifted to selected I/O buffers before transitioning to user mode.

User Mode

In user mode, the OCTUSRCLK, ENAOCT, nCLRUSR, and ENASER[9..0] signals are used to calibrate and serially transfer calibration codes from each OCT calibration block to any I/O. Table 6–12 lists the user-controlled calibration block signal names and their descriptions.

Table 6–12. OCT Calibration Block Ports for User Control

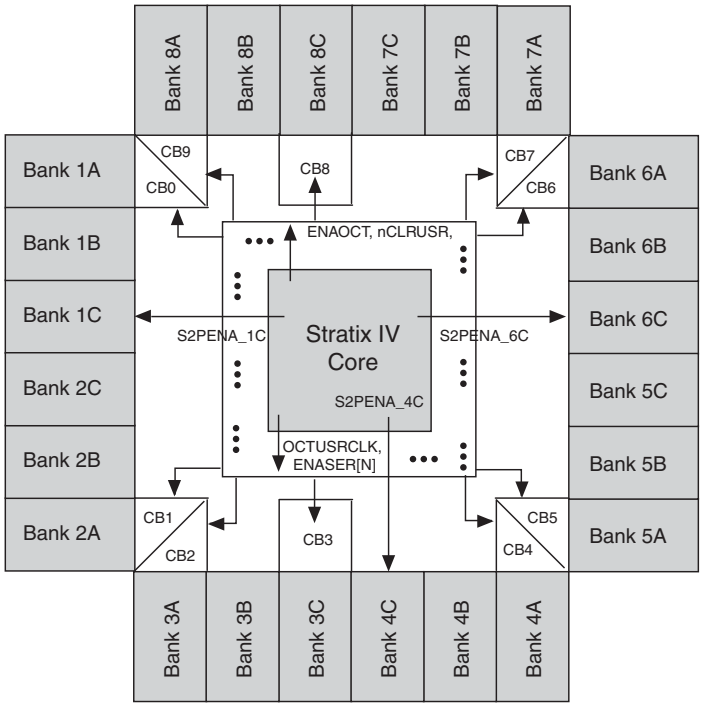
Signal Name	Description
OCTUSRCLK	Clock for OCT block.
ENAOCT	Enable OCT Termination (Generated by user IP).
ENASER[9..0]	When ENOCT = 0, each signal enables the OCT serializer for the corresponding OCT calibration block. When ENAOCT = 1, each signal enables OCT calibration for the corresponding OCT calibration block.
S2PENA_<*bank#*>	Serial-to-parallel load enable per I/O bank.
nCLRUSR	Clear user.

Figure 6–24 shows the flow of the user signal. When ENAOCT is 1, all OCT calibration blocks are in calibration mode; when ENAOCT is 0, all OCT calibration blocks are in serial data transfer mode. The OCTUSRCLK clock frequency must be 20 MHz or less.

You must generate all user signals on the rising edge of OCTUSRCLK.

Figure 6–24 does not show transceiver banks and transceiver calibration blocks.

Figure 6–24. Signals Used for User Mode Calibration



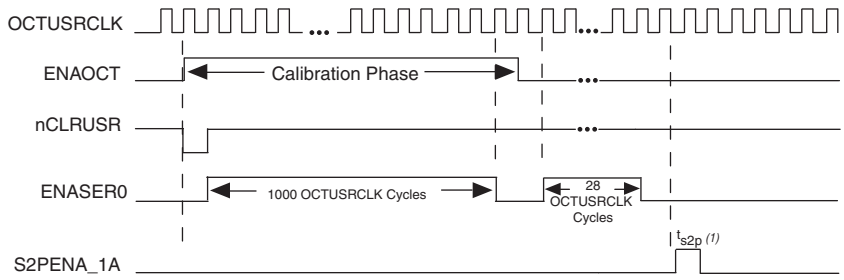
OCT Calibration

Figure 6–25 shows user mode signal-timing waveforms. To calibrate OCT block[N] (where N is a calibration block number), you must assert ENAOCT one cycle before asserting ENASER[N]. Also, nCLRUSR must be set to low for one OCTUSRCLK cycle before the ENASER[N] signal is asserted. Assert the ENASER[N] signals for 1000 OCTUSRCLK cycles to perform OCTRS and OCTRT calibration. You can de-assert ENAOCT one clock cycle after the last ENASER is de-asserted.

Serial Data Transfer

After you complete calibration, you must serially shift out the 28-bit OCT calibration codes (14-bit OCT R_S and 14-bit OCT R_T) from each OCT calibration block to the corresponding I/O buffers. Only one OCT calibration block can send out the codes at any time by asserting only one ENASER[N] signal at a time. After you de-assert ENAOCT, wait at least one OCTUSRCLK cycle to enable any ENASER[N] signal to begin serial transfer. To shift the 28-bit code from the OCT calibration block[N], you must assert ENASER[N] for exactly 28 OCTUSRCLK cycles. Between two consecutive asserted ENASER signals, there must be at least one OCTUSRCLK cycle gap. (Figure 6–25).

Figure 6–25. OCT User Mode Signal—Timing Waveform for One OCT Block



Note to Figure 6–25:

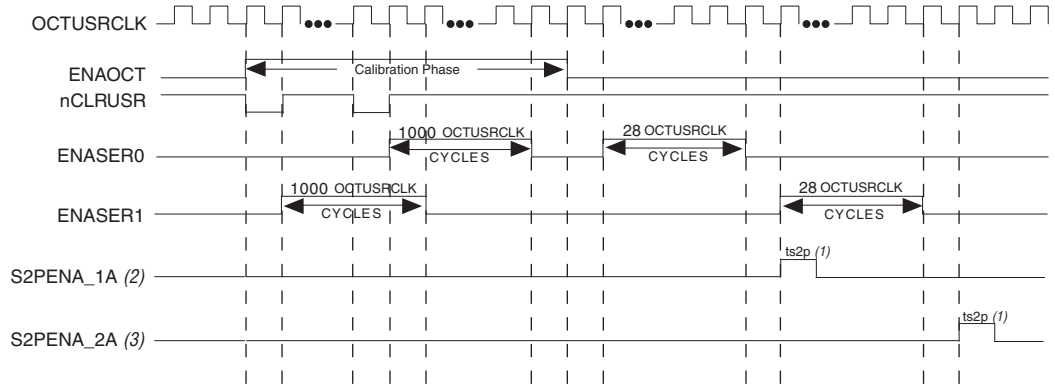
(1) $t_{s2p} \geq 25$ ns.

After calibrated codes are shifted in serially to each I/O bank, the calibrated codes must be converted from serial to parallel format before being used in the I/O buffers. Figure 6–25 shows the S2PENA signals that can be asserted at any time to update the calibration codes in each I/O bank. All I/O banks that received the codes from the same OCT calibration block can have S2PENA asserted at the same time, or at a different time, even while another OCT calibration block is calibrating and serially shifting codes. The S2PENA signal is asserted one OCTUSRCLK cycle after ENASER is de-asserted for at least 25 ns. You cannot use I/Os for transmitting or receiving data when their S2PENA is asserted for parallel codes transfer.

Example of Using Multiple OCT Calibration Blocks

Figure 6–26 shows a signal timing waveform for two OCT calibration blocks doing R_S and R_T calibration. Calibration blocks can start calibrating at different times by asserting the ENASER signals at different times. ENAOCT must remain asserted while any calibration is ongoing. You must set nCLRUSR low for one OCTUSRCLK cycle before each ENASER[N] signal is asserted. In Figure 6–26, when you set nCLRUSR to **0** for the second time to initialize OCT calibration block 0, this does not affect OCT calibration block 1, whose calibration is already in progress.

Figure 6–26. OCT User-Mode Signal Timing Waveform for Two OCT Blocks



Notes to Figure 6–26:

(1) ts2p ≥ 25 ns.
(2) S2PENA_1A is asserted in Bank 1A for calibration block 0.
(3) S2PENA_2A is asserted in Bank 2A for calibration block 1.

R_S Calibration

If only R_S calibration is used for an OCT calibration block, its corresponding ENASER signal only requires to be asserted for 240 OCTUSRCLK cycles.

You must assert the ENASER signal for 28 OCTUSRCLK cycles for serial transfer.

Termination Schemes for I/O Standards

The following sections describe the different termination schemes for the I/O standards used in Stratix IV devices.

Single-Ended I/O Standards Termination

Voltage-referenced I/O standards require both an input reference voltage, V_{REF}, and a termination voltage, V_{TT}. The reference voltage of the receiving device tracks the termination voltage of the transmitting device.

Figure 6–27 and Figure 6–28 show the details of SSTL and HSTL I/O termination on Stratix IV devices.

In Stratix IV devices, you cannot use series and parallel OCT simultaneously. For more information, refer to "Dynamic On-Chip Termination" on page 6–29.

Figure 6–27. SSTL I/O Standard Termination

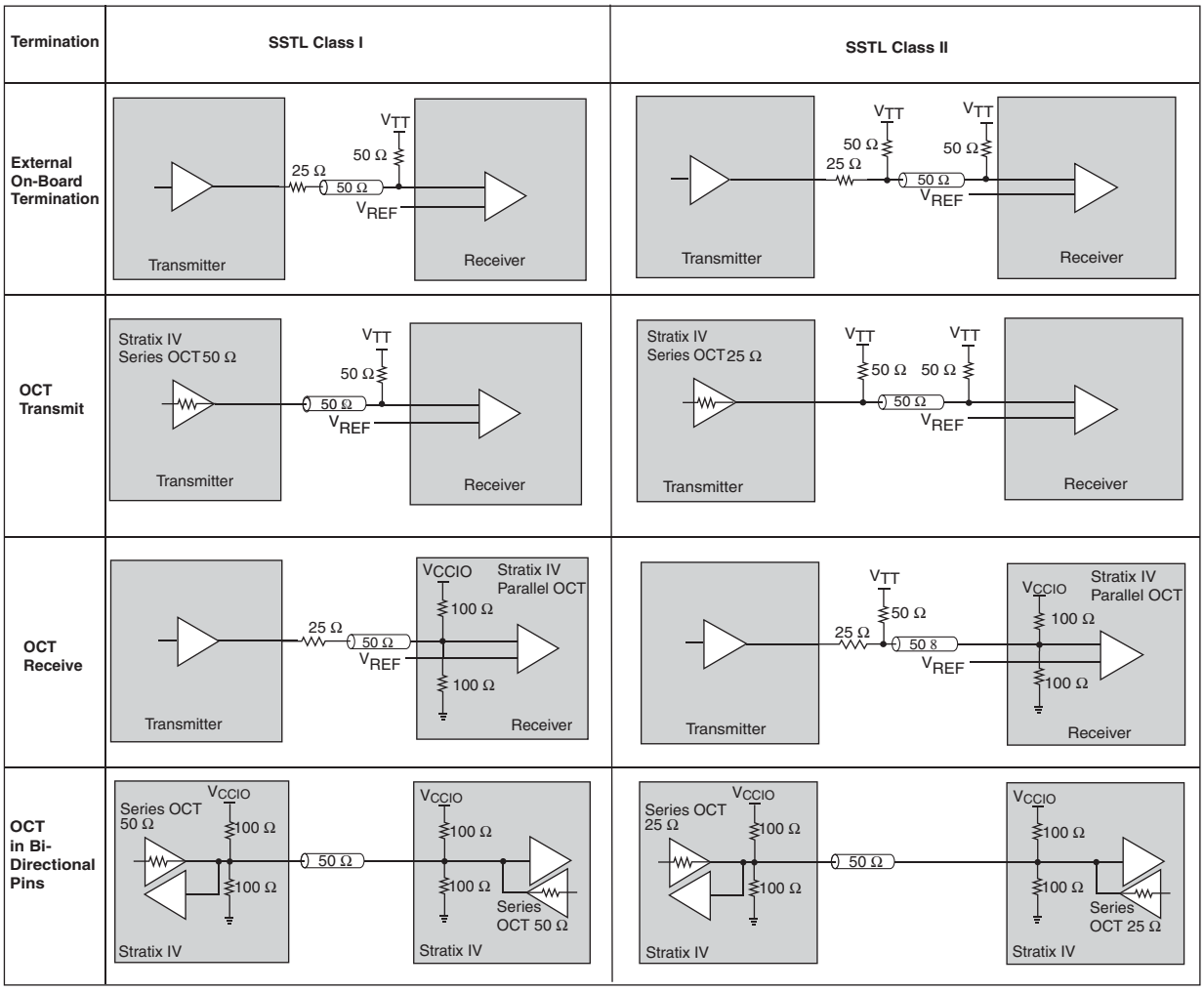
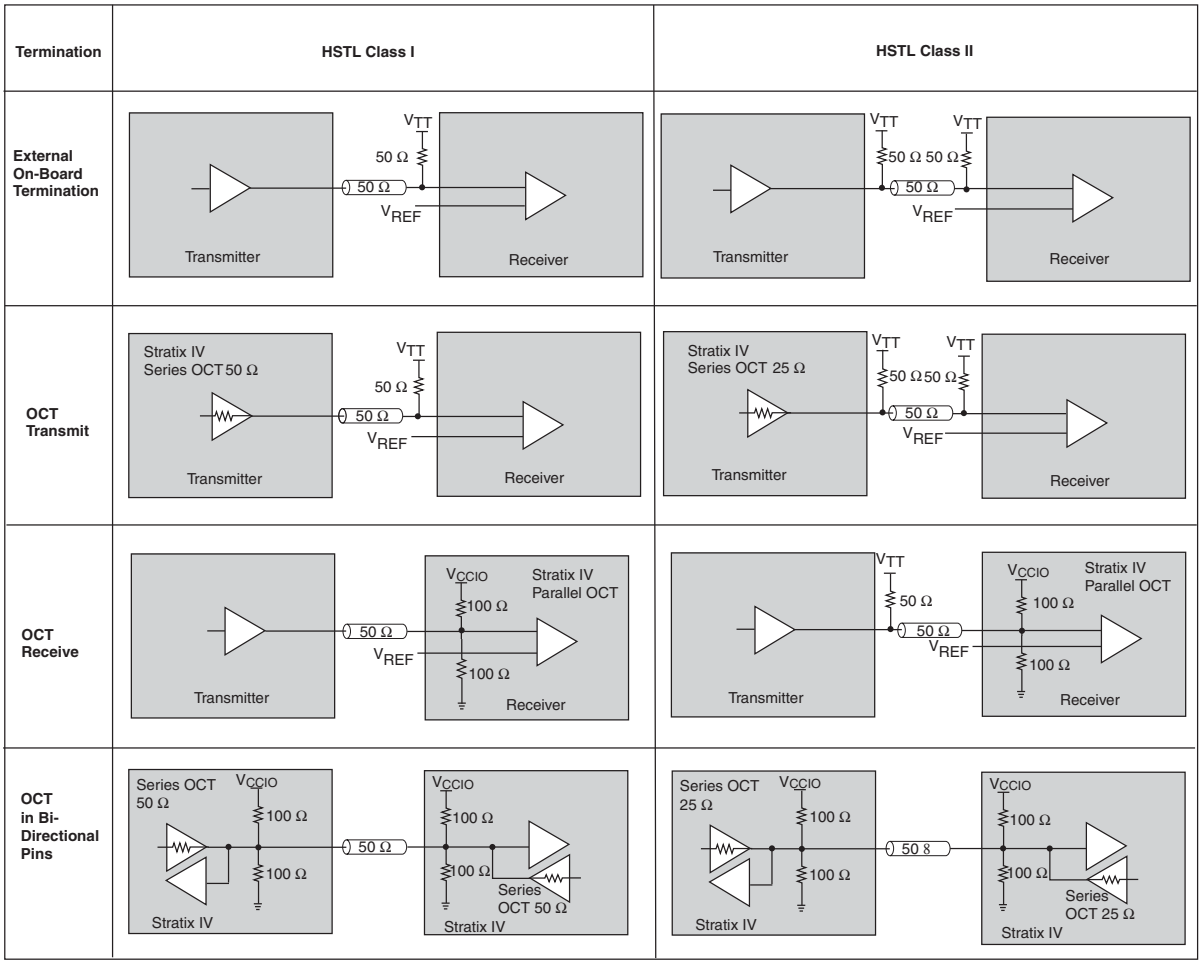


Figure 6–28. HSTL I/O Standard Termination



Differential I/O Standards Termination

Stratix IV devices support differential SSTL-18 and SSTL-2, differential HSTL-18, HSTL-15, HSTL-12, LVDS, LVPECL, RSDS, and mini-LVDS. Figure 6–29 through Figure 6–35 show the details of various differential I/O terminations on these devices.

Differential HSTL and SSTL outputs are not true differential outputs. They use two single-ended outputs with the second output programmed as inverted.

Figure 6–29. Differential SSTL I/O Standard Termination

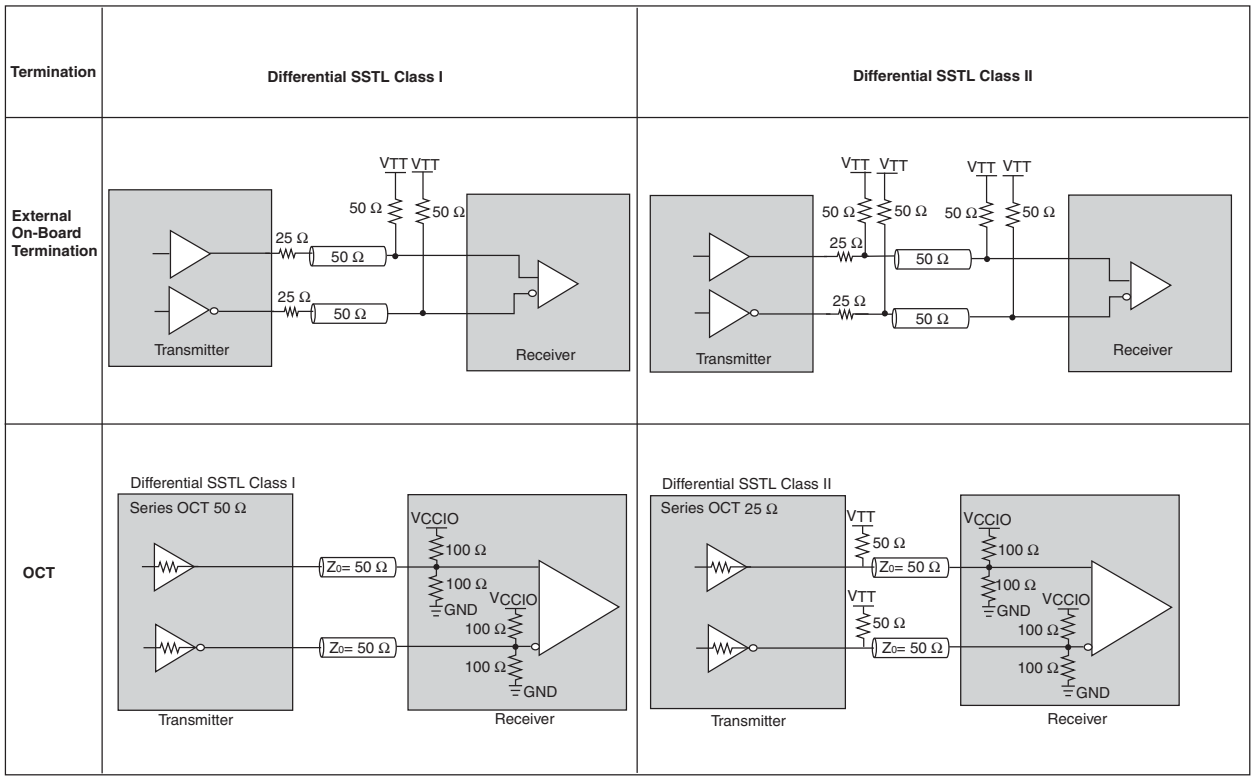
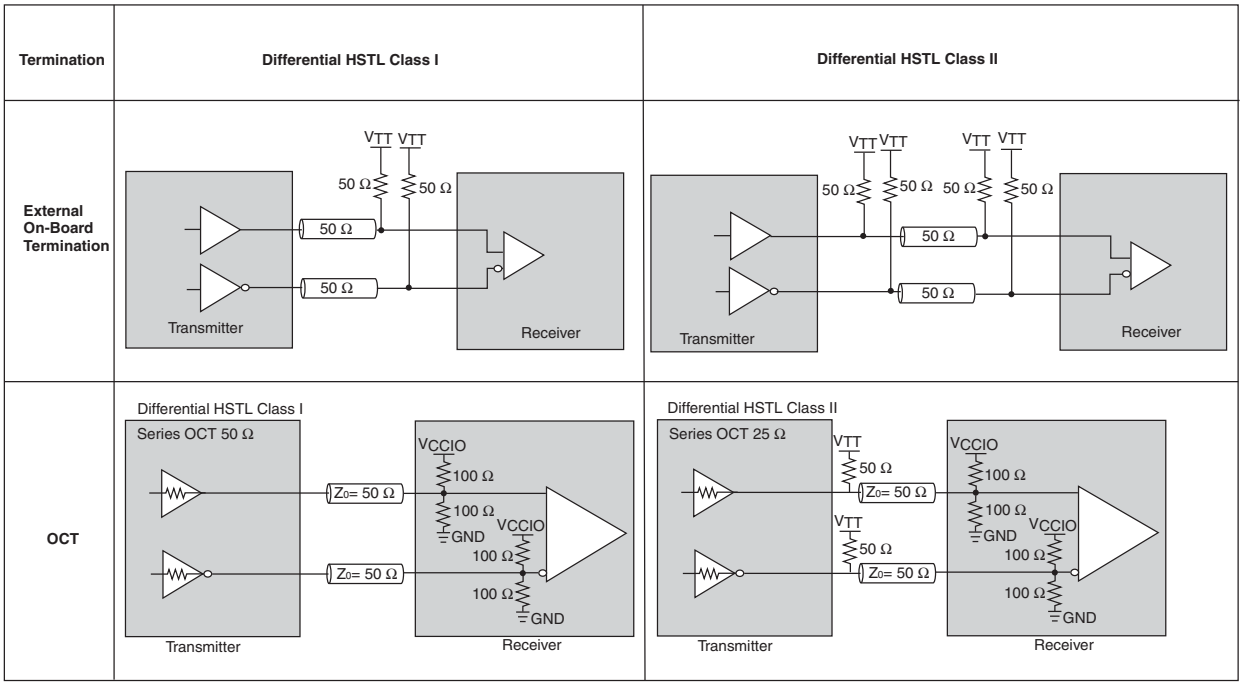


Figure 6–30. Differential HSTL I/O Standard Termination

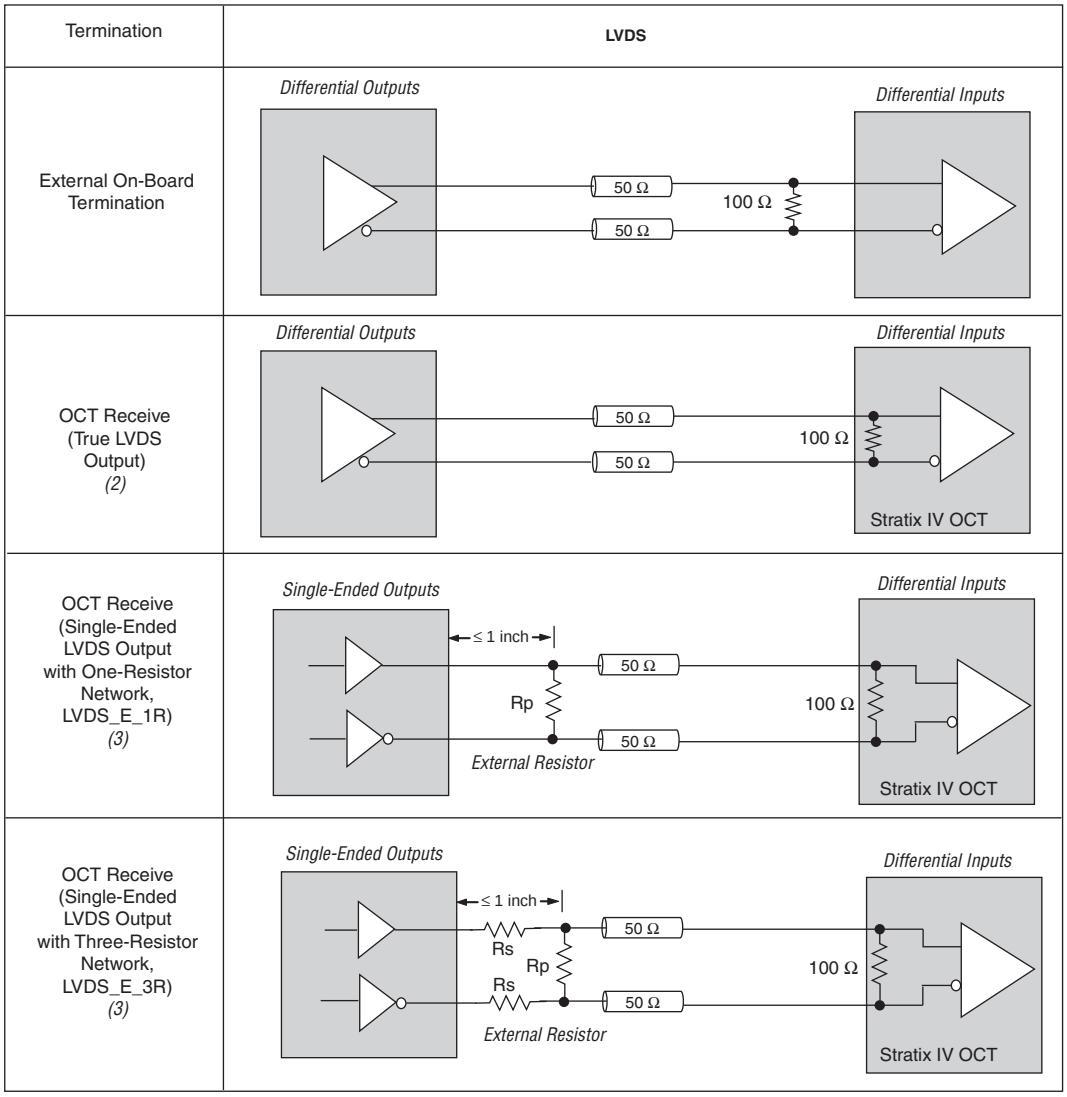


LVDS

The LVDS I/O standard is a differential high-speed, low-voltage swing, low-power, general-purpose I/O interface standard. In Stratix IV devices, the LVDS I/O standard requires a 2.5-V V_{CCIO} level. The LVDS input buffer requires 2.5-V V_{CCPD}. Use this standard in applications requiring high-bandwidth data transfer, such as backplane drivers and clock distribution. LVDS requires a 100-Ω termination resistor between the two signals at the input buffer. Stratix IV devices provide an optional 100-Ω differential termination resistor in the device using on-chip differential termination.

Figure 6–31 shows LVDS termination. The on-chip differential resistor is only available in the row I/O banks.

Figure 6–31. LVDS I/O Standard Termination *(1)*



Notes to Figure 6–31:

(1) For LVDS output with a three-resistor network, the R_S and R_P values are 120 and 170 Ω, respectively. For LVDS output with a one-resistor network, the R_P value is 120 Ω.

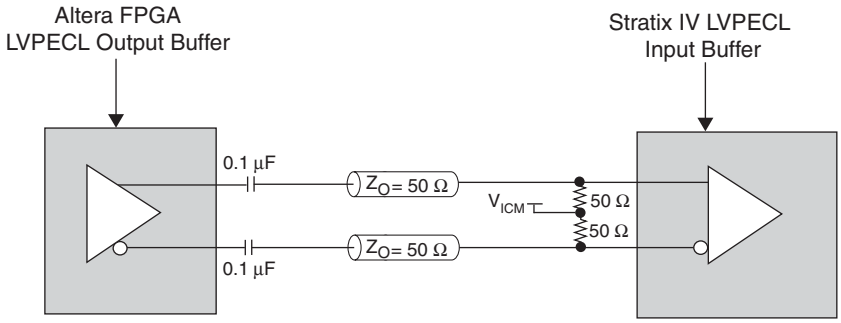
(2) Side I/O banks support true LVDS output buffers.

(3) Column and side I/O banks support LVDS_E_1R and LVDS_E_3R I/O standards using two single-ended output buffers.

Differential LVPECL

In Stratix IV devices, the LVPECL I/O standard is supported on input clock pins on column and row I/O banks. LVPECL output operation is not supported in Stratix IV devices. LVDS input buffers are used to support LVPECL input operation. AC coupling is required when the LVPECL common-mode voltage of the output buffer is higher than the LVPECL input common-mode voltage. Figure 6–32 shows the AC-coupled termination scheme. The 50-Ω resistors used at the receiver end are external to the device.

Figure 6–32. LVPECL AC-Coupled Termination *(1)*

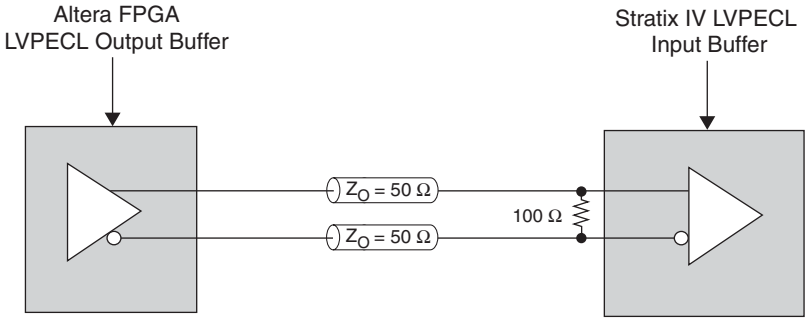


Note to Figure 6–32:

(1) The LVPECL AC-coupled termination is applicable only when you use an Altera FPGA LVPECL transmitter.

DC-coupled LVPECL is supported if the LVPECL output common mode voltage is within the Stratix IV LVPECL input buffer specification (Figure 6–33).

Figure 6–33. LVPECL DC-Coupled Termination *(1)*



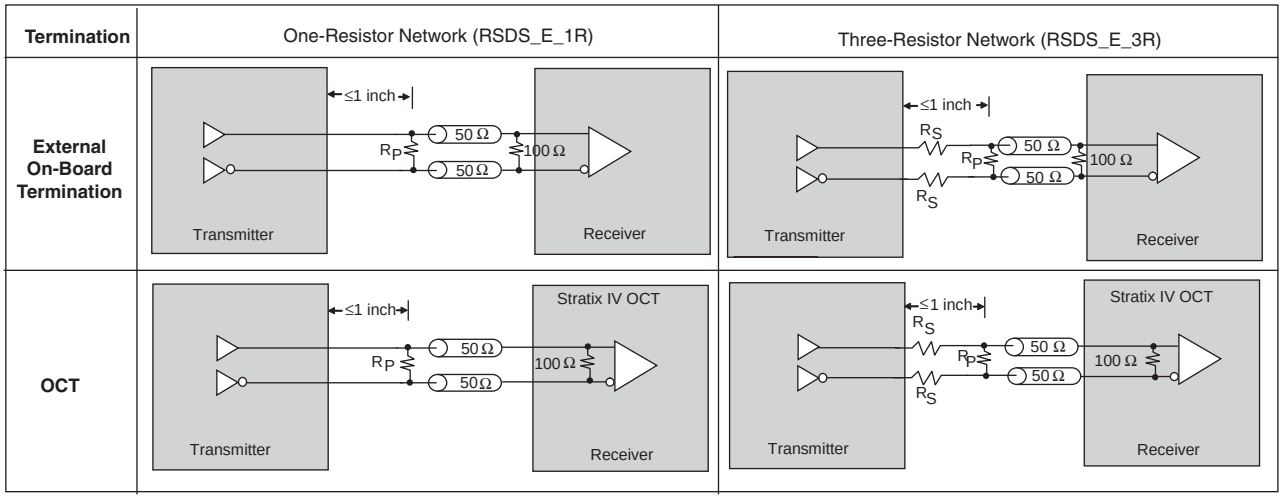
Note to Figure 6–33:

(1) The LVPECL DC-coupled termination is applicable only when you use an Altera FPGA LVPECL transmitter.

RSDS

Stratix IV devices support the RSDS output standard with data rates up to 230 Mbps using LVDS output buffer types. For transmitters, use two single-ended output buffers with the external one- or three-resistor networks in the column I/O bank, as shown in Figure 6–34. The one-resistor topology is for data rates up to 200 Mbps. The three-resistor topology is for data rates above 200 Mbps. The row I/O banks support RSDS output using true LVDS output buffers without an external resistor network.

Figure 6–34. RSDS I/O Standard Termination *(1)*



Note to Figure 6–34:

(1) The R_S and R_P values are pending characterization.

A resistor network is required to attenuate the LVDS output-voltage swing to meet RSDS specifications. You can modify the three-resistor network values to reduce power or improve noise margin. The resistor values chosen must satisfy Equation 6–1.

Equation 6–1.

$$\frac{R_s \times \frac{R_p}{2}}{R_s + \frac{R_p}{2}} = 50\Omega$$

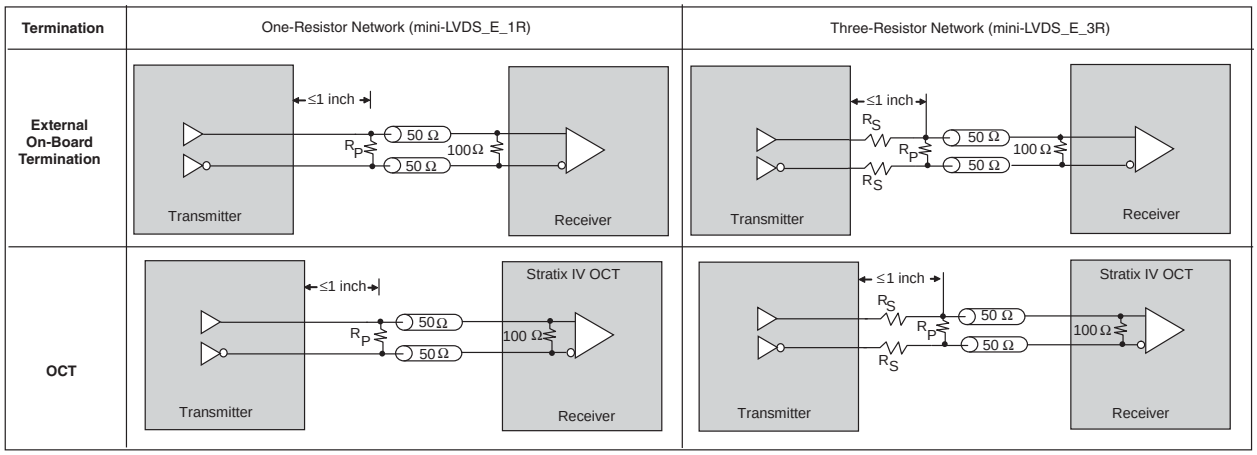
Altera recommends performing additional simulations using IBIS models to validate that custom resistor values meet the RSDS requirements.

For more information about the RSDS I/O standard, refer to the *RSDS Specification* from the National Semiconductor website at www.national.com.

Mini-LVDS

Stratix IV devices support the mini-LVDS output standard with data rates up to 340 Mbps using LVDS output buffer types. For transmitters, use two single-ended output buffers with external one- or three-resistor networks, as shown in Figure 6–35. The one-resistor topology is for data rates up to 200 Mbps. The three-resistor topology is for data rates above 200 Mbps. The row I/O banks support mini-LVDS output using true LVDS output buffers without an external resistor network.

Figure 6–35. Mini-LVDS I/O Standard Termination *(1)*



Note to Figure 6–35:

(1) The R_S and R_P values are pending characterization.

A resistor network is required to attenuate the LVDS output voltage swing to meet the mini-LVDS specifications. You can modify the three-resistor network values to reduce power or improve noise margin. The resistor values chosen must satisfy Equation 6–1 on page 6–45.

Altera recommends that you perform additional simulations using IBIS models to validate that custom resistor values meet the RSDS requirements.

For more information about the mini-LVDS I/O standard, see the *mini-LVDS Specification* from the Texas Instruments website at www.ti.com.

Design Considerations

Although Stratix IV devices feature various I/O capabilities for high-performance and high-speed system designs, there are several other design considerations that require your attention to ensure the success of your designs.

I/O Bank Restrictions

Each I/O bank can simultaneously support multiple I/O standards. The following sections provide guidelines for mixing non-voltage-referenced and voltage-referenced I/O standards in Stratix IV devices.

Non-Voltage-Referenced Standards

Each I/O bank of a Stratix IV device has its own VCCIO pins and supports only one V_{CCIO}, either 1.2, 1.5, 1.8, 2.5, or 3.0 V. An I/O bank can simultaneously support any number of input signals with different I/O standard assignments if it meets the V_{CCIO} and V_{CCPD} requirement, as shown in Table 6–2 on page 6–3.

For output signals, a single I/O bank supports non-voltage-referenced output signals that are driving at the same voltage as V_{CCIO}. Because an I/O bank can only have one V_{CCIO} value, it can only drive out that one value for non-voltage-referenced signals. For example, an I/O bank with a 2.5-V V_{CCIO} setting can support 2.5-V standard inputs and outputs as well as 3.0-V LVCMOS inputs (but not output or bidirectional pins).

Voltage-Referenced Standards

To accommodate voltage-referenced I/O standards, each Stratix IV device's I/O bank supports multiple VREF pins feeding a common V_{REF} bus. The number of available VREF pins increases as device density increases. If these pins are not used as VREF pins, they cannot be used as generic I/O pins and must be tied to V_{CCIO} or GND. Each bank can only have a single V_{CCIO} voltage level and a single V_{REF} voltage level at a given time.

An I/O bank featuring single-ended or differential standards can support voltage-referenced standards if all voltage-referenced standards use the same V_{REF} setting.

For performance reasons, voltage-referenced input standards use their own V_{CCPD} level as the power source. This feature allows you to place voltage-referenced input signals in an I/O bank with a V_{CCIO} of 2.5 V or below. For example, you can place HSTL-15 input pins in an I/O bank with 2.5-V V_{CCIO}. However, the voltage-referenced input with parallel OCT enabled requires the V_{CCIO} of the I/O bank to match the voltage of the input standard.

Voltage-referenced bidirectional and output signals must be the same as the I/O bank's V_{CCIO} voltage. For example, you can only place SSTL-2 output pins in an I/O bank with a 2.5-V V_{CCIO}.

Mixing Voltage-Referenced and Non-Voltage-Referenced Standards

An I/O bank can support both voltage-referenced and non-voltage-referenced pins by applying each of the rule sets individually. For example, an I/O bank can support SSTL-18 inputs and 1.8-V inputs and outputs with a 1.8-V V_{CCIO} and a 0.9-V V_{REF}. Similarly, an I/O bank can support 1.5-V standards, 1.8-V inputs (but not outputs), and HSTL and HSTL-15 I/O standards with a 1.5-V V_{CCIO} and 0.75-V V_{REF}.

Document Revision History

Table 6–13 lists the revision history for this chapter.

Table 6–13. Document Revision History (Part 1 of 2)

Date	Version	Changes
September 2012	3.4	■ Updated the "Programmable Slew Rate Control" section to close FB #68385. ■ Updated Figure 6–17 to close FB #57979.
December 2011	3.3	Updated Figure 6–2 and Figure 6–17.
February 2011	3.2	■ Updated the "Modular I/O Banks", "On-Chip Termination Support and I/O Termination Schemes", "Dynamic On-Chip Termination", and "Programmable Pull-Up Resistor" sections. ■ Updated Figure 6–17, Figure 6–32, and Figure 6–33. ■ Applied new template. ■ Minor text edits.
March 2010	3.1	■ Updated Table 6–2 and Table 6–5. ■ Updated Figure 6–18, Figure 6–19, Figure 6–27, Figure 6–28, and Figure 6–31. ■ Added the "Summary of OCT Assignments" section. ■ Added a note to the "Sharing an OCT Calibration Block on Multiple I/O Banks" section. ■ Updated the "OCT Calibration" section. ■ Minor text edits.
November 2009	3.0	■ Updated Table 6–2, Table 6–4, Table 6–6, Table 6–9, and Table 6–10. ■ Updated Figure 6–1, Figure 6–2, Figure 6–4, Figure 6–5, Figure 6–6, Figure 6–8, Figure 6–9, Figure 6–10, Figure 6–11, Figure 6–12, Figure 6–13, and Figure 6–31. ■ Added Table 6–8. ■ Added Figure 6–7, Figure 6–14, Figure 6–15, and Figure 6–16. ■ Added "Left-Shift Series Termination Control" and "Expanded On-Chip Series Termination with Calibration" sections. ■ Updated "MultiVolt I/O Interface", "RSDS", "Mini-LVDS", and "Non-Voltage-Referenced Standards" sections. ■ Deleted Figure 6-5: Number of I/Os in Each Bank in EP4SE290 and EP4SE360 in the 1517-Pin FineLine BGA Package. ■ Minor text edits.
June 2009	2.3	■ Added introductory sentences to improve search ability. ■ Removed the Conclusion section.
April 2009	2.2	■ Updated Figure 6–2. ■ Updated Table 6–8 and Table 6–9. ■ Deleted Figure 6-14.
March 2009	2.1	■ Updated Table 6–1, Table 6–2,Table 6–3, Table 6–4, Table 6–6, Table 6–8, and Table 6–9. ■ Updated Figure 6–2, Figure 6–7, Figure 6–8, Figure 6–9, Figure 6–10, Figure 6–11, and Figure 6–12. ■ Added Figure 6–14. ■ Removed Equation 6–2 and "Referenced Documents" section.

Table 6–13. Document Revision History (Part 2 of 2)

Date	Version	Changes
November 2008	2.0	■ Updated "Modular I/O Banks" on page 6–7. ■ Updated Figure 6–3 and Figure 6–21. ■ Made minor editorial changes.
May 2008	1.0	Initial release.