QDRII SRAM Controller MegaCore Function

May 2006, MegaCore Version 1.2.1 Errata Sheet

This document addresses known errata and documentation changes for the QDRII SRAM Controller MegaCore® function version 1.2.1.

Errata are design functional defects or errors. Errata may cause the QDRII SRAM Controller MegaCore function to deviate from published specifications.

Documentation changes include typos, errors, unclear descriptions, or omissions from current published specifications or product documents. These documentation changes or clarifications will be incorporated into an upcoming release of the QDRII SRAM Controller MegaCore function.

QDRII SRAM Controller MegaCore Function v1.2.1 Issues

Altera has identified the following issues that affect the QDRII SRAM Controller MegaCore function:

For the most up-to-date errata for this release, refer to the errata page on the Altera® website:

www.altera.com/literature/es/es_qdrii_sram_121.pdf

Quartus II Software Version 6.0

The QDRII SRAM Controller MegaCore function v1.2.1 is not compatible with the Quartus II software v6.0.

Affected Configurations

This issue affects all configurations.

Workaround

If you want to use the Quartus II software v6.0, upgrade to the QDRII SRAM Controller MegaCore function v1.3.0.

Solution Status

This issue will never be fixed.

Gate-Level Simulation Timing

The simulation delay models sent to the `cqn` pin in the Quartus® II software on Stratix® II devices are incorrect. This issue can result in an invalid capture of the data. The simulation delay should be similar to the ones on the `cq` pin.

Affected Configurations

This issue affects Stratix II devices only.

Workaround

Edit the gate-level netlist. Look for the `cqn` pin instantiation and copy the simulation timing parameters found on the `cq` (which tends to be close by).

Solution Status

This issue will be fixed in the Quartus II software v5.1 SP1.

IP Toolbench Allows Editing of Memory Devices

When you choose a memory device other than **Default** in the memory device list, all the following parameters are set for that specific device:

- Data width
- Address width
- Burst type

If you change any of these parameters, you no longer have the correct parameters for the chosen memory device, but instead have parameters for a custom memory device. However, IP Toolbench incorrectly indicates that you still have a specific device rather than a custom device, in the memory devices list.

Affected Configurations

This issue affects all noncustom configurations.

Design Impact

There is a design impact if you choose incompatible data width, address width, or burst type parameters for your chosen memory.

Workaround

If you edit any of the following parameters, choose **Default** in the memory device list:

- Data width
- Address width
- Burst type

Solution Status

This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

Multiple VHDL Support Files

The following Altera MegaCore functions generate the Altera VHDL support package (**altera_vhdl_support.vhd**):

- DDR or DDR2 SDRAM Controller MegaCore function
- QDRII SRAM Controller MegaCore function
- RLDRAM II Controller MegaCore function
- PCI Express MegaCore function

When you have a Quartus® II project that contains multiple MegaCore functions in separate directories, there are multiple instances of the **altera_vhdl_support.vhd** file. If the Quartus II compilation adds two or more separate copies of **altera_vhdl_support.vhd**, the compilation fails.

Affected Configurations

This issue affects all configurations.

Design Impact

There is no design impact.

Workaround

to avoid compilation failure, either generate all the project MegaCore functions in the Quartus II project directory, or ensure only one instance of the **altera_vhdl_support.vhd** file exists in your project.

Ignore the warning that IP Toolbench running outside of SOPC Builder generates when it overwrites an existing **altera_vhdl_support.vhd** file.

To ensure your project only includes one instance of the **altera_vhdl_support.vhd** file, follow these steps:

1. Choose **Add/Remove Files in Project** (Project menu).
2. Choose all instances of **altera_vhdl_support.vhd** except the first instance.
3. Click **Remove**.

Solution Status

This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

Constraints Errors With Companion Devices

When you change the device in your project or add a HardCopy II companion device to a Stratix® II project and you reopen the variation with IP Toolbench, the constraints editor sometimes does not show all previously set byte groups in the floorplan. The constraints editor only shows the constraints applied to byte groups that are valid for the current device.

Affected Configurations

This issue affects all configurations.

Design Impact

The design fails.

Workaround

Reassign the byte groups for the new device in the constraints editor.

Solution Status

This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

Supported Device Families

The QDRII SRAM Controller MegaCore function only supports Stratix and Stratix II series, and HardCopy® II devices. However, if you choose an unsupported device for your Quartus II project and subsequently start the MegaWizard® Plug-In Manager, you can choose a different device family in the MegaWizard Plug-In Manager, which allows you to choose the QDRII SRAM Controller MegaCore function. There are no error messages when you perform this illegal operation.

Affected Configurations

This issue affects all configurations.

Design Impact

You cannot compile a design.

Workaround

Ensure you choose a supported device family for the Quartus II project.

Solution Status

This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

No Description of Datapath Signals

The *QDRII SRAM Controller MegaCore Function User Guide* does not describe the controller's internal signals that interface the datapath to the control logic and the resynchronization logic. For the signal descriptions, contact Altera mySupport.

Affected Configurations

This issue affects all configurations.

Design Impact

There is no design impact.

Workaround

For the signal descriptions, contact Altera mySupport.

Solution Status

This issue will be fixed in a future version of the *QDRII SRAM Controller MegaCore Function User Guide*.

Changing HDL

Be aware that when you change the HDL (Verilog HDL to VHDL or VHDL to Verilog HDL) of your custom variation. IP Toolbench does not delete all the necessary files and during compilation the Quartus II software may try to access incorrect files, which results in errors.

Affected Configurations

This issue affects all configurations.

Design Impact

When you choose **Start Compilation**, there may be error messages and the design may not compile.

Workaround

If you change which HDL you use, ensure you remove all unnecessary files from the Quartus II project.

Solution Status

This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

Compilation Error When You Choose ByteGroups On the Top & Bottom of the Device (Stratix II Series & HardCopy II Devices Only)

You will see an error during compilation if in the Constraints window you choose bytegroups on the top and the bottom of a Stratix II series or HardCopy II device.

Affected Configurations

This issue affects all Stratix II series and HardCopy II devices.

Design Impact

When you choose **Start Compilation**, there is an error message and the design does not compile.

Workaround

If you are targeting Stratix II series or HardCopy II devices, in the Constraints window ensure you choose bytegroups on either the top or the bottom of the device, but not both.

Solution Status

This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

Gate-Level Simulation Filenames

Various Quartus II software options may cause it to generate a netlist with a different filename than that expected by the gate-level simulation script. The simulation script expects <*project name*>**.vho** or **.vo** and <*project name*>**_v** or **_vhd.sdo** files to be present.

Affected Configurations

This issue affects all configurations.

Design Impact

You cannot run gate-level simulations.

Workaround

For VHDL gate-level simulations, in the **simulation/modelsim** directory follow these steps:

1. Rename <*filename*>**.vho** file to <*project name*>**.vho.**
2. Rename <*filename*>**.sdo** file to <*project name*>**_vhd.sdo**.

For Verilog HDL gate-level simulations, in the **simulation/modelsim** directory follow these steps:

1. Rename the <*filename*>**.vo** file to <*project name*>**.vo.**
2. Rename the <*filename*>**.sdo** file to <*project name*>**_v.sdo**.
3. In the <*project name*>.**vo** file change the following line to point to the <*project name*>**_v.sdo** file:

```
initial $sdf_annotate("<project name>_v.sdo");
```

Solution Status

This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

The ModelSim Script Does Not Support Companion Devices

If you have a HardCopy II companion device in a Stratix II project, be aware that the ModelSim simulation scripts do not work if you change to your companion device.

Affected Configurations

This issue affects designs with companion devices.

Design Impact

The simulation script does not run.

Workaround

Edit the Modelsim script to include the correct libraries.

Solution Status

This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

Contact Information

For more information, contact Altera's mySupport website at **www.altera.com/mysupport** and click **Create New Service Request**. Choose the **Product Related Request** form.

Revision History

Table 1 shows the errata sheet revision history for the QDRII SRAM Controller MegaCore function v1.2.1.

Table 1. QDRII SRAM Controller Errata Sheet Revision History

Version	Date	Errata Summary
1.1	April 2006	Added "Quartus II Software Version 6.0" on page 2 issue.
1.0	November 2005	First release.

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