Arria V Timing Optimization Guidelines



AN-652-1.0

Application Note

This document presents timing optimization guidelines for a set of identified critical timing path scenarios in Arria[®] V FPGA designs. Timing analysis is provided for each critical timing path scenario discussed to help you understand the critical timing path. Timing guidelines are provided for design timing performance optimization. A Quartus Archive File (**.qar**) is provided for each example scenario as a design example.

Example scenarios are used to show various critical timing paths. Timing results may vary, depending on the Quartus[®] II software version and the Arria V device used. The guidelines provided can help you optimize specific critical timing paths.

Cascaded DSP Blocks

This section shows the critical timing path scenario that occurs within cascaded DSP blocks. Table 1 lists the ALTMULT_ADD megafunction settings used to implement cascaded DSP blocks.



For a design example of cascaded DSP blocks, refer to the Cascaded DSP Design Example.

Table 1. ALTMULT_ADD Megafunction Options

Section	Setting	Value
	What is the number of multipliers?	4 multipliers
	How wide should the A input buses be?	18 bits
General	How wide should the B input buses be?	19 bits
	How wide should the 'result' output bus be?	39 bits
	Create an associated clock enable for each clock	Disabled
Multiplier Perrocontation	What is the representation format for Multiplier A inputs?	Signed
	What is the representation format for Multiplier B inputs?	Signed
	Register input A of the multiplier	Enabled
Input Configuration	Register input B of the multiplier	Enabled
	What is the input A of the multiplier connected to?	Multiplier Input
Output Configuration	Register output of the multiplier	Disabled



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Figure 1 shows the cascaded DSP blocks implemented with the megafunction settings listed in Table 1. The critical timing path occurs between the input registers of the first DSP block to the output register of the second DSP block.

Figure 1. Long Cascaded Path



Timing Analysis

This section shows the timing analysis for the critical timing path for cascaded DSP blocks. The design example is constrained at 312.5 MHz.

f_{MAX} and Slack

Figure 2 shows the f_{MAX} and slack for the cascaded DSP block implementation design example with the setting in Table 1.

	Figure 2.	f _{MAY} and Slack	Values from the	TimeQuest TImin	g Analyzer fo	r Cascaded DSP	Blocks
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sic	ow 1100mV 8	5C Model Fmax Su	SI	w 1100	m¥ 85C	Model Setup Sumr	ma ry	
	Fmax	Restricted Fmax	Clock Name		Clock	Slack	End Point TNS	
1	275.48 MHz	275.48 MHz	clock0	1	clock0	-0.430	-16.770	

The blue highlights in Figure 3 show the critical path in the worst path timing report. The critical path occurs between the transfers from one DSP block to the other DSP block (as shown in the highlighted portion), increasing the data arrival path. The location of the DSP blocks shows that they are adjacent to each other, which indicates that the placement is already optimized.

Figure 3. Critical Path Between DSP Blocks

Pa	th Summary	Statistics	s D	ata Path	Waveform	n Extra Fitter Informa	ation
Da	ita Arrival Pa	th					
	Total	Incr	RF	Туре	Fanout	Location	Element
1	0.000	0.000					launch edge time
2	8 4.269	4.269					clock path
1	0.000	0.000					source latency
2	0.000	0.000			1	PIN G21	clock0
3	0.000	0.000	RR	IC	1	IOIBUF X74 Y111 N1	clock0~inputli
4	0.552	0.552	RR	CELL	1	IOIBUF X74 Y111 N1	clock0~inputIo
5	0.948	0.396	RR	IC	1	CLKCTRL G14	clock0~inputCLKENA01inclk
6	1.188	0.240	RR	CELL	2	CLKCTRL G14	clock0~inputCLKENA0Ioutclk
7	3.597	2.409	RR	IC	74	DSP X70 Y109 N0	CascadedDSP mult add uk06 componinal adder bloc
8	4.269	0.672	RR	CELL	64	DSP X70 Y109 N0	CascadedDSP mult add uk06:Cascadedta register blo
3	= 7.650	3.381					data path
1	4.269	0.000		uTco	64	DSP X70 Y109 N0	CascadedDSP mult add uk06:Cascadedta register blo
2	6.176	1 907	RR	CELL	1	DSP X70 Y109 NO	CascadedDSP mult add uk06 componadder blockIAd
3	6.176	0.000	RR	IC	39	DSP X70 Y107 N0	CascadedDSP mult add uk06 compon adder blockIA
4	7.650	1.474	RR	CELL	1	DSP X70 Y107 N0	CascadedDSP mult add uk06:Cascadedoutput reg bl
D	ata Requireo	l Path					
	Total	Incr	RF	Туре	Fanout	Location	Element
1	3.200	3.200					latch edge time
2	8 7.244	4.044					clock path
1	3.200	0.000					source latency
2	3.200	0.000			1	PIN_AD20	clock0
3	3.200	0.000	RR	IC IC	1	IOIBUF_X74_Y0_N	L clock0~input]i
4	3.752	0.552	RR	CELL	. 1	IOIBUF_X74_Y0_N	L clock0~input o
5	4.124	0.372	RR	IC	1	CLKCTRL_G5	clock0~inputCLKENA0 inclk
6	4.349	0.225	RR	CELL	2	CLKCTRL_G5	clock0~inputCLKENA0]outclk
7	6.591	2.242	RR	IC	113	DSP_X62_Y107_N	inst altmultadd_mult_add_k7v5_compo1 final_adder_block Add1~mac clk[0]
8	7.205	0.614	RR	CELL	. 1	DSP_X62_Y107_N	altmultadd:instjaltmultadd_mult_add_kion:output_reg_blockjdata_out_wire[0]
9	7.244	0.039					clock pessimism
3	7.224	-0.020					clock uncertainty
1.0	7 3 3 4	0.000		UTeu	1	DEP X62 Y107 M	altroutadd instialtroutadd rout add k ion output ren blockidata out wire[0]

Optimization Guidelines

This section provides two guidelines to optimize the timing performance of the cascaded DSP blocks.

Guideline 1: Pipelining

Pipelining can be used to reduce the data arrival path. Refer to the example HDL in the "Appendix" to infer the registers in Figure 4.





• For a design example of using a pipeline with cascaded DSP blocks, refer to the Pipeline with Cascaded DSP Blocks Design Example.

f_{MAX} and Slack

Figure 5 shows the f_{MAX} and slack when you use pipelining with the cascaded DSP block implementation design example.

Figure 5. f_{MAX} and Slack Values from the TimeQuest Timing Analyzer

SI	ow 1100mV 8	nV 85C Model Fmax Summary		Slow 1100mV 85C Model Setup Summa				
	Fmax	Restricted Fmax	Clock Name	Note		Clock	Slack	End Point TNS
1	381.24 MHz	370.1 MHz	clock0	limit due to minimum period restriction (tmin)	1	clock0	0.577	0.000

Figure 6 shows the worst path timing report after applying the pipelining timing optimization guideline. The critical path occurs within the same DSP block (as shown in the highlighted portion in Figure 6), but it does not affect the target f_{MAX} of 312.5 MHz.

Figure 6. Worst Path Timing Report When Applying the Pipelining Optimization Guideline

P	ath Summary	Statisti	cs	Data Path	Wave	form Extra Fitter Inf	ormation
D	ata Arrival Pa	ath					
	Total	Incr	RF	Туре	Fanout	Location	Element
1	0.000	0.000					launch edge time
2	- 4.242	4.242					clock path
L	0.000	0.000					source latency
2	0.000	0.000			1	PIN G21	clock0
3	0.000	0.000	RR	IC	1	IOIBUF X74 Y111	N1 clock0~input]i
1	0.552	0.552	RR	CELL	1	IOIBUF X74 Y111	N1 clock0~input/o
5	0.948	0.396	RR	IC	1	CLKCTRL G14	clock0~inputCLKENA01inclk
5	1.188	0.240	RR	CELL	115	CLKCTRL G14	clock0~inputCLKENA0Ioutclk
7	3.570	2.382	RR	IC	113	DSP X102 Y67 NO	instl[Addl~maclclk[0]
3	4.242	0.672	BB	CELL	39	DSP X102 Y67 NO	FOUR MULT:instLIDATAA 3B[0]
3	= 6.620	2.378					data path
L	4.242	0.000		uTco	39	DSP X102 Y67 NO	FOUR MULT:inst1IDATAA 3B[0]
2	6.620	2.378	BB	CELL	1	DSP X102 Y67 N0	FOUR MULT:inst11mult result 1234
	ta Bequired	Path				Berlinki Williakakar Wilakat Milaka	
-	Total	Incr	RE	Туре	Fanout	Location	Element
R.	3 200	3 200		Type	Tanoar	Locatori	latch edge time
,	E 7.217	4.017		-		-	clock path
	3.200	0.000					source latency
	3.200	0.000			1	PIN_G21	clock0
3	3.200	0.000	RR	IC	1	IOIBUF_X74_Y111_N1	clock0~input]i
1	3.752	0.552	RR	CELL	1	IOIBUF_X74_Y111_N1	<lock0~input o< td=""></lock0~input o<>
5	4.124	0.372	RR	IC	1	CLKCTRL_G14	clock0~inputCLKENA0 inclk
i .	4.349	0.225	RR	CELL	115	CLKCTRL_G14	clock0~inputCLKENA0 outclk
	6.564	2.215	RR	IC	113	DSP_X102_Y67_N0	inst1 Add1~mac clk[0]
3	7.178	0.614	RR	CELL	1	DSP_X102_Y67_N0	FOUR_MULT:inst1 mult_result_1234[0]
9	7.217	0.039					clock pessimism
3	7.197	-0.020					clock uncertainty
				A.T.a.s	1	DCD VIAD VET NA	FOUR MULTING THE PROVIDE RECENT 1024101

Guideline 2: Parallel DSP Blocks

To meet your timing requirements, you can change your cascaded DSP blocks to parallel DSP blocks.

DSP blocks are connected in parallel to an external adder logic. Instead of configuring the ALTMULT_ADD megafunction to consist of four multipliers, configure the ALTMULT_ADD megafunction to have two multipliers. Enable the registers at the output of the adder unit and output of the multiplier (Table 2). Instantiate two of these modules and connect them using an adder as shown in Figure 7.

For a design example of parallel DSP blocks, refer to the Using Parallel DSP Blocks Design Examples.

Table 2. ALTMULT_ADD Me	gafunction Options
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Section	Setting	Value
	What is the number of multipliers?	2 multipliers
	How wide should the A input buses be?	18 bits
General	How wide should the B input buses be?	19 bits
	How wide should the 'result' output bus be?	38 bits
	Create an associated clock enable for each clock	Disabled
Multiplier Pepreceptation	What is the representation format for Multiplier A inputs?	Signed
	What is the representation format for Multiplier B inputs?	Signed
	Register output of the adder unit	Enabled
	Register input A of the multiplier	Enabled
Input Configuration	Register input B of the multiplier	Enabled
	What is the input A of the multiplier connected to?	Multiplier Input
Output Configuration	Register output of the multiplier	Enabled

Figure 7. Parallel DSP Blocks



f_{MAX} and Slack

Figure 8 shows the f_{MAX} and slack when you implement parallel DSP blocks.

Figure 8. f _{MA}	_x and Slack	for Paralle	I DSP Blocks
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Slow 1100mV 85C Model Fmax Summary					SI	ow 1100	m¥ 85C	Model Setup Sumn	nary
	Fmax	Restricted Fmax	Clock Name	Note		Clock	Slack	End Point TNS	
1	380.23 MHz	370.1 MHz	clock0	limit due to minimum period restriction (tmin)	1	clock0	0.570	0.000	

Figure 9 shows the worst path timing report, which is within the DSP block, but does not affect the desired performance

Figure 9. Worst	Path T	'iming l	Report for	Parallel	DSP E	Blocks
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Pa	th #1: Setup	slack is	0.570)			
P	ath Summary	Statistic	s C	Data Path	Waveform	m Extra Fitter Inform	ation
D	ata Arrival Pa	ath					
	Total	Incr	RF	Туре	Fanout	Location	Element
1	0.000	0.000					launch edge time
2	E-4.302	4.302					clock path
1	0 000	0 000	-				source latency
2	0.000	0.000			1	PIN G21	clock0
2	0.000	0.000	BB	IC	1	IOIBUE X74 Y111 N1	clock0~ipputli
4	0.000	0.550	DD	CELL	1	IOIDUE X74_1111_N1	clock0-inputIo
4 E	0.552	0.332	00	IC	1	CLECTRI CIA	clocko-input/o
2	0.948	0.396	RR	IC .	1	CLKCTRL_GI4	CIOCKU~INPUTULKEINAUJINCIK
6	1.188	0.240	RR	CELL	117	CLKCTRL_G14	clock0~inputCLKENA0 outclk
7	3.630	2.442	RR	IC	112	DSP_X78_Y55_N0	inst altmultadd_mult_add_ad94_comp final_adder_block
8	4.302	0.672	RR	CELL	38	DSP_X78_Y55_N0	altmultadd:inst altmultadd_mult_add_a:data_register_bloc
3	E 6.680	2.378					data path
1	4.302	0.000		uTco	38	DSP X78 Y55 N0	altmultadd:inst[altmultadd_mult_add_a:data_register_bloc
2	6.680	2.378	RR	CELL	1	DSP_X78_Y55_N0	altmultadd:inst altmultadd_mult_add_afunction:final_adde
D	ata Required	Path					
	Total	Incr	RF	Туре	Fanout	Location	Element
1	3.200	3.200					latch edge time
2	E 7.270	4.070					clock path
1	3.200	0.000					source latency
2	3.200	0.000			1	PIN_G21	clock0
з	3.200	0.000	RR	IC	1	IOIBUF_X74_Y111_N1	clock0~input i
4	3.752	0.552	RR	CELL	1	IOIBUF_X74_Y111_N1	clock0~input o
5	4.124	0.372	RR	IC	1	CLKCTRL_G14	clock0~inputCLKENA0 inclk
б	4.349	0.225	RR	CELL	117	CLKCTRL_G14	clock0~inputCLKENA0joutclk
7	6.617	2.268	RR	IC	112	DSP_X78_Y55_N0	inst altmultadd_mult_add_ad94_comp final_adder_block #
8	7.231	0.614	RR	CELL	1	DSP_X78_Y55_N0	altmultadd:inst altmultadd_mult_add_afunction:final_adde
9	7.270	0.039					clock pessimism
3	7.250	-0.020	_				clock uncertainty
4	7.250	0.000		uTsu	1	DSP X78 Y55 N0	altmultadd:instjaltmultadd mult add afunction:final adde

Comparison Between Guideline 1 and Guideline 2

Both optimization techniques for DSP block implementation have a similar performance achievement. Table 3 lists the latency and resource use advantages of "Guideline 1: Pipelining" versus "Guideline 2: Parallel DSP Blocks".

Table 3. Guidelines Comparison

Guideline 1: Pipelining	Guideline 2: Parallel DSP Blocks
3 clock latencies	4 clock latencies
DSP block by utilizing the adder within the DSP block	Additional LEs to implement the adder logic

DSP Block and Core Logic Interface

This section shows the critical timing path scenario that occurs between a DSP block and core logic. Table 4 lists the ALTMULT_ADD megafunction settings used to implement the configuration shown in Figure 10, resulting in the critical timing path.





Core logic refers to the dedicated registers in a LAB.

For a design example of a DSP block and core logic interface, refer to the Parallel DSP Blocks Interfacing Core Logic Design Example.

Table 4. ALTM	JLT_ADD Mega	afunction Options	s for DSP Block	and Core Lo	gic Interface	(Part 1 of 2)
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Section	Setting	Value
	What is the number of multipliers?	4 multipliers
	How wide should the A input buses be?	18 bits
General	How wide should the B input buses be?	19 bits
	How wide should the 'result' output bus be?	39 bits
	Create an associated clock enable for each clock	Disabled

Section	Setting	Value
Multiplier Peprocentation	What is the representation format for Multiplier A inputs?	Signed
	What is the representation format for Multiplier B inputs?	Signed
	Register input A of the multiplier	Enabled
Input Configuration	Register input B of the multiplier	Enabled
	What is the input A of the multiplier connected to?	Multiplier Input
Output Configuration	Register output of the multiplier	Enabled

Table 4. ALTMULT_ADD Megafunction Options for DSP Block and Core Logic Interface (Part 2 of 2)

The critical timing path occurs between the output register inside the DSP block and the output register of the ALTMULT_ADD megafunction (which is implemented in the LAB), because of the long IC delay and long logic levels.

Timing Analysis

This section shows the critical timing path analysis for a DSP block and core logic interface. The design example is constrained at 312.5 MHz.

f_{MAX} and Slack

Figure 11 shows the $\rm f_{MAX}$ and slack for a design that has a DSP block and core logic interface.

Figure 11. f_{MAX} and Slack Values from the TimeQuest TIming Analyzer for a DSP Block and Core Logic Interface

SI	ow 1100mV	OC Model Fmax S	ummary	SI	w 110 0	mV 0C №	lodel Setup Summa	ary
	Fmax	Restricted Fmax	Clock Name		Clock	Slack	End Point TNS	
1	271.0 MHz	271.0 MHz	clock0	1	clock0	-0.490	-6.838	

The blue highlights in Figure 12 show the critical path in the worst path timing report. The critical path occurs between the transfers from the DSP block to the register in LAB. Long logic levels occur because of the adder logic implemented in the LAB. The IC delay from the DSP block to the first level of the LABCELL is comprised of 32% (0.945 ps) of total data delay.

- a1	un #1. Secup	1			1	1	2000
Pa Da	th Summary	Statistic	s l	Data Path	Wavef	orm Extra Fitter Informat	ion
	Total	Incr	RF	Type	Fanout	Location	Element
	0.000	0.000					launch edge time
	8 4.183	4.183	_		_		clock path
	0.000	0.000					source latency
	0.000	0.000			1	PIN_G21	clock0
1	0.000	0.000	RR	IC	1	IOIBUF_X74_Y111_N1	clock0~input]i
	0.538	0.538	RR	CELL	1	IOIBUF_X74_Y111_N1	clock0~input]o
6	0.917	0.379	RR	IC	1	CLKCTRL_G14	clock0~inputCLKENA0 inclk
	- 1.150	0.233	RR	CELL	41	CLKCTRL_G14	clock0~inputCLKENA0 outclk
	3.511	2.361	RR	IC	112	DSP_X62_Y65_N0	ParallelDSP_mult_add_mvq5_componen final_adder_blo
	4.183	0.672	RR	CELL	1	DSP_X62_Y65_N0	ParallelDSP_mult_add_mvq5:ParallelDSction:final_adder
	7.206	3.023	-				data path
	4.183	0.000	-	uTco	1	DSP_X62_Y65_N0	ParallelDSP_mult_add_mvq5:ParallelDSction:final_adder
	4.519	0.336	RF	CELL	1	DSP_X62_Y65_N0	ParallelDSP_mult_add_mvq5_componeI_adder_block Ad
	5.464	0.945	FF	IC	2	LABCELL X63 Y65 N15	ParallelDSP_mult_add_mvq5_compone1 final_adder_blo
	6.064	0.600	FF	CELL	1	LABCELL_X63_Y65_N15	ParallelDSP_mult_add_mvq5_componed1[final_adder_bl
	6.064	0.000	FF	C	2	LABCELL_X63_165_N18	ParallelDSP_mult_add_mvq5_componedd1[final_adder_l
	6.133	0.069	PP-	CELL	2	LABCELL_X63_165_N18	ParallelDSP_mult_add_mvq5_componedt]rinal_adder_bi
	:					•	
5	6.538	0.000	FF	IC	2	LABCELL_X63_Y64_N48	ParallelDSP_mult_add_mvq5_componed1 final_adder_blo
5	6.538 6.874	0.000	FF	IC CELL	2	LABCELL_X63_Y64_N48 LABCELL_X63_Y64_N48 LABCELL_X63_Y64_N48	ParallelDSP_mult_add_mvq5_componed1 final_adder_blo ParallelDSP_mult_add_mvq5_componefinal_adder_block ParallelDSP_mult_add_mvq5_componen_trutt_rea_block
5 6 7 0	6.538 6.874 6.874	0.000	FF FF FF	IC CELL IC	2	LABCELL_X63_Y64_N48 LABCELL_X63_Y64_N48 FF_X63_Y64_N50 EF_Y63_Y64_N50	ParallelDSP_mult_add_mvq5_componed1 final_adder_blo ParallelDSP_mult_add_mvq5_componefinal_adder_block ParallelDSP_mult_add_mvq5_componentput_reg_block d ParallelDSP_mult_add_mvq5_componentput_reg_block d
5 6 7 8 0a	6.538 6.874 6.874 7.206 ta Required	0.000 0.336 0.000 0.332 Path	FF FF FF	IC CELL IC CELL	2 1 1 1	LABCELL_X63_Y64_N48 LABCELL_X63_Y64_N48 FF_X63_Y64_N50 FF_X63_Y64_N50	ParalleIDSP_mult_add_mvq5_componed1 final_adder_blo ParalleIDSP_mult_add_mvq5_componefinal_adder_block ParalleIDSP_mult_add_mvq5_componentput_reg_block di ParalleIDSP_mult_add_mvq5:ParalleIDSn:output_reg_block
5 6 7 8 3 a	6.538 6.874 6.874 7.206 ta Required	0.000 0.336 0.000 0.332 Path	FF FF FF FF	IC CELL IC CELL	2 1 1 1	LABCELL_X63_Y64_N48 LABCELL_X63_Y64_N48 FF_X63_Y64_N50 FF_X63_Y64_N50	ParalleIDSP_mult_add_mvq5_componed1 final_adder_blo ParalleIDSP_mult_add_mvq5_componefinal_adder_block . ParalleIDSP_mult_add_mvq5_componentput_reg_block da ParalleIDSP_mult_add_mvq5:ParalleIDSn:output_reg_block
5 6 7 8 0a	6.538 6.874 6.874 7.206 ta Required Total	0.000 0.336 0.000 0.332 Path Incr 3.200	FF FF FF FF	IC CELL IC CELL Type	2 1 1 1 Fanout	LABCELL_X63_Y64_N48 LABCELL_X63_Y64_N48 FF_X63_Y64_N50 FF_X63_Y64_N50 Location	ParalleIDSP_mult_add_mvq5_componed1[final_adder_blo ParalleIDSP_mult_add_mvq5_componefinal_adder_block] ParalleIDSP_mult_add_mvq5_componentput_reg_block di ParalleIDSP_mult_add_mvq5:ParalleIDSn:output_reg_block Element
5 6 7 8 3 a	6.538 6.874 6.874 7.206 ta Required Total 3.200 ⊕ 6.736	0.000 0.336 0.000 0.332 Path Incr 3.200 3.536	FF FF FF RF	IC CELL IC CELL Type	2 1 1 1 Fanout	LABCELL_X63_Y64_N48 LABCELL_X63_Y64_N48 FF X63_Y64_N50 FF X63_Y64_N50 Location	ParalleIDSP_mult_add_mvq5_componed1 final_adder_blo ParalleIDSP_mult_add_mvq5_componefinal_adder_block ParalleIDSP_mult_add_mvq5_componentput_reg_block da ParalleIDSP_mult_add_mvq5:ParalleIDSn:output_reg_block Element latch edge time clock path
5 6 7 8 Da	6.538 6.874 6.874 7.206 ta Required Total 3.200 6.736 3.200	0.000 0.336 0.000 0.332 Path Incr 3.200 3.536 0.000	FF FF FF FF	IC CELL IC CELL Type	2 1 1 1 Fanout	LABCELL X63 Y64 N48 LABCELL X63 Y64 N48 FF X63 Y64 N50 FF X63 Y64 N50 Location	ParalleIDSP_mult_add_mvq5_componed1. final_adder_blo ParalleIDSP_mult_add_mvq5_componefinal_adder_block}, ParalleIDSP_mult_add_mvq5_componentput_reg_block da ParalleIDSP mult add mvq5:ParalleIDSn:output reg_block Element Iatch edge time clock path source latency
5 6 7 8 Da	6.538 6.874 6.874 7.206 ta Required Total 3.200 ○ 6.736 3.200 3.200	0.000 0.336 0.000 0.332 Path Incr 3.536 0.000 0.000	FF FF FF RF	IC CELL IC CELL Type	2 1 1 1 Fanout	LABCELL_X63_Y64_N48 LABCELL_X63_Y64_N48 FF X63 Y64 N50 FF X63 Y64 N50 Location	ParalleIDSP_mult_add_mvq5_componed1 final_adder_blo ParalleIDSP_mult_add_mvq5_componefinal_adder_block , ParalleIDSP_mult_add_mvq5_componentput_reg_block da ParalleIDSP mult add mvq5:ParalleIDSn:output reg block Element latch edge time clock path source latency clock0
5 6 7 8 3 a	6.538 6.874 6.874 7.206 ta Required Total 3.200 9.6.736 3.200 3.200 3.200 3.200	0.000 0.336 0.000 0.332 Path 3.200 3.536 0.000 0.000 0.000	FF FF FF RF	IC CELL IC CELL Type	2 1 1 1 Fanout	LABCELL_X63_Y64_N48 LABCELL_X63_Y64_N48 FF_X63_Y64_N50 FF_X63_Y64_N50 Location	ParalleIDSP_mult_add_mvq5_componed1 final_adder_blo ParalleIDSP_mult_add_mvq5_componefinal_adder_block ParalleIDSP_mult_add_mvq5_componentput_reg_block da ParalleIDSP_mult_add_mvq5:ParalleIDSn:output reg_block Element latch edge time clock path source latency clock0 clock0
5 6 7 8 3 a	6.538 6.874 6.874 7.206 ta Required Total 3.200 5.736 3.200 3.200 3.200 3.200 3.200 3.200	0.000 0.336 0.000 0.332 Path Incr 3.200 3.536 0.000 0.000 0.000 0.538	FF FF FF RF RF	IC CELL IC CELL Type IC CELL	2 1 1 1 Fanout	LABCELL_X63_Y64_N48 LABCELL_X63_Y64_N48 FF_X63_Y64_N50 FF_X63_Y64_N50 Location PIN_G21 IOIBUF_X74_Y111_N1 IOIBUF_X74_Y111_N1	ParalleIDSP_mult_add_mvq5_componed1 final_adder_block ParalleIDSP_mult_add_mvq5_componefinal_adder_block ParalleIDSP_mult_add_mvq5_componentput_reg_block di ParalleIDSP_mult_add_mvq5:ParalleIDSn:output reg_block Element latch edge time clock path source latency clock0 clock0-input l clock0-input o
5 6 7 8 9 a	6.538 6.874 6.874 7.206 ta Required 7.206 ta 3.200 ○ 6.736 3.200 3.200 3.200 3.200 3.200 3.200 3.4100	0.000 0.336 0.000 0.332 Path Incr 3.200 3.536 0.000 0.000 0.000 0.538 0.362	FF FF FF RF RF RR RR RR RR	IC CELL IC CELL Type IC CELL IC	2 1 1 1 1 Fanout	LABCELL X63 Y64 N48 LABCELL X63 Y64 N48 FF X63 Y64 N50 FF X63 Y64 N50 Location PIN_G21 IOIBUF_X74_Y111_N1 IOIBUF_X74_Y111_N1 IOIBUF_X74_Y111_N1 CUKCTRL_G14	ParalleIDSP_mult_add_mvq5_componed1 final_adder_block ParalleIDSP_mult_add_mvq5_componefinal_adder_block ParalleIDSP_mult_add_mvq5_componentput_reg_block di ParalleIDSP_mult_add_mvq5:ParalleIDSn:output_reg_block ParalleIDSP_mult_add_mvq5:ParalleIDSn:output_reg_block Element latch edge time clock apth source latency clock0 clock0~input[l clock0~input[lo clock0~input[lo
5 6 7 8 3 a 2	6.538 6.874 6.874 7.206 Total 3.200 3.200 3.200 3.200 3.200 3.200 3.738 4.100 4.322	0.000 0.336 0.000 0.332 Path 3.200 3.536 0.000 0.000 0.000 0.532 0.522	FF FF FF RF RF RR RR RR RR RR RR	IC CELL IC CELL Type IC CELL IC CELL	2 1 1 1 1 1 1 1 1 41	LABCELL_X63_Y64_N48 LABCELL_X63_Y64_N48 FF X63 Y64 N50 FF X63 Y64 N50 Location PIN_G21 IOIBUF_X74_Y111_N1 IOIBUF_X74_Y111_N1 IOIBUF_X74_Y111_N1 CLKCTRL_G14 CLKCTRL_G14	ParalleIDSP_mult_add_mvq5_componed1 final_adder_blo ParalleIDSP_mult_add_mvq5_componefnal_adder_block ParalleIDSP_mult_add_mvq5_componetput_reg_block da ParalleIDSP mult add mvq5:ParalleIDSn:output reg_block Element Iatch edge time clock path source Iatency clock0 clock0~input[clock0~input[l clock0~input[LKENA0]inclk clock0_inputCLKENA0]inclk
5 6 7 8 3 a 2 3 4 5 5 5	6.538 6.874 6.874 7.206 ta Required 7.206 5.3200 3.200 3.200 3.200 3.200 3.200 3.200 4.322 6.582	0.000 0.336 0.000 0.332 Path 3.200 3.536 0.000 0.000 0.538 0.362 0.528 0.322	FF FF FF RF RR RR RR RR RR RR RR	IC CELL IC CELL Type IC CELL IC CELL IC	2 1 1 1 1 1 1 1 1 1 1 1 1 1 1	LABCELL_X63_Y64_N48 LABCELL_X63_Y64_N48 FF X63 Y64 N50 FF X63 Y64 N50 Location PIN_G21 IOIBUF_X74_Y111_N1 IOIBUF_X74_Y111_N1 IOIBUF_X74_Y111_N1 CLKCTRL_G14 CLKCTRL_G14 FF_X63_Y64_N50	ParalleIDSP_mult_add_mvq5_componed1 final_adder_block ParalleIDSP_mult_add_mvq5_componefinal_adder_block ParalleIDSP_mult_add_mvq5_componentput_reg_block da ParalleIDSP mult add mvq5:ParalleIDSn:output reg block Element latch edge time clock path source latency clock0 clock0~input[l clock0~inputCLKENA0 inclk clock0~inputCLKENA0 inclk clock0~inputCLKENA0 inclk paralleIDSP_mult_add_mvq5_componenut_reg_block data_c
i5 i6 j7 i8 Da 2 L 2 2 3 1 5 5 7 3	6.538 6.874 6.874 7.206 ta Required 3.200 9.6.736 3.200 3.200 3.200 3.200 3.200 3.200 3.200 3.200 3.200 3.200 5.738 4.100 4.322 6.582 6.708	0.000 0.336 0.000 0.332 Path 1ncr 3.200 3.536 0.000 0.000 0.538 0.362 0.222 2.260 0.126	FF FF FF RF RR RR RR RR RR RR RR RR RR	IC CELL IC CELL Type IC CELL IC CELL IC CELL	2 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	LABCELL_X63_Y64_N48 LABCELL_X63_Y64_N48 FF_X63_Y64_N50 FF_X63_Y64_N50 Location PIN_G21 IOIBUF_X74_Y111_N1 IOIBUF_X74_Y111_N1 IOIBUF_X74_Y111_N1 CLKCTRL_G14 FF_X63_Y64_N50 FF_X63_Y64_N50	ParallelDSP_mult_add_mvq5_componed1 final_adder_block ParallelDSP_mult_add_mvq5_componefinal_adder_block ParallelDSP_mult_add_mvq5_componentput_reg_block da ParallelDSP_mult_add_mvq5:ParallelDSn:output reg_block Element latch edge time clock path source latency clock0 clock0-input[i clock0~input[j clock0~input]o clock0~input[JetXA0]unclk clock0~inputCLKENA0]inclk clock0~inputCLKENA0]inclk ParallelDSP_mult_add_mvq5_ParallelDSn:output_reg_block data_cP ParallelDSP_mult_add_mvq5-ParallelDSn:output_reg_block data_cP
5 6 7 8 3 a 2 3 4 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 6 7 8 3 8 3 8 3 8 5 5 5 7 8 3 8 3 8 3 8 3 8 3 8 5 9 5 9 5 9 5 9 5 9 5 9 5 9 5 9 5 9 5		0.000 0.336 0.000 0.332 Path 3.200 3.536 0.000 0.000 0.000 0.000 0.532 0.222 2.260 0.126	FF FF FF RF RR RR RR RR RR RR RR RR	IC CELL IC CELL Type IC CELL IC CELL IC CELL	2 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	LABCELL X63 Y64 N48 LABCELL X63 Y64 N48 FF X63 Y64 N50 FF X63 Y64 N50 PIN_G21 IOIBUF_X74_Y111_N1 IOIBUF_X74_Y111_N1 IOIBUF_X74_Y111_N1 CLKCTRL_G14 CLKCTRL_G14 FF_X63_Y64_N50 FF_X63_Y64_N50	ParalleIDSP_mult_add_mvq5_componed1 final_adder_block ParalleIDSP_mult_add_mvq5_componefinal_adder_block ParalleIDSP_mult_add_mvq5_componentput_reg_block di ParalleIDSP_mult_add_mvq5:ParalleIDSn:output reg_block Element latch edge time clock path source latency clock0 clock0-input[i clock0-i
5 6 7 8 3 a 2 3 4 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5	6.538 6.874 6.874 7.206 Total 3.200 3.200 3.200 3.200 3.200 3.200 3.200 3.200 3.200 4.100 4.322 6.582 6.708 6.736 6.736 6.736	0.000 0.336 0.000 0.332 Path 3.200 3.536 0.000 0.000 0.000 0.538 0.358 0.358 0.222 2.260 0.126 0.028 0.028	FF FF FF RF RR RR RR RR RR RR RR	IC CELL IC CELL Type IC CELL IC CELL IC CELL	2 1 1 1 1 1 1 1 1 1 1 1 1 1 1	LABCELL_X63_Y64_N48 LABCELL_X63_Y64_N48 FF X63 Y64 N50 FF X63 Y64 N50 Location PIN_G21 IOIBUF_X74_Y111_N1 IOIBUF_X74_Y111_N1 IOIBUF_X74_Y111_N1 CLKCTRL_G14 CLKCTRL_G14 FF_X63_Y64_N50 FF_X63_Y64_N50	ParalleIDSP_mult_add_mvq5_componed1 final_adder_blo ParalleIDSP_mult_add_mvq5_componefnal_adder_block ParalleIDSP_mult_add_mvq5_componetput_reg_block da ParalleIDSP_mult_add_mvq5:ParalleIDSn:output_reg_block Element Iatch edge time clock path source Iatency clock0~input[clock0~input[clock0~input[LKENA0]outclk ParalleIDSP_mult_add_mvq5_componenut_reg_block data_cc ParalleIDSP_mult_add_mvq5:ParalleIDSn:output_reg_block data_cc clock passimm clock passimm

Optimization Guideline

To optimize this critical timing path, do not use 4 multipliers, especially if you require an f_{MAX} of 310 MHz and above. Use the same optimization guidelines provided in "Cascaded DSP Blocks".

M10K Block and Core Logic Interface

This section describes the critical timing path scenario that occurs between M10K blocks and core logic. Figure 13 shows an example of a 16 x 216 simple-dual-port RAM function (implemented in M10K blocks) interfacing with adders to illustrate the critical timing path.



For a design example of the M10K block and core logic interface, refer to the M10K Block and Core Logic Interface Design Example.

Core logic refers to the dedicated registers in the LAB.



Figure 13. Example of M10K and Core Logic Interface

Timing Analysis

This section describes the critical timing path analysis of the M10K block and core logic interface. The design example is constrained at 312.5 MHz.

f_{MAX} and Slack

Figure 14 shows the f_{MAX} and slack for a design that contains an M10K block and core logic interface.

Figure 14. f_{MAX} and Slack Values from the TimeQuest Timing Analyzer for an M10K Block and Core Logic Interface

SI	ow 1100mV	85C Model Fmax S	ummary	SI	o w 110 0	m V 85C	Model Setup Summary
	Fmax	Restricted Fmax	Clock Name		Clock	Slack	End Point TNS
1	255.49 MHz	255.49 MHz	CLK	1	CLK	-0.714	-81.388

The blue highlights in Figure 15 show the critical path in the worst path timing report. The critical path occurs between the transfers from the M10K block to the register in the LAB. Long logic levels occur because of the adder logic implemented in the LAB. The IC delay from the M10K block to the first level of the LABCELL comprises 54% (1.701 ns) of the total data delay.

Figure 15. Worst Path Timing Report for a M10K Block and Core Logic Interface

	th #1: Setup	slack is	-0.71	4 (VIOL	ATED)		
Pa	th Summary	Statistic	cs (Data Path	Wavef	orm Extra Fitter Informatio	on
Da	ta Arrival P	ath			2		
	Total	Incr	RF	Туре	Fanout	Location	Element
1	0.000	0.000					launch edge time
2	8 4.238	4.238					clock path
1	0.000	0.000					source latency
2	0.000	0.000	-	-	1	PIN_D20	CLK
3	0.000	0.000	RR	IC	1	IOIBUF_X76_Y111_N18	CLK~input]i
4	0.535	0.535	RR	CELL	1	IOIBUF_X76_Y111_N18	CLK~input]o
5	0.931	0.396	RR	IC	1	CLKCTRL_G12	CLK~inputCLKENA0]inclk
6	1.171	0.240	RR	CELL	3716	CLKCTRL_G12	CLK~inputCLKENA0joutclk
7	3.600	2.429	RR	IC	41	M10K_X94_Y46_N0	Generic_DUC3_block_2[DUC3_Dual_HBauto_gen
8	4.238	0.638	RR	CELL	1	M10K_X94_Y46_N0	Generic_DUC3_block:Generic_DUC3_bncram_7t
3		3.187					data path
1	4.350	0.112	_	uTco	1	M10K_X94_Y46_N0	Generic_DUC3_block:Generic_DUC3_bncram_7t
2	4.431	0.081	FF	CELL	2	M10K_X94_Y46_N0	Generic_DUC3_block_2[DUC3_Dual_HBted]ram_
3	6.132	1.701	FF	IC	2	MLABCELL_X73_Y46_N3	Generic_DUC3_block_2[DUC3_Dual_HBC3_Arithm
4	6.592	0.460	FF	CELL	1	MLABCELL_X73_Y46_N3	Generic_DUC3_block_2[DUC3_Dual_HBUC3_Arith
5	6.592	0.000	FF	IC	2	MLABCELL_X73_Y46_N6	Generic_DUC3_block_2[DUC3_Dual_HBDUC3_Ari
33	6.787	0.000	FF	IC	2	MLABCELL X73 Y46 N48	Generic DUC3 block 2IDUC3 Dual HBUC3 Arithm
33 34 35	6.787 7.108 7.108	0.000 0.321 0.000	FF FF FF	IC CELL IC	2 1 1	MLABCELL_X73_Y46_N48 MLABCELL_X73_Y46_N48 FF_X73_Y46_N50	Generic_DUC3_block_2[DUC3_Dual_HBUC3_Arithm Generic_DUC3_block_2[DUC3_Dual_HBArithmetic_ Generic_DUC3_block_2[DUC3_Dual_HBIc_Unit_I[Sy
33 34 35 36	6.787 7.108 7.108 7.425	0.000 0.321 0.000 0.317	FF FF FF FF	IC CELL IC CELL	2 1 1 1	MLABCELL_X73_Y46_N48 MLABCELL_X73_Y46_N48 FF_X73_Y46_N50 FF_X73_Y46_N50	Generic_DUC3_block_2[DUC3_Dual_HBUC3_Arithm Generic_DUC3_block_2[DUC3_Dual_HBArithmetic_ Generic_DUC3_block_2[DUC3_Dual_HBLc].uhit_[JSy Generic_DUC3_block:Generic_DUC3_bletic_Unit_I[Sy
33 34 35 36 D4	6.787 7.108 7.108 7.425 ata Required	0.000 0.321 0.000 0.317 Path	FF FF FF FF	IC CELL IC CELL	2 1 1 1	MLABCELL_X73_Y46_N48 MLABCELL_X73_Y46_N48 FF X73 Y46 N50 FF X73 Y46 N50	Generic_DUC3_block_2 DUC3_Dual_HBUC3_Arithme Generic_DUC3_block_2 DUC3_Dual_HB,Arithmetic_ Generic_DUC3_block_2 DUC3_Dual_HB,Ic_Unit_ Sy Generic_DUC3_block:Generic_DUC3_bletic_Unit_ Sy
33 34 35 36 Da	6.787 7.108 7.108 7.425 ata Required	0.000 0.321 0.000 0.317 Path Incr	FF FF FF FF	IC CELL IC CELL	2 1 1 1 Fanout	MLABCELL_X73_Y46_N48 MLABCELL_X73_Y46_N48 FF X73 Y46_N50 FF X73 Y46_N50 Location	Generic_DUC3_block_2 DUC3_Dual_HBUC3_Arithmu Generic_DUC3_block_2 DUC3_Dual_HBArithmetic_ Generic_DUC3_block_2 DUC3_Dual_HBlc_Unit_ Sy Generic_DUC3_block:Generic_DUC3_bletic_Unit_ Sy Element
33 34 35 36 Da	6.787 7.108 7.108 7.425 ata Required Total 3.200	0.000 0.321 0.000 0.317 Path Incr 3.200	FF FF FF FF	IC CELL IC CELL Type	2 1 1 1 Fanout	MLABCELL_X73_Y46_N48 MLABCELL_X73_Y46_N48 FF_X73_Y46_N50 FF_X73_Y46_N50 Location	Generic_DUC3_block_2 DUC3_Dual_HBUC3_Arithme Generic_DUC3_block_2 DUC3_Dual_HBArithmetic_ Generic_DUC3_block_2 DUC3_Dual_HBlc_Unit_ Sy Generic_DUC3_block:Generic_DUC3_bletic_Unit_ Sy Element latch edge time
33 34 35 36 Di 1 2	6.787 7.108 7.108 7.425 ata Required Total 3.200 © 6.731	0.000 0.321 0.000 0.317 Path Incr 3.200 3.531	FF FF FF FF	IC CELL IC CELL Type	2 1 1 1 Fanout	MLABCELL_X73_Y46_N48 MLABCELL_X73_Y46_N48 FF_X73_Y46_N50 FF_X73_Y46_N50 Location	Generic_DUC3_block_2[DUC3_Dual_HBUC3_Arithmetic_ Generic_DUC3_block_2[DUC3_Dual_HB,Crithmetic_ Generic_DUC3_block;2[DUC3_Dual_HB,Crithmetic_ Generic_DUC3_block;Generic_DUC3_bletic_Unit_[]S Element latch edge time clock path
33 34 35 36 Di 1 2	6.787 7.108 7.109 7.425 ata Required Total 3.200 ▷ 6.731 3.200	0.000 0.321 0.000 0.317 Path Incr 3.200 3.531 0.000	FF FF FF RF	IC CELL IC CELL Type	2 1 1 Fanout	MLABCELL_X73_Y46_N48 MLABCELL_X73_Y46_N48 FF_X73_Y46_N50 FF_X73_Y46_N50 Location	Generic_DUC3_block_2 DUC3_Dual_HBUC3_Arithme Generic_DUC3_block_2 DUC3_Dual_HB,Arithmetic_ Generic_DUC3_block_2 DUC3_Dual_HB,Arithmetic_ Generic_DUC3_block:2 DUC3_Dual_HB,Arithmetic_ Generic_DUC3_block:Generic_DUC3_bletic_Unit_I Sy Generic_DUC3_block:Generic_DUC3_bletic_Unit_I Sy Generic_DUC3_block:Generic_DUC3_bletic_Unit_I Sy Generic_DUC3_block:Generic_DUC3_bletic_Unit_I Sy Generic_DUC3_block:Generic_DUC3_bletic_Unit_I Sy Generic_DUC3_block:Generic_DUC3_bletic_Unit_I Sy Generic_DUC3_block:Generic_DUC3_bletic_Unit_I Sy Generic_DUC3_block:Generic_DUC3_bletic_Unit_I Sy Generic_DUC3_block.generic_DUC3_bletic_Unit_I Sy Generic_DUC3_block.generic_DUC3_bletic_DUC3_bletic_DUC3_bletic_DUC3_bletic_DUC3_bletic_DUC3_bletic_DUC3_bletic_DUC3_bletic_DUC3_bletic_DUC3_bletic_DUC3_bletic_DUC3_bletic_DUC3_bletic_DUC3_bletic_DUC3_bletic_DUC3_bletic_DUC3_bletic_DUC3_bl
33 34 35 36 Di 1 2 1 2	6.787 7.108 7.108 7.425 Total 3.200 € 6.731 3.200 3.200 3.200	0.000 0.321 0.000 0.317 Path Incr 3.200 3.531 0.000 0.000	FF FF FF RF	IC CELL IC CELL Type	2 1 1 Fanout	MLABCELL_X73_Y46_N48 MLABCELL_X73_Y46_N48 FF X73 Y46_N50 FF X73 Y46_N50 Location	Generic_DUC3_block_2 DUC3_Dual_HBUC3_Arithms Generic_DUC3_block_2 DUC3_Dual_HBArithmetic_ Generic_DUC3_block_2 DUC3_Dual_HBLc_Unit_ Sy Generic_DUC3_block:Generic_DUC3_bletic_Unit_ Sy Generic_DUC3_block:Generic_DUC3_bletic_Unit_ Sy Element latch edge time clock path source latency CLK
33 34 35 36 D 1 2 1 2 3	6.787 7.108 7.108 7.108 7.425 7.425 7.425 7.425 6.731 3.200 6.731 3.200 3.200 3.200 3.200	0.000 0.321 0.000 0.317 Path Incr 3.200 3.531 0.000 0.000 0.000	FF FF FF RF	IC CELL IC CELL Type	2 1 1 1 Fanout	MLABCELL_X73_Y46_N48 MLABCELL_X73_Y46_N48 FF_X73_Y46_N50 FF_X73_Y46_N50 Location	Generic_DUC3_block_2[DUC3_Dual_HBUC3_Arithm Generic_DUC3_block_2[DUC3_Dual_HB,Arithmetic_ Generic_DUC3_block_2[DUC3_Dual_HB,Lc_Unit_I]Sy Generic_DUC3_block:Generic_DUC3_bletic_Unit_I]Sy Element latch edge time clock path source latency CLK CLK~inputII
33 34 35 36 1 2 1 2 3 4	6.787 7.108 7.425 ata Required 3.200 □ 6.731 3.200 3.200 3.200 3.200 3.200	0.000 0.321 0.000 0.317 Path Incr 3.200 3.531 0.000 0.000 0.000 0.535	FF FF FF RF RF	IC CELL IC CELL Type	2 1 1 1 Fanout	MLABCELL_X73_Y46_N48 MLABCELL_X73_Y46_N48 FF X73 Y46_N50 FF X73 Y46_N50 Location PIN_D20 IOIBUF_X76_Y111_N18 IOIBUF_X76_Y111_N18	Generic_DUC3_block_2[DUC3_Dual_HBUC3_Arithme Generic_DUC3_block_2[DUC3_Dual_HBArithmetic_ Generic_DUC3_block_2[DUC3_Dual_HBIc_Unit_][Sy Generic_DUC3_block:Generic_DUC3_bletic_Unit_][Sy Element latch edge time clock path source latency CLK CLK~input[i CLK~input[i
33 34 35 36 Di 1 2 1 2 3 4 5	6.787 7.108 7.108 7.425 Total 3.200 ⊕ 6.731 3.200 3.200 3.200 3.200 3.200 3.735	0.000 0.321 0.000 0.317 Path Incr 3.200 3.531 0.000 0.000 0.000 0.000 0.535 0.375	FF FF FF RF RF	IC CELL IC CELL Type IC CELL	2 1 1 Fanout	MLABCELL_X73_Y46_N48 MLABCELL_X73_Y46_N48 FF X73 Y46_N50 FF X73 Y46 N50 Location PIN_D20 IOIBUF_X76_Y111_N18 IOIBUF_X76_Y111_N18 IOIBUF_X76_Y111_N18	Generic_DUC3_block_2 DUC3_Dual_HBUC3_Arithme Generic_DUC3_block_2 DUC3_Dual_HB,Arithmetic_ Generic_DUC3_block_2 DUC3_Dual_HB,ic_Unit_ Sy Generic_DUC3_block:Generic_DUC3_bletic_Unit_ Sy Generic_DUC3_block:Generic_
33 34 35 36 1 2 1 2 3 4 5 6	6.787 7.108 7.425 Total 3.200 6.731 3.200 3.200 3.200 3.200 3.735 4.107	0.000 0.321 0.000 0.317 Path Incr 3.200 0.000 0.000 0.000 0.000 0.535 0.372	FF FF FF RF RF	IC CELL IC CELL Type IC CELL IC CELL IC	2 1 1 1 1 1 1 1 1 1 1 2716	MLABCELL_X73_Y46_N48 MLABCELL_X73_Y46_N48 FF_X73_Y46_N50 FF X73_Y46_N50 Location PIN_D20 IOIBUF_X76_Y111_N18 IOIBUF_X76_Y111_N18 ICIBUF_X76_Y111_N18 CLKCTRL_G12 CLKCTRL_G12	Generic_DUC3_block_2 DUC3_Dual_HBUC3_Arithme Generic_DUC3_block_2 DUC3_Dual_HBArithmetic_ Generic_DUC3_block_2 DUC3_Dual_HBArithmetic_ Generic_DUC3_block:Generic_DUC3_bletic_Unit_I Sy Generic_DUC3_block:Generic_DUC3_bletic_Unit_I Sy Generic_DUC3_Block:Generic
33 34 35 36 1 2 1 2 3 4 5 6	6.787 7.108 7.108 7.425 ata Required 3.200 6.731 3.2000 3.200 3.2000 3.2000 3.2000 3.20000000000	0.000 0.321 0.000 0.317 Path Incr 3.200 3.531 0.000 0.000 0.535 0.372 0.225 0.225	FF FF FF RF RF RR RR RR RR RR	IC CELL IC CELL Type IC CELL IC CELL IC	2 1 1 1 1 1 1 1 1 1 1 1 1 1 1 2716	MLABCELL_X73_Y46_N48 MLABCELL_X73_Y46_N48 FF X73 Y46 N50 FF X73 Y46 N50 Location PIN_D20 IOIBUF_X76_Y111_N18 IOIBUF_X76_Y111_N18 CLKCTRL_G12 CLKCTRL_G12 CLKCTRL_G12	Generic_DUC3_block_2 DUC3_Dual_HBUC3_Arithmetic_ Generic_DUC3_block_2 DUC3_Dual_HBArithmetic_ Generic_DUC3_block_2 DUC3_Dual_HBic_Unit_ Sy Generic_DUC3_block:Generic_DUC3_bletic_Unit_ Sy Element latch edge time clock path source latency CLK CLK~input[i CLK~input[i CLK~inputCLKENA0]inclk CLK~inputCLKENA0]inclk CLK~inputCLKENA0]inclk
33 34 35 36 1 2 1 2 3 4 5 6 7	6.787 7.108 7.425 sta Required Total 3.200 9 6.731 3.2000 3.200 3.2000 3.2000 3.2000 3.20000000000	0.000 0.321 0.000 0.317 Path Incr 3.200 3.531 0.000 0.000 0.000 0.000 0.003 0.035 0.372 0.225 2.239	FF FF FF RF RR RR RR RR RR RR RR	IC CELL IC CELL Type IC CELL IC CELL IC	2 1 1 1 1 1 1 1 1 3716 1	MLABCELL_X73_Y46_N48 MLABCELL_X73_Y46_N48 FF_X73_Y46_N50 FF_X73_Y46_N50 Location PIN_D20 IOIBUF_X76_Y111_N18 IOIBUF_X76_Y111_N18 CLKCTRL_G12 CLKCTRL_G12 FF_X73_Y46_N50	Generic_DUC3_block_2 DUC3_Dual_HBUC3_Arithme Generic_DUC3_block_2 DUC3_Dual_HB,Arithmetic_ Generic_DUC3_block_2 DUC3_Dual_HB,Ic_Unit_ Sy Generic_DUC3_block:Generic_DUC3_bletic_Unit_ Sy Generic_DUC3_block:Generic_DUC3_bletic_Unit_ Sy Element latch edge time clock path source latency CLK CLK-input[i CLK-input[i CLK-input[i CLK-inputCLKENA0]inclk CLK-inputCLKENA0]inclk CLK-inputCLKENA0]outclk Generic_DUC3_block_2 DUC3_Dual_HBUnit_ Syme
33 34 35 36 D 3 1 2 1 2 3 4 5 6 7 8	6.787 7.108 7.108 7.425 Total 3.200 6.731 3.200 3.200 3.200 3.200 3.200 3.200 3.200 3.735 4.107 4.332 6.571 6.692	0.000 0.321 0.000 0.317 Path Incr 3.200 3.531 0.000 0.000 0.000 0.535 0.372 0.225 2.239 0.121	FF FF FF RF RR RR RR RR RR RR RR RR RR	IC CELL IC CELL Type IC CELL IC CELL IC CELL	2 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	MLABCELL_X73_Y46_N48 MLABCELL_X73_Y46_N48 FF X73_Y46_N50 FF X73_Y46_N50 FDN_D20 IOIBUF_X76_Y111_N18 IOIBUF_X76_Y111_N18 IOIBUF_X76_Y111_N18 CLKCTRL_G12 CLKCTRL_G12 FF_X73_Y46_N50 FF_X73_Y46_N50	Generic_DUC3_block_2[DUC3_Dual_HBUC3_Arithmetic_ Generic_DUC3_block_2[DUC3_Dual_HB,Arithmetic_ Generic_DUC3_block.2[DUC3_Dual_HB,Lc_Unit_J[Sy Generic_DUC3_block:Generic_DUC3_bletic_Unit_J[Sy Element latch edge time clock path source latency CLK CLK~input[] CLK~input[] CLK~input[] CLK~input[] CLK~input[] CLK~input[] CLK~input[] CLK~input[] CLK~input[] CLK~input[] CLK~input[] CLK~input[] CLK~input[] CLK~input[] CLK~input[] CLK~input[] CLK~input[] CLK~input[] CLK~input[] Seneric_DUC3_block.2[DUC3_Dual_HB,Unit_J[Syme Generic_DUC3_block.Generic_DUC3_bletic_Unit_J[Syme
33 34 35 36 1 2 1 2 3 4 5 6 7 8 9	6.787 7.108 7.108 7.425 ata Required 3.200 6.731 3.200 3.200 3.200 3.200 3.200 3.200 3.200 3.200 3.200 3.200 3.200 6.731 4.107 4.332 6.571 6.692 6.731	0.000 0.321 0.000 0.317 Path Incr 3.200 3.531 0.000 0.000 0.000 0.000 0.000 0.535 0.372 0.225 2.239 0.121 0.039	FF FF FF RF RR RR RR RR RR RR RR RR RR	IC CELL IC CELL IC CELL IC CELL IC CELL	2 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	MLABCELL_X73_Y46_N48 MLABCELL_X73_Y46_N48 FF X73 Y46 N50 FF X73 Y46 N50 IDBUF_X76_Y111_N18 IDBUF_X76_Y110_N18_N18_N18_N18_N18_N18_N18_N18_N18_N18	Generic_DUC3_block_2 DUC3_Dual_HBUC3_Arithmetic_ Generic_DUC3_block_2 DUC3_Dual_HBLC_Unit_I[Sy Generic_DUC3_block_2 DUC3_Dual_HBic_Unit_I[Sy Generic_DUC3_block:Generic_DUC3_bletic_Unit_I[Sy Element latch edge time clock path source latency CLK CLK~input[i CLK~input[i CLK~input[i CLK~inputCLKENA0]inclk CLK~inputCLKENA0]inclk CLK~inputCLKENA0]outclk Generic_DUC3_block:2 DUC3_Dual_HBUnit_I[Syme Generic_DUC3_block:Generic_DUC3_bletic_Unit_I[Syme
33 34 35 36 1 2 1 2 3 4 5 6 7 8 9 3	6.787 7.108 7.425 ta Required 3.200 ⊕ 6.731 3.200 3.200 3.200 3.200 3.735 4.107 4.332 6.571 6.692 6.731	0.000 0.321 0.000 0.317 Path Incr 3.200 3.531 0.000 0.000 0.000 0.000 0.000 0.372 0.225 2.239 0.121 0.039 -0.020	FF FF FF RF RR RR RR RR RR RR RR RR	IC CELL IC CELL IC CELL IC CELL IC CELL	2 1 1 1 1 1 1 1 1 1 1 1 1 1 1	MLABCELL_X73_Y46_N48 MLABCELL_X73_Y46_N48 FF X73_Y46_N50 FF X73_Y46_N50 Location PIN_D20 IOBUF_X76_Y111_N18 IOBUF_X76_Y111_N18 IOBUF_X76_Y111_N18 CLKCTRL_G12 CLKCTRL_G12 FF_X73_Y46_N50 FF_X73_Y46_N50	Generic_DUC3_block_2 DUC3_Dual_HBUC3_Arithmet Generic_DUC3_block_2 DUC3_Dual_HB,Arithmetic_] Generic_DUC3_block_2 DUC3_Dual_HB,ic_Unit_I Sy Generic_DUC3_block:Generic_DUC3_bletic_Unit_I Sy Element latch edge time clock path source latency CLK CLKinput[i CLKinput[i CLKinputCLKENA0]inclk CLKinputCLKENA0]inclk CLKinputCLKENA0]outclk Generic_DUC3_block_2 DUC3_Dual_HBUnit_I Syme Generic_DUC3_block.Generic_DUC3_bletic_Unit_I Syme Generic_DUC3_block.Generic_DUC3_bletic_Unit_I Syme Generic_DUC3_block.Generic_DUC3_bletic_Unit_I Syme Generic_DUC3_block.Generic_DUC3_bletic_Unit_I Syme Generic_DUC3_block.Generic_DUC3_bletic_Unit_I Syme

Figure 16 shows the interconnect delay is comprised of 54% of the total data delay.



Figure 16. Interconnect Delay

Optimization Guideline

To optimize the performance of this particular critical timing path, add registers to the outputs of the M10K blocks (Figure 17). This improves the f_{MAX} of the timing path, but introduces additional clock cycle latency.





For a design example of the adding a register to the output of M10K blocks, refer to the Registers for Outputs of M10K Blocks Design Example.

fMAX and Slack

Figure 18 shows the f_{MAX} and slack for a design that has added a pipeline register to the output of the M10K block.

Figure 18. Meeting the Desired f_{MAX} of 312.5 MHz

SIC	ow 1100mV :	BSC Model Fmax S	ummary	SI	ow 1100	0m¥ 85C	Model Setup Summary	
	Fmax	Restricted Fmax	Clock Name	ТГ	Clock	Clock Slack End Point TNS		
1	324.78 MHz	324.78 MHz	CLK	1	CLK	0.421	0.000	

Figure 19 shows the worst path timing report.

Figure 19. Worst Path Timing Report for Registers Added to the Outputs of M10K Blocks

P	ath Summary	Statistic	s C	Data Path	Wavefor	m Extra Fitter Information	
D	ata Arrival Pa	ath					
1	Total	Incr	RF	Туре	Fanout	Location	Element
1	0.000	0.000					source latency
2	0.000	0.000			1	PIN_D20	CLK
3	0.000	0.000	RR	IC	1	IOIBUF_X76_Y111_N18	CLK~input i
4	0.535	0.535	RR	CELL	1	IOIBUF_X76_Y111_N18	CLK~input]o
5	0.931	0.396	RR	IC	1	CLKCTRL_G12	CLK~inputCLKENA0jinclk
б	1.171	0.240	RR	CELL	5472	CLKCTRL_G12	CLK~inputCLKENA0 outclk
7	3.596	2.425	RR	IC	43	M10K_X94_Y52_N0	Generic_DUC3_block_1 DUC3_Dual_HBauto_generate
8	4.199	0.603	RR	CELL	1	M10K_X94_Y52_N0	Generic_DUC3_block:Generic_DUC3cram_m1r1:auto
з	5.708	1.509					data path
1	4.311	0.112		uTco	1	M10K_X94_Y52_N0	Generic_DUC3_block:Generic_DUC3cram_m1r1:auto
2	4.392	0.081	FF	CELL	1	M10K_X94_Y52_N0	Generic_DUC3_block_1 DUC3_Dual_HBted[ram_block]
3	5.335	0.943	FF	IC	1	MLABCELL_X100_Y52_N57	Generic_DUC3_block_1[DUC3_Dual_HBUC3_PipeLine_I
4	5.391	0.056	FF	CELL	1	MLABCELL_X100_Y52_N57	Generic_DUC3_block_1 DUC3_Dual_HB3_PipeLine_I q[
5	5.391	0.000	FF	IC	1	FF_X100_Y52_N58	Generic_DUC3_block_1 DUC3_Dual_HUC3_HB_2 DUC3
6	5.708	0.317	FF	CELL	1	FF X100 Y52 N58	Generic DUC3 block:Generic DUC3 b C3 PipeLine:DU

General Timing Optimization Guidelines

This section contains other timing optimization guidelines that you can use to improve the design timing performance of the different design scenarios.

Quartus II Fitter Settings

By default, the Quartus II software Fitter optimizes your design based on your SDC constraints. However, the Quartus II Fitter may not always be able to optimize your design based with its default settings. Use the following recommended settings for the Quartus II Fitter if your design does not meet your SDC constraints requirements:

- 1. Increase the placement and router effort to 8 and 16 respectively.
- 2. Use different seed numbers with the Design Space Explorer (DSE), especially if minor slack causes timing failures.
- 3. Use the Standard Fit option in the Setting dialog box for the Fitter effort.

Quartus II Physical Synthesis Settings

Quartus II physical synthesis settings provide another option to optimize your design to meet your SDC constraints requirements. You can use the following Quartus II physical synthesis settings in various combinations to optimize your design:

- Perform physical synthesis for combinatorial logic
- Perform register retiming
- **Effort level** set to **Normal** or **Extra**
- Perform automatic asynchronous signal pipelining
- Perform register duplication

Automated Timing Closure Analysis Tool

The Automated Timing Closure Analysis feature in the TimeQuest Timing Analyzer provides you with a set of recommendations to improve timing on your design. If you are unclear of where to look for timing failures in your design, the Automated Timing Closure Analysis feature will provide you with a starting point.

You can access the Automated Timing Closure Analysis feature under "Report Timing Closure Recommendations" in "Custom Reports" from the Task window.

Timing Optimization Advisor

The Timing Optimization Advisor feature in the Quartus II Advisors uses current project settings and design constraints to make recommendations of project settings and assignments, individual entity assignments, and design changes for partitioning a design or optimizing a project for power, resource usage, or timing.

- ⑦ For more information about the Quartus II Advisors, refer to About Advisors in the Quartus II Software topic in Quartus II Help.
- ⑦ For more information about the Quartus II Timing Optimization Advisor, refer to the Timing Optimization Advisor Command (Tools Menu) topic in Quartus II Help.

Appendix

Example VHDL code that infers pipeline registers to cascading DSP blocks:

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_unsigned.all;
use IEEE.std_logic_arith.all;
ENTITY FOUR_MULT IS
   PORT (
       CLK
             : INSTD_LOGIC;
       DATAA_0 : IN STD_LOGIC_VECTOR (17 DOWNTO 0);
       DATAA_1 : IN STD_LOGIC_VECTOR (17 DOWNTO 0);
       DATAA_2 : IN STD_LOGIC_VECTOR (17 DOWNTO 0);
DATAA_3 : IN STD_LOGIC_VECTOR (17 DOWNTO 0);
       DATAB_0 : IN STD_LOGIC_VECTOR (18 DOWNTO 0);
       DATAB_1 : IN STD_LOGIC_VECTOR (18 DOWNTO 0);
       DATAB 2 : IN STD LOGIC VECTOR (18 DOWNTO 0);
       DATAB_3 : IN STD_LOGIC_VECTOR (18 DOWNTO 0);
       RESULT : OUT STD_LOGIC_VECTOR (38 DOWNTO 0)
      );
END FOUR_MULT;
ARCHITECTURE FOUR_MULT_ARC OF FOUR_MULT IS
SIGNAL RESET_N: STD_LOGIC:='1';
SIGNAL DATAA_OR : SIGNED (17 DOWNTO 0);
SIGNAL DATAA_1R : SIGNED (17 DOWNTO 0);
SIGNAL DATAA_2R : SIGNED (17 DOWNTO 0);
SIGNAL DATAA_3R : SIGNED (17 DOWNTO 0);
SIGNAL DATAB_OR : SIGNED (18 DOWNTO 0);
SIGNAL DATAB_1R : SIGNED (18 DOWNTO 0);
SIGNAL DATAB_2R : SIGNED (18 DOWNTO 0);
SIGNAL DATAB_3R : SIGNED (18 DOWNTO 0);
--Arria-V DSP support signed 19x18, no precision lost here
```

```
--Intermediate result on output adder chain
SIGNAL mult_1 : SIGNED(36 DOWNTO 0);
SIGNAL mult_2 :SIGNED(36 DOWNTO 0);SIGNAL mult_3 :SIGNED(36 DOWNTO 0);SIGNAL mult_4 :SIGNED(36 DOWNTO 0);
SIGNAL mult_result_12: SIGNED(37 DOWNTO 0);
SIGNAL mult_result_1234: SIGNED(38 DOWNTO 0);
--Final result
SIGNAL mult_result: STD_LOGIC_VECTOR(38 DOWNTO 0);
--This is pure RTL, no MegaFunction needed.
BEGIN
Sh_Pipe_vector_out:process(CLK)
BEGIN
IF RISING_EDGE(CLK) THEN
DATAA_OR <= SIGNED(DATAA_0);</pre>
DATAA_1R <= SIGNED(DATAA_1);</pre>
DATAA_2R <= SIGNED(DATAA_2);</pre>
DATAA_3R <= SIGNED(DATAA_3);</pre>
DATAB_OR <= SIGNED(DATAB_0);</pre>
DATAB_1R <= SIGNED(DATAB_1);</pre>
          <= SIGNED(DATAB_2);
DATAB_2R
DATAB_3R <= SIGNED(DATAB_3);</pre>
END IF;
END PROCESS;
--Multiplier section
mult_1 <= DATAA_OR*DATAB_OR;</pre>
mult_2 <= DATAA_1R*DATAB_1R;</pre>
mult_3 <= DATAA_2R*DATAB_2R;</pre>
mult_4 <= DATAA_3R*DATAB_3R;</pre>
  Last_stage_Adder_gen:process(CLK,RESET_N)
  BEGIN
  IF RESET N = '0'THEN
mult_result_12<= (OTHERS => '0');
mult_result_1234<= (OTHERS => '0');
mult_result<= (OTHERS => '0');
-- Sh
  ELSIF RISING EDGE(CLK) THEN
    --1st DSP sum-of-2 19x18
   mult_result_12 <= SIGNED(SXT(STD_LOGIC_VECTOR(mult_1),38))+</pre>
   SIGNED(SXT(STD_LOGIC_VECTOR(mult_2),38));
   --2nd DSP sum-of-2 19x18 with output adder
   mult_result_1234 <= SIGNED(SXT(STD_LOGIC_VECTOR(mult_result_12),39)) +</pre>
   (SIGNED(SXT(STD_LOGIC_VECTOR(mult_3), 39))+
                                         SIGNED(SXT(STD_LOGIC_VECTOR(mult_4),39)));
   mult_result <= STD_LOGIC_VECTOR(mult_result_1234) ;</pre>
  END IF;
  END PROCESS;
RESULT <= mult_result;</pre>
END FOUR_MULT_ARC;
```

Document Revision History

Table 5 lists the revision history for this document.

Table 5. Document Revision History

Date	Version	Changes
November 2011	1.0	Initial release.