12. JTAG Boundary-Scan Testing in Stratix IV Devices

SIV51012-3.2

The IEEE Std. 1149.1 boundary-scan test (BST) circuitry available in Stratix® IV devices provides a cost-effective and efficient way to test systems that contain devices with tight lead spacing. Circuit boards with Altera and other IEEE Std. 1149.1-compliant devices can use EXTEST, SAMPLE/PRELOAD, and BYPASS modes to create serial patterns that internally test the pin connections between devices and check device operation.

This chapter describes how to use the IEEE Std. 1149.1 BST circuitry in Stratix IV devices. The features are similar to Stratix III devices, unless stated otherwise in this chapter.

This chapter contains the following sections:

BST Architecture

A device operating in IEEE Std. 1149.1 BST mode uses four required pins, TDI, TDO, TMS, TCK, and one optional pin, TRST. The TCK pin has an internal weak pull-down resistor, while the TDI, TMS, and TRST pins have internal weak pull-up resistors. The TDO output pin and all the JTAG input pins are powered by the 2.5-V/3.0-V V_{CCPD} supply of I/O bank 1A. All user I/O pins are tri-stated during JTAG configuration.

For more information about the description and functionality of all JTAG pins, registers used by the IEEE Std. 1149.1 BST circuitry, and the test access port (TAP) controller, refer to the *IEEE 1149.1 (JTAG) Boundary-Scan Testing in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*.

BST Operation Control

Table 12–1 lists the boundary-scan register length for Stratix IV devices.

Table 12–1. Boundary-Scan Register Length in Stratix IV Devices

Device	Boundary-Scan Register Length
EP4SGX70	1506
EP4SGX110	1506
EP4SGX180	2274
EP4SGX230	2274
EP4SGX290 *(1)*	2682
EP4SGX360 *(1)*	2682
EP4SGX530	2970
EP4SE230	2274
EP4SE360	2682
EP4SE530	2970
EP4SE820	3402
EP4S40G2	2274
EP4S40G5	2970
EP4S100G2	2274
EP4S100G3	2970
EP4S100G4	2970
EP4S100G5	2970

Note to Table 12–1:

(1) For the F1932 package of EP4SGX290 and EP4SGX360 devices, the boundary-scan register length is 2970.

Table 12–2 lists the IDCODE information for Stratix IV devices.

Table 12–2. IDCODE Information for Stratix IV Devices (Part 1 of 2)

Device	IDCODE (32 Bits) *(1)*			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer Identity (11 Bits)	LSB (1 Bit) *(2)*
EP4SGX70	0000	0010 0100 0010 0000	000 0110 1110	1
EP4SGX110	0000	0010 0100 0000 0000	000 0110 1110	1
EP4SGX180	0000	0010 0100 0010 0001	000 0110 1110	1
EP4SGX230	0000	0010 0100 0000 1001	000 0110 1110	1
EP4SGX290 *(3)*	0000	0010 0100 0010 0010	000 0110 1110	1
EP4SGX290 *(4)*	0000	0010 0100 0100 0011	000 0110 1110	1
EP4SGX360 *(3)*	0000	0010 0100 0000 0010	000 0110 1110	1
EP4SGX360 *(4)*	0000	0010 0100 1000 0011	000 0110 1110	1
EP4SGX530	0000	0010 0100 0000 0011	000 0110 1110	1
EP4SE230	0000	0010 0100 0001 0001	000 0110 1110	1
EP4SE360	0000	0010 0100 0001 0010	000 0110 1110	1

Table 12–2. IDCODE Information for Stratix IV Devices (Part 2 of 2)

Device	IDCODE (32 Bits) *(1)*			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer Identity (11 Bits)	LSB (1 Bit) *(2)*
EP4SE530	0000	0010 0100 0001 0011	000 0110 1110	1
EP4SE820	0000	0010 0100 0000 0100	000 0110 1110	1
EP4S40G2 *(5)*	0000	0010 0100 0100 0001	000 0110 1110	1
EP4S40G5 *(6)*	0000	0010 0100 0010 0011	000 0110 1110	1
EP4S100G2 *(5)*	0000	0010 0100 0100 0001	000 0110 1110	1
EP4S100G3	0000	0010 0100 1010 0011	000 0110 1110	1
EP4S100G4	0000	0010 0100 0110 0011	000 0110 1110	1
EP4S100G5 *(6)*	0000	0010 0100 0010 0011	000 0110 1110	1

Notes to Table 12–2:

(1) The MSB is on the left.
(2) The LSB of the IDCODE is always 1.
(3) The IDCODE is applicable for all packages except F1932.
(4) The IDCODE is applicable for package F1932 only.
(5) For the ES1 device, the IDCODE is the same as the IDCODE of EP4SGX230.
(6) For the ES1 device, the IDCODE is the same as the IDCODE of EP4SGX530.

If the device is in reset state, when the nCONFIG or nSTATUS signal is low, the device IDCODE might not be read correctly. To read the device IDCODE correctly, you must issue the IDCODE JTAG instruction only when the nSTATUS signal is high.

For more information about the following topics, refer to the *IEEE 1149.1 (JTAG) Boundary-Scan Testing in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*:

- JTAG instruction codes with descriptions
- TAP controller state-machine
- Timing requirements for IEEE Std. 1149.1 signals
- Instruction mode
- Mandatory JTAG instructions (SAMPLE/PRELOAD, EXTEST, and BYPASS)
- Optional JTAG instructions (IDCODE, USERCODE, CLAMP, and HIGHZ)

I/O Voltage Support in a JTAG Chain

The JTAG chain supports several devices. However, you must use caution if the chain contains devices that have different V_{CCIO} levels.

For more information, refer to the *IEEE 1149.1 (JTAG) Boundary-Scan Testing in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*.

BST Circuitry

The IEEE Std. 1149.1 BST circuitry is enabled after device power-up. You can perform BST on Stratix IV devices before, during, and after configuration. Stratix IV devices support `BYPASS`, `IDCODE`, and `SAMPLE` JTAG instructions during configuration without interrupting configuration. To send all other JTAG instructions, you must interrupt configuration using the `CONFIG_IO` JTAG instruction.

For more information, refer to *AN 39: IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices*.

For more information about using the `CONFIG_IO` JTAG instruction for dynamic I/O buffer configuration, considerations when performing BST for configured devices, and JTAG pin connections to mask-out the BST circuitry, refer to the *IEEE 1149.1 (JTAG) Boundary-Scan Testing in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*.

For more information about using the IEEE Std.1149.1 circuitry for device configuration, refer to the *Configuration, Design Security, Remote System Upgrades in Stratix IV Devices* chapter.

If you must perform BST for configured devices, you must use the Quartus II software version 8.1 and onwards to generate the design-specific boundary-scan description language (BSDL) files. For the procedure to generate post-configured BSDL files using the Quartus II software, refer to the *BSDL Files Generation in Quartus II* on the Altera website.

BSDL Support

BSDL, a subset of VHDL, provides a syntax that allows you to describe the features of an IEEE Std. 1149.1 BST-capable device that can be tested.

For more information about BSDL files for IEEE Std. 1149.1-compliant Stratix IV devices, refer to the *Stratix IV BSDL Files* on the Altera website.

BSDL files for IEEE std. 1149.1-compliant Stratix IV devices can also be generated using the Quartus II software version 8.1 and onwards. For more information about the procedure to generate BSDL files using the Quartus II software, refer to the *BSDL Files Generation in Quartus II* on the Altera website.

Document Revision History

Table 12–3 lists the revision history for this chapter.

Table 12–3. Document Revision History

Date	Version	Changes
February 2011	3.2	■ Applied new template. ■ Minor text edits.
March 2010	3.1	■ Updated the hand note in the "BST Operation Control" section. ■ Changed "IDCODE JTAG Instruction" to read "IDCODE" as needed. ■ Minor text edits
November 2009	3.0	■ Updated Table 12–1 and Table 12–2. ■ Minor text edits.
June 2009	2.3	■ Added an introductory paragraph to increase search ability. ■ Removed the Conclusion section. ■ Minor text edits.
April 2009	2.2	■ Updated Table 12–1.
March 2009	2.1	■ Updated Table 12–1 and Table 12–2. ■ Removed "Referenced Documents" section.
November 2008	2.0	Minor text edits.
April 2010	1.0	Initial release.