8. JTAG Boundary-Scan Testing in MAX V Devices

MV51008-1.0

This chapter describes the IEEE Std.1149.1 (JTAG) boundary-scan testing for Altera® MAX® V devices. The IEEE Std. 1149.1 BST circuitry available in MAX V devices provides a cost-effective and efficient way to test systems that contain devices with tight lead spacing. Circuit boards with Altera and other IEEE Std. 1149.1-compliant devices can use `EXTEST`, `SAMPLE/PRELOAD`, and `BYPASS` modes to create serial patterns that internally test the pin connections between devices and check device operation.

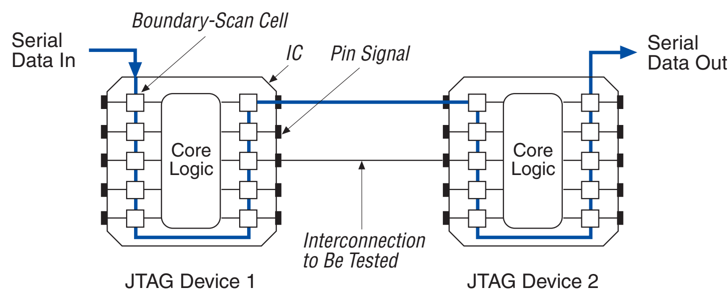
As PCBs become more complex, the requirement for thorough testing becomes increasingly important. Advances in surface-mount packaging and PCB manufacturing have resulted in smaller boards, making traditional test methods (for example, external test probes and "bed-of-nails" test fixtures) harder to implement. As a result, cost savings from PCB space reductions are sometimes offset by cost increases in traditional testing methods.

In the 1980s, JTAG developed a specification for boundary-scan testing that was later standardized as the IEEE Std. 1149.1 specification. This boundary-scan test (BST) architecture offers the capability to efficiently test components on PCBs with tight lead spacing.

BST architecture can test pin connections without using physical test probes and capture functional data while a device is operating normally. Boundary-scan cells (BSCs) in a device can force signals onto pins, or capture data from pin or core logic signals. Forced test data is serially shifted into the BSCs. Captured data is serially shifted out and externally compared to expected results.

Figure 8–1 shows the concept of boundary-scan testing.

Figure 8–1. IEEE Std. 1149.1 Boundary-Scan Testing



This chapter describes the following topics:

- "IEEE Std. 1149.1 BST Architecture" on page 8–2
- "IEEE Std. 1149.1 Boundary-Scan Register" on page 8–3
- "IEEE Std. 1149.1 BST Operation Control" on page 8–6
- "I/O Voltage Support in the JTAG Chain" on page 8–13
- "Boundary-Scan Test for Programmed Devices" on page 8–14

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■ "Disabling IEEE Std. 1149.1 BST Circuitry" on page 8–15
■ "Guidelines for IEEE Std. 1149.1 Boundary-Scan Testing" on page 8–15
■ "Boundary-Scan Description Language Support" on page 8–15

In addition to BST, you can use the IEEE Std. 1149.1 controller for in-system programming for MAX V devices. MAX V devices support IEEE 1532 programming, which uses the IEEE Std. 1149.1 test access port (TAP) interface. However, this chapter only describes the BST feature of the IEEE Std. 1149.1 circuitry.

IEEE Std. 1149.1 BST Architecture

A MAX V device operating in IEEE Std. 1149.1 BST mode uses four required pins, TDI, TDO, TMS, and TCK.

Table 8–1 lists the functions of each of these pins. MAX V devices do not have a TRST pin.

Table 8–1. IEEE Std. 1149.1 Pin Descriptions

Pin	Description	Function
TDI *(1)*	Test data input	Serial input pin for instructions as well as test and programming data. Data is shifted in on the rising edge of TCK.
TDO	Test data output	Serial data output pin for instructions as well as test and programming data. Data is shifted out on the falling edge of TCK. The pin is tri-stated if data is not being shifted out of the device.
TMS *(1)*	Test mode select	Input pin that provides the control signal to determine the transitions of the TAP controller state machine. Transitions within the state machine occur at the rising edge of TCK. Therefore, you must set up the TMS before the rising edge of TCK. TMS is evaluated on the rising edge of TCK.
TCK *(2)*	Test clock input	The clock input to the BST circuitry. Some operations occur at the rising edge, while others occur at the falling edge.

Notes to Table 8–1:

(1) The TDI and TMS pins have internal weak pull-up resistors.

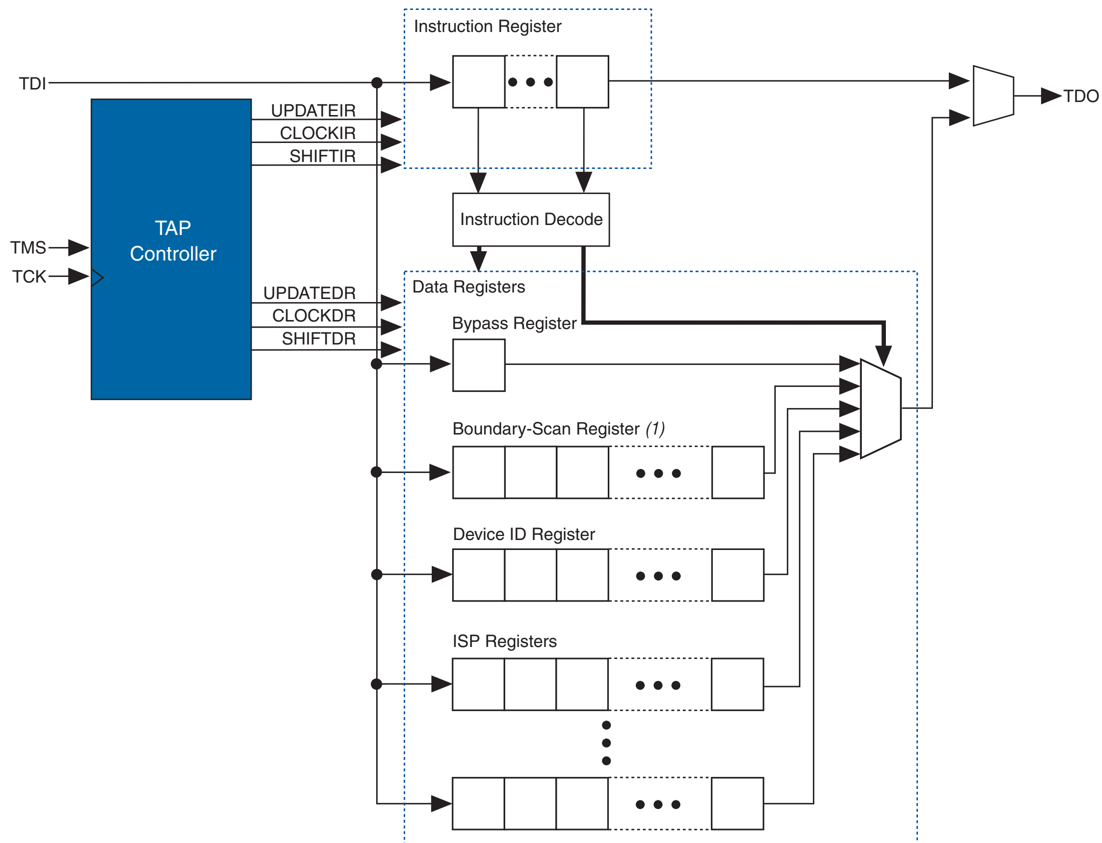
(2) The TCK pin has an internal weak pull-down resistor.

The IEEE Std. 1149.1 BST circuitry requires the following registers:

- The instruction register determines which action to perform and which data register to access.
- The bypass register (which is a 1-bit long data register) provides a minimum-length serial path between the TDI and TDO pins.
- The boundary-scan register that is a shift register composed of all the BSCs of the device.

Figure 8–2 shows a functional model of the IEEE Std. 1149.1 circuitry.

Figure 8–2. IEEE Std. 1149.1 Circuitry



Note to Figure 8–2:

(1) For the boundary-scan register length in MAX V devices, refer to the *JTAG and In-System Programmability in MAX V Devices* chapter.

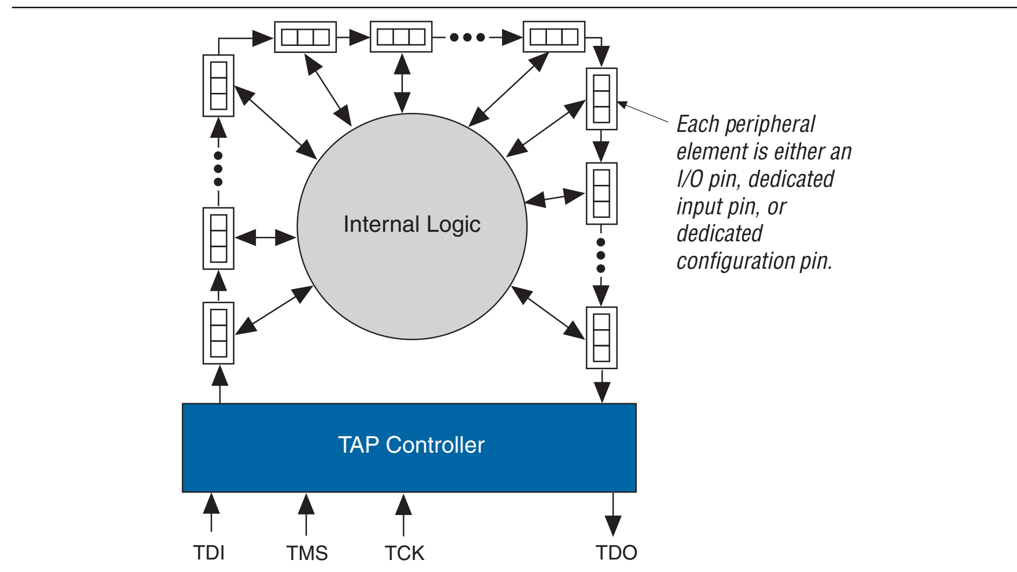
The TAP controller controls the IEEE Std. 1149.1 boundary-scan testing, as described in "IEEE Std. 1149.1 BST Operation Control" on page 8–6. The `TMS` and `TCK` pins operate the TAP controller and the `TDI` and `TDO` pins provide the serial path for the data registers. The `TDI` pin also provides data to the instruction register, which then generates the control logic for the data registers.

IEEE Std. 1149.1 Boundary-Scan Register

The boundary-scan register is a large serial shift register that uses the `TDI` pin as an input and the `TDO` pin as an output. The boundary-scan register consists of 3-bit peripheral elements that are associated with the I/O pins of the MAX V devices. You can use the boundary-scan register to test the external pin connections or to capture internal data.

Figure 8–3 shows how test data is serially shifted around the periphery of the IEEE Std. 1149.1 device.

Figure 8–3. Boundary-Scan Register



Boundary-Scan Cells of a MAX V Device I/O Pin

Except for the four JTAG pins and power pins, you can use all the pins of a MAX V device (including clock pins) as user I/O pins and have a BSC. The 3-bit BSC consists of a set of capture registers and a set of update registers. The capture registers can connect to internal device data through the OUTJ and OEJ signals, while the update registers connect to external data through the PIN_OUT and PIN_OE signals. The TAP controller internally generates the SHIFT, CLOCK, and UPDATE global control signals for the IEEE Std. 1149.1 BST registers; a decode of the instruction register generates the MODE signal. The data signal path for the boundary-scan register runs from the serial data in (SDI) signal to the serial data out (SDO) signal. The scan register begins at the TDI pin and ends at the TDO pin of the device.

Figure 8–4 shows the user I/O BSC for MAX V devices.

Figure 8–4. User I/O BSC with IEEE Std. 1149.1 BST Circuitry for MAX V Devices

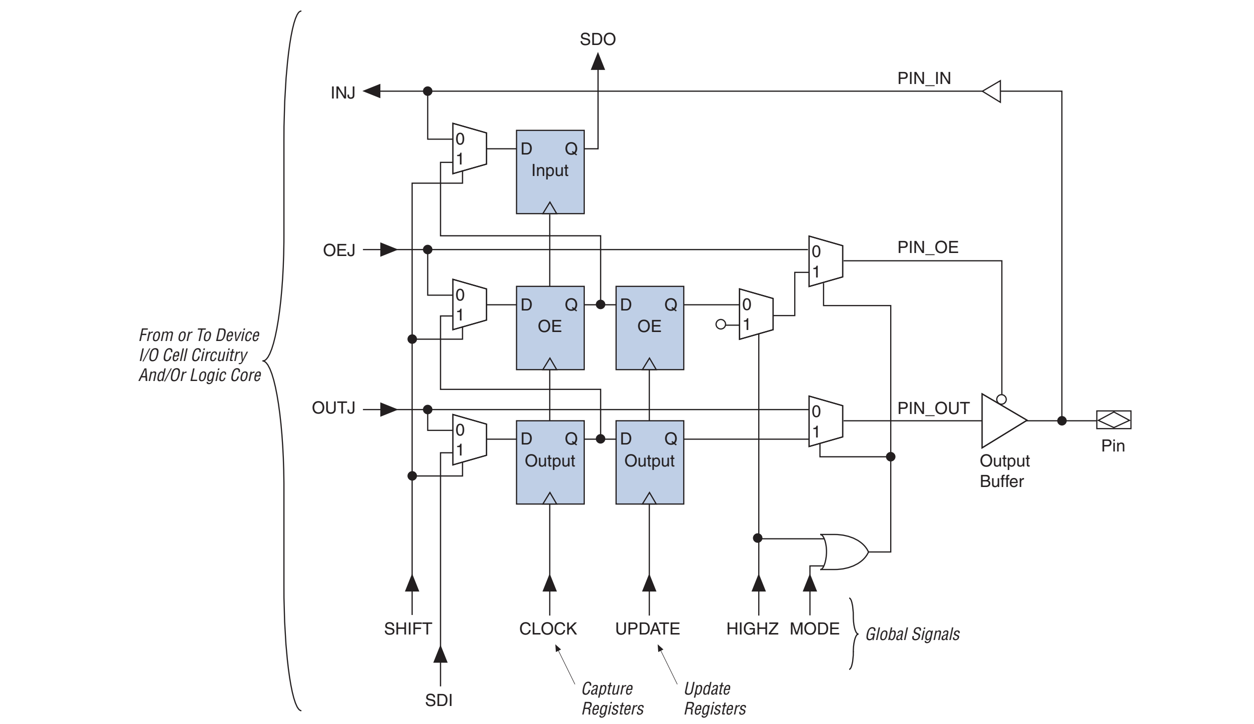


Table 8–2 lists the capture and update register capabilities of all BSC within MAX V devices.

Table 8–2. BSC Description for MAX V Devices ***(Note 1)***

Pin Type	Captures			Drives			Notes
	Output Capture Register	OE Capture Register	Input Capture Register	Output Update Register	OE Update Register	Input Update Register	
User I/O	OUTJ	OEJ	PIN_IN	PIN_OUT	PIN_OE	—	Includes user clocks

Note to Table 8–2:

(1) TDI, TDO, TMS, and TCK pins and all VCC and GND pin types do not have BSCs.

JTAG Pins and Power Pins

MAX V devices do not have BSCs for dedicated JTAG pins (TDI, TDO, TMS, and TCK) and power pins (VCCINT, VCCIO, GNDINT, and GNDIO).

IEEE Std. 1149.1 BST Operation Control

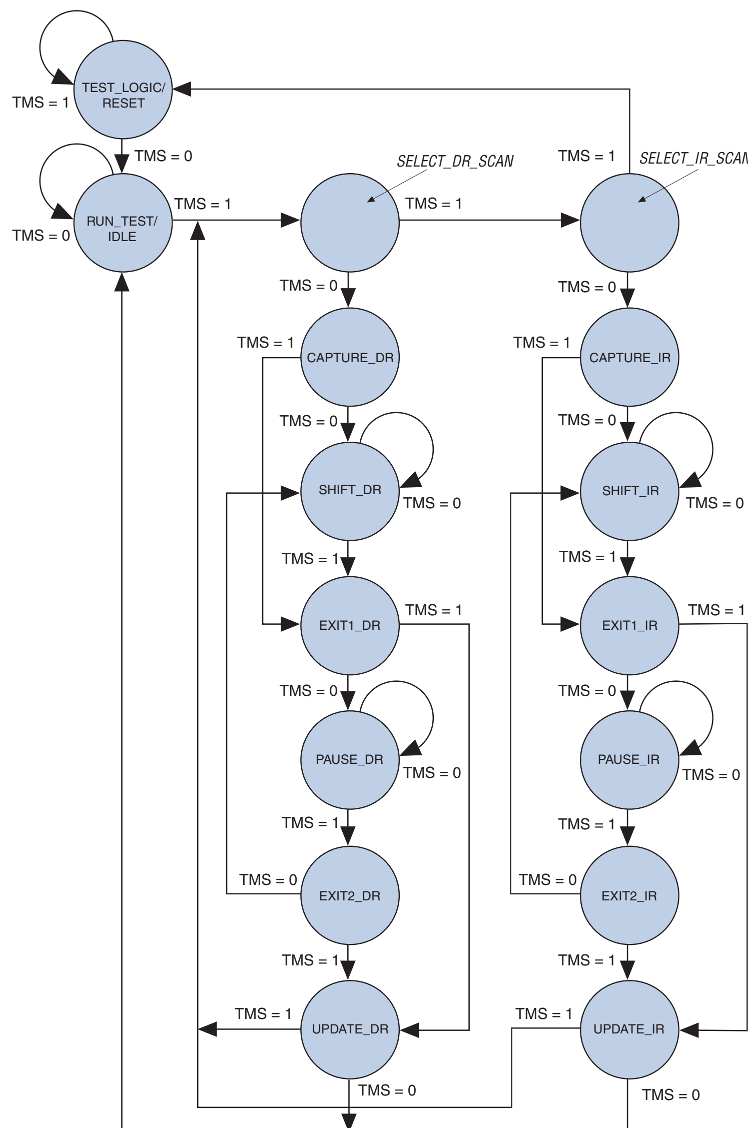
MAX V devices implement the `SAMPLE/PRELOAD`, `EXTEST`, `BYPASS`, `IDCODE`, `USERCODE`, `CLAMP` and `HIGHZ` IEEE Std. 1149.1 BST instructions. The length of the BST instructions is 10 bits. These instructions are described in detail later in this chapter.

For a summary of the BST instructions and their instruction codes, refer to the *JTAG and In-System Programmability in MAX V Devices* chapter.

The IEEE Std. 1149.1 TAP controller, a 16-state state machine clocked on the rising edge of `TCK`, uses the `TMS` pin to control IEEE Std. 1149.1 operation in the device.

Figure 8–5 shows the TAP controller state machine.

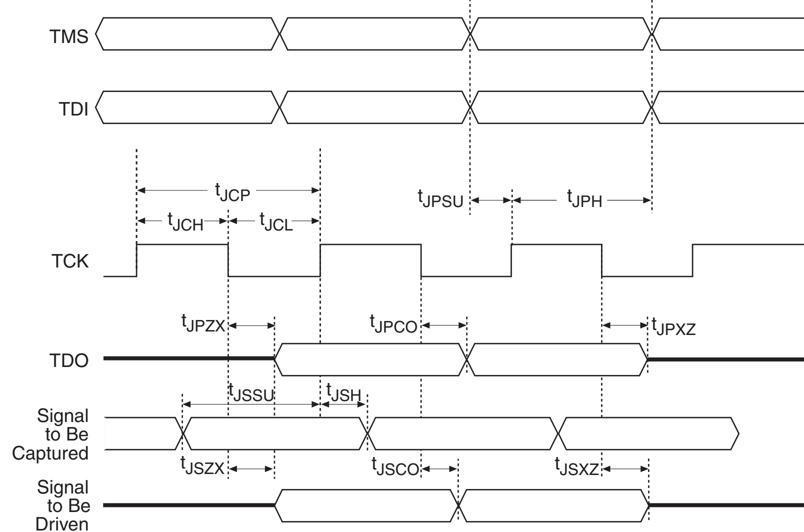
Figure 8–5. IEEE Std. 1149.1 TAP Controller State Machine



When the TAP controller is in the TEST_LOGIC/RESET state, the BST circuitry is disabled, the device is in normal operation, and the instruction register is initialized with IDCODE as the initial instruction. During device power up, the TAP controller starts in this TEST_LOGIC/RESET state. In addition, the TAP controller may be forced to the TEST_LOGIC/RESET state by holding TMS high for five TCK clock cycles. After the TEST_LOGIC/RESET state, the TAP controller remains in this state as long as TMS continues to be held high while TCK is clocked.

Figure 8–6 shows the timing requirements for the IEEE Std. 1149.1 signals.

Figure 8–6. IEEE Std. 1149.1 Timing Waveforms *(Note 1)*



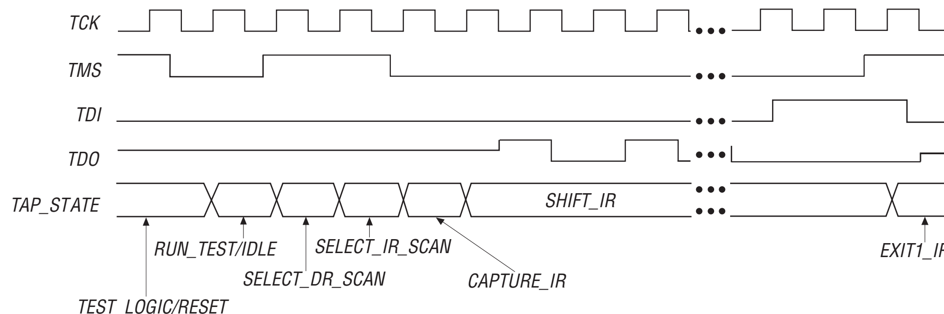
Note to Figure 8–6:

(1) For timing parameter values, refer to the *DC and Switching Characteristics for MAX V Devices* chapter.

To start the IEEE Std. 1149.1 operation, select an instruction mode by advancing the TAP controller to the shift instruction register (SHIFT_IR) state and shift in the appropriate instruction code on the TDI pin.

Figure 8–7 shows the entry of the instruction code into the instruction register. From the RESET state, TMS is clocked with the pattern 01100 to advance the TAP controller to SHIFT_IR state.

Figure 8–7. Selecting the Instruction Mode



The TDO pin is tri-stated in all states except the SHIFT_IR and SHIFT_DR states. The TDO pin is activated at the first falling edge of TCK after entering either of the shift states and is tri-stated at the first falling edge of TCK after leaving either of the shift states.

When the SHIFT_IR state is activated, TDO is no longer tri-stated, and the initial state of the instruction register is shifted out on the falling edge of TCK. TDO continues to shift out the contents of the instruction register as long as the SHIFT_IR state is active. The TAP controller remains in the SHIFT_IR state as long as TMS remains low.

During the SHIFT_IR state, an instruction code is entered by shifting data on the TDI pin on the rising edge of TCK. You must clock the last bit of the OPCODE at the same time that the next state, EXIT1_IR, is activated; EXIT1_IR is entered by clocking a logic high on TMS. After in the EXIT1_IR state, TDO becomes tri-stated again. TDO is always tri-stated except in the SHIFT_IR and SHIFT_DR states. After an instruction code is entered correctly, the TAP controller advances to perform the serial shifting of test data in one of three modes (SAMPLE/PRELOAD, EXTEST, or BYPASS).

For MAX V devices, there are weak pull-up resistors for TDI and TMS, and pull-down resistors for TCK. However, in a JTAG chain, there might be some devices that do not have internal pull-up or pull-down resistors. In this case, Altera recommends pulling the TMS pin high (through an external 10-kΩ resistor), and pulling TCK low (through an external 1-kΩ resistor) during BST or in-system programmability (ISP) to prevent the TAP controller from going into an unintended state. Pulling-up the TDI signal externally for the MAX V device is optional.

For more information about the pull-up and pull-down resistors, refer to *AN 100: In-System Programmability Guidelines*.

SAMPLE/PRELOAD Instruction Mode

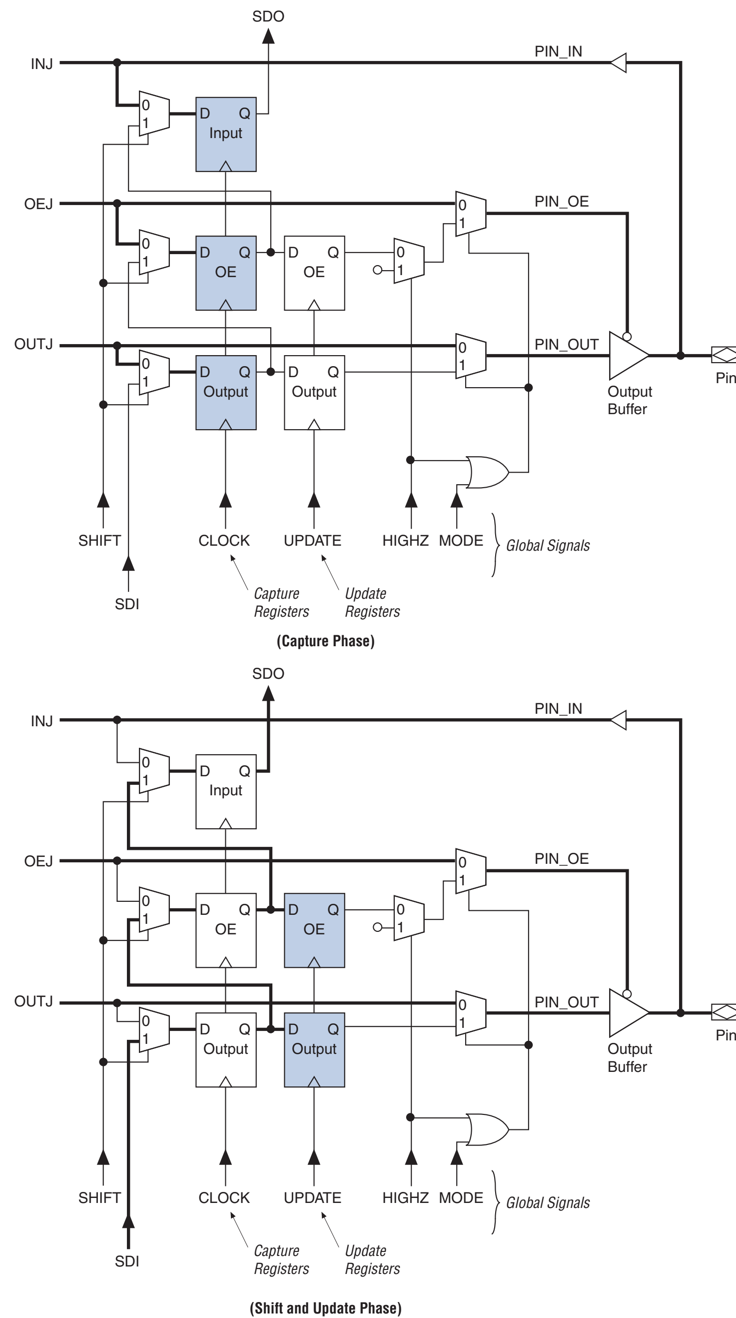
SAMPLE/PRELOAD instruction mode allows you to take a snapshot of device data without interrupting normal device operation. However, SAMPLE/PRELOAD instruction mode is most often used to preload the test data into the update registers before loading the EXTEST instruction.

During the capture phase, multiplexers preceding the capture registers select the active device data signals and clocked data into the capture registers. The multiplexers at the outputs of the update registers also select active device data to prevent functional interruptions to the device.

During the shift phase, the boundary-scan shift register is formed by clocking data through capture registers around the device periphery and then out of the TDO pin. New test data can simultaneously be shifted into TDI and replace the contents of the capture registers. During the update phase, data in the capture registers is transferred to the update registers.You can then use this data in EXTEST instruction mode. For more information, refer to "EXTEST Instruction Mode" on page 8–10.

Figure 8–8 shows the capture, shift, and update phases of SAMPLE/PRELOAD mode.

Figure 8–8. IEEE Std. 1149.1 BST SAMPLE/PRELOAD Mode



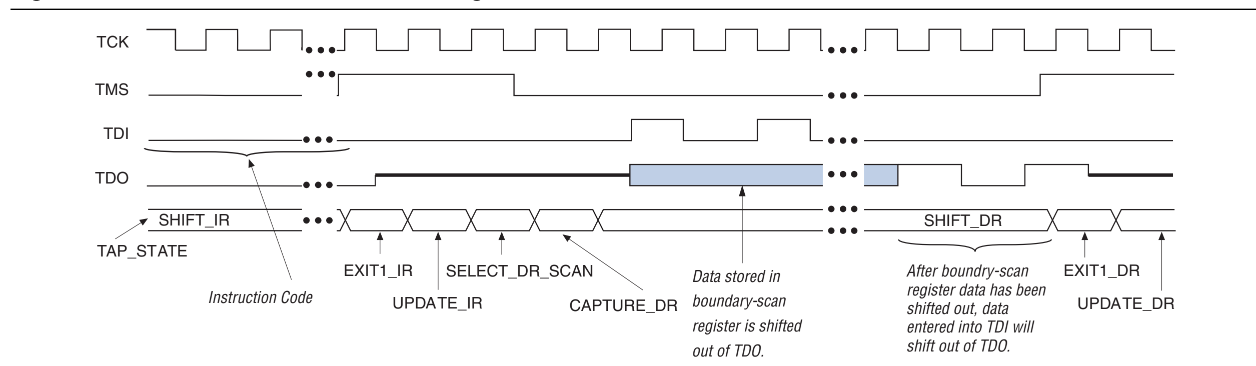
SAMPLE/PRELOAD instruction code shifts in through the TDI pin. The TAP controller advances to the CAPTURE_DR state and then to the SHIFT_DR state, where it remains if TMS is held low. The data shifted out of the TDO pin consists of the data that was present in the capture registers after the capture phase. New test data shifted into the TDI pin appears at the TDO pin after being clocked through the entire boundary-scan register.

Figure 8–9 shows that the test data that shifted into TDI does not appear at the TDO pin until after the capture register data that is shifted out. If TMS is held high on two consecutive TCK clock cycles, the TAP controller advances to the UPDATE_DR state for the update phase.

If you enable the device output enable feature but the DEV_OE pin is not asserted during boundary-scan testing, the output enable boundary-scan registers of the BSCs capture data from the core of the device during SAMPLE/PRELOAD. These values are not high impedance, although the I/O pins are tri-stated.

Figure 8–9 shows the SAMPLE/PRELOAD waveforms.

Figure 8–9. SAMPLE/PRELOAD Shift Data Register Waveforms



EXTEST Instruction Mode

Use EXTEST instruction mode to check the external pin connections between devices. Unlike SAMPLE/PRELOAD mode, EXTEST allows test data to be forced onto the pin signals. By forcing known logic high and low levels on output pins, you can detect opens and shorts at pins of any device in the scan chain.

EXTEST selects data differently than SAMPLE/PRELOAD. EXTEST chooses data from the update registers as the source of the output and output enable signals. After the EXTEST instruction code is entered, the multiplexers select the update register data; thus, you can force the data stored in these registers from a previous EXTEST or SAMPLE/PRELOAD test cycle onto the pin signals. In the capture phase, the results of this test data are stored in the capture registers and then shifted out of TDO during the shift phase. You can store the new test data in the update registers during the update phase.

Figure 8–10 shows the capture, shift, and update phases of `EXTEST` mode.

Figure 8–10. IEEE Std. 1149.1 BST EXTEST Mode

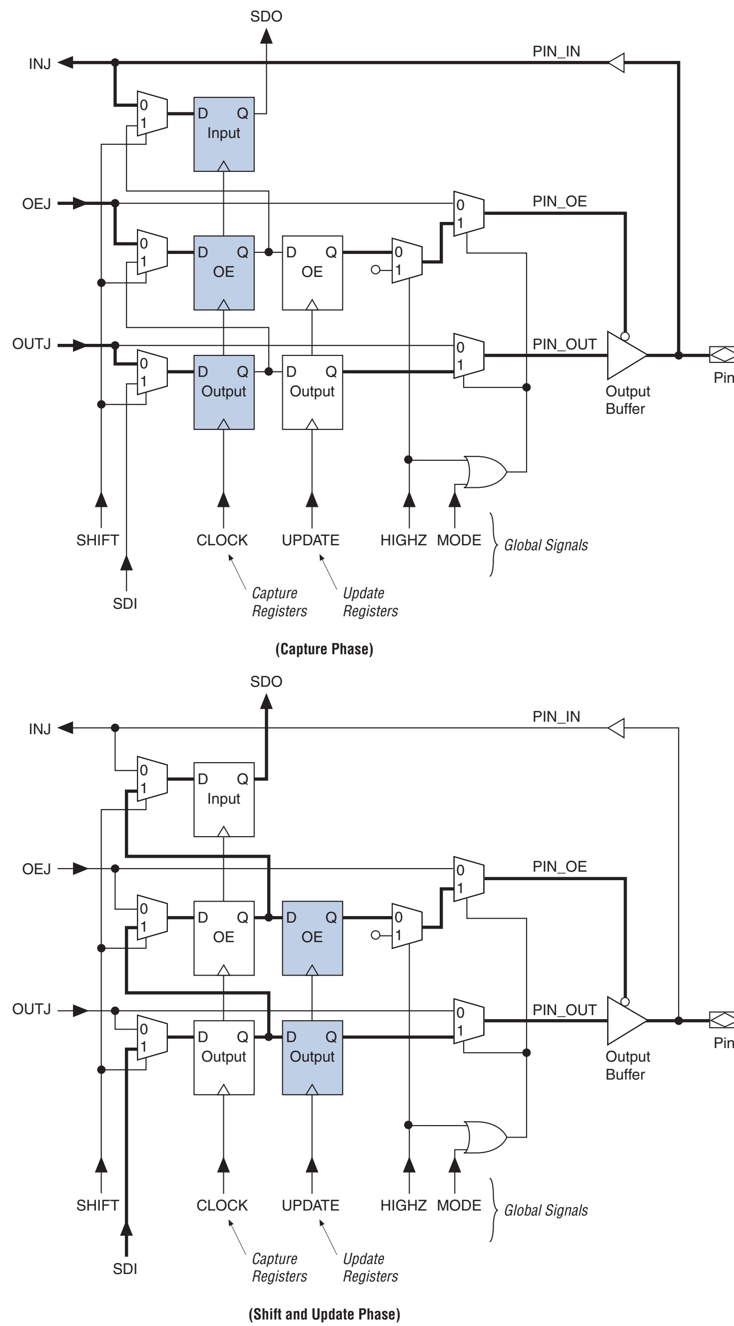
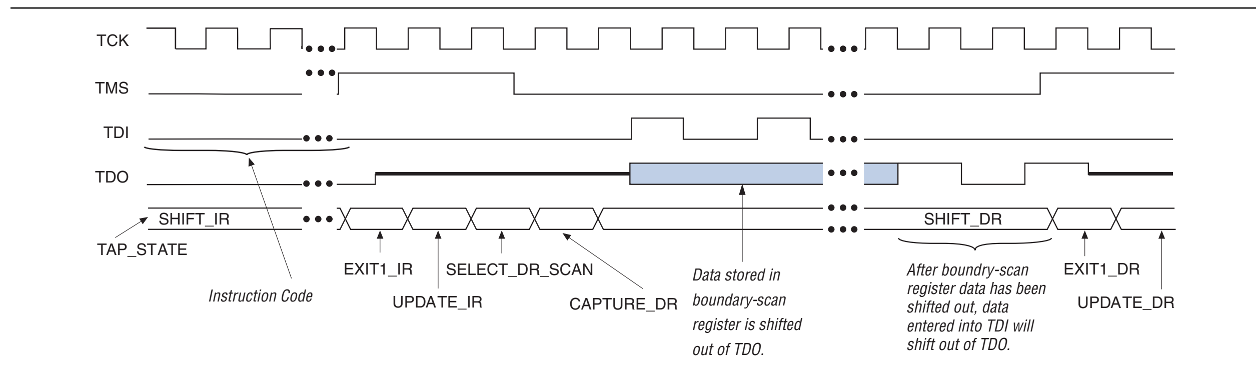


Figure 8–11 resembles the SAMPLE/PRELOAD waveform diagram, except that the instruction code for EXTEST is different. The data shifted out of TDO consists of the data that was present in the capture registers after the capture phase. New test data shifted into the TDI pin appears at the TDO pin after being clocked through the entire boundary-scan register.

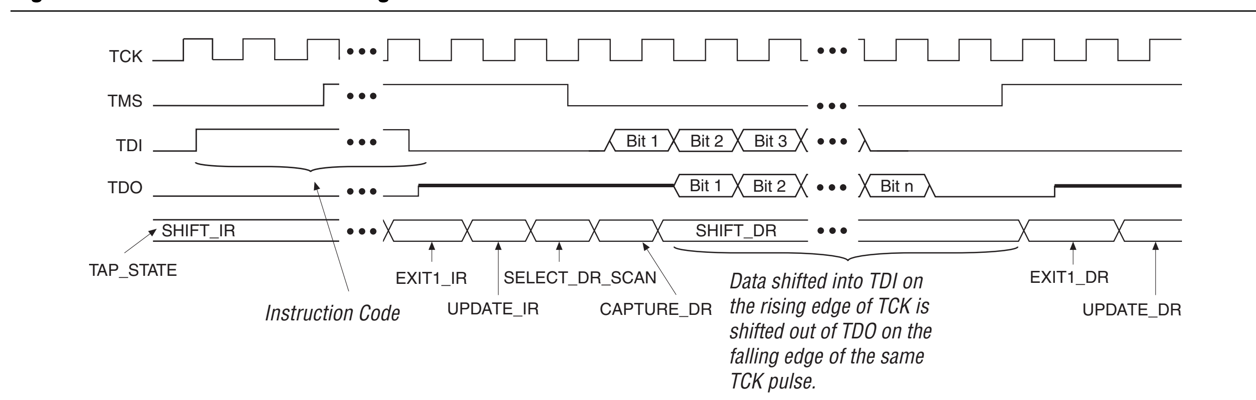
Figure 8–11. EXTEST Shift Data Register Waveforms



BYPASS Instruction Mode

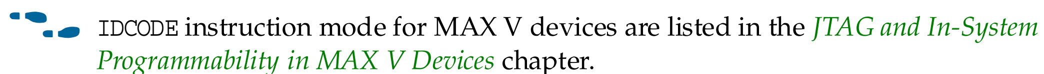
You can activate BYPASS instruction mode with an instruction code made up of only ones. Figure 8–12 shows how scan data passes through a device after the TAP controller is in the SHIFT_DR state. In this state, data signals are clocked into the bypass register from TDI on the rising edge of TCK and out of TDO on the falling edge of the same clock pulse.

Figure 8–12. BYPASS Shift Data Register Waveforms



IDCODE Instruction Mode

Use IDCODE instruction mode to identify the devices in an IEEE Std. 1149.1 chain. When you select IDCODE, the device identification register loads with the 32-bit vendor-defined identification code. The device ID register is connected between the TDI and TDO ports and the device IDCODE is shifted out.


IDCODE instruction mode for MAX V devices are listed in the *JTAG and In-System Programmability in MAX V Devices* chapter.

USERCODE Instruction Mode

Use USERCODE instruction mode to examine the user electronic signature (UES) within the devices along an IEEE Std. 1149.1 chain. When you select this instruction, the device identification register is connected between the TDI and TDO ports. The user-defined UES shifts into the device ID register in parallel from the 32-bit USERCODE register. The UES then shifts out through the device ID register. The USERCODE information is only available after the device is successfully configured.

Non-volatile USERCODE data is written to the configuration flash memory (CFM) block and then written to the SRAM at power up. The USERCODE instruction reads the data values from the SRAM. When you use real-time ISP to update the CFM block and write new USERCODE data, executing the USERCODE instruction returns the USERCODE of the current running design (stored in the SRAM), not the new USERCODE data. The USERCODE of the new design (stored in the CFM) can only be read back correctly if a power cycle or forced SRAM download has transpired after the real-time ISP update.

In the Quartus® II software, there is an Auto Usercode feature where you can choose to use the checksum value of a programming file as the JTAG user code. If selected, the checksum is automatically loaded to the USERCODE register.

To enable the Auto Usercode feature, follow these steps:

1. On the Assignments menu, click **Device**.
2. In the Device dialog box, click **Device and Pin Options** and click the General tab.
3. Turn on **Auto Usercode**.

CLAMP Instruction Mode

Use CLAMP instruction mode to allow the state of the signals driven from the pins to be determined from the boundary-scan register while the bypass register is selected as the serial path between the TDI and Tmv51008.fmDO ports. Data held in the boundary-scan register completely defines the state of all signals driven from the output pins. However, CLAMP instruction mode will not override the I/O weak pull-up resistor or the I/O bus hold if you have any of them selected.

HIGHZ Instruction Mode

Use HIGHZ instruction mode to set all of the user I/O pins to an inactive drive state. These pins are tri-stated until you execute a new JTAG instruction. When you select this instruction, the bypass register is connected between the TDI and TDO ports. HIGHZ instruction mode will not override the I/O weak pull-up resistor or I/O bus hold if you have any of them selected.

I/O Voltage Support in the JTAG Chain

There can be several different Altera or non-Altera devices in a JTAG chain. However, you must pay attention to whether or not the chain contains devices with different V_{CCIO} levels. The TDO pin of a device drives out at the voltage level according to the V_{CCIO} of the device. For MAX V devices, the TDO pin drives out at the voltage level according to the V_{CCIO} of I/O Bank 1. Although the devices may have different V_{CCIO}

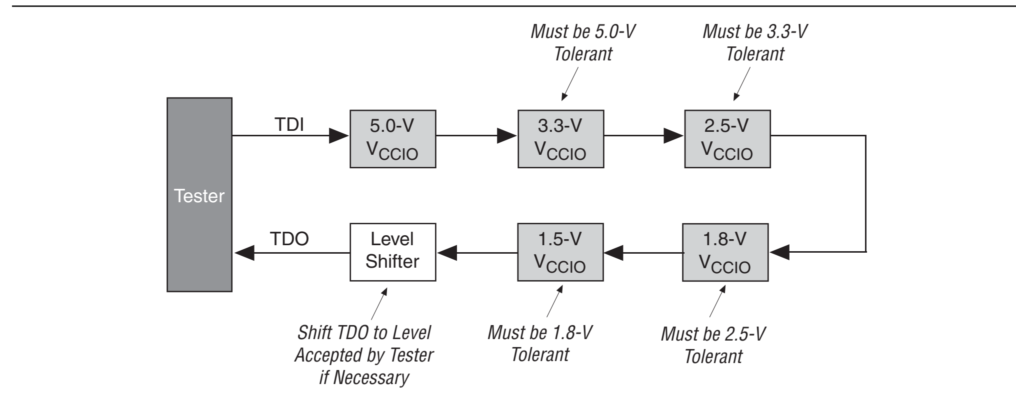
levels, the devices can interface with each other. For example, a device with 3.3-V V_{CCIO} can drive to a device with 5.0-V V_{CCIO} because 3.3 V meets the minimum V_{IH} on transistor-to-transistor logic (TTL)-level input for the 5.0-V V_{CCIO} device. JTAG pins on MAX V devices can support 1.5-, 1.8-, 2.5-, or 3.3-V input levels, depending on the V_{CCIO} voltage of I/O Bank 1.

For more information about MultiVolt I/O support, refer to the *MAX V Device Architecture* chapter.

You can interface the `TDI` and `TDO` lines of the JTAG pins of devices that have different V_{CCIO} levels by inserting a level shifter between the devices. If possible, the JTAG chain must be built such that a device with a higher V_{CCIO} level drives to a device with an equal or lower V_{CCIO} level. By building the JTAG chain in this manner, a level shifter may be required only to shift the `TDO` level to a level acceptable to the JTAG tester.

Figure 8–13 shows the JTAG chain of mixed voltages and how a level shifter is inserted in the chain.

Figure 8–13. JTAG Chain of Mixed Voltages



Boundary-Scan Test for Programmed Devices

For a programmed device, the input buffers are turned off by default for I/O pins that are set as output only in the design file. You cannot sample on the programmed device output pins with the default boundary-scan description language (BSDL) file when the input buffers are turned off.

For boundary-scan testing, you can set the Quartus II software to always enable the input buffers on a programmed device so it behaves the same as an unprogrammed device, allowing sample function on output pins in the design. This aspect can cause slight increase in standby current as the unused input buffer is always on.

To enable the unused input buffers on a programmed device, follow these steps:

1. On the Assignments menu, click **Settings.**
2. Under **Category**, select **Assembler**.
3. Turn on **Always Enable Input Buffers**.

Disabling IEEE Std. 1149.1 BST Circuitry

You can enable the IEEE Std. 1149.1 BST circuitry for MAX V devices after device powers up. You must enable this circuitry only if you use the BST or ISP features. This section describes how to disable the IEEE Std. 1149.1 circuitry to ensure that the circuitry is not inadvertently enabled when it is not required.

Table 8–3 lists the pin connections necessary for disabling JTAG in MAX V devices that have dedicated IEEE Std. 1149.1 pins.

Table 8–3. Disabling IEEE Std. 1149.1 Circuitry for MAX V Devices

JTAG Pins *(1)*			
TMS	TCK	TDI	TDO
VCC *(2)*	GND *(3)*	VCC *(2)*	Leave Open

Notes to Table 8–3:

(1) There is no software option to disable JTAG in MAX V devices. The JTAG pins are dedicated.

(2) VCC refers to V_{CCIO} of Bank 1.

(3) The TCK signal may also be tied high. If TCK is tied high, power-up conditions must ensure that TMS is pulled high before TCK. Pulling TCK low avoids this power-up condition.

Guidelines for IEEE Std. 1149.1 Boundary-Scan Testing

When performing boundary-scan testing with IEEE Std. 1149.1 devices, use the following guidelines:

- If a pattern (for example, a 10-bit 1010101010 pattern) does not shift out of the instruction register through the TDO pin during the first clock cycle of the SHIFT_IR state, the proper TAP controller state has not been reached. To solve this problem, try one of the following procedures:
  - Verify that the TAP controller has reached the SHIFT_IR state correctly. To advance the TAP controller to the SHIFT_IR state, return to the RESET state and clock the code 01100 on the TMS pin.
  - Check the connections to the VCC, GND, and JTAG pins on the device.
- Perform a SAMPLE/PRELOAD test cycle before the first EXTEST test cycle to ensure that known data is present at the device pins when EXTEST mode is entered. If the OEJ update register contains a 0, the data in the OUTJ update register will be driven out. The state must be known and correct to avoid contention with other devices in the system.
- Do not perform EXTEST and SAMPLE/PRELOAD tests during ISP. These instructions are supported before and after ISP but not during ISP.

If problems persist, contact Technical Support.

Boundary-Scan Description Language Support

The BSDL—a subset of VHDL—provides a syntax that allows you to describe the features of an IEEE Std. 1149.1 BST-capable device that can be tested. Test software development systems then use the BSDL files for test generation, analysis, failure diagnostics, and in-system programming.

For more information, or to receive BSDL files for IEEE Std. 1149.1-compliant MAX V devices, refer to the IEEE 1149.1 BSDL Files page on the Altera website.

Document Revision History

Table 8–4 shows the revision history for this chapter.

Table 8–4. Document Revision History

Date	Version	Changes
December 2010	1.0	Initial release.