10. JTAG Boundary-Scan Testing for Cyclone IV Devices

CYIV-51010-1.3

This chapter describes the boundary-scan test (BST) features that are supported in Cyclone® IV devices. The features are similar to Cyclone III devices, unless stated in this chapter.

Cyclone IV devices (Cyclone IV E devices and Cyclone IV GX devices) support IEEE Std. 1149.1. Cyclone IV GX devices also support IEEE Std. 1149.6. The IEEE Std. 1149.6 (AC JTAG) is only supported on the high-speed serial interface (HSSI) transceivers in Cyclone IV GX devices. The purpose of IEEE Std. 1149.6 is to enable board-level connectivity checking between transmitters and receivers that are AC coupled.

This chapter includes the following sections:

For more information about the JTAG instructions code with descriptions and IEEE Std.1149.1 BST guidelines, refer to the *IEEE 1149.1 (JTAG) Boundary-Scan Testing for Cyclone III Devices* chapter.

For more information about the following topics, refer to *AN 39: IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices*:

- IEEE Std. 1149.1 BST architecture and circuitry
- TAP controller state-machine
- Instruction mode

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IEEE Std. 1149.6 Boundary-Scan Register

The boundary-scan cell (BSC) for HSSI transmitters (GXB_TX[p,n]) and receivers (GXB_RX[p,n]) in Cyclone IV GX devices are different from the BSCs for I/O pins.

Figure 10–1 shows the Cyclone IV GX HSSI transmitter boundary-scan cell.

Figure 10–1. HSSI Transmitter BSC with IEEE Std. 1149.6 BST Circuitry for Cyclone IV GX Devices

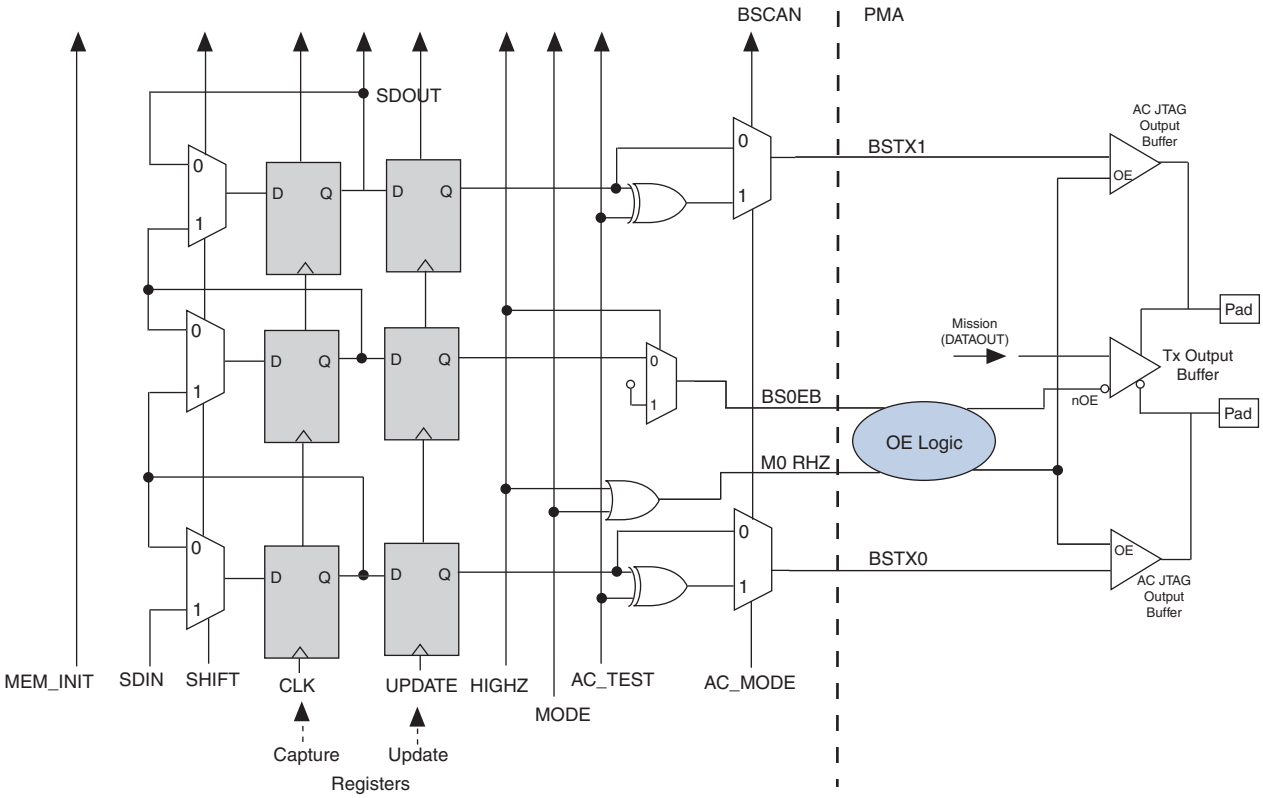
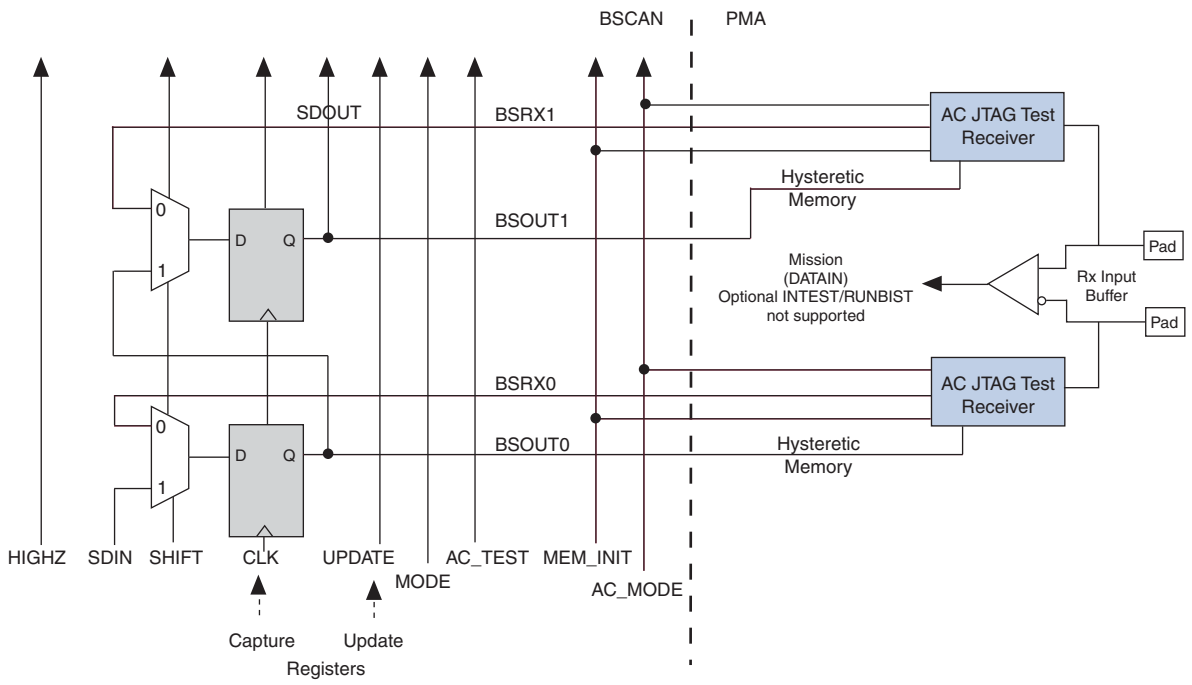


Figure 10–2 shows the Cyclone IV GX HSSI receiver BSC.

Figure 10–2. HSSI Receiver BSC with IEEE Std. 1149.6 BST Circuitry for the Cyclone IV GX Devices



For more information about Cyclone IV devices user I/O boundary-scan cells, refer to the *IEEE 1149.1 (JTAG) Boundary-Scan Testing for Cyclone III Devices* chapter.

BST Operation Control

Table 10–1 lists the boundary-scan register length for Cyclone IV devices.

Table 10–1. Boundary-Scan Register Length for Cyclone IV Devices (Part 1 of 2)

Device	Boundary-Scan Register Length
EP4CE6	603
EP4CE10	603
EP4CE15	1080
EP4CE22	732
EP4CE30	1632
EP4CE40	1632
EP4CE55	1164
EP4CE75	1314
EP4CE115	1620
EP4CGX15	260
EP4CGX22	494
EP4CGX30 (1)	494
EP4CGX50	1006

Table 10–1. Boundary-Scan Register Length for Cyclone IV Devices (Part 2 of 2)

Device	Boundary-Scan Register Length
EP4CGX75	1006
EP4CGX110	1495
EP4CGX150	1495

Note to Table 10–1:

(1) For the F484 package of the EP4CGX30 device, the boundary-scan register length is 1006.

Table 10–2 lists the IDCODE information for Cyclone IV devices.

Table 10–2. IDCODE Information for 32-Bit Cyclone IV Devices

Device	IDCODE (32 Bits) (1)			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer Identity (11 Bits)	LSB (1 Bit) (2)
EP4CE6	0000	0010 0000 1111 0001	000 0110 1110	1
EP4CE10	0000	0010 0000 1111 0001	000 0110 1110	1
EP4CE15	0000	0010 0000 1111 0010	000 0110 1110	1
EP4CE22	0000	0010 0000 1111 0011	000 0110 1110	1
EP4CE30	0000	0010 0000 1111 0100	000 0110 1110	1
EP4CE40	0000	0010 0000 1111 0100	000 0110 1110	1
EP4CE55	0000	0010 0000 1111 0101	000 0110 1110	1
EP4CE75	0000	0010 0000 1111 0110	000 0110 1110	1
EP4CE115	0000	0010 0000 1111 0111	000 0110 1110	1
EP4CGX15	0000	0010 1000 0000 0001	000 0110 1110	1
EP4CGX22	0000	0010 1000 0001 0010	000 0110 1110	1
EP4CGX30 (3)	0000	0010 1000 0000 0010	000 0110 1110	1
EP4CGX30 (4)	0000	0010 1000 0010 0011	000 0110 1110	1
EP4CGX50	0000	0010 1000 0001 0011	000 0110 1110	1
EP4CGX75	0000	0010 1000 0000 0011	000 0110 1110	1
EP4CGX110	0000	0010 1000 0001 0100	000 0110 1110	1
EP4CGX150	0000	0010 1000 0000 0100	000 0110 1110	1

Notes to Table 10–2:

(1) The MSB is on the left.

(2) The IDCODE LSB is always 1.

(3) The IDCODE is applicable for all packages except for the F484 package.

(4) The IDCODE is applicable for the F484 package only.

IEEE Std.1149.6 mandates the addition of two new instructions: EXTEST_PULSE and EXTEST_TRAIN. These two instructions enable edge-detecting behavior on the signal path containing the AC pins.

EXTEST_PULSE

The instruction code for EXTEST_PULSE is 0010001111. The EXTEST_PULSE instruction generates three output transitions:

- Driver drives data on the falling edge of TCK in UPDATE_IR/DR.
- Driver drives inverted data on the falling edge of TCK after entering the RUN_TEST/IDLE state.
- Driver drives data on the falling edge of TCK after leaving the RUN_TEST/IDLE state.

If you use DC-coupling on HSSI signals, you must execute the EXTEST instruction. If you use AC-coupling on HSSI signals, you must execute the EXTEST_PULSE instruction. AC-coupled and DC-coupled HSSI are only supported in post-configuration mode.

EXTEST_TRAIN

The instruction code for EXTEST_TRAIN is 0001001111. The EXTEST_TRAIN instruction behaves the same as the EXTEST_PULSE instruction with one exception. The output continues to toggle on the TCK falling edge as long as the test access port (TAP) controller is in the RUN_TEST/IDLE state.

These two instruction codes are only supported in post-configuration mode for Cyclone IV GX devices.

When you perform JTAG boundary-scan testing before configuration, the nCONFIG pin must be held low.

I/O Voltage Support in a JTAG Chain

A Cyclone IV device operating in BST mode uses four required pins: TDI, TDO, TMS, and TCK. The TDO output pin and all JTAG input pins are powered by the V_{CCIO} power supply of I/O Banks (I/O Bank 9 for Cyclone IV GX devices and I/O Bank 1 for Cyclone IV E devices).

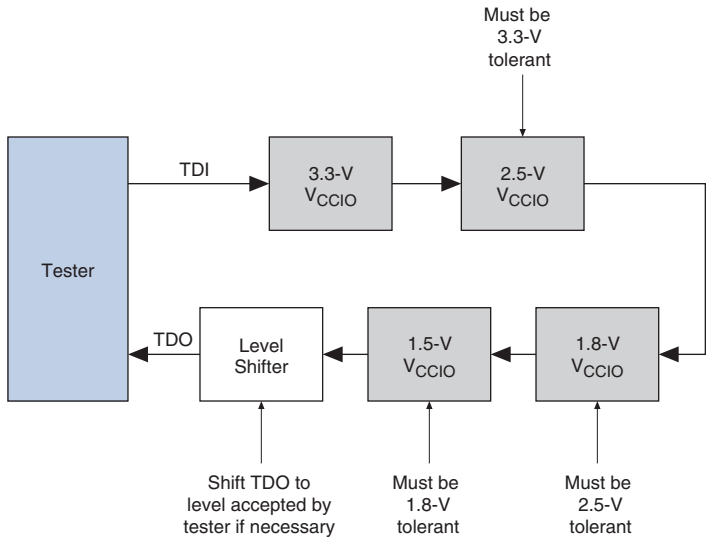
A JTAG chain can contain several different devices. However, you must use caution if the chain contains devices that have different V_{CCIO} levels. The output voltage level of the TDO pin must meet the specification of the TDI pin it drives. For example, a device with a 3.3-V TDO pin can drive a device with a 5.0-V TDI pin because 3.3 V meets the minimum TTL-level V_{IH} for the 5.0-V TDI pin.

For multiple devices in a JTAG chain with the 3.0-V/3.3-V I/O standard, you must connect a 25-Ω series resistor on a TDO pin driving a TDI pin.

You can also interface the TDI and TDO lines of the devices that have different V_{CCIO} levels by inserting a level shifter between the devices. If possible, the JTAG chain should have a device with a higher V_{CCIO} level driving a device with an equal or lower V_{CCIO} level. This way, a level shifter may be required only to shift the TDO level to a level acceptable to the JTAG tester.

Figure 10–3 shows the JTAG chain of mixed voltages and how a level shifter is inserted in the chain.

Figure 10–3. JTAG Chain of Mixed Voltages



Boundary-Scan Description Language Support

The boundary-scan description language (BSDL), a subset of VHDL, provides a syntax that allows you to describe the features of an IEEE Std. 1149.1/IEEE Std. 1149.6 BST-capable device that can be tested.

For more information about how to download BSDL files for IEEE Std. 1149.1-compliant Cyclone IV E devices, refer to *IEEE Std. 1149.1 BSDL Files*.

For more information about how to download BSDL files for IEEE Std. 1149.6-compliant Cyclone IV GX devices, refer to *IEEE Std. 1149.6 BSDL Files*.

You can also generate BSDL files (pre-configuration and post-configuration) for IEEE Std. 1149.1/IEEE Std. 1149.6-compliant Cyclone IV devices with the Quartus® II software version 9.1 SP1 and later. For more information about the procedure to generate BSDL files using the Quartus II software, refer to *BSDL Files Generation in Quartus II*.

Document Revision History

Table 10–3 lists the revision history for this chapter.

Table 10–3. Document Revision History

Date	Version	Changes
December 2013	1.3	■ Updated the "EXTEST_PULSE" section.
November 2011	1.2	■ Updated the "BST Operation Control" section. ■ Updated Table 10–2.
February 2010	1.1	■ Added Cyclone IV E devices in Table 10–1 and Table 10–2 for the Quartus II software version 9.1 SP1 release. ■ Updated Figure 10–1 and Figure 10–2. ■ Minor text edits.
November 2009	1.0	Initial release.