MegaCore IP Library

Release Notes and Errata

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RN-IP-7.3

Document last updated for Altera Complete Design Suite version: 10.1
Document publication date: March 2011

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About These Release Notes

These release notes cover versions 9.1 through 10.1 of the Altera® MegaCore® IP Library. The chapters in these release notes describe the revision history and errata for each product in the MegaCore IP Library.

From v8.0 onwards, this document replaces all individual IP product release notes and errata sheets that Altera previously published.

Errata are functional defects or errors, which may cause the product to deviate from published specifications. Documentation issues include errors, unclear descriptions, or omissions from current published specifications or product documents.

The product errata tables use the following indicators:

- A checkmark "✓" indicates an issue is applicable to that version
- "Fixed" indicates the issue was fixed in that version
- A dash "—" indicates the issue is not applicable to that version

For the most up-to-date errata for this release, refer to the latest version of the *MegaCore IP Library Release Notes* on the Altera website.

For more information about Quartus® II issues, refer to the *Quartus II Software Release Notes*.

Trademarks

These release notes use the following Altera trademarks:

- Arria® devices
- Avalon® interface
- Cyclone® devices
- HardCopy® devices
- MegaCore function
- MegaWizard™ Plug-In
- ModelSim® simulator
- Nios® II processor
- Quartus II software
- SignalTap® II logic analyzer
- Stratix® devices

System Requirements

The MegaCore IP Library is distributed with the Quartus II software and downloadable from the Altera website, www.altera.com.

For system requirements and installation instructions, refer to *Altera Software Installation and Licensing*.

Revision Dates

The chapters in this document, MegaCore IP Library Release Notes and Errata, were revised on the following dates.

Chapter 1. 8B10B Encoder/Decoder
Revised: *15 December 10*

Chapter 2. 10GBASE-R PHY
Revised: *15 January 2011*

Chapter 3. 10-Gbps Ethernet MAC
Revised: *15 December 2010*

Chapter 4. ASI
Revised: *15 February 2011*

Chapter 5. CIC
Revised: *15 March 2011*

Chapter 6. CPRI
Revised: *15 March 2011*

Chapter 7. CRC Compiler
Revised: *15 December 10*

Chapter 8. DDR and DDR2 SDRAM Controller Compiler
Revised: *15 December 10*

Chapter 9. DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP
Revised: *15 December 2010*

Chapter 10. DDR2 and DDR3 SDRAM Controller with UniPHY
Revised: *15 January 2011*

Chapter 11. DDR3 SDRAM Controller with ALTMEMPHY IP
Revised: *15 December 2010*

Chapter 12. FFT
Revised: *15 March 2011*

Chapter 13. FIR Compiler
Revised: *15 March 2011*

Chapter 14. FIR Compiler II

Revised: *15 December 2010*

Chapter 15. Interlaken
Revised: *15 January 2011*

Chapter 16. Interlaken PHY
Revised: *15 December 2010*

Chapter 17. NCO
Revised: *15 March 2011*

Chapter 18. Nios II Processor
Revised: *15 December 2010*

Chapter 19. PCI Compiler
Revised: *15 February 2011*

Chapter 20. PCI Express Compiler
Revised: *15 March 2011*

Chapter 21. POS-PHY Level 4
Revised: *15 March 2011*

Chapter 22. QDRII SRAM
Revised: *15 December 10*

Chapter 23. QDR II and QDR II+ SRAM Controller with UniPHY
Revised: *15 March 2011*

Chapter 24. RapidIO
Revised: *15 March 2011*

Chapter 25. Reed-Solomon Compiler
Revised: *15 March 2011*

Chapter 26. Reed-Solomon II
Revised: *15 December 2010*

Chapter 27. RLDRAM II
Revised: *15 December 10*

Chapter 28. RLDRAM II Controller with UniPHY
Revised: *15 March 2011*

Chapter 29. SDI
Revised: *15 February 2011*

Chapter 30. SerialLite II
Revised: *15 February 2011*

Chapter 31. Triple Speed Ethernet
Revised: *15 March 2011*

Chapter 32. Video and Image Processing Suite

Revised: *15 March 2011*

Chapter 33. Viterbi Compiler
Revised: *15 March 2011*

Chapter 34. XAUI PHY
Revised: *15 December 2010*

1. 8B10B Encoder/Decoder

Revision History

Table 1–1 shows the revision history for the 8B10B Encoder/Decoder MegaCore function.

For more information about the new features, refer to the *8B10B Encoder/Decoder MegaCore Function User Guide*.

Table 1–1. 8B10B Encoder/Decoder MegaCore Function Revision History

Version	Date	Description
10.1	December 2010	Final support for Stratix IV GT devices.
10.0	July 2010	Maintenance release.
9.1	November 2009	Preliminary support for Cyclone III LS and Cyclone IV devices.
9.0 SP1	May 2009	Preliminary support for HardCopy III and HardCopy IV E devices.
9.0	March 2009	Preliminary support for Arria II GX device family.

Errata

No known issues in v10.1, v10.0, and 9.1.

Revision History

Table 2–1 shows the revision history for the 10GBASE-R PHY IP core.

For more information about the new features, refer to the "10GBASE-R PHY IP Core" chapter in the *Altera Transceiver PHY IP Core User Guide*.

Table 2–1. 10GBASE-R PHY Revision History

Version	Date	Description
10.1	December 2010	Added Stratix V support.
10.0 SP1	September 2010	Added simulation support.
10.0	July 2010	First release.

Errata

Table 2–2 shows the issues that affect the 10GBASE-R PHY IP core versions 10.1 and 10.0.

Table 2–2. 10GBASE-R PHY Errata

Added or Updated	Issue	Affected Version	
		10.1	10.0
15 Jan 11	FIFO Full Signals Are Swapped	✓	✓
	rx_ready Bit Does not Update When Synchronization Is Lost	✓	✓
15 Dec 10	Incorrect Device Support Listed 10GBASE-R PHY IP Core User Guide	Fixed	✓
15 Dec 10	Mixed Language Simulation Fails when Optimization Is On	✓	—

FIFO Full Signals Are Swapped

The TX_FIFO_FULL and RX_FIFO_FULL status bits are swapped.

Affected Configurations

This issue affects Stratix IV and Stratix V implementations of the 10GBASE–R PHY.

Workaround

The workaround is to note that for the 10.1 release RX_FIFO_FULL is actually stored as bit 3 of address 0x82 and TX_FIFO_FULL is stored as bit 4 of address 0x82.

Solution Status

This issue will be fixed in a future version of the 10GBASE–R PHY IP core.

rx_ready Bit Does not Update When Synchronization Is Lost

The RX_DATA_READY which is bit 7 of the PCS status register (0x82) does not deassert when synchronization is lost.

Affected Configurations

This issue affects both Stratix IV and Stratix V implementations of the 10GBASE–R PHY.

Workaround

The workaround is to monitor the internal signals that indicate lock status and perform a digital reset of the channel when synchronization is lost.

Solution Status

This issue will be fixed in a future version of the 10GBASE–R PHY IP core.

Incorrect Device Support Listed 10GBASE-R PHY IP Core User Guide

The *10GBase-R PHY IP Core* chapter of the *Altera Transceiver PHY IP Core User Guide* states that the 10GBASE-R IP Core provides final support for the Stratix IV E device family; however, the 10GBASE-R PHY IP core provides no support for Stratix IV E devices.

Affected Configurations

This is a documentation error only.

Workaround

No workaround is required.

Solution Status

This issue is fixed in version 10.1 of the *Altera Transceiver PHY IP Core User Guide*.

Mixed Language Simulation Fails when Optimization Is On

Simulation fails when using ModelSim with mixed-languages.

Affected Configurations

This issue affects mixed language simulation including Verilog modules and VHDL entities when optimization is on.

Workaround

The workaround is to turn ModelSim optimization off by using the `-novpt` option to the `vsim` command.

Solution Status

This issue may be fixed in a future version of ModelSim.

Revision History

Table 3–1 shows the revision history for the 10-Gbps Ethernet MAC MegaCore function.

For more information about the new features, refer to the *10-Gbps Ethernet MAC MegaCore Function User Guide*.

Table 3–1. 10-Gbps Ethernet MAC MegaCore Function Revision History

Version	Date	Description
10.1	December 2010	■ Preliminary support for Arria Ii GZ and Stratix V devices. ■ Final support for Arria II GX and Stratix IV devices.
10.0	July 2010	Initial release.

Errata

Table 3–2 shows the issues that affect the 10-Gbps Ethernet MAC MegaCore function v10.0.

Table 3–2. 10-Gbps Ethernet MAC MegaCore Function Errata

Added or Updated	Issue	Affected Version
		10.0
15 July 10	No Length Checking for VLAN and Stacked VLAN Frames	✓
15 July 10	Simulation Not Supported for Stratix V Designs	✓

No Length Checking for VLAN and Stacked VLAN Frames

The IP core does not perform length checking on all VLAN and stacked VLAN frames.

Affected Configuration

All configurations.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the 10-Gbps Ethernet MAC MegaCore function.

Simulation Not Supported for Stratix V Designs

The IP core does not support simulation for designs that target Stratix V devices.

Affected Configuration

All configurations.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the 10-Gbps Ethernet MAC MegaCore function.

Revision History

Table 4–1 shows the revision history for the ASI MegaCore function.

For more information about the new features, refer to the *ASI MegaCore Function User Guide*.

Table 4–1. ASI MegaCore Function Revision History

Version	Date	Description
10.1 SP1	February 2011	Maintenance release.
10.1	December 2010	■ Preliminary support for Arria II GZ devices. ■ Final support for Arria II GX devices.
10.0	July 2010	Maintenance release.
9.1	November 2009	Preliminary support for Cyclone III LS and Cyclone IV (soft SERDES) devices.
9.0 SP2	July 2009	Maintenance release.
9.0 SP1	May 2009	Maintenance release.
9.0	March 2009	Preliminary support for Arria II GX devices.
8.1	November 2008	Maintenance release.

Errata

Table 4–2 shows the issues that affect the ASI MegaCore function v10.1, 10.0, and 9.1.

Not all issues affect all versions of the ASI MegaCore function.

Table 4–2. ASI MegaCore Function Errata

Added or Updated	Issue	Affected Version		
		10.1	10.0	9.1
15 Feb 11	ASI Does Not Support VHDL Functional Simulation Model for Cyclone IV GX	✓	—	—
15 Dec 10	ASI 10.1 Does Not Support Qsys	✓	—	—
01 Dec 06	NativeLink Does Not Support Gate-Level Simulation	✓	✓	✓

ASI Does Not Support VHDL Functional Simulation Model for Cyclone IV GX

Serial loopback designs that target Cyclone IV GX devices using the VHDL functional simulation model fail to simulate.

Affected Configurations

This issue only affects designs that target Cyclone IV GX devices using the VHDL functional simulation model.

Design Impact

The design fails to simulate using the VHDL functional simulation model.

Workaround

Use the Verilog HDL functional simulation model instead.

Solution Status

This issue will be fixed in a future version of the ASI MegaCore function.

ASI 10.1 Does Not Support Qsys

You will not be able to generate the ASI MegaCore function v10.1 using Qsys. Adding the ASI MegaCore function in a Qsys system triggers the following warning message: `ASI does not support Qsys-compatible generation`.

Affected Configurations

This issue affects all configurations.

Design Impact

The design will not generate successfully in Qsys.

Workaround

Use SOPC Builder instead.

Solution Status

This issue will be fixed in a future version of the ASI MegaCore function.

NativeLink Does Not Support Gate-Level Simulation

When using the NativeLink simulation example, the gate-level simulation design fails.

Affected Configurations

This issue affects all simulators supported by NativeLink.

Design Impact

This issue only affects simulation and does not affect the design compilation.

Workaround

Perform an RTL simulation of the NativeLink simulation example.

Solution Status

This issue will be fixed in a future version of the ASI MegaCore function.

Revision History

Table 5–1 shows the revision history for the CIC MegaCore function.

For information about the new features, refer to the *CIC MegaCore Function User Guide*.

Table 5–1. CIC MegaCore Function Revision History

Version	Date	Description
10.1	December 2010	■ Preliminary support for Arria II GZ devices. ■ Final support for Stratix IV GT devices.
10.0	July 2010	Preliminary support for Stratix V devices.
9.1 SP2	March 2010	Maintenance release.
9.1 SP1	February 2010	Maintenance release.
9.1	November 2009	■ Preliminary support for HardCopy IV GX, Stratix IV, and Cyclone III LS devices. ■ Withdrawn support for HardCopy family of devices.

Errata

Table 5–2 shows the issues that affect the CIC MegaCore function v10.1, v10.0, v9.1 SP2, v9.1 SP1, and v9.1.

Table 5–2. CIC MegaCore Function Errata

Added or Updated	Issue	Affected Version				
		10.1	10.0	9.1 SP2	9.1 SP1	9.1
15 Mar 11	Compilation Targeting a Stratix V Device Fails	✓	—	—	—	—
15 July 10	Error Generating HDL for Decimator with More Than 9 Stages and 11 Interfaces	—	Fixed	✓	✓	✓
1 Apr 10	OpenCore Plus Feature Not Supported for Cyclone IV E and Cyclone IV GX Devices	—	—	Fixed	✓	—

Compilation Targeting a Stratix V Device Fails

Designs that include a CIC IP core and target a Stratix V device, do not compile even if you have a valid license for the IP core. Refer to Altera solution rd03082011_116 at www.altera.com/support/kdb/solutions/rd03082011_116.html.

Affected Configurations

CIC IP core designs that target a Stratix V device.

Design Impact

Designs that include this IP core and target a Stratix V device cannot compile.

Workaround

To fix this issue, if you have a valid license for this IP core, follow these steps:

1. Upgrade your Quartus II software installation to the 10.1 Service Pack 1 version.
2. Apply Patch 1.19 to your Quartus II software installation.
3. Regenerate your IP core and any others in your design that are affected by this issue.
4. Recompile your design.

Solution Status

This issue will be fixed in a future version of the Quartus II software.

Error Generating HDL for Decimator with More Than 9 Stages and 11 Interfaces

An error is issued when you generate HDL after selecting a **Decimator** filter with **Number of Stages** set to more than **9** and **Number of Interface** to more than **11**.

Affected Configurations

Decimator filters with more than 9 stages and more than 11 interfaces.

Design Impact

An error is issued when you generate HDL.

Workaround

If you want more than 9 stages you must select 11 interfaces or fewer. If you want more than 11 interfaces you must choose 9 stages or fewer.

Solution Status

This issue is fixed in version 10.0 of the CIC MegaCore function.

OpenCore Plus Feature Not Supported for Cyclone IV E and Cyclone IV GX Devices

When using the OpenCore Plus evaluation feature, the CIC MegaCore function does not generate a functional simulation model for Cyclone IV E and Cyclone IV GX devices.

Affected Configurations

All CIC variations that target a Cyclone IV E device or a Cyclone IV GX device.

Design Impact

This issue has no design impact.

Workaround

To avoid this issue, purchase a license for the CIC MegaCore function.

Solution Status

This issue is fixed in version 9.1 SP2 of the CIC MegaCore function.

Revision History

Table 6–1 shows the revision history for the CPRI MegaCore function.

For information about the new features, refer to the *CPRI MegaCore Function User Guide*.

Table 6–1. CPRI MegaCore Function Revision History

Version	Date	Description
10.1 SP1	February 2011	Maintenance release.
10.1	December 2010	■ Added support for Arria II GZ devices. ■ Added support for additional CPRI data rates in Arria II GX devices. ■ Added scrambler/descrambler support. ■ Added CPU interrupt for remote hardware reset.
10.0	July 2010	■ Added support for Cyclone IV GX devices. ■ Added GUI parameter to enable auto-rate negotiation and two signals to support visibility of the feature status. ■ Enhanced testbench suite to include two new testbenches, to demonstrate operation with no MAP interface and to demonstrate auto-rate negotiation.
9.1 SP2	March 2010	Maintenance release.
9.1 SP1	February 2010	Initial release.

Errata

Table 6–2 shows the issues that affect the CPRI MegaCore function v10.1 SP1, v10.1, v10.0, and v9.1 SP2. Issues that affect v9.1 SP1 are available in a **readme.txt** file that accompanies the CPRI MegaCore function v9.1 SP1 patch.

Not all issues affect all versions of the CPRI MegaCore function. Altera recommends upgrading to the latest available version of the MegaCore IP Library.

Table 6–2. CPRI MegaCore Function Errata (Part 1 of 2)

Added or Updated	Issue	Affected Version			
		10.1 SP1	10.1	10.0	9.1 SP2
15 Mar 11	MII Interface Description in v10.1 User Guide Contains Errors	✓	✓	—	—

Table 6–2. CPRI MegaCore Function Errata (Part 2 of 2)

Added or Updated	Issue	Affected Version			
		10.1 SP1	10.1	10.0	9.1 SP2
15 Feb 11	CPRI Protocol Version Default Value is Invalid	✓	✓	—	—
	CPU Interface Deadlocks After Attempt to Access Ethernet or HDLC Registers When MII Interface Enabled	Fixed	✓	✓	✓
	Errors in .mif File Names in Auto-rate Negotiation Testbenches	Fixed	✓	—	—
	Testbench tb_altera_cpri.vhd Does Not Simulate	Fixed	✓	—	—
	Cyclone IV GX REC Master Cannot Achieve Link Synchronization	Fixed	✓	—	—
	Some MegaCore Variations Have Invalid cpri_clkout Frequency	Fixed	✓	—	—
15 Jan 11	cpri_rx_cnt_sync port Description and Frame Synchronization FSM in User Guide are Incorrect	✓	✓	✓	—
15 Dec 10	Cannot Simulate CPRI MegaCore Function in Verilog HDL	✓	✓	—	—
	Timing Violations in Some Device Families, Speed Grades, and Line Rates	✓	✓	✓	✓
	Erroneous File Names in CPRI 10.1 Testbench Description in User Guide	✓	✓	—	—
15 Aug 10	PRBS is Not Supported in Cyclone IV GX Devices	—	Fixed	✓	—
15 July 10	Auto-Rate Negotiation Does Not Support 614.4 Mbps Line Rate in Cyclone IV GX Devices	—	Fixed	✓	—
	Wrong Extended Rx Delay Measurement Clock Period	—	Fixed	✓	—
	Simulation Testbench Does Not Support Cyclone IV GX Variations	—	Fixed	✓	—
	Cannot Simulate Auto-Rate Negotiation in Verilog HDL With ModelSim 6.4b or Later	—	Fixed	✓	—
	Warning Messages from Transceiver While Generating and Compiling CPRI MegaCore Function	✓	✓	✓	✓
	CPRI MegaCore Function v10.0 User Guide Does Not Contain Complete Instructions for Running v10.0 Simulation Testbench	—	—	✓	—
	CPU Interrupt Bit Always Set When Interrupts are Enabled	—	—	Fixed	✓
	MII Interface Description in v9.1SP1 User Guide Contains Errors	—	—	Fixed	✓
	CPRI MegaCore Function User Guide Unavailable From MegaWizard Interface Info Link	—	—	Fixed	✓
	MegaWizard Plug-In Manager Does Not Recognize Transceiver Instances	—	—	Fixed	✓
	CPRI Frame Synchronization Machine Unable to Return to XACQ1 from XSYNC1	—	—	Fixed	✓
	Setup Time Violations Might Occur in Arria II GX 3072 Mbps Designs	—	—	Fixed	✓
01 Apr 10	CPRI MegaCore Function Does Not Support HardCopy IV GX Devices	✓	✓	✓	✓
	CPRI MegaCore Function v9.1SP1 User Guide Does Not Contain Complete Instructions for Running v9.1SP1 Simulation Testbench	—	—	—	✓

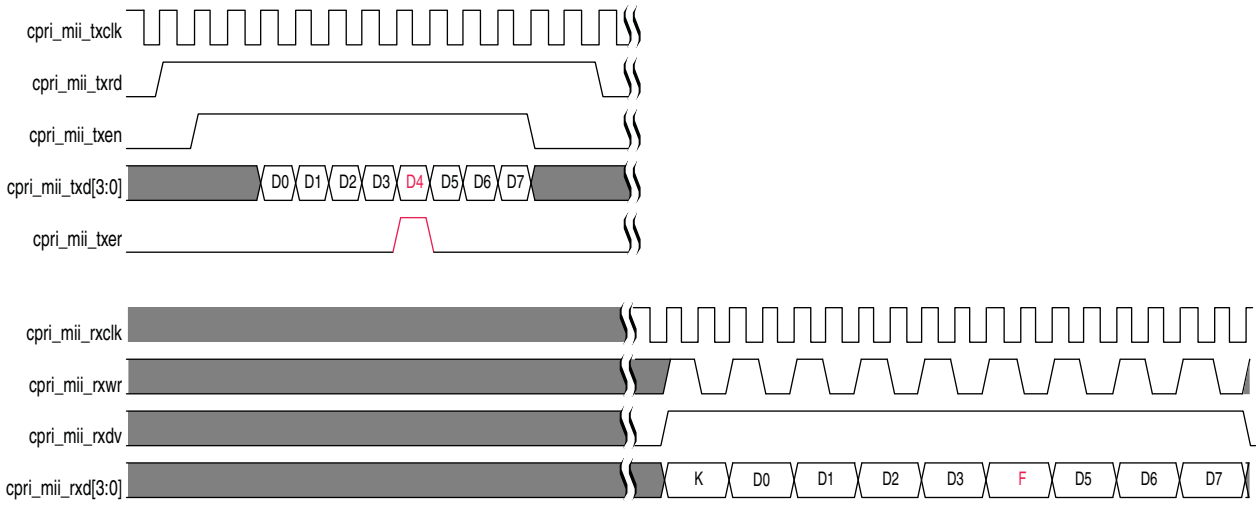
MII Interface Description in v10.1 User Guide Contains Errors

The CPRI MegaCore Function v10.1 User Guide contains an erroneous example of MII interface behavior. Figure 4-23, CPRI MII Interface Transmitter Example 1, on page 78 of the *CPRI MegaCore Function User Guide* shows input behavior that the MII interface cannot handle. Specifically, if the `cpri_mii_txen` signal toggles during transmission of a single packet, as shown in Figure 4-23, the incoming data is not transmitted correctly on the CPRI link.

You should not rely on Figure 4-23, nor any part of its explanation that describes a toggling `cpri_mii_txen` input signal. Refer instead to Figure 4-24 on the same page, CPRI MII Interface Transmitter Example 2.

Figure 4-26, CPRI MII Interface Signals on Transmitting RE or REC Master and on Receiving RE Slave, also shows this behavior. Replace Figure 4-26 on page 80 of the *CPRI MegaCore Function User Guide* with the following Figure 6–1.

Figure 6–1. Corrected CPRI MII Interface Signals on Transmitting RE or REC Master and on Receiving RE Slave



Affected Configurations

This documentation issue affects all CPRI MegaCore function variations configured with the MII interface.

Design Impact

Data received on the CPRI IP core MII interface is not transmitted correctly on the CPRI link if the data originates at an external Ethernet block that toggles the `cpri_mii_txen` signal input to the CPRI IP core.

Workaround

Do not refer to Figure 4-23 in the CPRI MegaCore Function v10.1 User Guide. Instead, refer to Figure 4-24 and its description for correct behavior of an external Ethernet block.

Solution Status

This issue will be fixed in a future version of the *CPRI MegaCore Function User Guide*.

CPRI Protocol Version Default Value is Invalid

The default value of the tx_prot_version field of the CPRI_TX_PROT_VER register is 0. However, this is not a valid value for this field. Valid values are 1 and 2. Currently, the CPRI MegaCore function recognizes the value 0 as a 1, in system configurations with two CPRI MegaCore function instances connected through a CPRI link. However, this invalid value might not be recognized as a 1 by third-party CPRI partners.

Affected Configurations

All CPRI MegaCore function variations.

Design Impact

The invalid value might not be recognized as a 1 by third-party CPRI partners. In this case, the CPRI MegaCore function and its link partner cannot achieve link synchronization.

Workaround

Immediately following system initialization, set the tx_prot_version field of the CPRI_TX_PROT_VER register to value 1 or 2.

Solution Status

This issue will be fixed in a future version of the CPRI MegaCore function.

CPU Interface Deadlocks After Attempt to Access Ethernet or HDLC Registers When MII Interface Enabled

If the application attempts to access Ethernet or HDLC registers in a CPRI MegaCore function variation with the MII interface enabled, the CPU might hang while awaiting deassertion of the cpu_waitrequest signal.

Affected Configurations

All CPRI MegaCore function variations with the MII interface enabled (**Include MAC block** is turned off).

Design Impact

The CPU might hang and require reprogramming.

Workaround

This issue has no workaround. You should avoid accessing the non-existent Ethernet and HDLC registers when your CPRI MegaCore function variation does not include an internal MAC block.

Solution Status

This issue is fixed in version 10.1 SP1 of the CPRI MegaCore function.

In version 10.1 SP1 and beyond, accessing the non-existent Ethernet and HDLC registers no longer causes the CPRI MegaCore function to hang. Instead, the CPRI MegaCore function treats these accesses as accesses to reserved register space: write accesses are ignored and read accesses return zero values.

Errors in .mif File Names in Auto-rate Negotiation Testbenches

The Memory Initialization File (**.mif**) names in the ROM files included in the auto-rate negotiation testbenches do not match the generated file names. You can fix this error manually and run the testbenches.

Affected Configurations

This issue affects only the **tb_altera_cpri_autorate** and **tb_altera_cpri_c4gx_autorate** customer demonstration testbenches.

Design Impact

The **tb_altera_cpri_autorate** and **tb_altera_cpri_c4gx_autorate** customer demonstration testbenches cannot simulate.

Workaround

To avoid this issue, before simulating the **tb_altera_cpri_autorate** or **tb_altera_cpri_c4gx_autorate** testbench, edit the following files to remove the string `alt<chars>gxb` from the **.mif** file names:

- **rom_stratix4gx_**<*rate*>**_m.v**
- **rom_stratix4gx_**<*rate*>**_m.vhd**
- **rom_cyclone4gx_**<*rate*>**_m.v**
- **rom_cyclone4gx_**<*rate*>**_m.vhd**

The Testbenches chapter in the *CPRI MegaCore Function User Guide* tells you do this only in the **.vhd** files. However, this step is necessary in the **.v** files as well.

The **tb_altera_cpri_autorate** testbench uses the **rom_stratix4gx** files, and the **tb_altera_cpri_c4gx_autorate** testbench uses the **rom_cyclone4gx** files.

Solution Status

This issue is fixed in version 10.1 SP1 of the CPRI MegaCore function.

Testbench tb_altera_cpri.vhd Does Not Simulate

The testbench **tb_altera_cpri** does not simulate in VHDL because of an error in the **compile_vhdl.do** file. You can fix this error manually and run the testbench.

Affected Configurations

This issue affects only the **tb_altera_cpri** customer demonstration testbench in VHDL.

Design Impact

The **tb_altera_cpri** customer demonstration testbench cannot simulate in VHDL.

Workaround

To avoid this issue, before simulating the **tb_altera_cpri** testbench, follow these steps:

1. Open the testbench **compile_vhdl.do** file in a text editor.
2. Replace the line

   ```
   vcom -work altera_mf -93 -explicit altera_mf_components.vhd
   ```

   with

   ```
   vcom -work altera_mf -93 -explicit lib/altera_mf_components.vhd
   ```

Solution Status

This issue is fixed in version 10.1 SP1 of the CPRI MegaCore function.

Cyclone IV GX REC Master Cannot Achieve Link Synchronization

An REC master that targets a Cyclone IV GX device cannot achieve link synchronization with an RE slave. You can modify some source files to avoid the issue.

Affected Configurations

All CPRI MegaCore function REC masters that target a Cyclone IV GX device.

Design Impact

The REC master cannot achieve link synchronization.

Workaround

You can modify the source or generated files to fix this issue.

If you have write access to your IP installation files, before you generate your CPRI MegaCore function, follow these steps.

1. In a command shell, change directory to <*IP installation*>**/altera/cpri/src/altgx**.
2. Change directory to **614** and type the following command:

   ```
   qmegawiz -silent -wiz_override="sim_en_pll_fs_res=true" \
               cyclone4gx_614_s_tx.vhd
   ```

3. Change directory to **../1228** and type the following command:

   ```
   qmegawiz -silent -wiz_override="sim_en_pll_fs_res=true" \
               cyclone4gx_1228_s_tx.vhd
   ```

4. Change directory to **../2457** and type the following command:

   ```
   qmegawiz -silent -wiz_override="sim_en_pll_fs_res=true" \
               cyclone4gx_2457_s_tx.vhd
   ```

5. Change directory to **../3072** and type the following command:

   ```
   qmegawiz -silent -wiz_override="sim_en_pll_fs_res=true" \
               cyclone4gx_3072_s_tx.vhd
   ```

If you do not have write access to your IP installation files, you can run the same commands after you generate your CPRI MegaCore function. After generation, the same files appear in different folders in your project directory. Change directory to the appropriate folders to run the same commands.

Solution Status

This issue is fixed in version 10.1 SP1 of the CPRI MegaCore function.

Some MegaCore Variations Have Invalid cpri_clkout Frequency

CPRI MegaCore function variations with data rate 6.144 Gbps and with auto-rate negotiation disabled that target an Arria II GX device are generated with an invalid `cpri_clkout` frequency.

Affected Configurations

All CPRI MegaCore function variations with data rate 6.144 Gbps and with auto-rate negotiation disabled that target an Arria II GX device.

Design Impact

As a result of the invalid `cpri_clkout` frequency, the physical link cannot achieve link synchronization.

Workaround

To avoid this issue, implement one of the following two workarounds:

- Turn on auto-rate negotiation in your CPRI MegaCore function.
- Modify the source or generated files to fix this issue.

  If you have write access to your IP installation files, before you generate your CPRI MegaCore function, follow these steps:

  a. Open the <*IP installation*>**/altera/cpri/src/altera_cpri.vhd** file in a text editor.

  b. On line 3251, replace `clk0 => tx_clkout` with `clk0 => txclk_div2`.

  c. On line 3259, replace `clk0 => rx_clkout` with `clk0 => rxclk_div2`.

  If you do not have write access to your IP installation files, you can modify the top-level file after you generate your CPRI MegaCore function. After generation, the file appears in your project directory.

Solution Status

This issue is fixed in version 10.1 SP1 of the CPRI MegaCore function.

cpri_rx_cnt_sync port Description and Frame Synchronization FSM in User Guide are Incorrect

The description of the cpri_rx_cnt_sync port (bits [4:2] of the extended_rx_status_data bus) in the *CPRI MegaCore Function User Guide* is incorrect for CPRI MegaCore function versions 10.0 and 10.1. The description in the Extended Rx Status Signals table in Chapter 5, Signals incorrectly describes the port, and the description of the initialization sequence for the testbenches, in Chapter 7, Testbenches, incorrectly implies this port has value 0x2 when frame synchronization completes.

In addition, Figure 4-10 in Chapter 4, Functional Description is mislabeled. The state labeled XSYNC3 should instead be labeled HFNSYNC1, and the state labeled HFNSYNC should instead be labeled HFNSYNC2.

The correct description of this port tells you that the port indicates the current state number (starting from zero rather than one) among the states whose category is indicated by the cpri_rx_state port (bits [1:0] of the extended_rx_status_data bus). For example, if the value of cpri_rx_state is 2'b10, the frame synchronization machine is in an XSYNC state. The cpri_rx_cnt_sync port tells you which XSYNC state the machine is in: if cpri_rx_cnt_sync has value 2'b00, the machine is in the state XSYNC1, and if it has value 2'b01, the machine is in state XSYNC2. Refer to the frame synchronization state machine figure in Chapter 4, Functional Description, with the modifications described in this erratum.

Therefore, when cpri_rx_state has value 2'b11, cpri_rx_cnt_sync cannot have value 0x2. The frame synchronization machine has only two HFNSYNC states. After frame synchronization completes, the value of cpri_rx_cnt_sync is 3b'001, not 3b'010 as erroneously indicated in the Testbenches chapter.

Affected Configurations

All CPRI MegaCore function variations.

Design Impact

If you interpret the cpri_rx_cnt_sync port according to the description in the user guide, you wait for a value that will never appear to signal the HFNSYNC state of the CPRI frame synchronization machine.

Workaround

Interpret the cpri_rx_cnt_sync port (bits [4:2] of the extended_rx_status_data bus) according to this erratum rather than according to the description in the Signals chapter of the *CPRI MegaCore Function User Guide*.

Solution Status

This issue will be fixed in a future version of the *CPRI MegaCore Function User Guide*.

Cannot Simulate CPRI MegaCore Function in Verilog HDL

Simulation of the CPRI MegaCore function in Verilog HDL is not functional, due to an underlying Quartus II software v10.1 issue with RAM modelling in Verilog HDL.

Affected Configurations

All CPRI MegaCore functions with functional models generated in Verilog HDL.

Design Impact

This issue has no design impact. This issue affects simulation only.

Workaround

This issue has no workaround. You can generate your CPRI MegaCore function simulation model in VHDL.

Solution Status

This issue will be fixed in a future version of the CPRI MegaCore function.

Timing Violations in Some Device Families, Speed Grades, and Line Rates

Timing violations may occur in CPRI MegaCore functions that target the combinations of device family, speed grade, and CPRI line rate shown in Table 6–3.

Table 6–3. Device Family, Speed Grade, and Line Rate that Might Cause Timing Violations

Device Family	Speed Grade	Line Rate
Arria II GX	I3	6144 Mbps
Cyclone IV GX	I7, C7	3072 Mbps

Affected Configurations

This issue affects the CPRI MegaCore function variations shown in Table 6–3.

Design Impact

Data might be lost on TX PLD-PCS paths in the CPRI MegaCore function.

Workaround

To avoid this issue, demote the TX PCS clock `tx_clkout` from a periphery or global clock to a LAB clock, by adding the following line to the Quartus II Project Settings File (**.qsf**) before compilation:

```
set_instance_assignment -name GLOBAL_SIGNAL OFF -to <variation>*tx_clkout*
```

Solution Status

This issue will be fixed in a future version of the CPRI MegaCore function.

Erroneous File Names in CPRI 10.1 Testbench Description in User Guide

In the Testbenches chapter of the *CPRI MegaCore Function User Guide*, in the instructions to prepare to simulate Verilog HDL files with ModelSim SE, some filename suffixes are wrong. However, note that the erratum "Cannot Simulate CPRI MegaCore Function in Verilog HDL" on page 6–8 supersedes this issue.

Affected Configurations

Testbenches simulated in Verilog HDL with ModelSim SE.

Design Impact

This issue has no design impact. It affects only the testbenches simulated in Verilog HDL with ModelSim SE.

Workaround

To fix this issue, in the user guide instructions to prepare to simulate Verilog HDL files with ModelSim SE, follow these steps.

- Replace all instances of `cpri_top_level.v` with `cpri_top_level.vo`.
- Replace all instances of `tb_altera_cpri[_<variation>].v` with `tb_altera_cpri[_<variation>].vhd`.

However, note that the erratum "Cannot Simulate CPRI MegaCore Function in Verilog HDL" on page 6–8 supersedes this issue.

Solution Status

This issue will be fixed in a future version of the *CPRI MegaCore Function User Guide*.

PRBS is Not Supported in Cyclone IV GX Devices

CPRI MegaCore function variations that target a Cyclone IV GX device do not support generation and validation of predetermined pseudo-random sequences (PRBS) for antenna-carrier interface testing.

Affected Configurations

All CPRI MegaCore function variations that target a Cyclone IV GX device.

Design Impact

For these CPRI MegaCore function variations, you cannot use the PRBS feature for testing the antenna-carrier interfaces.

Workaround

This issue has no workaround.

Solution Status

This issue is fixed in version 10.1 of the CPRI MegaCore function.

Auto-Rate Negotiation Does Not Support 614.4 Mbps Line Rate in Cyclone IV GX Devices

CPRI MegaCore function variations that target a Cyclone IV GX device cannot achieve a CPRI communication line rate of 614.4 Mbps using auto-rate negotiation.

Affected Configurations

All CPRI MegaCore function variations with auto-rate negotiation enabled that target a Cyclone IV GX device.

Design Impact

For these CPRI MegaCore function variations, auto-rate negotiation can change the CPRI communication line rate among 1228.8 Mbps, 2457.6 Mbps, and 3072.0 Mbps only.

Workaround

This issue has no workaround.

Solution Status

This issue is fixed in version 10.1 of the CPRI MegaCore function.

Wrong Extended Rx Delay Measurement Clock Period

In the Synopsys Design Constraints File (**.sdc**) for the CPRI MegaCore function, the `clk_ex_delay` clock period is specified incorrectly for some CPRI MegaCore function variations.

Affected Configurations

All CPRI MegaCore function variations that use the default **.sdc** script.

Design Impact

Extended Rx delay measurement is inaccurate.

Workaround

Edit the **.sdc** with the correct values for an M/N ratio of 128/127 or 64/63. In the `create_clock` command for the `clk_ex_delay` clock, modify the `-period` parameter to the appropriate clock period value shown in Table 6–4.

Table 6–4. Appropriate Clock Period Value

CPRI Line Rate (Mbps)	System Clock (MHz)	Extended Rx Delay Measurement Clock (clk_ex_delay)					
		M/N = 128/127			M/N = 64/63		
		Frequency (MHz)	Clock Period (ns)	Duty Cycle (ns)	Frequency (MHz)	Clock Period (ns)	Duty Cycle (ns)
614.4	15.36	15.24	65.617	32.809	15.12	66.138	33.069
1228.8	30.72	30.48	32.808	16.404	30.24	33.069	16.535
2457.6	61.44	60.96	16.404	8.202	60.48	16.534	8.267
3072.0	76.80	76.20	13.123	6.562	75.60	13.228	6.614
4915.2	122.88	121.92	8.202	4.101	120.96	8.267	4.134
6144.0	153.60	152.40	6.562	3.281	151.20	6.614	3.307

Solution Status

This issue is fixed in version 10.1 of the CPRI MegaCore function.

Simulation Testbench Does Not Support Cyclone IV GX Variations

The demonstration testbench does not support simulation of CPRI MegaCore function variations that target a Cyclone IV GX device.

Affected Configurations

CPRI MegaCore functions that target a Cyclone IV GX device.

Design Impact

This issue has no design impact.

Workaround

None.

Solution Status

This issue is fixed in version 10.1 of the CPRI MegaCore function.

Cannot Simulate Auto-Rate Negotiation in Verilog HDL With ModelSim 6.4b or Later

CPRI MegaCore function variations with auto-rate negotiation enabled and with Verilog HDL output files cannot simulate successfully in the Mentor Graphics ModelSim 6.4b simulator or in later versions of this simulator.

Affected Configurations

All CPRI MegaCore function variations with auto-rate negotiation enabled and with Verilog HDL output files.

Design Impact

Simulation cannot complete for these variations using these simulators.

Workaround

Use the ModelSim 6.4a simulation tool to simulate these variations.

Solution Status

This issue is fixed in version 10.1 of the CPRI MegaCore function.

Warning Messages from Transceiver While Generating and Compiling CPRI MegaCore Function

While the MegaWizard Plug-In Manager is generating a functional simulation model for the CPRI MegaCore function, and again while it is compiling, several warning messages related to the transceiver are displayed. Starting in version 10.0, these messages include warnings about clear box output or design files. These messages can be ignored.

Affected Configurations

This Quartus II software issue affects all CPRI MegaCore function variations.

Design Impact

This issue has no design impact. These messages can be safely ignored.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the Quartus II software.

CPRI MegaCore Function v10.0 User Guide Does Not Contain Complete Instructions for Running v10.0 Simulation Testbench

The Testbenches chapter of the CPRI MegaCore Function v10.0 User Guide does not provide adequate details to run the v10.0 testbench successfully.

Affected Configurations

This issue affects all CPRI MegaCore function variations.

Design Impact

This issue has no design impact.

Workaround

To run the demonstration testbenches successfully, in Step 4.b. of the instructions in the "Running the Testbenches" section of Chapter 7, Testbenches, do not copy any of the files with prefix **cycloneiv**.

Solution Status

This issue will be fixed in a future version of the CPRI MegaCore function.

CPU Interrupt Bit Always Set When Interrupts are Enabled

The CPU interrupt output status signal `cpu_irq` is always asserted when the interrupt enable field, `intr_en`, of the `CPRI_INTR` register is asserted.

Affected Configurations

All CPRI MegaCore functions with CPU interrupts enabled.

Design Impact

While CPU interrupts are enabled, the `cpu_irq` signal is asserted, and cannot be cleared.

Workaround

Ignore the CPU interrupt output status signal `cpu_irq` or upgrade to the CPRI MegaCore function v10.0.

Solution Status

This issue is fixed in version 10.0 of the CPRI MegaCore function.

MII Interface Description in v9.1SP1 User Guide Contains Errors

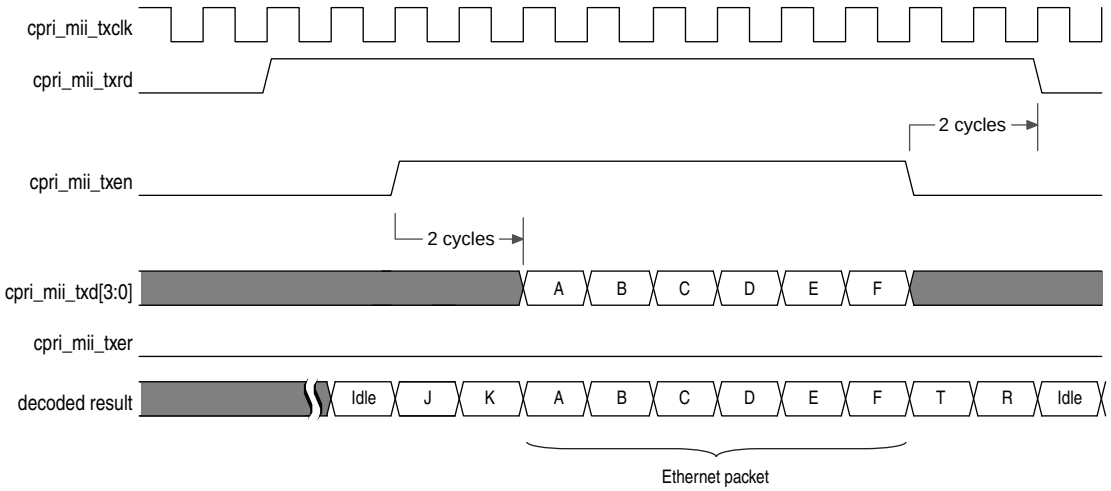
The *CPRI MegaCore Function v9.1SP1 User Guide* contains erroneous information about the MII interface. Figure 4-16 and Figure 4-17 in the *CPRI MegaCore Function User Guide* should be replaced with the figures in this erratum.

In contrast to the description in the CPRI MegaCore Function User Guide, the CPRI MII Interface transmitter inserts start-of-frame only after `cpri_mii_txen` is asserted. During the first two cycles in which `cpri_mii_txen` is asserted, the CPRI MII Interface transmitter inserts the J and K symbols in the buffer of data to be transmitted to the CPRI link, and ignores incoming data on `cpri_mii_txd`.

Typically, the external Ethernet block asserts `cpri_mii_txen` one clock cycle after `cpri_mii_txrd` is asserted. If not, in each clock cycle following that first cycle, while `cpri_mii_txrd` remains asserted but `cpri_mii_txen` is not yet asserted, the CPRI MII Interface transmitter inserts an Idle cycle in the buffer of data to be transmitted to the CPRI link. After `cpri_mii_txen` is asserted following the assertion of `cpri_mii_txrd`, if `cpri_mii_txen` is subsequently deasserted following a cycle in which `cpri_mii_txrd` remains asserted, the CPRI MII Interface transmitter assumes the external Ethernet block has reached end-of-frame, and begins insertion of the T and R nibbles.

Replace Figure 4-16 on page 56 of the CPRI MegaCore Function User Guide with the following Figure 6–2.

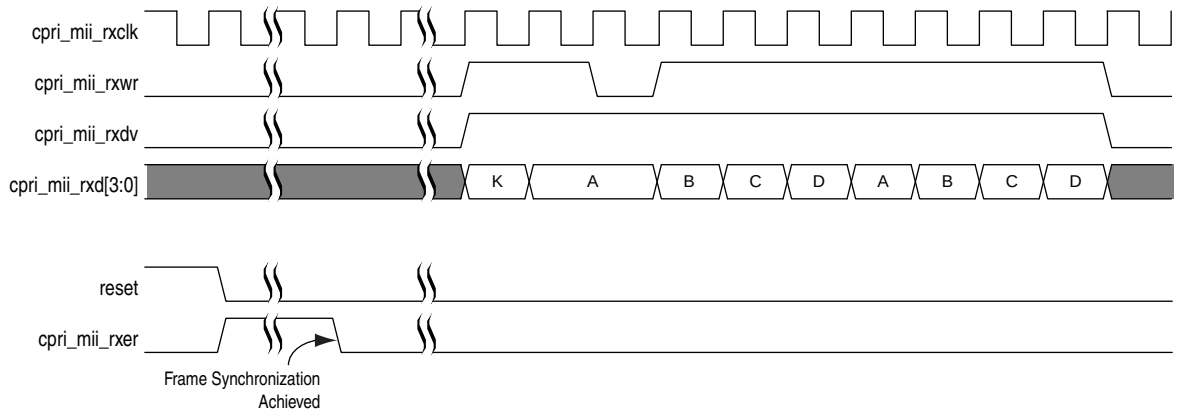
Figure 6–2. Corrected CPRI MII Interface Transmitter Example



Although Figure 6–2 shows `cpri_mii_txrd` asserted continuously during transmission of an Ethernet packet on `cpri_mii_txd`, this is not always the case. The CPRI MII Interface transmitter can deassert `cpri_mii_txrd` while `cpri_mii_txen` is still asserted, to backpressure the external Ethernet block. If this happens, the Ethernet block must deassert `cpri_mii_txen` on the following cycle, to prevent the MII Interface transmitter buffer from overflowing. The `cpri_mii_txen` signal should remain deasserted until the cycle following reassertion of `cpri_mii_txrd`. If `cpri_mii_txen` is not reasserted in the cycle following the reassertion of `cpri_mii_txrd`, then an Idle cyle is inserted in the packet; therefore, the external Ethernet block must reassert `cpri_mii_txen` in the cycle following reassertion of `cpri_mii_txrd`.

The CPRI MII Interface receiver transmits the K nibble to indicate start-of-frame on the MII interface. Replace Figure 4-17 on page 57 of the CPRI MegaCore Function User Guide with the following Figure 6–3.

Figure 6–3. Corrected CPRI MII Interface Receiver Example



The J nibble of the start-of-frame is consumed by the CPRI MegaCore function, and is not transmitted on the MII interface.

The corrections indicated above apply to Figure 4-18 on page 57 of the CPRI MegaCore Function User Guide as well.

Affected Configurations

This issue affects all CPRI MegaCore function variations configured with the MII interface.

Design Impact

Designs that rely on the description of the MII interface in the CPRI MegaCore Function User Guide exhibit data corruption on the MII interface.

Workaround

Use the corrected description in this erratum in designing your external Ethernet block.

Solution Status

This issue is fixed in version 10.0 of the *CPRI MegaCore Function User Guide*.

CPRI MegaCore Function User Guide Unavailable From MegaWizard Interface Info Link

The Info link to the CPRI MegaCore Function User Guide from the CPRI MegaWizard interface does not work.

Affected Configurations

This issue affects all CPRI MegaCore function variations.

Design Impact

This issue has no design impact.

Workaround

To view the CPRI MegaCore Function User Guide, open the **ug_cpri.pdf** file in your <*Quartus II v9.1 SP2 IP installation*>**/cpri/doc** folder, or click the CPRI MegaCore Function User Guide link on the Altera Literature: User Guides web page.

Solution Status

This issue is fixed in version 10.0 of the CPRI MegaCore function.

MegaWizard Plug-In Manager Does Not Recognize Transceiver Instances

After you generate an instance of the CPRI MegaCore function, its transceiver is not available for editing by the ALTGX MegaWizard interface. The MegaWizard Plug-In Manager does not recognize the transceiver as an existing instance of the ALTGX megafunction.

Affected Configurations

This issue affects all CPRI MegaCore function variations.

Design Impact

The MegaWizard Plug-In Manager does not recognize the CPRI transceiver as an existing instance of the ALTGX megafunction.

Workaround

This issue is caused by a copyright notice at the top of the clear-text version of the ALTGX megafunction HDL code file. You can avoid this issue by editing the clear-text file to remove the copyright notice. To remove the text that causes the problem, perform the following steps:

1. Open the HDL file for your transceiver instance in a text editor.
2. Remove the copyright notice and following blank lines. The first characters in the file should be the following line:

   ```
   --megafunction wizard: %ALTGX%
   ```

3. Save the file. Now you can edit the transceiver instance using the ALTGX MegaWizard interface.

Solution Status

This issue is fixed in version 10.0 of the CPRI MegaCore function.

CPRI Frame Synchronization Machine Unable to Return to XACQ1 from XSYNC1

If the CPRI frame synchronization machine is in the XSYNC1 state and does not receive the K28.5 byte, the frame synchronization machine remains in state XSYNC1 instead of moving to state XACQ1 as it should.

Affected Configurations

This issue affects all CPRI MegaCore function variations.

Design Impact

While the core is in the XSYNC1 state, the frame synchronization logic locks up until a K28.5 byte is detected.

Workaround

This issue has no workaround.

Solution Status

This issue is fixed in version 10.0 of the CPRI MegaCore function.

Setup Time Violations Might Occur in Arria II GX 3072 Mbps Designs

Designs that include a CPRI MegaCore function that runs the CPRI link at 3072 Mbps and targets an Arria II GX device, might exhibit setup time violations.

Affected Configurations

This issue affects some 3072-Mbps CPRI MegaCore functions that target an Arria II GX device.

Design Impact

You might observe hardware failures after you configure the device.

Workaround

To avoid this issue, use the Design Space Explorer for seed sweeping.

Solution Status

This issue is fixed in version 10.0 of the CPRI MegaCore function.

CPRI MegaCore Function Does Not Support HardCopy IV GX Devices

The HardCopy IV GX device family is not supported by the current release of the CPRI MegaCore function.

Affected Configurations

This issue affects all CPRI MegaCore function variations that target a HardCopy IV GX device.

Design Impact

CPRI MegaCore function designs that target a HardCopy IV GX device cannot be compiled or simulated.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the CPRI MegaCore function.

CPRI MegaCore Function v9.1SP1 User Guide Does Not Contain Complete Instructions for Running v9.1SP1 Simulation Testbench

The Testbenches chapter of the CPRI MegaCore Function v9.1SP1 User Guide does not provide adequate details to run the testbench successfully.

Affected Configurations

This issue affects all CPRI MegaCore function variations.

Design Impact

This issue has no design impact.

Workaround

To run the demonstration testbenches successfully, perform the following steps:

1. Copy the Demonstration Testbench from the Installation Folder.
2. Specify the library file settings by performing one of the following two sets of instructions:
   - If you use the Mentor Graphics ModelSim SE simulator, follow the instructions in Set Up the Library Files for the ModelSim SE Simulator.
   - If you use the Altera ModelSim AE simulator, follow the instructions in Set Up the Library Files for the ModelSim AE Simulator.
3. Edit the .do File.
4. Run the Simulation.

Copy the Demonstration Testbench from the Installation Folder

To run the demonstration testbench successfully, you must copy all the testbench files from <*Quartus II installation directory*>**/ip/altera/cpri/cus_demo_tb** to a new subdirectory of your working directory, called <*working directory*>**/cus_demo_tb**.

Set Up the Library Files for the ModelSim SE Simulator

To run the demonstration testbench using the Mentor Graphics ModelSim SE simulator, perform the following steps:

1. Create a library folder, <*working directory*>**/lib**.
2. Perform one of the following steps:
   - If you are using Verilog HDL models, copy the following files to <*working directory*>**/lib**:

```
$QUARTUS_ROOTDIR/eda/sim_lib/altera_mf.v
$QUARTUS_ROOTDIR/eda/sim_lib/arriaii_hssi_atoms.v
$QUARTUS_ROOTDIR/eda/sim_lib/stratixiv_hssi_atoms.v
$QUARTUS_ROOTDIR/eda/sim_lib/220model.v
$QUARTUS_ROOTDIR/eda/sim_lib/sgate.v
```

   - If you are using VHDL models, copy the following files to <*working directory*>**/lib**:

```
$QUARTUS_ROOTDIR/eda/sim_lib/altera_mf_components.vhd
$QUARTUS_ROOTDIR/eda/sim_lib/altera_mf.vhd
$QUARTUS_ROOTDIR/eda/sim_lib/220pack.v
$QUARTUS_ROOTDIR/eda/sim_lib/220model.v
$QUARTUS_ROOTDIR/eda/sim_lib/sgate_pack.vhd
$QUARTUS_ROOTDIR/eda/sim_lib/sgate.vhd
$QUARTUS_ROOTDIR/eda/sim_lib/arriaii_hssi_components.v
$QUARTUS_ROOTDIR/eda/sim_lib/arriaii_hssi_atoms.v
$QUARTUS_ROOTDIR/eda/sim_lib/stratixiv_hssi_components.v
$QUARTUS_ROOTDIR/eda/sim_lib/stratixiv_hssi_atoms.v
```

Set Up the Library Files for the ModelSim AE Simulator

Copy the following library files from <*Quartus II installation directory*>**/modelsim_ase/altera/vhdl** to your testbench directory <*working directory*>:

- **altera**
- **altera_mf**
- **arriaii_hssi**
- **stratixiv_hssi**
- **sgate**

Edit the .do File

Edit the appropriate ModelSim **.do** file for your CPRI MegaCore function variation. and your choice of HDL. The VHDL files are **compile.do** and **compile_mii.do**, and the Verilog HDL files are **compile_verilog.do** and **compile_mii_verilog.do**.

Perform the following edits, depending on your ModelSim version and HDL:

- To prepare to simulate with ModelSim AE, perform the following edits:
  - Comment out all `vlib` commands, except for `vlib -unix work`
  - Comment out all `vmap` commands.
  - Comment out all Quartus II library `vcom` commands.
  - Change all instances of `src/cpri_top_level.vho` to `../cpri_top_level.vho`.
  - Change all instances of `test/tb_altera_cpri.vhd` to `tb_altera_cpri.vhd`.
- To prepare to simulate Verilog HDL or VHDL files with ModelSim SE, perform the following edits:
  - Change all instances of `src/cpri_top_level.vho` to `../cpri_top_level.vho`.
  - Change all instances of `test/tb_altera_cpri.vhd` to `tb_altera_cpri.vhd`.
- To prepare to simulate Verilog HDL files with ModelSim SE, perform the following edits:
  - Change all instances of `src/cpri_top_level.vo` to `../cpri_top_level.vo`.
  - Change all instances of `test/tb_altera_cpri.vhd` to `tb_altera_cpri.vhd`.

Run the Simulation

To compile and run the simulation, perform the following steps:

1. Depending on your CPRI MegaCore function variation and your HDL, identify the correct **.do** file, <*my_variation*>**.do**. The following files are available: **compile.do** (VHDL), **compile_verilog.do**, **compile_mii.do** (VHDL), and **compile_mii_verilog.do**.
2. To compile the design variation, type the following command:

   ```
   do <my_variation>.do ↵
   ```

3. To simulate the testbench, type the following command:

   ```
   run -all ↵
   ```

The appropriate waveform display file, **wave.do** or **wave_mii.do**, runs and displays the waveforms for a predetermined set of signals automatically.

Solution Status

This issue is irrelevant in version 10.0 of the CPRI MegaCore function.

7. CRC Compiler

Revision History

Table 7–1 shows the revision history for the CRC Compiler.

For more information about the new features, refer to the *CRC Compiler User Guide*.

Table 7–1. CRC Compiler Revision History

Version	Date	Description
10.1	December 2010	Final support for Stratix IV GT devices.
10.0	July 2010	Maintenance release.
9.1	November 2009	Preliminary support for Cyclone III LS and Cyclone IV devices.
9.0 SP2	July 2009	Maintenance release.
9.0 SP1	May 2009	Preliminary support for HardCopy III and HardCopy IV E devices.
9.0	March 2009	Preliminary support for Arria II GX device family.

Errata

Table 7–2 shows the issues that affect the CRC Compiler v10.1, 10.0, and 9.1.

Not all issues affect all versions of the CRC Compiler.

Table 7–2. CRC Compiler Errata

Added or Updated	Issue	Affected Version		
		10.1	10.0	9.1
01 Dec 06	Testbench Directory Generated When You Create a Simulation Model	✓	✓	✓

Testbench Directory Generated When You Create a Simulation Model

When you create a simulation model, the CRC compiler automatically creates a **testbench** directory in the project directory for you. If you follow the **Running the Testbench Example** steps in the *CRC Compiler User Guide* to create the generator and checker files, another **testbench** directory is created as a subdirectory of the initial **testbench** directory, resulting in the following directory structure:

c:\altera\projects\crc_project\testbench\testbench

when the initial directory is

c:\altera\projects\crc_project\testbench

Affected Configuration

All CRC MegaCore function variations are affected.

Design Impact

This issue has no design impact.

Workaround

The **testbench** subdirectory (**testbench\testbench**) of the initial **c:\altera\projects\crc_project\testbench** directory may be deleted.

Solution Status

No change is planned currently.

8. DDR and DDR2 SDRAM Controller Compiler

Revision History

Table 8–1 shows the revision history for the DDR and DDR2 SDRAM Controller Compiler.

For more information about the new features, refer to the *DDR and DDR2 SDRAM Controller Compiler User Guide*.

Table 8–1. DDR and DDR2 SDRAM Controller Compiler Revision History

Version	Date	Description
10.1	December 2010	Maintenance release.
10.0	July 2010	Maintenance release.
9.1	November 2009	Maintenance release.
9.0 SP2	July 2009	Maintenance release.
9.0 SP1	May 2009	Maintenance release.
9.0	March 2009	Maintenance release.
8.1	November 2008	Maintenance release.

Errata

Table 8–2 shows the issues that affect the DDR and DDR2 SDRAM Controller Compiler v10.1, 10.0, and 9.1.

Not all issues affect all versions of the DDR and DDR2 SDRAM Controller Compiler.

Table 8–2. DDR and DDR2 SDRAM Controller Compiler Errata

Added or Updated	Issue	Affected Version		
		10.1	10.0	9.1
15 July 10	Quartus Compilation Error	✓	✓	—
	Partitioned Design Compilation Error	✓	✓	—
15 Oct 07	Error: Can't Find the Clock Output Pins. Stop.	✓	✓	✓
01 Jul 07	ODT Launches Off System Clock	✓	✓	✓
01 Jun 06	Error Message When Recompiling a Project	✓	✓	✓
	Pin Planner HDL Syntax Error	✓	✓	✓

Quartus Compilation Error

Designs that target the Cyclone II devices fail to compile in version 10.0 of the Quartus II software.

Affected Configurations

This issue affects all designs that use Cyclone II devices.

Design Impact

Your design fails to compile.

Workaround

Use version 9.1 of the Quartus II software.

Solution Status

This issue will not be fixed.

Partitioned Design Compilation Error

Partitioned designs that use the DDR2 SDRAM Controller fail compilation at `cke` and `odt` pins.

Affected Configurations

This issue affects all designs that use the DDR2 SDRAM Controller.

Design Impact

Your design fails to compile.

Workaround

To compile your design successfully, in the **.qsf** file add the following command:

```
set_instance_assignment -name REMOVE_DUPLICATE_REGISTERS OFF -to
"ddr2_ctrl:ddr2_ctrl_ddr_sdram|ddr2_ctrl_auk_ddr_sdram:ddr2_ctrl_auk_ddr_s
dram_inst|auk_ddr_controller:ddr_control|cke"
```

Solution Status

This issue will not be fixed.

Error: Can't Find the Clock Output Pins. Stop.

The post-compile timing script reports the following error:

```
‘Couldn't find the clock output pins. Stop.’
```

Affected Configurations

This issue affects designs using the DDR SDRAM controller, when the PLL counters have been reordered or the clocks for the DDR SDRAM interface are not on global clocks. This issue may occur automatically in the Fitter if there is pressure on global clock resources.

Design Impact

The design fails.

Workaround

Make the following two assignments:

```
ddr_pll_stratixii:g_stratixpll_ddr_pll_inst Preserve PLL Counter Order
On
ddr_pll_stratixii:g_stratixpll_ddr_pll_inst|altpll:altpll_component|_c
lk3* Global Signal Global Clock
```

☞ Replace the file names of the PLL with those in your DDR SDRAM controller design.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controller Compiler.

ODT Launches Off System Clock

In designs with a separate address and command clock, the ODT output launches from the system clock, not from this address and command clock.

Affected Configurations

This issue affects the following configurations:

- DDR2 SDRAM controller (not DDR SDRAM)
- ODT is turned on
- CAS latency is set to three
- The design uses a separate address and command clock and not the default system clock

Design Impact

This issue has no design impact.

Workaround

Use a CAS latency of four, which means one extra cycle of read latency, or use the DDR2 SDRAM High-Performance controller, which uses the ALTMEMPHY megafunction to transfer all the address and command outputs to the correct clock.

Solution Status

This issue will not be fixed.

Error Message When Recompiling a Project

If you move the directory containing your Quartus II project, or rename your Quartus II project and recompile it without regenerating the DDR or DDR2 SDRAM Controller, you may receive the following error:

```
Error: DDR timing cannot be verified until project has been successfully
compiled.
```

This error indicates that some of the settings files contain references to the previous location or project name and the verify timing script is unable to find the current project.

Affected Configurations

This issue affects all configurations.

Design Impact

The timing script does not verify your design.

Workaround

Regenerate your controller in IP Toolbench and recompile the project. The timing analysis script now completes correctly.

Solution Status

This issue will not be fixed.

Pin Planner HDL Syntax Error

There is an HDL syntax error in Pin Planner-generated top-level design files that contain a DDR or DDR2 SDRAM Controller variation.

Affected Configurations

Pin Planner-generated top-level design files that use a design that contains a DDR or DDR2 SDRAM Controller variation.

Design Impact

If you import the DDR or DDR2 SDRAM Controller Pin Planner file into Pin Planner and then generate a top-level design file for your design, it contains an HDL syntax error and does not compile in the Quartus II software. You cannot use this top -level design file for IO Assignment Analysis.

Workaround

Use the IP Toolbench top-level example design and automatically assigned constraints to verify your pin and IO assignments.

Solution Status

This issue will not be fixed.

9. DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP

Revision History

Table 9–1 shows the revision history for the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP MegaCore function.

For more information about the new features, refer to the *DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP User Guide*.

Table 9–1. DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP MegaCore Function Revision History

Date	Version	Description
December 2010	10.1	Maintenance release.
September 2010	10.0 SP1	Maintenance release.
July 2010	10.0	■ Added information for new GUI parameters: **Controller latency**, **Enable reduced bank tracking for area optimization**, and **Number of banks to track**. ■ Removed information about IP Advisor. This feature is removed from the DDR/DDR2 SDRAM IP support for version 10.0.
April 2010	9.1 SP2	Maintenance release.
February 2010	9.1 SP1	Preliminary support for Cyclone IV E devices.
November 2009	9.1	■ New controller architecture added. ■ Preliminary support for Cyclone III LS and Cyclone IV devices.

Errata

Table 9–2 shows the issues that affect the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP v10.1, v10.0SP1, 10.0, 9.1, and 9.0.

Not all issues affect all versions of the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP.

Table 9–2. DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP MegaCore Function Errata (Part 1 of 2)

Added or Updated	Issue	Affected Version				
		10.1	10.0 SP1	10.0	9.1 SP2	9.1
15 Dec 10	Resynchronization Registers Incorrectly Placed in Core instead of I/O	✓	✓	—	—	—
	Half Rate Bridge Not Supported	✓	—	—	—	—
	pin_assignments.tcl Contains Incorrect Pin Names in Qsys Systems	✓	—	—	—	—
	Warning Messages Reporting Ignored SDC Constraints	✓	—	—	—	—
	SOPC Builder Not Supported for DDR SDRAM Controller with ALTMEMPHY	✓	—	—	—	—
15 Sept 10	Reduced Clock Rate Specification for Column and Row I/Os	✓	✓	✓	—	—

Table 9–2. DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP MegaCore Function Errata (Part 2 of 2)

Added or Updated	Issue	Affected Version				
		10.1	10.0 SP1	10.0	9.1 SP2	9.1
15 July 10	Error in Board Settings GUI	✓	✓	✓	—	—
	Using Merging Feature	✓	✓	✓	—	—
	Memory Controller Returns Wrong Data	✓	✓	✓	—	—
	Refresh to Precharge Command Timing Violation	✓	✓	✓	—	—
	Power-Down Entry Command Timing Violation	✓	✓	✓	—	—
	Failure to Regenerate 9.0 Designs in Silent Mode	✓	✓	✓	—	—
	csr_waitrequest Signal Exhibits “X” in Simulation	—	—	Fixed	✓	✓
	Wrong or Corrupted Data on Reads	—	—	Fixed	✓	✓
15 May 10	Cyclone III Speed Grade Support for Full-Rate DDR2 SDRAM Memory Specification	✓	✓	✓	✓	✓
	DQS and DQSn Signals Generate Extra Pulse	✓	✓	✓	✓	✓
01 Apr 10	Postamble Calibration Scheme in Sequencer Violates Timing	✓	✓	✓	✓	✓
	CSR Address 0×005 and 0×006 Contents Cannot be Accessed	✓	✓	✓	✓	✓
	Half-Rate Clock Not Connected When Clock Sharing is Enabled	✓	✓	✓	✓	✓
15 Feb 10	Wrong Default Value	✓	✓	✓	✓	—
15 Nov 09	Timing Violation In Half-Rate Bridge Enabled Designs	✓	✓	✓	✓	✓
	Generate Simulation Model Option Gets Disabled	✓	✓	✓	✓	✓
	DDR Controller Designs in AFI Mode with Memory Burst Length of 2 Fail in Simulation	✓	✓	✓	✓	✓
	Designs with Eight Chip Selects Fail Compilation	✓	✓	✓	✓	✓
15 Mar 09	Designs with Error Correction Coding (ECC) Do Not Work After Subsequent Reset	✓	✓	✓	✓	✓
01 Dec 08	SOPC Builder Does Not Recognize Decimal Points	✓	✓	✓	✓	✓
15 May 08	RTL Simulation May Fail When Dedicated Memory Clock Outputs Are Selected	✓	✓	✓	✓	✓
	Gate Level Simulation Fails	✓	✓	✓	✓	✓
	VHDL Simulation Fails When DDR CAS Latency 2.0 or 2.5 Is Selected	✓	✓	✓	✓	✓
	Memory Presets Contain Some Incorrect Memory Timing Parameters	✓	✓	✓	✓	✓
15 Oct 07	Mimic Path Incorrectly Placed	✓	✓	✓	✓	✓
01 Dec 06	Simulating with the NCSim Software	✓	✓	✓	✓	✓
	Simulating with the VCS Simulator	✓	✓	✓	✓	✓

Resynchronization Registers Incorrectly Placed in Core instead of I/O

For designs targeting Arria II GX devices, the Quartus II software incorrectly places resynchronization registers in the core instead of the I/O.

Affected configurations

This issue affects designs targeting Arria II GX devices and using the DDR or DDR2 SDRAM Controllers with ALTMEMPHY IP.

Design Impact

Possible intermittent data corruption of the last word in a burst.

Workaround

For Quartus II software versions 10.1 and 10.0SP1, download and install the Quartus II software patch described in the solution available here: http:/www.altera.com/support/kdb/solutions/rd12132010_638.html.

Solution Status

This issue will be fixed in a future version of the Quartus II software.

Half Rate Bridge Not Supported

The Half Rate Bridge feature is not available in version 10.1 of the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP.

Affected configurations

This issue affects all configurations.

Design Impact

Simulation fails.

Workaround

Do not enable the Half Rate Bridge feature.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP.

pin_assignments.tcl Contains Incorrect Pin Names in Qsys Systems

For systems generated with Qsys, the <*variation_name*>**_pin_assignments.tcl** script does not assign correct pin names. This situation occurs because the entity name assigned by Qsys is not yet known at generation time when the <*variation_name*>**_pin_assignments.tcl** script is generated.

Affected configurations

This issue affects all configurations.

Design Impact

Your design fails to simulate and does not work in hardware.

Workaround

After generating your IP core, edit the <*variation_name*>**_pin_assignments.tcl** script and change the `set instance_name` line to specify the correct name of your controller instance.

Solution Status

This issue will not be fixed.

Warning Messages Reporting Ignored SDC Constraints

During compilation of a Qsys-generated IP core, the TimeQuest Timing Analyzer may display warning messages indicating that SDC constraints are being ignored. These messages appear because TimeQuest reads the **altera_avalon_half_rate_bridge_constraints.sdc** file even though the Half Rate Bridge feature is not used.

Affected configurations

This issue affects all Qsys-generated configurations.

Design Impact

This issue has no design impact.

Workaround

To prevent display of the warning messages, remove the **altera_avalon_half_rate_bridge_constraints.sdc** file from the project and from any **.qip** file.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP.

SOPC Builder Not Supported for DDR SDRAM Controller with ALTMEMPHY

SOPC Builder does not support the DDR SDRAM Controller with ALTMEMPHY in version 10.1. The DDR2 SDRAM Controller with ALTMEMPHY is supported.

Affected configurations

This issue affects all configurations.

Design Impact

Your design fails.

Workaround

There is no workaround for this issue.

Solution Status

This issue will be fixed in a future version of the DDR SDRAM Controller with ALTMEMPHY IP.

Reduced Clock Rate Specification for Column and Row I/Os

Commencing with the Quartus II software version 10.0 SP1, the clock rate specification for column and row I/Os is decreased from 150MHz to 133MHz for full-rate DDR2 IP cores on Cyclone IV E I8L devices with vcc=1.0V. This reduction in specification is due to changes associated with finalized timing models.

Affected Configurations

This issue affects all configurations.

Design Impact

The maximum clock rate for column and row I/Os is decreased.

Workaround

Do not use the IP core with column and row I/Os greater than 133MHz in full-rate mode on Cyclone IV E I8L devices with vcc=1.0V.

Designs already using Cyclone IV E I8L devices with vcc=1.0V with full-rate DDR2 SDRAM at 150MHz (the previous clock rate specification) which pass timing in the Quartus II software version 10.0SP1 and later should continue to work, as long as you accurately populate the Board Settings panel in the MegaWizard and you correctly enter board trace models representative of the system in the Pin Planner.

Solution Status

This issue will not be fixed.

Error in Board Settings GUI

The following board settings errors occur in the ALTMEMPHY MegaWizard interface:

- For Cyclone IV E and Cyclone IV GX designs, the single-rank board presets are used even if you specify more than one chip select.
- For Stratix III designs, the board parameters are editable but cannot be used for timing analysis.

Affected Configurations

This issue affects all designs that target the Cyclone IV or Stratix III devices.

Design Impact

Your design may be parameterized wrongly.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP.

Using Merging Feature

When you generate designs with DDR or DDR2 high-performance controller II (HPC II), the merging feature is turned off by default. If your traffic exercises pattern that you can merge, you should turn on merging. Turning merging on may affect f_{MAX} performance.

Affected Configurations

This issue affects all designs that use the DDR or DDR2 HPC II architecture in version 10.0 of the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP.

Design Impact

If you can merge traffic when you turn on the merging feature, there is a performance improvement.

Workaround

To turn on the command merging feature, follow these steps:

1. Open the <*variation_name*>**_alt_ddrx_controller_wrapper.v** file.
2. Search for the `ENABLE_BURST_MERGE` parameter.
3. Change the value from 0 to 1.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP.

Memory Controller Returns Wrong Data

For designs that use the DDR or DDR2 HPC II architecture with **CHIP-ROW-BANK-COL** selected for the **Local-to-Memory Address Mapping** option in SOPC Builder, the memory controller returns incorrect data. When you initialize the memory content with the initialization data file, the fetched memory content does not match the initialization data file. This issue does not affect operation in hardware.

Affected Configurations

This issue affects all designs that use the DDR or DDR2 HPC II architecture with **CHIP-ROW-BANK-COL** selected for the **Local-to-Memory Address Mapping** option in SOPC Builder.

Design Impact

Your design fails to simulate.

Workaround

Select **CHIP-BANK-ROW-COL** for the **Local-to-Memory Address Mapping** option instead.

Solution Status

This issue will not be fixed.

Refresh to Precharge Command Timing Violation

Designs that use the DDR or DDR2 HPC II architecture with the **Enable User Auto-Refresh Controls** option turned on, violate refresh to precharge command timing, breaching JEDEC requirement.

Affected Configurations

This issue affects all designs that use the DDR or DDR2 HPC II architecture with the **Enable User Auto-Refresh Controls** option turned on.

Design Impact

Your design fails to simulate and doesn't work in hardware.

Workaround

To meet the JEDEC requirement, perform the following steps:

1. Open the **alt_ddrx_bank_timer.v** file.
2. Locate the following command:

   ```
   cs_can_precharge_all [w_cs] = chip_idle;
   ```

   and change to:

   ```
   cs_can_precharge_all [w_cs] = power_saving_enter_ready [w_cs] & chip_idle;
   ```

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP.

Power-Down Entry Command Timing Violation

Designs that use the DDR or DDR2 HPC II architecture with the **Enable Auto Power Down** option turned on, violate refresh to precharge command timing, breaching JEDEC requirement.

Affected Configurations

This issue affects all designs that use the DDR or DDR2 HPC II architecture with the **Enable Auto Power Down** option turned on.

Design Impact

Your design fails to simulate and doesn't work in hardware.

Workaround

To meet the JEDEC requirement, perform the following steps:

1. Open the **alt_ddrx_bank_timer.v** file.
2. Locate the following command:

```
always @ (*)
begin
cs_can_power_down [w_cs] = power_saving_enter_ready [w_cs] & chip_idle;
end
and change to:
always @ (posedge ctl_clk or negedge ctl_reset_n)
begin
if (!ctl_reset_n)
cs_can_power_down [w_cs] <= 1'b0;
else
cs_can_power_down [w_cs] <= power_saving_enter_ready [w_cs] & chip_idle;
end
```

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP.

Failure to Regenerate 9.0 Designs in Silent Mode

If you regenerate your version 9.0 designs in silent mode, the controller is defaulted to the HPC II architecture and triggers a "memory burst length" error.

Affected Configurations

This issue affects all version 9.0 configurations.

Design Impact

Your design fails to generate successfully.

Workaround

Open your design in version 10.0 of the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP, and regenerate your design.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP.

csr_waitrequest Signal Exhibits "X" in Simulation

If you generate a DDR or DDR2 controller with the **High Performance Controller II** and **Enable Configuration and Status Register Interface** options turned on, the `csr_waitrequest` signal exhibits 'X' in simulation.

Affected Configurations

This issue affects all designs that use the high-performance controller II architecture with the **Enable Configuration and Status Register Interface** option turned on.

Design Impact

Your design fails to simulate.

Workaround

Remove the `csr_waitrequest` signal connection from your design.

Solution Status

This issue is fixed in version 10.0 of the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP.

Wrong or Corrupted Data on Reads

Certain traffic patterns in designs using DDR2 SDRAM high-performance controllers may cause writes to fail, making reads return unexpected data.

Affected Configurations

This issue affects all designs that use the DDR2 SDRAM HPC II architecture with close read to write transactions.

Design Impact

The data written is corrupted.

Workaround

Open your design in the version 10.0 of the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP, and regenerate your design.

Solution Status

This issue is fixed in version 10.0 of the DDR2 SDRAM Controller with ALTMEMPHY IP.

Cyclone III Speed Grade Support for Full-Rate DDR2 SDRAM Memory Specification

The maximum clock rate for Cyclone III speed grades supporting full-rate DDR2 SDRAM on column I/Os are downgraded for version 9.1 and later. The maximum clock rate is downgraded because the Quartus II tool is unable to achieve push-button placement at the faster clock rates with DDR2 SDRAM high-performance controller II (HPC II).

Table 9–3 shows the downgraded specifications for the Quartus II software version 9.1.

Table 9–3. Full-Rate DDR2 SDRAM Support for Cyclone III Devices

Memory Standard	Device	Speed Grade	Maximum Full-Rate Clock Rate (MHz)
			Column I/O (Single Chip Select)
DDR2 SDRAM	Cyclone III	C6	167 *(1)*
		C7	150 *(2)*
		C8, I7, A7	150 *(1)*

Notes to Table 9–3:

(1) You need 267-MHz memory component speed grade when using class I I/O standard and 333-MHz memory component speed grade when using class II I/O standard.

(2) You need 200-MHz memory component speed grade.

Affected Configurations

This issue affects all designs that use full-rate DDR2 SDRAM with HPC II architecture and target the Cyclone III devices. If you are using DDR2 SDRAM with HPC architecture, you are not affected by this downgrade.

Design Impact

There is no design impact.

Workaround

To achieve higher clock rates, refer to the solution provided at http://www/support/kdb/solutions/rd05112010_783.html.

Solution Status

This issue will be fixed in a future version of the DDR2 Controller with ALTMEMPHY IP.

DQS and DQSn Signals Generate Extra Pulse

The DQS and DQSn signals generate an extra pulse after a write for designs that use the half-rate DDR or DDR2 SDRAM with HPC architecture.

Because the controller asserts the DM pin high after the write burst, the extra pulse does not cause any incorrect data to be written into the memory.

Affected Configurations

This issue affects all designs that use half-rate DDR or DDR2 SDRAM with HPC architecture and target Arria II GX, Stratix III, or Stratix IV devices.

Design Impact

If your board is not using DM pins, incorrect data may be written into the memory.

Workaround

Use the HPC II architecture instead.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP.

Postamble Calibration Scheme in Sequencer Violates Timing

For DDR memory interfaces with low frequency, the postamble calibration scheme in the sequencer violates the refresh memory timing parameter, breaching the JEDEC specifications.

Affected Configurations

This issue affects all designs with DDR SDRAM controller using the following frequencies and devices:

- Frequency between 110 and 120 MHz for Arria II GX devices.
- Frequency between 100 and 110 MHz for Stratix II devices.
- Frequency below 133 MHz frequency for Stratix III and Stratix IV devices.

Design Impact

Your design fails to simulate.

Workaround

Reduce the initial postamble latency by performing the following steps:

1. Open <*variation name*>**_phy_alt_mem_phy.v** file.
2. Search for the `POSTAMBLE_INITIAL_LAT` parameter.
3. Subtract a few cycles off from the current value.

Solution Status

This issue will be fixed in a future version of the DDR SDRAM Controller with ALTMEMPHY IP.

CSR Address 0×005 and 0×006 Contents Cannot be Accessed

Designs that use the DDR or DDR2 HPC II architecture with the **Enable Configuration and Status Register Interface** option turned on, cannot access the CSR address 0×005 and 0×006 contents.

Affected Configurations

This issue affects all designs that use the DDR or DDR2 high-performance controller II architecture with the **Enable Configuration and Status Register Interface** option turned on.

Design Impact

Your design fails to simulate and doesn't work in hardware.

Workaround

To access the CSR address 0×005 and 0×006 contents, perform the following steps:

1. Open <*variation name*>**_controller_phy.v** file.
2. Search for the following debug ports under the <variation *name*>_phy instantiation.
   - `dbg_clk` (Clock)
   - `dbg_addr` (Address)
   - `dbg_cs` (Chip select)
   - `dbg_waitrequest` (Wait request)
   - `dbg_wr` (Write request)
   - `dbg_wr_data` (Write data)
   - `dbg_rd` (Read request)
   - `dbg_dr_data` (Read data)
3. Export these ports into <*variation name*>**_example.v** file.
4. Use the Avalon-MM protocol to access the CSR address 0×005 and 0×006 contents through the debug ports.

Solution Status

This issue will not be fixed.

Half-Rate Clock Not Connected When Clock Sharing is Enabled

If you generate a DDR or DDR2 controller with the **High Performance Controller II** and **Multiple Controller Clock Sharing** options enabled in SOPC Builder, the half-rate clock is not connected.

Affected Configurations

This issue affects all designs that use the high-performance controller II architecture with the **Multiple Controller Clock Sharing** option enabled in SOPC Builder.

Design Impact

The internal half-rate bridge for the sharing PLL controller does not function.

Workaround

To connect the half-rate clock, perform the following steps:

1. Edit the sharing PLL controller top-level file to include the half-rate clock input port as in the following example:

- Verilog HDL

```
module <variation name> (

sys_clk_in,
sys_half_clk_in,
soft_reset_n,

input sys_clk_in;
input    sys_half_clk_in;
input soft_reset_n;

.sys_clk_in(sys_clk_in),
.sys_half_clk_in(sys_half_clk_in),
.soft_reset_n(soft_reset_n),
```

- VHDL

```
ENTITY <variation name_master> IS
PORT (

sys_clk_in  : IN STD_LOGIC;
sys_half_clk_in   : IN STD_LOGIC;
soft_reset_n      : IN STD_LOGIC;

COMPONENT <variation name>_controller_phy
PORT (

sys_clk_in  : IN STD_LOGIC;
sys_half_clk_in   : IN STD_LOGIC;
soft_reset_n      : IN STD_LOGIC;

sys_clk_in  =>  sys_clk_in,
sys_half_clk_in => sys_half_clk_in,
aux_full_rate_clk  =>  aux_full_rate_clk,
```

2. Edit the SOPC top-level file to connect the half-rate clock from the source to the sharing controller as in the following example:

- Verilog HDL

```
<variation name> the_ <variation name>
(

.soft_reset_n (clk_0_reset_n),
.sys_half_clk_in     ( <variation name_master>_aux_half_rate_clk_out),
.sys_clk_in   (<variation name_master>_phy_clk_out)
```

- VHDL

```
component <variation name> is
port (
-- inputs:

signal soft_reset_n : IN STD_LOGIC;
signal sys_half_clk_in : IN STD_LOGIC;
signal sys_clk_in : IN STD_LOGIC;

the_<variation name> : <variation name>
port map(

soft_reset_n => clk_0_reset_n,
sys_half_clk_in => out_clk_<variation name_master>_aux_half_rate_clk,
sys_clk_in => internal_<variation name_master>_phy_clk_out
```

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP.

Wrong Default Value

If you generate the core targeting a Cyclone IV E device with the high-performance controller architecture, without creating a new project first , the MegaWizard Plug-In Manager selects the default speed grade and clock frequency values that are not supported. If you generate the core, "`The given combination of PLL input and output cannot be synthesized.`" error message appears.

Affected Configurations

This issue affects all designs that use the high-performance controller architecture targeting Cyclone IV E devices .

Design Impact

Your system cannot be generated.

Workaround

Create a new project and select the device first before generating the core. Make sure to specify the speed grade to a value higher that 8, and the clock frequency to a value higher that 200 MHz.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP.

Timing Violation In Half-Rate Bridge Enabled Designs

Timing violation occurs during TimeQuest timing analysis for designs that use the high-performance controller II architecture with the **Enable Half Rate Bridge** option turned on.

Affected Configurations

This issue affects all designs that use the high-performance II controller architecture with the **Enable Half Rate Bridge** option turned on.

Design Impact

Timing violation occurs during compilation in the TimeQuest timing analyzer.

Workaround

Open the **altera_avalon_half_rate_bridge_constraints.sdc** file in your project directory, and edit the `slow_clock` variable and add `derive_pll_clocks`.

- Full-rate design

```
derive_pll_clocks
set slow_clk "*|altpll_component|auto_generated|pll1|clk[1]"
```

- Half-rate design

```
derive_pll_clocks
```

set slow_clk "* | altpll_component | auto_generated | pll1 | clk[0]"

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP

Generate Simulation Model Option Gets Disabled

The **Generate simulation model** option gets disabled after every generation.

Affected Configurations

This issue affects all configurations.

Design Impact

The simulation model for your design is not generated for the second time.

Workaround

Turn on the **Generate simulation model** option each time you want to generate a simulation model.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP.

DDR Controller Designs in AFI Mode with Memory Burst Length of 2 Fail in Simulation

Designs that use the full-rate DDR SDRAM high-performance controller in AFI mode with a memory burst length of 2 fail to simulate.

Affected Configurations

This issue affects all designs that use DDR SDRAM high-performance controller in full-rate mode with a memory burst length of 2.

Design Impact

As the generated memory model does not support memory burst length of 2, your design fails to simulate.

Workaround

Use a vendor memory model instead.

Solution Status

This issue will not be fixed in a future version of the DDR SDRAM Controller with ALTMEMPHY IP.

Designs with Eight Chip Selects Fail Compilation

Designs that use eight chip selects with the high-performance controller architecture fail to compile.

Affected Configurations

This issue affects all designs that use eight chip selects with the high-performance controller architecture.

Design Impact

Your design fails to compile.

Workaround

In the MegaWizard interface, select **High Performance Controller II** as your controller architecture.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP.

Designs with Error Correction Coding (ECC) Do Not Work After Subsequent Reset

Some designs with DDR or DDR2 SDRAM high-performance controllers do not work with the **Enable Error Detection and Correction Logic** option turned on.

Affected Configurations

This issue affects all designs that use DDR and DDR2 SDRAM high-performance controllers that have the **Enable Error Detection and Correction Logic** option turned on.

Design Impact

Your design does not work properly in both simulation and hardware after the subsequent reset.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP.

SOPC Builder Does Not Recognize Decimal Points

If you assign the PLL clock with a value with decimals, SOPC Builder takes only the whole number and does not recognize the value after the decimal point. When you generate the system, the "`The PLL reference clock of` <*value*> `does not match the clock frequency input to refclk`" error message appears.

Affected Configurations

This issue affects all designs that have a PLL clock value with decimals.

Design Impact

Your system cannot be generated.

Workaround

Ignore the error message, and generate the system by holding down the Ctrl key on the keyboard while clicking **Generate** in SOPC Builder.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP.

RTL Simulation May Fail When Dedicated Memory Clock Outputs Are Selected

The example testbench RTL simulation may not simulate correctly when a dedicated memory clock phase is selected because clock net delay between the PLL and the clock output pins is not modelled in the RTL.

Affected Configurations

This issue affects designs that enable the **Use dedicated PLL outputs to drive memory clocks** option and set a value for the **Dedicated memory clock phase** parameter.

Design Impact

The design does not simulate correctly.

Workaround

Add `MEM_CLK_DELAY` to `clk_to_ram` signal at example top-level testbench, to compensate for the on-chip clock net delay to `mem_dqs` which is not present in the RTL simulation.

```
parameter DED_MEM_CLK = 1;
parameter real DED_MEM_CLK_PHASE = <value for dedicated memory clock phase>
parameter real mem_clk_ratio = ((360.0DED_MEM_CLK_PHASE)/360.0);
parameter MEM_CLK_DELAY = mem_clk_ratio*CLOCK_TICK_IN_PS * (DED_MEM_CLK ? 1 : 0);
wire clk_to_ram0, clk_to_ram1, clk_to_ram2;
assign #(MEM_CLK_DELAY/4.0) clk_to_ram2 = clk_to_sdram[0];
assign #(MEM_CLK_DELAY/4.0) clk_to_ram1 = clk_to_ram2;
assign #(MEM_CLK_DELAY/4.0) clk_to_ram0 = clk_to_ram1;
assign #((MEM_CLK_DELAY/4.0)) clk_to_ram = clk_to_ram0;
//Replace testbench clk_to_ram assignment by adding MEM_CLK_DELAY
//assign clk_to_ram = clk_to_sdram[0];
```

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP.

Gate Level Simulation Fails

Gate level simulation of the example design and example testbench fails when **Use differential DQS** is enabled in the DDR2 High-Performance Controller.

Affected Configurations

This issue affects DDR2 SDRAM High-Performance Controller designs in Stratix III and Stratix IV devices that have the **Use differential DQS** option enabled.

Design Impact

Gate level simulation of the example design does not behave correctly.

Workaround

You can use the following options:

1. To connect dqs_n example top-level design:

```
- .mem_dqsn(mem_dqsn)
```

2. To connect dqs_n in memory model:

```
-.DQSN mem_dqsn[index])
```

Solution Status

This issue will be fixed in a future version of the DDR2 SDRAM Controller with ALTMEMPHY IP.

VHDL Simulation Fails When DDR CAS Latency 2.0 or 2.5 Is Selected

VHDL generated sequencer block for CAS latency 2.0 and 2.5 designs using DDR SDRAM High-Performance Controller results in simulation failure. The issue is due to delta cycle delays on a clock net.

Affected Configurations

This issue affects DDR SDRAM High-Performance Controller CAS latency 2.0 and 2.5 designs.

Design Impact

This issue only affects simulation on VHDL and does not affect the functionality of the design.

Workaround

To work around this issue, follow these steps:

1. Open the *<variation_name>*_**phy.vho** file in the project directory.
2. Search for the altsyncram instantiation for the postamble block (this can be done by searching for " altsyncram" —note the white space). This should be the altsyncram component with a label that includes the word "postamble".
3. Search for the signal that is attached to the clock1 port to find the point in the design where this signal is assigned to (in a test case, this is on line 4043).

```
wire_<variation_name>_phy_<variation_name>_phy_alt_mem_phy_sii_<variat
ion_name>_phy_alt_mem_phy_sii_inst_<variation_name>phy_alt_mem_phy_pos
tamble_sii_poa_altsyncram_half_rate_ram_gen_altsyncram_inst_19557_cloc
k1
```

4. Change the assignment as shown. The signal inside not(..) should be the same as the signal on clock0 port of a second instance of the altsyncram component which is associated to the read datapath (with "read_dp" in the label).

```
wire_<variation_name>_phy_<variation_name>_phy_alt_mem_phy_sii_<variat
ion_name>_phy_alt_mem_phy_sii_inst_<variation_name>_phy_alt_mem_phy_po
stamble_sii_poa_altsyncram_half_rate_ram_gen_altsyncram_inst_19557_clo
ck1 <= not
(wire_<variation_name>_phy_<variation_name>_phy_alt_mem_phy_sii_<varia
tion_name>_phy_alt_mem_phy_sii_inst_<variation_name>_phy_alt_mem_phy_c
lk_reset_sii_clk_<variation_name>_phy_alt_mem_phy_pll_sii_pll_19462_c4
);
```

☞ This step removes a delta delay for simulation but leaves the code unchanged. The right side of the assignment above is taken as the right side of the assignment to the signal which is previously assigned to the "wire_<variation_name>_phy_<variation_name>_phy_alt_mem_phy_sii_<variation_name>_phy_alt_mem_phy_sii_inst_<variation_name>_phy_alt_mem_phy_postamble_sii_poa_altsyncram_half_rate_ram_gen_altsyncram_inst_19557_clock1" signal.

5. If the <*variation_name*>**_phy** component is recompiled in your simulator, the design should now pass.

Solution Status

This issue will be fixed in a future version of the DDR SDRAM Controller with ALTMEMPHY IP.

Memory Presets Contain Some Incorrect Memory Timing Parameters

The memory presets contain incorrect data for the tDSa and tDHa memory timing parameters.

Affected Configurations

This issue affects all configurations.

Design Impact

Timing analysis results for write and address/command paths may be incorrect.

Workaround

Make sure that the memory timing parameters in the MegaWizard Plug-In Manager match the datasheet of the target memory device. The output edge rate and the use of single-ended versus differential DQS may affect certain memory parameters.

Solution Status

This issue will be fixed in a future version of the DDR2 SDRAM Controller with ALTMEMPHY IP.

Mimic Path Incorrectly Placed

The Quartus II software may fail to place the mimic path correctly. The report timing script then indicates a timing setup failure on the mimic path.

Affected Configurations

This issue affects all designs.

Design Impact

Your design may fail.

Workaround

Manually edit the following parameter in the auto-generated Synopsis design constraint (.**sdc**) script to correct the timing analysis:

```
mimic_shift
```

Add a value of at least the worst case failed slack to the value already stated in the Synopsis design constraint file.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP.

Simulating with the NCSim Software

The DDR and DDR2 SDRAM High-Performance Controller MegaCore functions do not fully support the NCSim software.

Affected Configurations

This issue affects all configurations.

Design Impact

The design does not simulate.

Workaround

Set the `-relax` switch for all calls to the VHDL analyzer.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP.

Simulating with the VCS Simulator

The DDR and DDR2 SDRAM High-Performance Controller MegaCore functions do not fully support the VCS simulator.

Affected Configurations

This issue affects all configurations.

Design Impact

The design does not simulate.

Workaround

The following workarounds exist.

VHDL

Change the following code:

- In file <*variation name*>**_example_driver.vhd**, change all `when` statements between lines 333 and 503 from `when std_logic_vector'("<bit_pattern>")` to `when "<bit_pattern>"`.
- In file **testbench**<*example name*>**_tb**, change line 191 from `signal zero_one(gMEM_BANK_BITS -1 downto 0) := (0 => '1', others => '0')` to `signal zero_one(gMEM_BANK_BITS -1 downto 0) := ('1', others=> '0')`.

Verilog HDL

No changes are necessary. Calls to the Verilog analyzer sets the `+v2k` switch to enable Verilog 2000 constructs.

Solution Status

This issue will be fixed in a future version of the DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP.

10. DDR2 and DDR3 SDRAM Controller with UniPHY

Revision History

Table 10–1 shows the revision history for the DDR2 and DDR3 SDRAM Controller with UniPHY IP core.

For more information about the new features, refer to the *DDR2 and DDR3 SDRAM Controller with UniPHY IP User Guide*.

Table 10–1. DDR2 and DDR3 SDRAM Controller with UniPHY Revision History

Date	Version	Description
December 2010	10.1	■ Added preliminary support for Arria II GZ. ■ Added full-rate DDR2 support. ■ Added DDR2 and DDR3 RDIMM support. ■ Added new generated directory structure. ■ Added new OCT Sharing Interface feature. ■ Added External Memory Interface Toolkit.
July 2010	10.0	First release.

Errata

Table 10–2 shows the issues that affect the DDR2 and DDR3 SDRAM Controller with UniPHY IP core v10.1 and v10.0.

Table 10–2. DDR2 and DDR3 SDRAM Controller with UniPHY Errata (Part 1 of 2)

Added or Updated	Issue	Affected Version	
		10.1	10.0
15 Jan 11	Error in Graphical Display of DQ Calibration Margin in EMIF Toolkit	✓	—
15 Dec 10	NativeLink Simulation fails for VHDL Output	✓	—
	NativeLink Simulation fails for VHDL Output	—	✓
	Timing-related Warning Messages When Sharing PLLs on Stratix V Devices	✓	—
	Half Rate Bridge Not Supported	✓	—
	Devices Faster than 533MHz Require Manual Derating	✓	—
	Reset Synchronizer May Cause Design to Fail Timing	✓	—
	Compilation Fails if Synthesis Fileset is Mixed with Example Project Files	✓	—
	Warning Messages Displayed When Compiling for Stratix V Devices	✓	—
	Cannot Launch MegaWizard Plug-In Manager by Opening Example Design	✓	—
	Example Design May Not Compile for IP Cores from Earlier Versions	✓	—
	SOPC Builder-generated Systems Cannot Serve as Top-Level Design	✓	—
	Higher Delays and Skews Expected for Corner I/Os in Stratix V Devices	✓	—

Table 10–2. DDR2 and DDR3 SDRAM Controller with UniPHY Errata (Part 2 of 2)

Added or Updated	Issue	Affected Version	
		10.1	10.0
15 Aug 10	Incorrect Clock Uncertainty	✓	✓
	User Guide Contains Incorrect Clock Information	✓	✓
15 July 10	Using Burst Merging Feature	✓	✓
	Autoprecharge Feature is Not Available	✓	✓
	Global Signal Assignments Not Applied	✓	✓
	BSF File Not Generated	Fixed	✓
	Selecting VHDL Gives a Verilog HDL IP Core	Fixed	✓
	Designs Without Leveling Fail in Stratix V Devices	Fixed	✓
	Quartus II Software Cannot Read .mif File for PLL	✓	✓
	Example Design Fails as a Slave	Fixed	✓
	Simulation Fails in Riviera	✓	✓
	Simulation Fails—PLL Clocks Out of Synchronization	✓	✓
	SOPC Builder Designs Suffer Low Efficiency	✓	✓

Error in Graphical Display of DQ Calibration Margin in EMIF Toolkit

The right-hand side of the Read Data Valid Windows and Write Data Valid Windows display in the External Memory Interface Toolkit displays one too many green boxes in each row.

Affected configurations

This issue affects all configurations.

Design Impact

Information displayed in the Read Data Valid Windows and Write Data Valid Windows is inaccurate.

Workaround

Margin values reported in the Margining Status Report are correct. Rely on the values in the Margining Status Report rather than the graphical representations of the Read Data Valid Windows and Write Data Valid Windows.

Solution Status

This issue will be fixed in a future version of the EMIF Toolkit.

NativeLink Simulation fails for VHDL Output

In version 10.1 of the Quartus II software, when a user specifies VHDL output for the DDR2 and DDR3 SDRAM Controller with UniPHY and attempts to simulate using NativeLink, NativeLink fails and reports that it cannot find the file **<***design_name***>.vho** in the top-level directory.

Affected Configurations

This issue affects all VHDL designs.

Design Impact

The simulation fails.

Workaround

This workaround for this issue is to not use NativeLink for simulations of VHDL designs, but to set up simulation manually instead.

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

NativeLink Simulation fails for VHDL Output

In version 10.0 of the Quartus II software, when a user specifies VHDL output for the DDR2 and DDR3 SDRAM Controller with UniPHY and attempts to simulate using NativeLink, NativeLink fails and reports that it cannot find the file **<***design_name***>.vho** in the top-level directory.

Affected Configurations

This issue affects all VHDL designs.

Design Impact

The simulation fails.

Workaround

This workaround for this issue is to edit the **<***design_name***>.vhd** file and remove the line similar to the following:

```
-- IPFS_FILES : <design_name>.vho
```

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

Timing-related Warning Messages When Sharing PLLs on Stratix V Devices

When instantiating a design in PLL/DLL slave mode on a Stratix V device, the TimeQuest Timing Analyzer may display warning messages similar to the following:

```
Warning: Ignored filter at slave_report_timing_core.tcl(176):
slave_inst0|controller_phy_inst|memphy_top_inst|umemphy|uio_pads|
dq_ddio[1].ubidir_dq_dqs|altdq_dqs2_inst|thechain|clkin could not be
matched with a keeper or register or port or pin or cell or net
```

```
Warning: Command get_path failed
```

Affected Configurations

This issue affects Stratix V designs instantiated in PLL/DLL slave mode.

Design Impact

The resulting timing analysis is incorrect.

Workaround

This issue has no workaround. The warning messages can be safely ignored; however, do not rely on the accuracy of the resulting timing analysis.

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

Half Rate Bridge Not Supported

The Half Rate Bridge feature is not available in version 10.1 of the DDR2 and DDR3 SDRAM Controller with UniPHY.

Affected configurations

This issue affects all configurations

Design Impact

You cannot use the Half Rate Bridge feature.

Workaround

There is no workaround for this issue.

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

Devices Faster than 533MHz Require Manual Derating

The DDR3 SDRAM Controller with UniPHY provides automatic derating based on the AC175 threshold. Memory devices faster than 533 MHz require derating based on the AC150 threshold.

Affected configurations

This issue affects all configurations using memory devices faster than 533 MHz.

Design Impact

This issue can result in inaccurate timing analysis.

Workaround

You should calculate derated setup and hold values for your memory device, and enter those values in the DDR3 SDRAM Controller with UniPHY parameter editor.

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

Reset Synchronizer May Cause Design to Fail Timing

Systems generated with SOPC Builder or Qsys may fail timing closure due to paths that include a reset synchronizer.

Affected Configurations

This issue affects all configurations.

Design Impact

The design fails timing closure.

Workaround

A workaround for this issue is to apply the following constraint in the TimeQuest Timing Analyzer:

For SOPC Builder:

```
set_false_path -from {dut_sopc_top_reset_clk_0_domain_synch_module:
dut_sopc_top_reset_clk_0_domain_synch*}
```

For Qsys:

```
set_false_path -from *:rst_controller*|*:alt_rst_sync_uq1|
altera_reset_synchronizer_int_chain[*] -to *:controller_phy_inst|
*:memphy_top_inst|*:umemphy|*:ureset|*:ureset_*_clk|reset_reg[*]
```

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

Compilation Fails if Synthesis Fileset is Mixed with Example Project Files

Compilation fails if the **Files** list in the **Settings** dialog box in the Quartus II software includes files from both the example project located at <*working_dir*>/<*variation_name*>**_example_design_fileset/example_project/** and the synthesis fileset located at <*working_dir*>/<*variation_name*>.

Affected Configurations

This issue affects all configurations.

Design Impact

Compilation fails.

Workaround

A workaround for this issue is to perform the following steps:

1. In an editor, open the <*variation_name*>**_driver.sv** file, located in the <*working_dir*>/<*variation_name*>**_example_design_fileset/example_project/** directory.
2. In the <*variation_name*>**_driver.sv** file, change the entity name <*variation_name*>**_reset_sync** to <*variation_name*>_<*num*>**_reset_sync**, where *num* is the same value as in the <*variation_name*>_<*num*>**_reset_sync.v** filename in the <*working_dir*>/<*variation_name*>/ directory.

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

Warning Messages Displayed When Compiling for Stratix V Devices

When compiling a design for Stratix V devices, the system may display numerous PLL-related warning messages similar to the following:

```
Warning: PLL(s) placed in location FRACTIONALPLL_X0_Y1_N0 do not have a PLL
clock to compensate specified - the Fitter will attempt to compensate all
PLL

Warning: PLL(s) placed in location FRACTIONALPLL_X0_Y1_N0 use multiple
different clock network types - the PLL will compensate for output clocks

Warning: PLL cross checking found inconsistent PLL clock settings:

Warning: Node: mem_if|controller_phy_inst|memphy_top_inst|
pll1~FRACTIONAL_PLL|mcntout was found missing 1 generated clock that
corresponds to a base clock with a period of: 8.000

Warning: Clock: mem_if|ddr3_pll_write_clk was found on node:
mem_if|controller_phy_inst|memphy_top_inst|pll3|outclk with settings that
do not match the following PLL specifications:

Warning: -multiply_by (expected: 21, found: 4264000)
```

```
Warning: -divide_by (expected: 5, found: 1000000)
Warning: -phase (expected: 0.00, found: 90.00)
```

These warning messages are expected and can be ignored.

Affected Configurations

This issue affects all configurations targeting Stratix V devices.

Design Impact

This issue has no design impact.

Workaround

There is no workaround for this issue. You can safely ignore the error messages.

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

Cannot Launch MegaWizard Plug-In Manager by Opening Example Design

You cannot reopen your project in the MegaWizard Plug-In Manager by clicking on your generated IP instantiation **<***variation_name***>.v** in the **<***working_dir***>/<***variation_name***>_example_design_fileset/example_project/** directory.

Affected configurations

This issue affects all configurations.

Design Impact

This issue has no design impact.

Workaround

To reopen your project in the MegaWizard Plug-In Manager, follow these steps:

1. In the Quartus II software, click **MegaWizard Plug-In Manager** on the **Tools** menu.
2. Click **Edit an existing custom megafunction variation** and specify your project.

Solution Status

This issue will not be fixed.

Example Design May Not Compile for IP Cores from Earlier Versions

The example design provided with version 10.1 may not compile with IP cores migrated from earlier versions of the Quartus II software.

Affected configurations

This issue affects all configurations.

Design Impact

Attempting to compile the example design with IP cores migrated from earlier versions of the Quartus II software may fail with the following message:
`Error:instance “ureset_driver_clk” instantiates undefined entity “<variation_name>_reset_sync”`

Workaround

The workaround for this issue is to perform the following steps:

1. In the Quartus II software, open the **Settings** dialog box on the **Assignments** menu.
2. In the **Category** tree of the **Settings** dialog box, click **Files** to display the files list.
3. Remove all the UniPHY files, including the **.qip** file and example project files, from the migrated project assignments.
4. Add to the project the newly generated .**qip** file located in the **<***working_dir***>/<***variation_name***>_example_design_fileset** directory.
5. Add to the project all of the files except for the memory model, from the directory **<***working_dir***>/<***variation_name***>_example_design_fileset/example_project**.

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

SOPC Builder-generated Systems Cannot Serve as Top-Level Design

Systems generated with SOPC Builder cannot serve as the top-level design, because SOPC Builder automatically exports the `parallelterminationcontrol` and `seriesterminationcontrol` OCT control signals as top-level ports, but these signals must not be exposed at the top level.

Affected configurations

This issue affects all configurations generated with SOPC Builder.

Design Impact

Compilation fails.

Workaround

Perform either of the following procedures to work around this issue:

- Create a top-level wrapper which instantiates the SOPC Builder-generated system, and does not make any connection to the `parallelterminationcontrol` or `seriesterminationcontrol` signals.

or

- Open the top-level SOPC Builder system file (for example, *system.v*), and delete the wire names from within the brackets for the `parallelterminationcontrol` and `seriesterminationcontrol` signals for all UniPHY cores. The resulting lines should appear as follows:

```
.parallelterminationcontrol ()
.seriesterminationcontrol ()
```

  The wire names that you delete from within the brackets must also be removed from all other locations in the top-level system file, including the top-level port list.

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

Higher Delays and Skews Expected for Corner I/Os in Stratix V Devices

In Stratix V devices, the corner I/O banks are expected to have higher core-to-I/O and I/O-to-core delay and skew values than the other I/O banks, and are unsuitable for interfacing with external memory at frequencies above 667 MHz.

The characteristics of the corner I/O banks are not yet reflected in the Stratix V timing models available in version 10.1 of the Quartus II software; consequently, timing analysis will not accurately characterize the performance of the corner I/Os.

Affected Configurations

This issue affects all configurations targeting Stratix V devices at frequencies above 667 MHz.

Design Impact

This issue can adversely affect timing.

Workaround

Avoid using the outer I/O banks at the upper and lower sides of the device.

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

Incorrect Clock Uncertainty

A clock uncertainty related to the read FIFO buffer clocked by DQS can result in inaccurate setup and hold slack values.

Affected Configurations

This issue affects all configurations.

Design Impact

This issue can cause setup and hold slack values to be inaccurate.

Workaround

The workaround for this issue is to manually edit the PHY **.sdc** file located in the *<variation_name>***/constraints/** directory, and add the following two lines to the Multicycle Constraints section of the file:

```
set_max_delay -from *ddio_in_inst_regout* -0.05
set_min_delay -from *ddio_in_inst_regout* [expr -$t(CK) + 0.05]
```

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

User Guide Contains Incorrect Clock Information

In the user guide, table 6-1 contains incorrect clock phase information for `pll_mem_clk` and `pll_write_clk`.

Also, table 6-2 is inapplicable and should be ignored.

Affected Configurations

This issue affects all configurations.

Design Impact

This is a documentation issue and has no design impact.

Workaround

The correct phase for `pll_mem_clk` is 0° for interfaces with the Leveling Interface Mode set to **Leveling**, and -45° for interfaces with Leveling Interface Mode set to **Non-leveling**.

The correct phase for `pll_write_clk` is 90° for interfaces with the Leveling Interface Mode set to **Leveling**, and -135° for interfaces with Leveling Interface Mode set to **Non-leveling**.

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

Using Burst Merging Feature

The burst merging feature is turned off by default when a you generate a controller. If your traffic exercises patterns that you can merge, you should turn on merging. Turning merging on may affect f_{MAX} performance.

Affected Configurations

This issue affects all designs.

Design Impact

There is a performance improvement if you can merge traffic when you turn on this feature.

Workaround

To work around this issue, turn on merging, by changing the `ENABLE_BURST_MERGE` paramter from 0 to 1 in the *<variation>***.v** file.

Solution Status

This issue will never be fixed.

Autoprecharge Feature is Not Available

You can select autoprecharge in the MegaWizard interface and the *DDR2 and DDR3 SDRAM Controller with UniPHY IP User Guide v10.0* documents autoprecharge, but the feature is not enabled.

Affected Configurations

This issue affects all configurations.

Design Impact

This issue affects all designs.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

Global Signal Assignments Not Applied

The Fitter sometimes does not honor `GLOBAL` signal assignments applied by the *<variation name>***_pin_assignments.tcl** script.

Affected Configurations

This issue affects all configurations.

Design Impact

This issue has no impact on the design, but can result in suboptimal resource placement and can contribute to difficulties in achieving timing closure.

Workaround

To determine whether the Quartus II software properly applies `GLOBAL` assignments, check the Fitter Report and verify whether any `GLOBAL` signal assignment referring to a PLL output port (for example, `...|auto_generated|clk[*]`) appear in the Ignored Assignments section.

If there is a `GLOBAL` assignment to a PLL output port listed in Ignored Assignments, you can correct the problem by running Analysis and Synthesis and then running the Fitter. You should then verify in the Fitter Report that the assignment is no longer ignored.

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY.

BSF File Not Generated

The IP core does not generate a **.bsf** file, and therefore is not compatible with workflows requiring a **.bsf** file.

Affected Configurations

This issue affects all configurations.

Design Impact

Errors are likely to occur with workflows using the Schematic Editor or Symbol Editor.

Workaround

Do not use the Schematic Editor or the Symbol Editor with the IP core.

Solution Status

This issue is fixed in version 10.1 of the DDR2 and DDR3 SDRAM Controller with UniPHY.

Selecting VHDL Gives a Verilog HDL IP Core

If you select VHDL in the MegaWizard interface and generate a DDR2 or DDR3 SDRAM controller with UniPHY IP core, the generated core is in Verilog HDL.

Affected Configurations

This issue affects all VHDL designs.

Design Impact

The issue affects all VHDL designs.

Workaround

To generate a VHDL IP core follow these steps:

1. In a text editor open <*Quartus II directory*>**\ip\altera\uniphy\lib\common_ddrx.tcl**.
2. Search for the string "LANGUAGE" that appears in the following code:

```
append param_str ",LANGUAGE=[get_generation_property HDL_LANGUAGE]"
```

3. Change this line to the following code:

```
append param_str ",LANGUAGE=vhdl"
```

4. Continue searching for the next occurence of the string "LANGUAGE" which appears in the following code:

```
if {[string compare -nocase [get_generation_property HDL_LANGUAGE]
verilog] == 0} {
   add_file ${outdir}/${outputname}.v {SYNTHESIS SUBDIR}
   puts $qipfile "set_global_assignment -name VERILOG_FILE \[file
join \$::quartus(qip_path) ${outputname}.v\]"
} else {
   add_file ${outdir}/${outputname}.vhd {SYNTHESIS SUBDIR}
   puts $qipfile "set_global_assignment -name VHDL_FILE \[file join
\$::quartus(qip_path) ${outputname}.vhd\]"
}
```

5. Comment out the `if` line, the `else` line, and the block of code in the conditional section so that the code in the "`else`" block always executes, similar to the following code:

```
# if {[string compare -nocase [get_generation_property HDL_LANGUAGE]
verilog] == 0} {
#    add_file ${outdir}/${outputname}.v {SYNTHESIS SUBDIR}
#    puts $qipfile "set_global_assignment -name VERILOG_FILE \[file
join \$::quartus(qip_path) ${outputname}.v\]"
# } else {
   add_file ${outdir}/${outputname}.vhd {SYNTHESIS SUBDIR}
   puts $qipfile "set_global_assignment -name VHDL_FILE \[file join
\$::quartus(qip_path) ${outputname}.vhd\]"
# }
```

6. Use the MegaWizard interface to generate a UniPHY-based IP core.

To generate a Verilog HDL IP core, restore the original **common_ddrx.tcl** file.

Solution Status

This issue is fixed in version 10.1 of the DDR2 and DDR3 SDRAM Controller with UniPHY IP core.

Designs Without Leveling Fail in Stratix V Devices

If you target Stratix V devices with a IP core without leveling, the design fails.

Affected Configurations

This issue affects all Stratix V designs.

Design Impact

Compilation fails.

Workaround

To work around this issue, disable the DM pins.

The MegaWizard interface does not support design without leveling targeting Stratix V devices (the option is disabled), but you can generate a Stratix V design with leveling.

Solution Status

This issue is fixed in version 10.1 of the DDR2 and DDR3 SDRAM Controller with UniPHY IP core.

Quartus II Software Cannot Read .mif File for PLL

The Quartus II software gives a warning that it cannot read the **.mif** file, which causes the PLL to load with unexpected initial settings.

Affected Configurations

This issue affects all designs when you turn on **HardCopy Compatability Mode**.

Design Impact

Compilation fails.

Workaround

To work around this issue, copy the **.mif** file from the <*variation name*>**/rtl** directory to the project directoy.

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY IP core.

Example Design Fails as a Slave

In slave mode, the MegaWizard interface instantiates the PLL in the **example_top.v** file. However for DDR2 and DDR3 SDRAM example designs, the wizard fails to connect the DQS enable clock to the PLL.

Affected Configurations

This issue affects example designs with a slave interface.

Design Impact

This issue has no design impact.

Workaround

To work around this issue, modify **example_top.v** to connect the DQS enable clock (`pll_dqs_ena_clk`) to the c4 port of the PLL:

```
pll_memphy  upll_memphy(
        .areset                 (~global_reset_n),
        .inclk0                 (pll_ref_clk),
        .c0                     (pll_afi_clk),
        .c1                     (pll_mem_clk),
        .c2                     (pll_write_clk),
        .c3                     (pll_addr_cmd_clk),
        .c4                     (pll_dqs_ena_clk),
        .c5                     (pll_avl_clk),
        .c6                     (pll_config_clk),
        .locked                 (pll_locked)
);.
```

Solution Status

This issue is fixed in version 10.1 of the DDR2 and DDR3 SDRAM Controller with UniPHY IP core.

Simulation Fails in Riviera

Simulations with the Riviera software fail.

Affected Configurations

This issue affects all designs.

Design Impact

This issue has no design impact.

Workaround

To work around this issue, modify the following lines in **rand_burstcount_gen.sv** outside of the generate block:

```
localparam MIN_EXPONENT= ceil_log2(MIN_BURSTCOUNT);
localparam MAX_EXPONENT= log2(MAX_BURSTCOUNT);
localparam EXPONENT_WIDTH= ceil_log2(MAX_EXPONENT);
```

Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY IP core.

Simulation Fails—PLL Clocks Out of Synchronization

During simulation, the PLL clocks lose synchronization.

Affected Configurations

This issue affects all designs.

Design Impact

This issue causes simulation failures.

Workaround

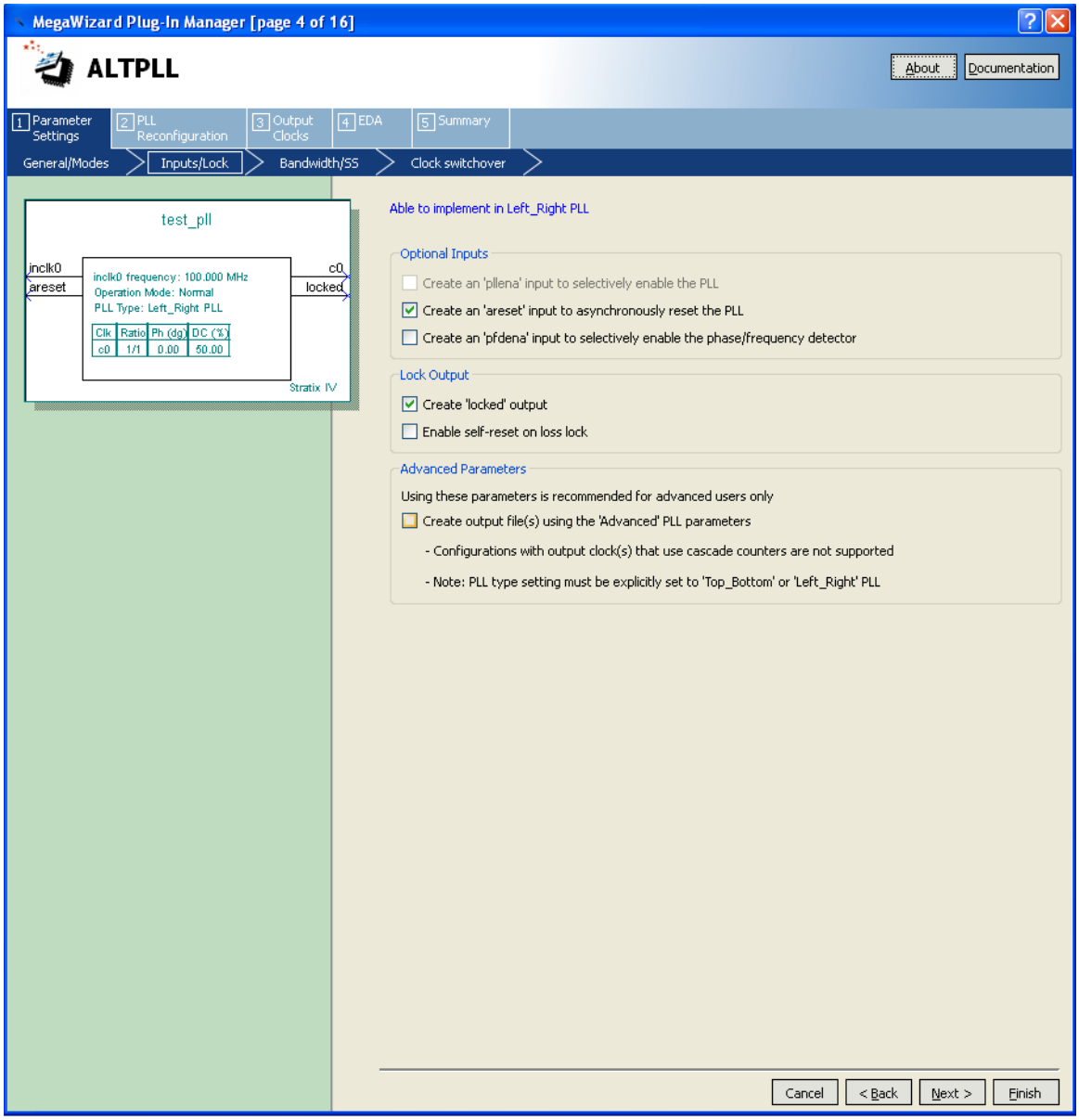
To work around this issue, follow these steps:

1. In text editor open the design file and remove the following line:

   ```
   coverage exclude_file
   ```

2. In the ALTPLL MegaWizard interface, turn on **Create output files using the Advanced PLL parameters** and regenerate the PLL ().

Figure 10–1. PLL Parameter



Solution Status

This issue will be fixed in a future version of the DDR2 and DDR3 SDRAM Controller with UniPHY IP core.

SOPC Builder Designs Suffer Low Efficiency

If you use SOPC Builder to instantiate a DDR2 or DDR3 SDRAM Controller with UniPHY IP core, you may find your design has low memory efficiency.

Affected Configurations

This issue affects all designs when you use SOPC Builder to instantiate a DDR2 or DDR3 SDRAM Controller with UniPHY IP core.

Design Impact

The design has low memory efficiency.

Workaround

To work around this issue, use the MegaWizard Plug-In flow to instantiate a DDR2 or DDR3 SDRAM Controller with UniPHY IP core.

Solution Status

This issue is fixed in version 10.0SP1 of the DDR2 and DDR3 SDRAM Controller with UniPHY IP core.

11. DDR3 SDRAM Controller with ALTMEMPHY IP

Revision History

Table 11–1 shows the revision history for the DDR3 SDRAM Controller with ALTMEMPHY IP MegaCore function.

For more information about the new features, refer to the *DDR3 SDRAM Controller with ALTMEMPHY IP User Guide*.

Table 11–1. DDR3 SDRAM Controller with ALTMEMPHY IP MegaCore Function Revision History

Date	Version	Description
December 2010	10.1	Maintenance release.
July 2010	10.0	■ Added information for new GUI parameters: **Controller latency**, **Enable reduced bank tracking for area optimization**, and **Number of banks to track**. ■ Removed information about IP Advisor. This feature is removed from the DDR3 SDRAM IP support for version 10.0.
April 2010	9.1 SP2	Maintenance release.
February 2010	9.1 SP1	Maintenance release.
November 2009	9.1	■ New controller architecture added. ■ Preliminary support for Cyclone III LS and Cyclone IV devices.

Errata

Table 11–2 shows the issues that affect the DDR3 SDRAM Controller with ALTMEMPHY IP v10.1, v10.0, 9.1, and 9.0.

Table 11–2. DDR3 SDRAM Controller with ALTMEMPHY IP MegaCore Function Errata (Part 1 of 2)

Added or Updated	Issue	Affected Version			
		10.1	10.0	9.1 SP2	9.1
15 Dec 10	Resynchronization Registers Incorrectly Placed in Core instead of I/O	✓	—	—	—
	Half Rate Bridge Not Supported	✓	—	—	—
	Devices Faster than 533MHz Require Manual Derating	✓	—	—	—
	pin_assignments.tcl Contains Incorrect Pin Names in Qsys Systems	✓	—	—	—
	Warning Messages Reporting Ignored SDC Constraints	✓	—	—	—

Table 11–2. DDR3 SDRAM Controller with ALTMEMPHY IP MegaCore Function Errata (Part 2 of 2)

Added or Updated	Issue	Affected Version			
		10.1	10.0	9.1 SP2	9.1
15 July 10	Error in Board Settings GUI	✓	✓	—	—
	Using Merging Feature	✓	✓	—	—
	Memory Controller Returns Wrong Data	✓	✓	—	—
	Refresh to Precharge Command Timing Violation	✓	✓	—	—
	Power-Down Entry Command Timing Violation	✓	✓	—	—
	Failure to Regenerate 9.0 Designs in Silent Mode	✓	✓	—	—
	csr_waitrequest Signal Exhibits “X” in Simulation	—	Fixed	✓	✓
	Wrong or Corrupted Data on Reads	—	Fixed	✓	✓
01 Apr 10	CSR Address 0×005 and 0×006 Contents Cannot be Accessed	✓	✓	✓	✓
	Memory Timing Violation During Activate Read Auto-Precharge to Refresh/Activate	✓	✓	✓	✓
	Half-Rate Clock Not Connected When Clock Sharing is Enabled	✓	✓	✓	✓
15 Nov 09	Timing Violation In Half-Rate Bridge Enabled Designs	✓	✓	✓	✓
	Generate Simulation Model Option Gets Disabled	✓	✓	✓	✓
	Designs with Eight Chip Selects Fail Compilation	✓	✓	✓	✓
01 Jul 09	Address Mirroring Not Supported By Memory Simulation Model	✓	✓	✓	✓
15 Mar 09	Memory Preset Parameters Do Not Get Updated	✓	✓	✓	✓
	Designs with Error Correction Coding (ECC) Do Not Work After Subsequent Reset	✓	✓	✓	✓

Resynchronization Registers Incorrectly Placed in Core instead of I/O

For designs targeting Arria II GX devices, the Quartus II software incorrectly places resynchronization registers in the core instead of the I/O.

Affected configurations

This issue affects designs targeting Arria II GX devices and using the DDR3 SDRAM Controller with ALTMEMPHY IP.

Design Impact

Possible intermittent data corruption of the last word in a burst.

Workaround

For Quartus II software versions 10.1 and 10.0SP1, download and install the Quartus II software patch described in the solution available here: http:/www.altera.com/support/kdb/solutions/rd12132010_638.html.

Solution Status

This issue will be fixed in a future version of the Quartus II software.

Half Rate Bridge Not Supported

The Half Rate Bridge feature is not available in version 10.1 of the DDR3 SDRAM Controller with ALTMEMPHY IP.

Affected configurations

This issue affects all configurations

Design Impact

Simulation fails.

Workaround

Do not enable the Half Rate Bridge feature.

Solution Status

This issue will be fixed in a future version of the DDR3 SDRAM Controller with ALTMEMPHY IP.

Devices Faster than 533MHz Require Manual Derating

The DDR3 SDRAM Controller with ALTMEMPHY provides automatic derating based on the AC175 threshold. Memory devices faster than 533 MHz require derating based on the AC150 threshold.

Affected configurations

This issue affects all configurations using memory devices faster than 533 MHz.

Design Impact

This issue can result in inaccurate timing analysis.

Workaround

You should calculate derated setup and hold values for your memory device, and enter those values in the DDR3 SDRAM Controller with ALTMEMPHY parameter editor.

Solution Status

This issue will be fixed in a future version of the DDR3 SDRAM Controller with ALTMEMPHY.

pin_assignments.tcl Contains Incorrect Pin Names in Qsys Systems

For systems generated with Qsys, the <*variation_name*>**_pin_assignments.tcl** script does not assign correct pin names. This situation occurs because the entity name assigned by Qsys is not yet known at generation time when the <*variation_name*>**_pin_assignments.tcl** script is generated.

Affected configurations

This issue affects all configurations

Design Impact

Your design fails to simulate and does not work in hardware.

Workaround

After generating your IP core, edit the <*variation_name*>**_pin_assignments.tcl** script and change the `set instance_name` line to specify the correct name of your controller instance.

Solution Status

This issue will not be fixed.

Warning Messages Reporting Ignored SDC Constraints

During compilation of a Qsys-generated IP core, the TimeQuest Timing Analyzer may display warning messages indicating that SDC constraints are being ignored. These messages appear because TimeQuest reads the **altera_avalon_half_rate_bridge_constraints.sdc** file even though the Half Rate Bridge feature is not used.

Affected configurations

This issue affects all Qsys-generated configurations.

Design Impact

This issue has no design impact.

Workaround

To prevent display of the warning messages, remove the **altera_avalon_half_rate_bridge_constraints.sdc** file from the project and from any **.qip** file.

Solution Status

This issue will be fixed in a future version of the DDR3 SDRAM Controller with ALTMEMPHY IP.

Error in Board Settings GUI

For Stratix III designs, the board parameters are editable in the ALTMEMPHY MegaWizard interface, but cannot be used for timing analysis.

Affected Configurations

This issue affects all designs that target the Stratix III devices.

Design Impact

Your design may be parameterized wrongly.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the DDR3 SDRAM Controller with ALTMEMPHY IP.

Using Merging Feature

When you generate designs with DDR3 high-performance controller II (HPC II), the merging feature is turned off by default. If your traffic exercises pattern that you can merge, you should turn on merging. Turning merging on may affect f_{MAX} performance.

Affected Configurations

This issue affects all designs that use the DDR3 HPC II architecture in version 10.0 of the DDR3 Controller with ALTMEMPHY IP.

Design Impact

If you can merge traffic when you turn on the merging feature, there is a performance improvement.

Workaround

To turn on the command merging feature, follow these steps:

1. Open the <*variation_name*>**_alt_ddrx_controller_wrapper.v** file.
2. Search for the `ENABLE_BURST_MERGE` parameter.
3. Change the value from 0 to 1.

Solution Status

This issue will be fixed in a future version of the DDR3 SDRAM Controller with ALTMEMPHY IP.

Memory Controller Returns Wrong Data

For designs that use the DDR3 HPC II architecture with **CHIP-ROW-BANK-COL** selected for the **Local-to-Memory Address Mapping** option in SOPC Builder, the memory controller returns incorrect data. When you initialize the memory content with the initialization data file, the fetched memory content does not match the initialization data file. This issue does not affect operation in hardware.

Affected Configurations

This issue affects all designs that use the DDR3 HPC II architecture with **CHIP-ROW-BANK-COL** selected for the **Local-to-Memory Address Mapping** option in SOPC Builder.

Design Impact

Your design fails to simulate.

Workaround

Select **CHIP-BANK-ROW-COL** for the **Local-to-Memory Address Mapping** option instead.

Solution Status

This issue will not be fixed.

Refresh to Precharge Command Timing Violation

Designs that use the DDR3 HPC II architecture with the **Enable User Auto-Refresh Controls** option turned on, violate refresh to precharge command timing, breaching JEDEC requirement.

Affected Configurations

This issue affects all designs that use the DDR3 HPC II architecture with the **Enable User Auto-Refresh Controls** option turned on.

Design Impact

Your design fails to simulate and doesn't work in hardware.

Workaround

To meet the JEDEC requirement, perform the following steps:

1. Open the **alt_ddrx_bank_timer.v** file.
2. Locate the following command:

   ```
   cs_can_precharge_all [w_cs] = chip_idle;
   ```

   and change to:

   ```
   cs_can_precharge_all [w_cs] = power_saving_enter_ready [w_cs] & chip_idle;
   ```

Solution Status

This issue will be fixed in a future version of the DDR3 SDRAM Controller with ALTMEMPHY IP.

Power-Down Entry Command Timing Violation

Designs that use the DDR3 HPC II architecture with the **Enable Auto Power Down** option turned on, violate refresh to precharge command timing, breaching JEDEC requirement.

Affected Configurations

This issue affects all designs that use the DDR3 HPC II architecture with the **Enable Auto Power Down** option turned on.

Design Impact

Your design fails to simulate and doesn't work in hardware.

Workaround

To meet the JEDEC requirement, perform the following steps:

1. Open the **alt_ddrx_bank_timer.v** file.
2. Locate the following command:

```
always @ (*)
begin
cs_can_power_down [w_cs] = power_saving_enter_ready [w_cs] & chip_idle;
end
and change to:
always @ (posedge ctl_clk or negedge ctl_reset_n)
begin
if (!ctl_reset_n)
cs_can_power_down [w_cs] <= 1'b0;
else
cs_can_power_down [w_cs] <= power_saving_enter_ready [w_cs] & chip_idle;
end
```

Solution Status

This issue will be fixed in a future version of the DDR3 SDRAM Controller with ALTMEMPHY IP.

Failure to Regenerate 9.0 Designs in Silent Mode

If you regenerate your version 9.0 designs in silent mode, the controller is defaulted to the HPC II architecture and triggers a "memory burst length" error.

Affected Configurations

This issue affects all version 9.0 configurations.

Design Impact

Your design fails to generate successfully.

Workaround

Open your design in version 10.0 of the DDR3 SDRAM Controller with ALTMEMPHY IP, and regenerate your design.

Solution Status

This issue will be fixed in a future version of the DDR3 SDRAM Controller with ALTMEMPHY IP.

csr_waitrequest Signal Exhibits "X" in Simulation

If you generate a DDR3 controller with the **High Performance Controller II** and **Enable Configuration and Status Register Interface** options enabled, the `csr_waitrequest` signal exhibits 'X' in simulation.

Affected Configurations

This issue affects all designs that use the high-performance controller II architecture with the **Enable Configuration and Status Register Interface** option turned on.

Design Impact

Your design fails to simulate.

Workaround

Remove the `csr_waitrequest` signal connection from your design.

Solution Status

This issue is fixed in version 10.0 of the DDR3 SDRAM Controller with ALTMEMPHY IP.

Wrong or Corrupted Data on Reads

Certain traffic patterns in designs using DDR3 SDRAM high-performance controllers may cause writes to fail, making reads return unexpected data.

Affected Configurations

This issue affects all designs that use the HPC II architecture with close read to write transactions.

Design Impact

The data written is corrupted.

Workaround

Open your design in the version 10.0 of the DDR3 SDRAM Controller with ALTMEMPHY IP, and regenerate your design.

Solution Status

This issue is fixed in version 10.0 of the DDR3 SDRAM Controller with ALTMEMPHY IP.

CSR Address 0×005 and 0×006 Contents Cannot be Accessed

Leveled DDR3 designs that use the ALTMEMPHY-based HPC II architecture with the **Enable Configuration and Status Register Interface** option turned on, cannot access the CSR address 0×005 and 0×006 contents.

Affected Configurations

This issue affects all non-leveled designs that use the ALTMEMPHY-based HPC II architecture with the **Enable Configuration and Status Register Interface** option turned on.

The leveled DDR3 designs, such as DIMMs, also do not have access to the CSR address 0×005 and 0×006 contents, but this is because the IP is not designed to support this feature.

Design Impact

Your design fails to simulate and doesn't work in hardware.

Workaround

To access the CSR address 0×005 and 0×006 contents (discrete device only), follow these steps:

1. Open <*variation name*>**_controller_phy.v** file.
2. Search for the following debug ports under the <variation *name*>_phy instantiation.
   - `dbg_clk` (Clock)
   - `dbg_addr` (Address)
   - `dbg_cs` (Chip select)
   - `dbg_waitrequest` (Wait request)
   - `dbg_wr` (Write request)
   - `dbg_wr_data` (Write data)
   - `dbg_rd` (Read request)
   - `dbg_dr_data` (Read data)
3. Export these ports into <*variation name*>**_example.v** file.
4. Use the Avalon-MM protocol to access the CSR address 0×005 and 0×006 contents through the debug ports.

Solution Status

This issue will not be fixed.

Memory Timing Violation During Activate Read Auto-Precharge to Refresh/Activate

Memory timing violation occurs during the activate to read precharge.

Affected Configurations

This issue affects all designs that use the high-performance controller architecture.

Design Impact

Your design may fail to simulate.

Workaround

For designs targeting 1066 specification and running with 533 MHz speed, increase one control clock cycle of the timing parameters **tRP** and **tRCD**, so that the tRC for the controller is greater than the tRC for the memory model.

For designs targeting 1066 specification and running with 400 MHz speed, increase one control clock cycle of the timing parameter **tRP**, so that the tRC for the controller is greater than the tRC for the memory model.

Solution Status

This issue will be fixed in a future version of the DDR3 SDRAM Controller with ALTMEMPHY IP.

Half-Rate Clock Not Connected When Clock Sharing is Enabled

If you generate a DDR3 controller with the **High Performance Controller II** and **Multiple Controller Clock Sharing** options enabled in SOPC Builder, the half-rate clock is not connected.

Affected Configurations

This issue affects all designs that use the high-performance controller II architecture with the **Multiple Controller Clock Sharing** option enabled in SOPC Builder.

Design Impact

The internal half-rate bridge for the sharing PLL controller does not function.

Workaround

To connect the half-rate clock, perform the following steps:

1. Edit the sharing PLL controller top-level file to include the half-rate clock input port as in the following example:

- Verilog HDL

```
module <variation name> (


sys_clk_in,
sys_half_clk_in,
```

```
soft_reset_n,
input sys_clk_in;
input    sys_half_clk_in;
input soft_reset_n;

.sys_clk_in(sys_clk_in),
.sys_half_clk_in(sys_half_clk_in),
.soft_reset_n(soft_reset_n),
```

- VHDL

```
ENTITY <variation name_master> IS
PORT (

sys_clk_in  : IN STD_LOGIC;
sys_half_clk_in   : IN STD_LOGIC;
soft_reset_n      : IN STD_LOGIC;

COMPONENT <variation name>_controller_phy
PORT (

sys_clk_in  : IN STD_LOGIC;
sys_half_clk_in   : IN STD_LOGIC;
soft_reset_n      : IN STD_LOGIC;
sys_clk_in  =>  sys_clk_in,
sys_half_clk_in => sys_half_clk_in,
aux_full_rate_clk  =>  aux_full_rate_clk,
```

2. Edit the SOPC top-level file to connect the half-rate clock from the source to the sharing controller as in the following example:

- Verilog HDL

```
<variation name> the_ <variation name>
(

.soft_reset_n (clk_0_reset_n),
.sys_half_clk_in     ( <variation
name_master>_aux_half_rate_clk_out),
.sys_clk_in   (<variation name_master>_phy_clk_out)
```

- VHDL

```
component <variation name> is
port (
-- inputs:
```

```
signal soft_reset_n : IN STD_LOGIC;
signal sys_half_clk_in : IN STD_LOGIC;
signal sys_clk_in : IN STD_LOGIC;

the_<variation name> : <variation name>
port map(

soft_reset_n => clk_0_reset_n,
sys_half_clk_in => out_clk_<variation name_master>_aux_half_rate_clk,
sys_clk_in => internal_<variation name_master>_phy_clk_out
```

Solution Status

This issue will be fixed in a future version of the DDR3 SDRAM Controller with ALTMEMPHY IP.

Timing Violation In Half-Rate Bridge Enabled Designs

Timing violation occurs during TimeQuest timing analysis for designs that use the high-performance controller II architecture with the **Enable Half Rate Bridge** option turned on using SOPC Builder.

Affected Configurations

This issue affects all designs that use the high-performance controller II architecture with the **Enable Half Rate Bridge** option turned on.

Design Impact

Timing violation occurs during compilation in the TimeQuest timing analyzer.

Workaround

Open the **altera_avalon_half_rate_bridge_constraints.sdc** file in your project directory, and add `derive_pll_clocks` above the `slow_clock` variable.

```
derive_pll_clocks
set slow_clk "*|altpll_component|auto_generated|pll1|clk[0]"
```

Solution Status

This issue will be fixed in a future version of the DDR3 SDRAM Controller with ALTMEMPHY IP.

Generate Simulation Model Option Gets Disabled

The **Generate simulation model** option gets disabled after every generation.

Affected Configurations

This issue affects all configurations.

Design Impact

The simulation model for your design is not generated for the second time.

Workaround

Turn on the **Generate simulation model** option each time you want to generate a simulation model.

Solution Status

This issue will be fixed in a future version of the DDR3 SDRAM Controller with ALTMEMPHY IP.

Designs with Eight Chip Selects Fail Compilation

Designs that use eight chip selects with the high-performance controller architecture fail to compile.

Affected Configurations

This issue affects all designs that use eight chip selects with the high-performance controller architecture

Design Impact

Your design fails to compile.

Workaround

In the MegaWizard interface, select **High Performance Controller II** as your controller architecture.

Solution Status

This issue will be fixed in a future version of the DDR3 SDRAM Controller with ALTMEMPHY IP.

Address Mirroring Not Supported By Memory Simulation Model

The default memory simulation model does not support address mirroring. When you generate your design in the example testbench with the address mirroring parameter enabled, your simulation fails. To simulate successfully, you must replace the current memory simulation model with a vendor memory model and mirror the address bits in the <*variation name*>**_example_top_tb.v** or **.vhd** file.

Affected Configurations

This issue affects the multiple chip selects DDR3 DIMM which require mirrored address bits.

Design Impact

The default memory simulation model does not support DDR3 DIMM multiple chip selects mirrored address bits. Your design fails to simulate.

Workaround

Use the vendor memory model and mirror the address bits in the example top for target chip selects by doing the following:

1. Regenerate the DDR3 testbench. After generating, in the top variant file, *<variation name>***.v** or **.vhd**, look for the following code:

```
//Retrieval info: <PRIVATE name = “use_generated_memory_model” value=”true” type=”STRING” enable=”1”/>
```

   and change to:

```
//Retrieval info: <PRIVATE name = “use_generated_memory_model” value=”false” type=”STRING” enable=”1”/>
```

2. Download the vendor memory model.
3. For the chip selects that require address mirroring, edit the *<variation name>***_example_top_tb.v** or **.vhd** file by performing the following:
   a. Add the following lines:

```
wire[gMEM_ADDR_BITS - 1:0] a_reversed;
wire[gMEM_BANK_BITS - 1:0] ba_reversed;
assign a_reversed[2:0] = a_delayed[2:0];
assign a_reversed[3] = a_delayed[4];
assign a_reversed[4] = a_delayed[3];
assign a_reversed[5] = a_delayed[6];
assign a_reversed[6] = a_delayed[5];
assign a_reversed[7] = a_delayed[8];
assign a_reversed[8] = a_delayed[7];
assign a_reversed[gMEM_ADDR_BITS - 1:9] = a_delayed[gMEM_ADDR_BITS - 1:9];
assign ba_reversed[0] = ba_delayed[1];
assign ba_reversed[1] = ba_delayed[0];
assign ba_reversed[gMEM_BANK_BITS - 1:2] = ba_delayed[gMEM_BANK_BITS - 1:2];
```

   b. Locate the following lines:

```
.ba (ba_delayed),
.addr (a_delayed[14-1: 0]),
```

   and change to:

```
.ba (ba_reversed),
.addr (a_reversed),
```

Solution Status

This issue will be fixed in a future version of the DDR3 SDRAM Controller with ALTMEMPHY IP.

Memory Preset Parameters Do Not Get Updated

Some memory presets are changed in version 9.0 of the DDR3 SDRAM High-Performance Controller. If you migrate your existing design from version 8.1 to 9.0, your memory preset paramaters do not get updated in version 9.0.

Affected Configurations

This issue affects all designs that are migrated to version 9.0.

Design Impact

The memory preset paramaters in your design do not get updated in version 9.0, even if you regenerate the MegaCore function.

Workaround

In the MegaWizard GUI, choose any random memory presets, and then reselect your original presets (remember to redo any modifications to the preset such as DQ width, CAS latency, and so on). Click **Finish** to regenerate the MegaCore function.

Solution Status

This issue will be fixed in a future version of the DDR3 SDRAM Controller with ALTMEMPHY IP.

Designs with Error Correction Coding (ECC) Do Not Work After Subsequent Reset

Some designs with DDR3 SDRAM high-performance controllers do not work with the **Enable Error Detection and Correction Logic** option enabled.

Affected Configurations

This issue affects all designs that use DDR3 SDRAM high-performance controllers that have the **Enable Error Detection and Correction Logic** option turned on.

Design Impact

Your design does not work properly in both simulation and hardware after the subsequent reset.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the DDR3 SDRAM Controller with ALTMEMPHY IP.

Revision History

Table 12–1 shows the revision history for the FFT MegaCore function.

For more information about the new features, refer to the *FFT MegaCore Function User Guide*.

Table 12–1. FFT MegaCore Function Revision History

Version	Date	Description
10.1	December 2010	■ Preliminary support for Arria II GZ devices. ■ Final support for Stratix IV GT devices. ■ Efficiency enhancements.
10.0	July 2010	■ Preliminary support for Stratix V devices. ■ New Transform Length values.
9.1	November 2009	■ Preliminary support for HardCopy IV GX, Stratix IV, and Cyclone III LS devices. ■ Withdrawn support for HardCopy family of devices.

Errata

Table 12–2 shows the issues that affect the FFT MegaCore function v10.1, v10.0, and v9.1.

Not all issues affect all versions of the FFT MegaCore function.

Table 12–2. FFT MegaCore Function Errata

Added or Updated	Issue	Affected Version		
		10.1	10.0	9.1
15 Mar 11	Compilation Targeting a Stratix V Device Fails	✓	—	—
15 Dec 10	Variable Streaming Floating Point Variations Cannot SImulate Inverse FFT Computation	✓	—	—
	Variable Streaming Floating Point Variations Might Produce ±1 Errors in Simulation	✓	—	—
	Simulation Errors—MATLAB Model Mismatch	Fixed	✓	✓
15 July 10	Some Variations with VHDL Output Files Generate Incorrect Simulation Models for Stratix V Devices	✓	✓	—
	Example Design Fails Compilation	—	Fixed	✓
01 Dec 06	Simulation Errors—Incorrect Results	✓	✓	✓

Compilation Targeting a Stratix V Device Fails

Designs that include an FFT IP core and target a Stratix V device, do not compile even if you have a valid license for the IP core. Refer to Altera solution rd03082011_116 at www.altera.com/support/kdb/solutions/rd03082011_116.html.

Affected Configurations

FFT IP core designs that target a Stratix V device.

Design Impact

Designs that include this IP core and target a Stratix V device cannot compile.

Workaround

To fix this issue, if you have a valid license for this IP core, follow these steps:

1. Upgrade your Quartus II software installation to the 10.1 Service Pack 1 version.
2. Apply Patch 1.19 to your Quartus II software installation.
3. Regenerate your IP core and any others in your design that are affected by this issue.
4. Recompile your design.

Solution Status

This issue will be fixed in a future version of the Quartus II software.

Variable Streaming Floating Point Variations Cannot SImulate Inverse FFT Computation

FFT MegaCore function variations with variable streaming floating point architecture produce errors in simulation when the `inverse` input signal is set to value 1. Variations with this architecture cannot simulate the inverse FFT operation correctly.

Affected Configurations

All FFT MegaCore function variations with variable streaming floating point architecture.

Design Impact

This issue has no design impact. It affects simulation only.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the FFT MegaCore function.

Variable Streaming Floating Point Variations Might Produce ±1 Errors in Simulation

FFT MegaCore function variations with variable streaming floating point architecture might produce ±1 errors in simulation output values.

Affected Configurations

All FFT MegaCore function variations with variable streaming floating point architecture.

Design Impact

This issue has no design impact. It affects simulation only.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the FFT MegaCore function.

Simulation Errors—MATLAB Model Mismatch

For one particular FFT parameter combination, the HDL output does not match the MATLAB simulation results (for some frames of data).

HDL simulation results are scaled down by a factor of two compared to the MATLAB simulation results. The exponent value produced by the HDL simulation is one less than the output of the MATLAB simulations. When the exponent is taken into account, the MATLAB and the HDL version may differ by one LSB.

Affected Configurations

This issue affects the following parameter combination:

- Transform length: 64
- I/O data flow: burst architecture
- FFT engine architecture: quad output
- Number of parallel engines: 2

Design Impact

There is no design impact; the design compiles and operates correctly.

Workaround

This issue has no workaround.

Solution Status

This issue is fixed in version 10.1 of the FFT MegaCore function.

Some Variations with VHDL Output Files Generate Incorrect Simulation Models for Stratix V Devices

Some FFT MegaCore function variations that target a Stratix V device and are generated as VHDL output files, generate incorrect simulation models.

Affected Configurations

All FFT MegaCore function variations that use complex 18×25 multiplication and target a Stratix V device and for which VHDL is specified as the output file HDL. Variations that use complex 18×25 multiplication include variations with variable streaming fixed point architecture, large transform length, and twiddle precision less than 18 bits, and variations with a different FFT architecture, data precision of 18–25 bits, and twiddle precision less than 18 bits.

Design Impact

This issue has no design impact; it affects simulation only.

Workaround

Specify Verilog HDL as the output file language.

Solution Status

This issue will be fixed in a future version of the FFT MegaCore function.

Example Design Fails Compilation

The example top-level VHDL design with bit-reversal module (variable streaming FFT) cannot run compilation.

Affected Configurations

This issue affects variable streaming FFT designs.

Design Impact

This issue has no design impact.

Workaround

This issue has no workaround.

Solution Status

This issue is fixed in version 10.0 of the FFT MegaCore function.

Simulation Errors—Incorrect Results

When the input is defined as N bits wide, the permissible input range is from $-2^{N-1} + 1$ to $2^{N-1} - 1$. If the input contains the value -2^{N-1}, the HDL output is incorrect, and does not match the MATLAB simulation result.

Affected Configurations

This issue affects all configurations.

Design Impact

The design compiles but gives incorrect results.

Workaround

If you expect your input signal to contain the value -2^{N-1}, you should add a block in front of the FFT, which maps the value -2^{N-1} to $-2^{N-1}+1$.

Solution Status

This issue will be fixed in a future version of the FFT MegaCore function.

13. FIR Compiler

Revision History

Table 13–1 shows the revision history for the FIR Compiler.

For information about the new features, refer to the *FIR Compiler User Guide*.

Table 13–1. FIR Compiler Revision History

Version	Date	Description
10.1 SP1	February 2011	Maintenance release.
10.1	December 2010	■ Preliminary support for Arria II GZ devices. ■ Final support for Stratix IV GT devices.
10.0 SP1	September 2010	Maintenance release.
10.0	July 2010	Preliminary support for Stratix V devices.
9.1 SP2	March 2010	Maintenance release.
9.1 SP1	February 2010	Maintenance release.
9.1	November 2009	■ Preliminary support for HardCopy IV GX, Stratix IV, and Cyclone III LS devices. ■ Withdrawn support for HardCopy family of devices.

Errata

Table 13–2 shows the issues that affect the FIR Compiler v10.1 SP1, v10.1, v10.0 SP1, v10.0, v9.1 SP2, v9.1 SP1, and v9.1.

Not all issues affect all versions of the FIR Compiler.

Table 13–2. FIR Compiler Errata (Part 1 of 2)

Added or Updated	Issue	Affected Version						
		10.1 SP1	10.1	10.0 SP1	10.0	9.1 SP2	9.1 SP1	9.1
15 Mar 11	Compilation Targeting a Stratix V Device Fails	✓	✓	—	—	—	—	—
15 Feb 11	Compilation Targeting a HardCopy Device Requires Removal of .hex Files	✓	✓	✓	✓	✓	✓	✓
15 Dec 10	Half-Band Decimation Filters That Use MLABs for Coefficient Storage in Stratix V Devices Fail	—	—	Fixed	✓	—	—	—
	Symmetric Interpolation Filters That Use M20K Blocks for Data Storage in Stratix V Devices Fail	—	—	Fixed	✓	—	—	—
15 July 10	FIR Filters With Large Numbers of Coefficients and Non-Symmetric Structure Do Not Generate Netlist and IPFS Model Correctly	✓	✓	✓	✓	✓	✓	✓
	Simulation Fails for the Coefficient Reloadable Filters	—	—	—	Fixed	✓	✓	✓
15 May 10	FIR Compiler Functional Simulation Model Is Not Generated	✓	✓	✓	✓	✓	✓	✓

Table 13–2. FIR Compiler Errata (Part 2 of 2)

Added or Updated	Issue	Affected Version						
		10.1 SP1	10.1	10.0 SP1	10.0	9.1 SP2	9.1 SP1	9.1
1 Apr 10	FIR Compiler Does Not Support OpenCore Plus for Cyclone IV E Devices	—	—	—	—	Fixed	✓	—
15 Mar 09	Incorrect Results for Multi-Bit Serial or Interpolation with Signed Binary Fractional	✓	✓	✓	✓	✓	✓	✓
01 Oct 08	Block Memory Incorrectly Used When Logic Storage Selected	✓	✓	✓	✓	✓	✓	✓
01 Oct 07	Simulation Result Incorrect Using MCV Interpolation Filters	✓	✓	✓	✓	✓	✓	✓
01 May 07	Reloadable Coefficient Filters Fail for Some MCV Filters	✓	✓	✓	✓	✓	✓	✓
01 Dec 06	Quartus II Simulation Vector File Not Generated	✓	✓	✓	✓	✓	✓	✓

Compilation Targeting a Stratix V Device Fails

Designs that include a FIR Compiler and target a Stratix V device, do not compile even if you have a valid license for the IP core. Refer to Altera solution rd03082011_116 at www.altera.com/support/kdb/solutions/rd03082011_116.html.

Affected Configurations

FIR Compiler designs that target a Stratix V device.

Design Impact

Designs that include this IP core and target a Stratix V device cannot compile.

Workaround

To fix this issue, if you have a valid license for this IP core, follow these steps:

1. Upgrade your Quartus II software installation to the 10.1 Service Pack 1 version.
2. Apply Patch 1.19 to your Quartus II software installation.
3. Regenerate your IP core and any others in your design that are affected by this issue.
4. Recompile your design.

Solution Status

This issue will be fixed in a future version of the Quartus II software.

Compilation Targeting a HardCopy Device Requires Removal of .hex Files

In the *FIR Compiler User Guide*, Appendix A, FIR Compiler Supported Device Structures, the section "HardCopy II Support" should refer to all supported HardCopy devices instead of HardCopy II devices only. In particular, the instructions to remove the memory initialization **.hex** files from the Quartus II project directory before compiling apply to all device families in the HardCopy series of devices.

Affected Configurations

All designs that target a HardCopy device family and use memory initialization files.

Design Impact

If you apply the instructions in the Appendix only to HardCopy II devices, as stated, your HardCopy design does not compile successfully.

Workaround

To ensure your FIR compiler design that targets a HardCopy device family can compile successfully, remove the relevant **.hex** file from the Quartus II project directory before compiling.

Solution Status

This issue will be fixed in a future version of the *FIR Compiler User Guide*.

Half-Band Decimation Filters That Use MLABs for Coefficient Storage in Stratix V Devices Fail

Half-band decimation filters that target a Stratix V device and use MLABs for code storage cannot generate a netlist successfully.

Affected Configurations

Half-band decimation filters with multicycle variable structure and **Coefficient Storage** set to **MLAB** that target a Stratix V device.

Design Impact

The Quartus II software cannot generate a netlist.

Workaround

For half-band decimation filters with multicycle variable structure that target a Stratix V device, set **Coefficient Storage** to **Auto**.

Solution Status

This issue is fixed in version 10.0 SP1 of the FIR Compiler.

Symmetric Interpolation Filters That Use M20K Blocks for Data Storage in Stratix V Devices Fail

Symmetric interpolation filters that target a Stratix V device and use M20K memory blocks for data storage fail in simulation or compilation.

Affected Configurations

Symmetric interpolation filters with multicycle variable structure and **Data Storage** set to **M20K** that target a Stratix V device.

Design Impact

The Quartus II software cannot generate a netlist, or simulation fails due to a mismatch with expected results.

Workaround

For symmetric interpolation filters with multicycle variable structure that target a Stratix V device, set **Data Storage** to **Auto**.

Solution Status

This issue is fixed in version 10.0 SP1 of the FIR Compiler.

FIR Filters With Large Numbers of Coefficients and Non-Symmetric Structure Do Not Generate Netlist and IPFS Model Correctly

FIR filters with large numbers of coefficients and with **Force Non-Symmetric Structure** turned on, cannot generate a netlist successfully.

Affected Configurations

FIR filters with large numbers of coefficients and with **Force Non-Symmetric Structure** turned on.

Design Impact

The Quartus II software cannot generate a netlist or an IP functional simulation model.

Workaround

For FIR filters with **Force Non-Symmetric Structure** turned on, restrict the set of coefficients to 1500 or fewer.

Solution Status

This issue will be fixed in a future version of the FIR Compiler.

Simulation Fails for the Coefficient Reloadable Filters

The reloadable coefficient filters might not produce the right output if you use the IP functional simulation models for simulation.

Affected Configurations

This issue affects the reloadable coefficient filters.

Design Impact

The produced output does not match the expected output.

Workaround

None.

Solution Status

This issue is fixed in version 10.0 of the FIR Compiler.

FIR Compiler Functional Simulation Model Is Not Generated

When you try to generate a FIR Compiler functional simulation model, one of the following two error messages appears:

"Cannot run program "<*Quartus II IP installation*>\fir_compiler\lib\ip_toolbench\netlist_writer.exe" (in directory <*project directory*> create process error=14001 this application has failed to start because the application configuration is incorrect"

or

"IP Functional Simulation Model Creation Failed. The following error was returned: Error: Node instance "fircore" instantiates undefined entity "<*instance_name*>_st" File ..."

and the functional simulation model is not generated.

Affected Configurations

All FIR Compiler variations.

Design Impact

FIR Compiler simulation model is not generated.

Workaround

To avoid this problem, perform the following steps:

1. Download the appropriate version of Microsoft Visual C++ 2008 SP1 Redistributable Package — (×86) for a 32-bit machine or (×64) for 64-bit Windows XP.
2. Double-click on the **vcredisk_x86.exe** or **vcredisk_x64.exe** file you downloaded.
3. Follow the instructions.

If you are prompted to uninstall or repair, click **Repair**.

Solution Status

This issue will be fixed in a future version of the FIR Compiler.

FIR Compiler Does Not Support OpenCore Plus for Cyclone IV E Devices

When using the OpenCore Plus evaluation feature, the FIR Compiler does not generate a functional simulation model for Cyclone IV E devices.

Affected Configurations

All FIR Compiler variations that target a Cyclone IV E device.

Design Impact

This issue has no design impact.

Workaround

To avoid this issue, purchase a license for the FIR Compiler.

Solution Status

This issue is fixed in version 9.1 SP2 of the FIR Compiler.

Incorrect Results for Multi-Bit Serial or Interpolation with Signed Binary Fractional

Incorrect results when **Structure** is set to **Distributed Arithmetic: Multi-Bit Serial Filter** or the **Rate Specification** is set to **Interpolation**, and **Signed Binary Fractional** is specified for the data type.

Affected Configurations

Configurations that have a signed binary fractional data type with either a multi-bit structure or an interpolation filter rate specification.

Design Impact

The output data is incorrect.

Workaround

Avoid using a multi-bit serial structure or an interpolation filter rate specification with signed binary fractional data types.

Solution Status

This issue will be fixed in a future version of the FIR Compiler.

Block Memory Incorrectly Used When Logic Storage Selected

For some instances of the FIR Compiler MegaCore function, if you select logic-based storage for data and coefficients, it is possible that the results of synthesis may include some block memory.

Affected Configurations

Configurations with FIR storage set to logic elements.

Design Impact

An unwanted block memory is used.

Workaround

Turn off **Auto Shift Register Replacement** in the Quartus II **More Analysis and Synthesis Settings** dialog box. This dialog box can be accessed by clicking **More Settings** in the **Analysis & Synthesis Settings** page of the **Settings** dialog box accessed from the Assignments menu in the Quartus II software.

Solution Status

This issue will be fixed in a future version of the FIR Compiler.

Simulation Result Incorrect Using MCV Interpolation Filters

Some multicycle variable interpolation filters with high interpolation factors may generate incorrect output.

Affected Configurations

This issue affects MCV interpolation filters with high interpolation factors and forced non-symmetric implementation where the pipelining level is set to greater than 1 for higher f_{MAX}.

Design Impact

The produced output does not match the expected output.

Workaround

Change the pipelining level to 1. This change may result in lower f_{MAX} but the filter output will match the expected output.

Solution Status

This issue will be fixed in a future version of the FIR Compiler.

Reloadable Coefficient Filters Fail for Some MCV Filters

Some reloadable coefficient filters with multicycle variable architecture do not produce the right output when a new set of coefficients is reloaded.

Affected Configurations

This error is observed in some of the reloadable coefficient MCV filters.

Design Impact

The produced output does not match the expected output when the new coefficient set is reloaded.

Workaround

There are two separate problems which may cause this failure. If your target device is **Cyclone III**, change the device to **Stratix II** or **Stratix III** in the FIR Compiler GUI and regenerate the filter. (Your device selection in the Quartus II project should stay the same). If the coefficient storage is set to logic cells, change to a block memory (such as **M512**, **M9K**, or **Auto**).

Solution Status

This issue will be fixed in a future version of the FIR Compiler.

Quartus II Simulation Vector File Not Generated

FIR Compiler does not create a vector file for Quartus II simulation.

Affected Configurations

This issue affects all configurations.

Design Impact

The design can be compiled, but there is no automatically generated vector file testbench available to simulate the design in the Quartus II software.

Workaround

Use NativeLink to simulate the VHDL testbench instead.

Solution Status

This issue will be fixed in a future version of the FIR Compiler.

14. FIR Compiler II

Revision History

Table 14–1 shows the revision history for the FIR Compiler II.

For information about the new features, refer to the *FIR Compiler II User Guide*.

Table 14–1. FIR Compiler II Revision History

Version	Date	Description
10.1	December 2010	Added new output options and multiple coefficient banks feature.
10.0	July 2010	Added backpressure and coefficient reloading features.
9.1 SP1	January 2010	First release.

Errata

Table 14–2 shows the issues that affect the FIR Compiler II v10.1, v10.0, and v9.1 SP1.

Not all issues affect all versions of the FIR Compiler II.

Table 14–2. FIR Compiler II Errata

Added or Updated	Issue	Affected Version		
		10.1	10.0	9.1 SP1
15 December 2010	Unable to Run FIR Compiler II	✓	✓	✓
15 July 2010	NativeLink is Not Supported	Fixed	✓	✓
15 Feb 2010	Simulation Fails with Single-Language Simulator	—	✓	✓
	M144K Memories Output X's in the ModelSim-Altera Software	—	✓	✓
	Incorrect Testbench Result When Interpolation Factor Is Greater Than The TDM Factor	—	Fixed	✓
	Incorrect Results for a Decimation Configuration	—	Fixed	✓
	Incorrect Results Might Be Produced When Input Bit Width is Greater Than 17 bits.	—	Fixed	✓
	Simulation fails with the NCSim/Riviera-Pro/ActiveHDL Simulator	—	Fixed	✓
	Compiler Does Not Create a Block Symbol File	Fixed	✓	✓

Unable to Run FIR Compiler II

The FIR Compiler II MegaCore fails to run with the following error message:

```
Error: couldn't execute"<Quartus installation
path>\quartus\common\ip\altera\windows32\fir_ip_api_interface": no such
file or directory.
```

Affected Configurations

This issue affects all FIR Compiler II variations.

Design Impact

The FIR Compiler II Core cannot be generated.

Workaround

To avoid this problem, follow these steps:

1. Download the appropriate version of Microsoft Visual C++ 2008 SP1 Redistributable Package — (×86) for a 32-bit machine or (×64) for 64-bit Windows XP.
2. Double-click on the **vcredisk_x86.exe** or **vcredisk_x64.exe** file you downloaded.
3. Follow the instructions.

If you are prompted to uninstall or repair, click **Repair**.

Solution Status

This issue will be fixed in a future version of the FIR Compiler II MegaCore function.

NativeLink is Not Supported

Unable to perform simulation using NativeLink.

Affected Configurations

This issue affects all simulators supported by NativeLink.

Design Impact

The design does not simulate.

Workaround

Use Modelsim SE or Modelsim AE to run simulation.

Solution Status

This issue is fixed in the FIR Compiler II MegaCore function v10.1.

Simulation Fails with Single-Language Simulator

When the ModelSim® AE or any single-language simulator is used, the simulation fails because FIR Compiler II is written in both Verilog and VHDL.

Affected Configurations

This issue affects all configurations.

Design Impact

The design does not simulate.

Workaround

Use the `quartus_map` API at the command line to create a simulation model by typing the following command:

```
    quartus_map <variant file name> --simgen --
simgen_parameter="CBX_HDL_LANGUAGE=<language>"
    language : VHDL / VERILOG
```

Solution Status

This issue will be fixed in a future version of the FIR Compiler II MegaCore function.

M144K Memories Output X's in the ModelSim-Altera Software

The simulation fails if the M-RAM memory threshold is set inappropriately.

Affected Configurations

This issue affects all configurations if the M-RAM threshold is set to a small value.

Design Impact

The simulation fails due to the output X's produced by the M144K memories.

Workaround

Set the M-RAM threshold to the default value (for example, set the value to 1000000)

Solution Status

This issue will be fixed in a future version of the FIR Compiler II MegaCore function.

Incorrect Testbench Result When Interpolation Factor Is Greater Than The TDM Factor

The testbench produces incorrect results when the filter is configured with interpolation factor greater than the TDM factor (the ratio of the clock rate to the sample rate).

Affected Configurations

This issue affects configurations with interpolation factor greater than the TDM factor.

Design Impact

There is no design impact. This is a testbench issue.

Workaround

Set the interpolation factor equals or lesser than the TDM factor.

Solution Status

This issue is fixed in the FIR Compiler II MegaCore function v10.0.

Incorrect Results for a Decimation Configuration

Incorrect results are produced when the filter is configured as decimation type with certain parameters.

Affected Configurations

This issue affects the following parameter combination:

- Decimation Factor: 2
- Coefficient Bit Width: 8
- Symmetry Mode: Non Symmetry

Design Impact

The output data is incorrect.

Workaround

Use different coefficient bit width or symmetry mode when you use decimation by two configuration.

Solution Status

This issue is fixed in the FIR Compiler II MegaCore function v10.0.

Incorrect Results Might Be Produced When Input Bit Width is Greater Than 17 bits.

Incorrect results might be produced when you set the input bit width other than 1–17 bits.

Affected Configurations

Configurations with input bit width greater than 17 bits.

Design Impact

The output data is incorrect.

Workaround

Set the input bit width within 1–17 bits.

Solution Status

This issue is fixed in the FIR Compiler II MegaCore function v10.0.

Simulation fails with the NCSim/Riviera-Pro/ActiveHDL Simulator

When you run design simulations with NCSim/Riviera-Pro/ActiveHDL, the simulations might fail with the following error message on the respective softwares.

```
Verilog module/VHDL port width mismatch -
ALTERA_AVALON_SC_FIFO.OUT_EMPTY. (NCSIM). Length of connection (0)
does not match the length of port "out_empty" (2) on instance.
(Riviera-Pro)
```

```
Fatal Error: ELAB2_0051 auk_dspip_avalon_streaming_sink_hpfir.vhd
(525): Length of connection (0) does not match the length of port
"out_empty" (2) on instance (Active-HDL)
```

Affected Configurations

This issue affects configurations with `PHYSCHANIN = 1`.

Design Impact

The design does not simulate.

Workaround

Remove the following lines from **auk_dspip_avalon_streaming_sink_hpfir.vhd**:

```
      signal out_empty : OUT STD_LOGIC_VECTOR
(log2_ceil(DATA_PORT_COUNT)-1 DOWNTO 0);
```

```
      out_empty => open,
```

Solution Status

This issue is fixed in the FIR Compiler II MegaCore function v10.0.

Compiler Does Not Create a Block Symbol File

The FIR Compiler II does not automatically create a Block Symbol File (**.bsf**) for the MegaCore function.

Affected Configurations

This issue affects all FIR Compiler II MegaCore function variations.

Design Impact

There is no design impact.

Workaround

In the Quartus II software, open *<variation_name>.<v|vhd>*. From the File menu, select **Create/Update** and then click **Create Symbol Files for Current File** to generate the **.bsf** file. Alternatively, use the `quartus_map` API at the command line to create the symbol file, by typing the following command:

```
quartus_map --generate_symbol=<variation_name>.<v|vhd>
```

Solution Status

This issue is fixed in the FIR Compiler II MegaCore function v10.1.

15. Interlaken

Revision History

Table 15–1 shows the revision history for the Interlaken MegaCore function.

For information about the new features, refer to the *Interlaken MegaCore Function User Guide*.

Table 15–1. Interlaken MegaCore Function Revision History

Version	Date	Description
10.1	December 2010	Initial release.

Errata

Table 15–2 shows the issues that affect the Interlaken MegaCore function v10.1.

Not all issues affect all versions of the Interlaken MegaCore function.

For Qsys errata, which might affect the Interlaken MegaCore function and other IP cores, refer to the *Quartus II Software Release Notes*.

Table 15–2. Interlaken MegaCore Function Errata

Added or Updated	Issue	Affected Version
		10.1
15 Jan 11	rxt_rxd Warning for 10- and 20-lane Variations With Transceivers	✓
15 Dec 10	Compiler Warnings When Transceivers are Excluded	✓
	Critical Warnings for 12- and 20-lane Variations Without Transceivers	✓
	C106 Warnings for 10- and 20-lane Variations With Transceivers	✓
	Aldec Riviera-PRO Simulator Cannot Simulate Interlaken 8-lane Variation	✓
	10.3125-Gbps Variation with Transceivers Runs at Incorrect Lane Rate	✓

rxt_rxd Warning for 10- and 20-lane Variations With Transceivers

When you compile an Interlaken MegaCore function 10- or 20-lane variation with transceivers, the following warning message appears:

```
Warning: Verilog HDL or VHDL warning at alt_ntrlkn_hsio_bank_pmad5.v(92):
object “rst_rxd” assigned a value but never read
```

Affected Configurations

All 10- and 20-lane Interlaken variations with transceivers.

Design Impact

This issue has no design impact. You can ignore this warning message.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the Interlaken MegaCore function.

Compiler Warnings When Transceivers are Excluded

When you compile an Interlaken MegaCore function variations that excludes transceivers, the following warning message appears:

```
Warning: Output pins are stuck at VCC or GND
    Warning (13410): Pin "common_rx_c_clk" is stuck at GND
```

Affected Configurations

All Interlaken MegaCore function variations that exclude transceivers.

Design Impact

This issue has no design impact. You can ignore this warning message.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the Interlaken MegaCore function.

Critical Warnings for 12- and 20-lane Variations Without Transceivers

When you compile an Interlaken MegaCore function 12- or 20-lane variation that excludes transceivers, the following warning message appears:

```
Critical Warning: (High) Rule C105: Clock signal should be a global signal.
       Found <num> node(s) related to this rule.
```

The warning message includes a list of `rx_lane_clk<`*n*`>_export[<`*l*`>]` signals, and if the out-of-band flow control block is included, some clock signals from that block.

Affected Configurations

All Interlaken MegaCore function 12- and 20-lane variations that exclude transceivers.

Design Impact

This issue has no design impact. You can ignore this warning message.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the Interlaken MegaCore function.

C106 Warnings for 10- and 20-lane Variations With Transceivers

When you compile an Interlaken MegaCore function 10- or 20-lane variation with transceivers, the following warning message appears:

```
Warning: (Medium) Rule C106:Clock signal source should not drive registers
triggered by different clock edges.
```

Affected Configurations

All 10- and 20-lane Interlaken variations with transceivers.

Design Impact

This issue has no design impact. You can ignore this warning message.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the Interlaken MegaCore function.

Aldec Riviera-PRO Simulator Cannot Simulate Interlaken 8-lane Variation

The Aldec, Inc. Riviera-PRO simulator cannot simulate an Interlaken MegaCore function eight-lane variation correctly.

Affected Configurations

All eight-lane Interlaken MegaCore function variations.

Design Impact

This issue has no design impact. The problem affects simulation only.

Workaround

Use a different simulator to simulate your design, if it includes an eight-lane Interlaken MegaCore function variation.

Solution Status

This issue will be fixed in a future version of the Interlaken MegaCore function.

10.3125-Gbps Variation with Transceivers Runs at Incorrect Lane Rate

The 10.3125-Gbps Interlaken MegaCore function variations require a different `ref_clk` frequency than they were originally designed for. If you use the MegaCore function as generated, the lane rate is 10.2 Gbps rather than 10.3125 Gbps. Therefore, in addition to running the `ref_clk` input clock at 322.265625 MHz as specified in the *Interlaken MegaCore Function User Guide*, you must also make some manual modifications to several of the RTL files.

Affected Configurations

All 10.3125-Gbps Interlaken MegaCore function variations with transceivers.

Design Impact

The 12-lane, 10-Gbps variation runs at 10.2 Gbps instead of the documented 10.3125 Gbps, in simulation and when programmed on the device.

Workaround

After you generate your Interlaken variation and before you simulate your design, follow these steps to modify your RTL files to fix the underlying problem:

1. Edit the file **alt_ntrlkn_gxb_10g.v** with the correct values to match the 322.265625-MHz `ref_clk` frequency by following these steps:
   a. To set the correct effective data rate, replace every instance of `10200` with `10312.5`.
   b. To set the correct input period, replace every instance of `3137` with `3103`.
   c. To set the correct input clock frequency, replace every instance of `318.75` with `322.265625`.
2. Edit the **submodules/**<*variation*>**.sdc** file with the correct clock frequencies by following these steps:
   a. Set the `tx_mac_c_clk` frequency to 257.81 MHz.
   b. Set the `rx_mac_c_clk` frequency to 257.81 MHz.
3. If you are using the Qsys design example provided with the Interlaken IP installation, follow these additional steps:
   a. In the **alt_interlaken_12lane_10g.sdc** file in the project directory, set the following clock frequencies:
      - Sample Channel Client clock frequencies to 257.81 MHz
      - `tx_mac_c_clk` frequency to 257.81 MHz
      - `rx_mac_c_clk` frequency to 257.81 MHz
      - `ref_clk` frequency to 322.265625 MHz
   b. In the **testbench/alt_interlaken_12lane_10g_tb.sv** file, update the `ref_clk` frequency by replacing `#1568` with `#1551.5`.

Solution Status

This issue will be fixed in a future version of the Interlaken MegaCore function.

16. Interlaken PHY

Revision History

Table 16–1 shows the revision history for the Interlaken PHY IP core.

For more information about the new features, refer to the "*Interlaken PHY IP Core*" chapter in the *Altera Transceiver PHY IP Core User Guide*.

Table 16–1. Interlaken PHY Revision History

Version	Date	Description
10.1	December 2010	Added simulation support in ModelSim SE, Synopsys VCS MX, Cadence NCSim Changed number of lanes supported from 4–24 to 1–24.
10.0 SP1	September 2010	Added simulation support.
10.0	July 2010	First release.

Errata

Table 16–2 shows the issues that affect the Interlaken PHY IP core in versions 10.1, 10.0 SP1, and 10.0.

Table 16–2. Interlaken PHY Errata

Added or Updated	Issue	Affected Version
		10.1
15 Dec 10	Mixed Language Simulation Fails when Optimization Is On	✓

Mixed Language Simulation Fails when Optimization Is On

Simulation fails when using ModelSim with mixed-languages.

Affected Configurations

This issue affects mixed language simulation including Verilog modules and VHDL entities when optimization is on.

Workaround

The workaround is to turn ModelSim optimization off by using the `-novpt` option to the `vsim` command.

Solution Status

This issue may be fixed in a future version of ModelSim.

Revision History

Table 17–1 shows the revision history for the NCO MegaCore function.

For information about the new features, refer to the *NCO MegaCore Function User Guide*.

Table 17–1. NCO MegaCore Function Revision History

Version	Date	Description
10.1	December 2010	■ Preliminary support for Arria II GZ devices. ■ Final support for Stratix IV GT devices.
10.0	July 2010	Preliminary support for Stratix V devices.
9.1	November 2009	■ Preliminary support for HardCopy IV GX, Stratix IV, and Cyclone III LS devices ■ Added frequency hopping feature. ■ Removed frequency hopping design example. ■ Withdrawn support for HardCopy family of devices.

Errata

Table 17–2 shows the issues that affect the NCO MegaCore function v10.1, v10.0, and v9.1.

Not all issues affect all versions of the NCO MegaCore function.

Table 17–2. NCO MegaCore Function Errata

Added or Updated	Issue	Affected Version		
		10.1	10.0	9.1
15 Mar 11	Compilation Targeting a Stratix V Device Fails	✓	—	—
15 Jul 10	Mismatches Between Multiplier-Based MATLAB and RTL Models With Throughput One Half	—	Fixed	✓
	Mismatches Between Some Serial CORDIC MATLAB and RTL Models	✓	✓	✓
	Mismatches Between Some Small ROM MATLAB and RTL Models	✓	✓	✓
15 Mar 09	Warning Message Displayed Twice	✓	✓	✓
01 Oct 07	Mismatches Between Multiplier-Based MATLAB and RTL Models With Throughput One	✓	✓	✓

Compilation Targeting a Stratix V Device Fails

Designs that include an NCO IP core and target a Stratix V device, do not compile even if you have a valid license for the IP core. Refer to Altera solution rd03082011_116 at www.altera.com/support/kdb/solutions/rd03082011_116.html.

Affected Configurations

NCO IP core designs that target a Stratix V device.

Design Impact

Designs that include this IP core and target a Stratix V device cannot compile.

Workaround

To fix this issue, if you have a valid license for this IP core, follow these steps:

1. Upgrade your Quartus II software installation to the 10.1 Service Pack 1 version.
2. Apply Patch 1.19 to your Quartus II software installation.
3. Regenerate your IP core and any others in your design that are affected by this issue.
4. Recompile your design.

Solution Status

This issue will be fixed in a future version of the Quartus II software.

Mismatches Between Multiplier-Based MATLAB and RTL Models With Throughput One Half

For the multiplier-based architecture with throughput = ½ (output every 2nd clock cycle), there can be mismatches between the outputs of the MATLAB model and the RTL for certain parameter combinations. These mismatches occur because some initial output values are not covered by either the MATLAB model or the RTL design, while the other values match.

Affected Configurations

Multiplier-based architecture of the NCO MegaCore function with halved throughput.

Design Impact

Automatic comparison of the output values from the MATLAB model and RTL design during testing may show mismatches.

Workaround

The RTL design works correctly, but comparison between MATLAB model and RTL cannot be done automatically.

Solution Status

This issue is fixed in version 10.0 of the NCO MegaCore function.

Mismatches Between Some Serial CORDIC MATLAB and RTL Models

For the serial CORDIC architecture with **Phase Accumulator Precision** and **Angular Resolution** both set to values less than or equal to 10, there can be mismatches between the outputs of the MATLAB model and the RTL. These mismatches are due to rounding differences.

Affected Configurations

Serial CORDIC architecture of the NCO MegaCore function with **Phase Accumulator Precision** and **Angular Resolution** both set to values less than or equal to 10.

Design Impact

Comparison of the output values from the MATLAB model and RTL design during testing may show mismatches. However, the error margin is only ±1.

Workaround

Set **Phase Accumulator Precision** and **Angular Resolution** to values greater than 10, or use a different architecture.

Solution Status

This issue will be fixed in a future version of the NCO MegaCore function.

Mismatches Between Some Small ROM MATLAB and RTL Models

For the Small ROM architecture with a small **Angular Resolution** value and a large **Magnitude Precision** value, there can be mismatches between the outputs of the MATLAB model and the RTL. These mismatches are due to rounding differences.

Affected Configurations

Small ROM architecture of the NCO MegaCore function with a small **Angular Resolution** value and a large **Magnitude Precision** value.

Design Impact

Comparison of the output values from the MATLAB model and RTL design during testing may show mismatches. However, the error margin is only ±1.

Workaround

To avoid this issue, modify your NCO MegaCore function in one of the following ways:

- Set **Angular Resolution** to a large value.
- Set **Magnitude Precision** to a small value.
- Use a different architecture.

Solution Status

This issue will be fixed in a future version of the NCO MegaCore function.

Warning Message Displayed Twice

If you change the **Clock Rate** units to **mHz** in the **Parameter Setting** dialog box a warning message is displayed. After closing the warning message, if you then click on both the **Clock Rate** and the **Desired Output Frequency** boxes, two separate warning messages with the same content are displayed.

Affected Configurations

All configurations.

Design Impact

None.

Workaround

Close both of the warning messages.

Solution Status

This issue will be fixed in a future version of the NCO MegaCore function.

Mismatches Between Multiplier-Based MATLAB and RTL Models With Throughput One

For the multiplier-based architecture with throughput = 1 (output every clock cycle), there can be mismatches between the outputs of the MATLAB model and the RTL design for values of magnitude precision. These mismatches seem to be rounding errors for very large values.

Affected Configurations

Multiplier-based architecture of the NCO MegaCore function with throughput = 1.

Design Impact

Comparison of the output values from the MATLAB model and RTL design during testing may show mismatches. However, the error margin is small in both absolute and relative terms. For example, the MATLAB model calculates -536,870,910, whereas the RTL calculates -536,870,911.

Workaround

The RTL design works correctly, but comparison between the MATLAB model and the RTL cannot be done automatically.

Solution Status

This issue will be fixed in a future version of the NCO MegaCore function.

18. Nios II Processor

Revision History

Table 18–1 shows the revision history for the Nios® II Processor MegaCore function.

For more information about the new features, refer to the *Nios II Processor Reference Handbook*. For information about new features and errata in the Nios II Embedded Design Suite, refer to the *Nios II Embedded Design Suite Release Notes and Errata*.

Table 18–1. Nios II Processor Revision History

Version	Date	Description
10.1	December 2010	Maintenance release
10.0	July 2010	Maintenance release
9.1 SP2	March 2010	Maintenance release
9.1 SP1	January 2010	Maintenance release
9.1	November 2009	■ External Interrupt Controller (EIC) Support ■ The EIC interface—Enables the processor to connect to an EIC ■ Support for multiple register sets (shadow register sets) ■ New fields in status registers: `IL` (Current Interrupt Level), `CRS` (Current register set index), `PRS` (Previous register set index), and `NMI` (nonmaskable interrupt active) ■ Shadow status register (`sstatus`) added ■ New instructions, `rdprs` and `wrprs`, support moving a register value between register sets ■ Status register field names simplified—All status registers use the following field names where implemented: `RSIE`, `NMI`, `PRS`, `CRS`, `IL`, `IH`, `EH`, `U`, and `PIE`. Register-specific field names, such as `EPIE`, are discontinued. This is a documentation change, and has no impact on the Nios II hardware or software.

Errata

Table 18–2 shows the issues that affect the Nios II Processor versions 9.1 through 10.1.

Not all issues affect all versions of the Nios II Processor.

Table 18–2. Nios II Processor Errata

Added or Updated	Issue	Affected Version					
		10.1 SP1	10.1	10.0	9.1 SP2	9.1 SP1	9.1
15 Jan 11	Cannot Remove EIC Interface from Nios II Processor	✓	✓	✓	—	—	—
	Error: Debug Slave <slave interface name> Not Connected to data_master	Fixed	✓	—	—	—	—

Table 18–2. Nios II Processor Errata

Added or Updated	Issue	Affected Version					
		10.1 SP1	10.1	10.0	9.1 SP2	9.1 SP1	9.1
15 Dec 10	The cpu_resetrequest and cpu_resettaken Signals Do Not Export	✓	✓	—	—	—	—
	Custom Instruction Import Fails and Freezes GUI	—	Fixed	✓	—	—	—
	HardCopy III and HardCopy IV Support Incorrectly Stated	—	—	Fixed	✓	✓	✓
15 Jul 10	Error Running Nios II Project: 'Downloading ELF Process failed'	✓	✓	✓	✓	✓	✓
15 May 10	Cannot Implement Multiplier as DSP Block in Cyclone IV Devices	—	—	—	Fixed	✓	✓
15 Nov 09	Design Assistant Error on Clock Signal Source in HardCopy Designs	✓	✓	✓	✓	✓	✓
	Nios II Ports Created Incorrectly	✓	✓	✓	✓	✓	✓
15 Oct 07	Errors Adding Custom Instruction to the Nios II Processor	✓	✓	✓	✓	✓	✓

Cannot Remove EIC Interface from Nios II Processor

In SOPC Builder, if you configure a Nios II/f processor core with the external interrupt controller (EIC) interface, then change the core to a Nios II/s or Nios II/e, the EIC interface remains. The Nios II/s and Nios II/e cores do not support the EIC. As a result, the following error message appears:

```
Error: cpu_0.interrupt_controller_in: "cpu_0.interrupt_controller_in"
must be connected to an Avalon-ST source
```

On the **Advanced Features** tab, the **Interrupt Controller** parameter is disabled and you cannot change from the EIC to the internal interrupt controller.

Affected Configurations

Nios II/s and Nios II/e processor cores

Workaround

To correct this condition, perform the following steps:

1. Change the processor core back to Nios II/f.
2. In the **Advanced Features** tab, select **Internal** to remove the EIC interface and revert to the internal interrupt controller.
3. Change the processor back to the desired core, Nios II/s or Nios II/e.

Solution Status

This issue will be fixed in a future release of the Nios II processor core.

Error: Debug Slave <*slave interface name*> Not Connected to data_master

In Qsys, for designs that have Nios II processors with tightly-coupled instruction masters and nontightly-coupled data masters, you might receive the following message:

```
Debug slave <slave_interface_name> not connected to data_master.
```

Affected Configurations

This issue affects all designs that use Nios II processor in Qsys, which has tightly-coupled instruction masters and nontightly-coupled data masters.

Design Impact

There is no design impact.

Workaround

Use SOPC Builder rather than Qsys.

Alternatively, upgrade to v10.1 SP1 or later.

Solution Status

Fixed in v10.1 SP1

The cpu_resetrequest and cpu_resettaken Signals Do Not Export

If you wish to include the `cpu_resetrequest` and `cpu_resettaken` signals for the Nios II processor, these signals do not appear on the top-level Qsys system.

Affected Configurations

This issue affects all configurations.

Design Impact

There is no design impact

Workaround

Use SOPC Builder rather than Qsys.

Solution Status

This issue will be fixed in a future release of the Nios II processor core.

Custom Instruction Import Fails and Freezes GUI

If you click the **Import** button on the **Custom Instructions** tab in the Nios II MegaWizard interface, the GUI freezes.

Workaround

There is currently no workaround for this problem.

Solution Status

This issue is fixed in the Nios II processor version 10.1.

HardCopy III and HardCopy IV Support Incorrectly Stated

In "Device Family Support" in the *Nios II Core Implementation Details* chapter of the *Nios II Processor Reference Handbook*, the "Device Family Support" table incorrectly lists full support for the HardCopy® IV GX and HardCopy III/IV E device families. The Nios II processor provides preliminary support for these device families.

Solution Status

This issue is fixed in the *Nios II Processor Reference Handbook* version 10.0.

Error Running Nios II Project: 'Downloading ELF Process failed'

If the Nios II processor's cpu.data_master port is not connected to all program memories (memories to which the .**elf** file is downloaded) the software project fails to run on Nios II hardware.

Failure to connect cpu.data_master to all program memories is a design error that the SBT does not detect.

Affected Configurations

Any Nios II system whose data masters are not correctly set up as described in the previous section

Design Impact

You cannot download software to the program memories.

Workaround

Connect cpu.data_master to all program memories.

Solution Status

This issue will be fixed in a future release of the Nios II EDS.

Cannot Implement Multiplier as DSP Block in Cyclone IV Devices

In the Nios II MegaWizard interface in SOPC Builder, if **Hardware Multiply** is set to **DSP Block**, and the SOPC Builder system is the top-level entity in the Quartus II design, Quartus II compilation fails with an error similar to the following:

```
The design contains 4 blocks of type "Embedded multiplier block" but the
selected device EP4Cxx does not support such blocks
```

DSP Block is an invalid option for **Hardware Multiply** on the Cyclone IV device family.

Affected Configurations

Nios II systems targeting the Cyclone IV device family

Design Impact

On Cyclone IV devices, you must use embedded multipliers to implement hardware multiply.

Workaround

Use embedded multipliers to implement hardware multiply in Cyclone IV designs.

Alternatively, upgrade to v. 9.1 SP2 or later.

Solution Status

Fixed in v. 9.1 SP2

Design Assistant Error on Clock Signal Source in HardCopy Designs

When you run the Quartus® II Design Assistant on a HardCopy III or HardCopy IV design, the following error message might appear:

```
Rule C106: Clock signal source should not drive registers that are \
    triggered by different clock edges ; clk ;
```

This error occurs if your HardCopy III or HardCopy IV design incorporates a Nios II/s processor core with a logic element (LE)-based multiplier. Only Stratix® designs can be converted for HardCopy III or HardCopy IV devices. In a Stratix design, it is preferable to implement the multiplier in a DSP block, which provides better performance than an LE-based multiplier.

Affected Configurations

HardCopy III and HardCopy IV designs incorporating the Nios II/s processor core with an LE-based multiplier.

Design Impact

You cannot compile a HardCopy III or HardCopy IV design incorporating the Nios II/s processor core with an LE-based multiplier.

Workaround

Implement the Nios II multiplier with DSP blocks when targeting a HardCopy III or HardCopy IV device.

Solution Status

This issue will be fixed in a future release of the Nios II processor core.

Nios II Ports Created Incorrectly

A threading issue between SOPC Builder and the Nios II MegaWizard™ interface occasionally causes HDL file analysis to fail. This creates all ports as std_logic input with width 1.

Affected Configurations

Nios II processor systems with custom instructions.

Design Impact

Design fails to run in ModelSim®.

Workaround

After adding your custom instruction, close and relaunch SOPC Builder.

Solution Status

Not fixed

Errors Adding Custom Instruction to the Nios II Processor

You might get spurious errors after adding custom instruction slave ports through the Nios II MegaWizard interface.

Affected Configurations

Any Nios II system featuring custom instructions.

Design Impact

No design impact. The error messages are benign.

Workaround

Save your system in SOPC Builder. Close and then relaunch SOPC Builder.

19. PCI Compiler

Revision History

Table 19–1 shows the revision history for the PCI Compiler.

For more information about the new features, refer to the *PCI Compiler User Guide*.

Table 19–1. PCI Compiler Revision History

Version	Date	Description
10.1 SP1	February 2011	Maintenance release.
10.1	December 2010	■ Preliminary support for Arria II GZ devices. ■ Final support for Arria II GX and Stratix IV GT devices.
10.0	July 2010	Maintenance release.
9.1 SP2	April 2010	Maintenance release.
9.1 SP1	February 2010	Maintenance release.
9.1	November 2009	Preliminary support for Cyclone III LS and Cyclone IV devices.
9.0 SP2	July 2009	Maintenance release.
9.0 SP1	May 2009	Preliminary support for HardCopy III and HardCopy IV E devices.
9.0	March 2009	Preliminary support for Arria II GX devices.
8.1	November 2008	Maintenance release.

Errata

Table 19–2 shows the issues that affect the PCI Compiler v10.1, 10.0, and 9.1.

Not all issues affect all versions of the PCI Compiler.

Table 19–2. PCI Compiler MegaCore Function Errata

Added or Updated	Issue	Affected Version		
		10.1	10.0	9.1
01 Apr 10	Configuration Write to Invalid Address Repeats Continuosly	✓	✓	✓
15 Nov 09	Designs With Cyclone III LS Devices Fail to Meet Timing	✓	✓	✓
15 May 09	F1152 Packages for HardCopy III and HardCopy IV-E Not Supported	✓	✓	✓
	Wirebond Packages for HardCopy III and HardCopy IV-E Not Supported	✓	✓	✓
01 Nov 08	Designs With Stratix IV Devices Fail to Meet Timing	✓	✓	✓

Configuration Write to Invalid Address Repeats Continuosly

A configuration write to an invalid configuration space address causes PCI Compiler to attempt continuous writes, and prevents further PCI reads or writes.

Affected Configuration

All PCI Compiler configurations.

Design Impact

The PCI Compiler continuously repeats the configuration write and does not proceed to the next operation.

Workaround

Make sure that you do not write to an invalid configuration space address.

Solution Status

This issue will not be fixed.

Designs With Cyclone III LS Devices Fail to Meet Timing

Timing fails when using Cyclone III LS devices with any core combination at 66 MHz.

Affected Configuration

All PCI Compiler designs targeting the Cyclone III LS device family with C8 speed grade, and all PCI Compiler designs targeting the EP3CLS150 or EP3CLS200 devices with C7 speed grade.

Design Impact

The PCI Compiler designs with some Cyclone III LS devices may not meet timing requirements.

Workaround

None.

Solution Status

This issue will not be fixed.

F1152 Packages for HardCopy III and HardCopy IV-E Not Supported

PCI Compiler does not support F1152 packages for HardCopy III and HardCopy IV-E.

Affected Configuration

All PCI Compiler configurations using the F1152 packages for HardCopy III and HardCopy IV-E.

Design Impact

The PCI Compiler designs with F1152 packages for HardCopy III and HardCopy IV-E fail to compile.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the PCI Compiler.

Wirebond Packages for HardCopy III and HardCopy IV-E Not Supported

PCI Compiler does not support wirebond packages for HardCopy III and HardCopy IV-E.

Affected Configuration

All PCI Compiler configurations using the wirebond packages for HardCopy III and HardCopy IV-E.

Design Impact

The PCI Compiler designs with wirebond packages for HardCopy III and HardCopy IV-E fail to compile.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the PCI Compiler.

Designs With Stratix IV Devices Fail to Meet Timing

Timing fails when using Stratix IV devices with any core combination at 66 MHz.

Affected Configuration

All PCI Compiler designs targeting the Stratix IV devices with the slowest speed grade, C4.

Design Impact

The PCI Compiler designs with some Stratix IV devices may fail to meet timing.

Workaround

None.

Solution Status

This issue will not be fixed.

20. PCI Express Compiler

Revision History

Table 20–1 shows the revision history for the PCI Express Compiler.

For complete information about the new features, refer to the *PCI Express Compiler User Guide*.

Table 20–1. PCI Express Compiler Revision History

Version	Date	Description
10.1 SP1	February 2011	■ Maintenance release.
10.1	December 2010	■ Added following new features to Stratix V support: ■ 256-bit interface. ■ Target design example demonstrating the 256-bit interface that connects the PCI Express IP core to a root complex and a downstream application with the 256-bit interface. ■ Verilog HDL and VHDL simulation support. ■ Added support for the Gen1 ×1 soft IP implementation in Cyclone IV GX device with the Avalon-ST interface. ■ Added support for the hard IP implementation in the Arria II GZ device with the Avalon-ST interface and the following capabilities: ■ Gen1 ×1, ×4 64-bit interface, Gen1 ×8 128-bit interface. ■ Gen2 ×1, 64-bit interface, Gen2 ×4, 128-bit interface.
10.0 SP1	September 2010	■ Added support for the soft IP implementation of the PCI Express MegaCore function in Cyclone IV E devices. ■ Added simulation support for the hard IP implementation of the PCI Express MegaCore function in Stratix V devices. ■ Added support for the Gen2 ×8 design example described in the "Testbench and Design Example" chapter of the *PCI Express Compiler User Guide.*
10.0	July 2010	■ Preliminary support for ×1, ×4, ×8 Gen1 and Gen2 PCI Express MegaCore function in Stratix V devices ■ Added new, integrated PCI Express hard IP endpoint variant that includes all reset and calibration logic ■ Added new, light-weight PCI Express completer-only endpoint variant with fixed transfer size of a single dword
9.1 SP2	April 2010	■ Maintenance release.

Table 20–1. PCI Express Compiler Revision History

Version	Date	Description
9.1 SP1	February 2010	■ Introduces device support for ×2 PCI Express hard IP in Cyclone® IV GX devices. ■ Adds support for 125 MHz reference clock (in addition to the 100 MHz input reference clock) for Gen1 for Arria® II GX, Cyclone IV GX, HardCopy® IV GX and Stratix® IV GX devices.
9.1	November 2009	■ Introduces device support for the ×1 and ×4 PCI Express hard IP in Cyclone IV GX devices. ■ Support for the Gen1 and Gen2 PCI Express ×1, ×4, and ×8 hard IP MegaCore Function in HardCopy IV GX devices. ■ Support for the Gen1 PCI Express ×1 and ×4 soft IP MegaCore Function in HardCopy IV GX devices. ■ Ability to configure many more parameters of the ALTGX transceiver directly from the PCI Express MegaWizard™ Plug-In Manager interface.

Errata

Table 20–2 shows the issues that affect the PCI Express Compiler in versions 10.1 SP1, 10.1, 10.0 SP1, 10.0, 9.1 SP2, 9.1 SP1, and 9.1.

☞ Not all issues affect all versions of the PCI Express Compiler.

Table 20–2. PCI Express Compiler Errata (Part 1 of 2)

Added or Updated	Issue	Affected Versions						
		10.1 SP1	10.1	10.0 SP1	10.0	9.1 SP2	9.1 SP1	9.1
15 Mar 11	User Guide and Parameter Editor Allow Incorrect Application Clock Frequency	✓	✓	✓	✓	—	—	—
15 Feb 11	Hold Time Violations for Hard IP Variations on Arria II GZ Devices	✓	✓	—	—	—	—	—
	PCI Express IP Core Cannot Negotiate to Gen 2 Data Rate on Some Devices	✓	✓	✓	✓	✓	✓	✓
	Memory Read Requests Hang in the SOPC Builder Soft IP Implementation	Fixed	✓	✓	✓	✓	✓	✓
15 Jan 11	Incorrect Arria II GZ Device Support in PCI Express Compiler User Guide	✓	✓	—	—	—	—	—
	PCI Express Compiler User Guide Incorrectly Includes an ALTGXB Reset Signal	✓	✓	—	—	—	—	—

Table 20–2. PCI Express Compiler Errata (Part 2 of 2)

Added or Updated	Issue	Affected Versions						
		10.1 SP1	10.1	10.0 SP1	10.0	9.1 SP2	9.1 SP1	9.1
15 Dec 10	Incorrect Numbering of 256-Bit Interface in PCI Express Compiler User Guide	✓	✓	—	—	—	—	—
	Posted Requests and Completions May Be Blocked if rx_st_mask Is Asserted	✓	✓	✓	✓	✓	✓	✓
	Root Port Example Design Simulation Fails for Some Versions of ModelSim	—	Fixed	✓	✓	—	—	—
	VCS Simulation Script Fails for PCIe Root Port Design Example	—	Fixed	✓	✓	—	—	—
	SOPC Builder Hard IP Implementation Hangs when Entering L1 State	—	Fixed	✓	✓	✓	✓	✓
	The Transceiver May Be Incorrectly Reset Leading to Unreliable Link Behavior	—	Fixed	✓	✓	✓	✓	✓
	Timing Analysis for Cyclone IV GX ×1 Variants	—	Fixed	✓	✓	✓	✓	✓
	PCI Express Compliance Test Does Not Generate Gen2 Compliance Pattern	—	Fixed	✓	✓	✓	✓	✓
15 Sept 10	Arria II GX Missing PLL_powerdown Signal when Using Custom Quartus II Installation	✓	✓	✓	✓	—	—	—
	Compilation Fails for Hard IP PCI Express MegaCore Function in Stratix IV GT Devices	—	—	Fixed	✓	—	—	—
	PCI Express Hard IP Compilation Is Disabled for Gen1 ×4 and ×8 in Some Devices	—	—	Fixed	✓	—	—	—
	PCI Express Design Example Does Always Not Close Timing in Stratix V GX and HardCopy IV GX in 250 MHz Modes	—	—	Fixed	✓	—	—	—
15 July 10	Incorrect Connections Shown in SOPC Builder Illustration	✓	✓	✓	✓	✓	✓	✓
	Incorrect HardCopy IV GX PCIe Gen2 ×8 Buffer Size Restriction Implementation	—	—	—	Fixed	✓	✓	✓
	refclk Cannot Be Used to Generate reconfig_clk	—	—	—	Fixed	✓	✓	✓
	Connecting r2c_err0 or r2c_err1 Output Ports to Your Application Causes Quartus II Compilation to Fail	—	—	—	Fixed	✓	✓	—
	Arria II GX Does Not Report ECC Error Correction and ECC Uncorrectable Error Detection	—	—	—	Fixed	✓	✓	✓
01 Apr 10	Link Training or Down Training Hardware Issues with Gen2 ×4 or ×8 in Stratix IV GX Hard IP	—	—	—	—	Fixed	✓	✓
	MSI Requests not Supported in Completer Only Mode	✓	✓	✓	✓	✓	✓	✓
	Incorrect <variation>_serdes.v(hd) File Produced When Editing an Older PCI Express Variation File	✓	✓	✓	✓	✓	✓	✓
15 Feb 10	Compilation Fails when Working Directory Name Has a Space	—	—	—	—	—	Fixed	✓
	MSI-X Capability Structure Not Working in Hardware	—	—	—	—	—	Fixed	✓
	PCI Express Compiler User Guide, Version 9.1 Error in Table 1-4, Hard IP Configurations	—	—	—	—	—	Fixed	✓

User Guide and Parameter Editor Allow Incorrect Application Clock Frequency

Gen1 ×1 PCI Express compiler hard IP variations that target a Stratix V GX device support application clock frequency 125 MHz only. However, Table 4-1 in the *PCI Express Compiler User Guide* incorrectly indicates that this clock can also have frequency 62.5 MHz, and the PCI Express parameter editor allows the selection of 62.5 MHz or 125 MHz for this clock.

Affected Configurations

All Gen1 ×1 PCI Express compiler hard IP variations that target a Stratix V GX device.

Workaround

For these variations, select application clock frequency 125 MHz in the PCI Express compiler parameter editor.

Solution Status

This issue will be fixed in a future version of the PCI Express Compiler and the *PCI Express Compiler User Guide*.

Hold Time Violations for Hard IP Variations on Arria II GZ Devices

PCI Express compiler hard IP variations that target an Arria II GZ device have hold time violations that affect simulation. The warning is caused by an incorrect timing model setting in the hard IP block for the `tl_cfg_sts` signals.

Affected Configurations

All PCI Express compiler hard IP variations that target an Arria II GZ device.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the PCI Express compiler.

PCI Express IP Core Cannot Negotiate to Gen 2 Data Rate on Some Devices

Auto negotiation to the Gen 2 data rate may fail in some devices. When this failure occurs, the PCI Express compiler is unable to switch to the Gen 2 data rate.

Affected Configurations

All PCI Express Gen 2 variations that target an Arria II GZ, Stratix IV GT, or Stratix IV GX device.

Workaround

No workaround exists for variations with transceivers configured to use the ATX PLL. You must configure the transceivers to use the CMU PLL.

To enable the PCI Express compiler to negotiate to the Gen 2 data rate, generate a configuration that uses the CMU PLL, and follow these steps:

1. After you generate the PCI Express compiler variations and before you compile the project, change directory to the location of the transceiver megafunction instance. The directory contains a <*variation*>**_serdes.v** or <*variation*>**_serdes.vhd** file, depending on the HDL.
2. Depending on the transceiver megafunction instance HDL, follow one of these steps:
   - If your transceiver megafunction instance is generated in Verilog HDL, type the following command:

```
qmegawiz -silent -wiz_override="enable_pcie_gen2_reset=true" \
                 <variant>_serdes.v
```

   - If your transceiver megafunction instance is generated in VHDL, type the following command:

```
qmegawiz -silent -wiz_override="enable_pcie_gen2_reset=true" \
                 <variant>_serdes.vhd
```

Solution Status

This issue will be fixed in a future version of the PCI Express compiler.

Memory Read Requests Hang in the SOPC Builder Soft IP Implementation

In SOPC Builder, the TX interface fails to forward read requests (MRd) to the data link layer due to incorrect decoding of the non-posted header credits.

Affected Configurations

This issue affects the soft IP implementation of the PCI Express IP core generated in SOPC Builder that uses the Avalon-MM interface to the application layer.

Workaround

The workaround is download the following solution:

http:/www.altera.com/support/kdb/solutions/rd12062010_985.html.

Solution Status

This issue is fixed in version 10.1 SP1 of the PCI Express compiler.

Incorrect Arria II GZ Device Support in PCI Express Compiler User Guide

Table 4-1 in the *PCI Express Compiler User Guide* incorrectly shows device support for Gen2 in Arria II GX devices and no Gen2 support in Arria II GZ devices. The opposite is true—Arria II GZ does support Gen2 and Arria II GX does not.

Affected Configurations

This is a documentation error only.

Workaround

No workarounds are required.

Solution Status

This issue will be fixed in a future version of the *PCI Express Compiler User Guide.*

PCI Express Compiler User Guide Incorrectly Includes an ALTGXB Reset Signal

Figures 5-1 and 5-2 and Table 5-30 in the 10.1 release of the *PCI Express Compiler User Guide* include the `reset_reconfig_altgxb_reconfig` signal; however, this signal does not exist.

Affected Configurations

This is a documentation error only.

Workaround

No workarounds are required.

Solution Status

This issue will be fixed in a future version of the *PCI Express Compiler User Guide.*

Incorrect Numbering of 256-Bit Interface in PCI Express Compiler User Guide

The bit ordering is reversed in Figure 5-24 of the *PCI Express Compiler User Guide.* Bit 0 should be at the bottom of the figure and Bit 255 at the top.

Affected Configurations

This is a documentation error only.

Workaround

No workarounds are required.

Solution Status

This issue will be fixed in a future version of the *PCI Express Compiler User Guide.*

Posted Requests and Completions May Be Blocked if rx_st_mask Is Asserted

When the Application Layer asserts `rx_st_mask` to allow Posted Requests or Completions to bypass Non-Posted Requests in the PCIe hard IP RX Buffer, the Posted Requests and Completions may still be blocked by Non-Posted Configuration Space Requests. Asserting `rx_st_mask` does allow Posted Requests or Completions to bypass Non-Posted Memory Space or I/O Space requests that are routed to the

Application Layer. As soon as a Non-Posted Configuration Space request (or a Non-Posted Memory or I/O space request that is being handled as an Unsupported Request) is encountered in the stream of requests in the RX Buffer while rx_st_mask is asserted, subsequent TLPs remain in the RX Buffer until all prior Non-Posted requests have been accepted by the Application Layer logic and rx_st_mask is deasserted.

Affected Configurations

This issue affects the hard IP implementation of the PCI Express IP core in Arria II GX, Cyclone IV GX, and Stratix IV GX devices when the rx_st_mask is being used for performance enhancement or to block Non-Posted requests.

Workaround

Do not design your application layer logic so that rx_st_mask remains asserted until certain Posted Requests or Completions are received. As long as rx_st_mask is eventually deasserted without waiting for posted requests or completions, the blocking Non-Posted Configuration Requests will eventually complete.

Solution Status

This issue will be documented in a future version of the *PCI Express Compiler User Guide*.

Root Port Example Design Simulation Fails for Some Versions of ModelSim

Root port simulation fails using ModelSim versions 6.6c_1 for the Linux operating sytem (OS) or 6.6d for the Windows OS.

Affected Configurations

This issue affects root port example design simulations when using ModelSim 6.6c_1 for the Linux OS or 6.6d for the Windows OS in release 10.0 of the PCI Express Compiler.

Workaround

To prevent this failure, add the -noimmedca option to the vsim command in the **runtb.do** file.

Alternatively, you can update to version 10.1 of the PCI Express compiler.

Solution Status

This issue is fixed in version 10.1 of the PCI Express example design testbench.

VCS Simulation Script Fails for PCIe Root Port Design Example

The VCS simulation script, **runtb_vcs.sh,** does not work for PCI Express Design example described in the *"Testbench and Design Example"* chapter of the *PCI Express Compiler User Guide*.

Affected Configurations

This issue affects VCS simulation of the of the root port example.

Workaround

The workaround is to implement the changes described in the following solution:

http:/www.altera.com/support/kdb/solutions/11022010_852.html.

A second alternative is to upgrade to version 10.1 of the Quartus II software.

Solution Status

This issue is fixed in version 10.1 of the PCI Express compiler.

SOPC Builder Hard IP Implementation Hangs when Entering L1 State

When the host programs the PMCSR register at address 0x1f to the D3 state, Hard IP endpoint variants created in SOPC Builder might hang while performing the power management message handshaking protocol with the root port.

Affected Configurations

This issue affects hard IP implementations of the PCI Express MegaCore function in SOPC Builder.

Workaround

The workaround is to set test_in[7] = 1 to disable all low state power negotiations.

Solution Status

This issue is fixed in version 10.1 of the PCI Express MegaCore function.

The Transceiver May Be Incorrectly Reset Leading to Unreliable Link Behavior

On rare occasions, the transceiver may be incorrectly reset leading to unreliable link behavior.

Affected Configurations

This issue affects the PCI Express MegaCore function targeting Stratix IV GX, Arria II GX, and Cyclone IV GX devices.

Workaround

Contact Altera Support for possible work arounds.

Solution Status

This issue is fixed in version 10.1 of the PCI Express MegaCore function.

Timing Analysis for Cyclone IV GX ×1 Variants

The Quartus II software does not perform timing analysis for the FPGA fabric in Cyclone IV GX ×1 variants; consequently, variants that would fail timing analysis are not identified.

Affected Configurations

This issue affects ×1 variants in the Cyclone IV GX device.

Workaround

You can manually create the required clock constraint. Example 20–1 provides the equation for this constraint. In this equation <*n*> is 8.000 for a 125 MHz application clock and 16 for a 62.5 MHz application clock.

Example 20–1. Clock Constraint

```
# create_clock -name {core_clk_out} -period <n> -waveform { 0.000 8.000 } [get_nets
{*altpcie_hip_pipen1b_inst | core_clk_out~clkctrl}]
```

Solution Status

This issue is fixed in version 10.1 of the Quartus II software.

PCI Express Compliance Test Does Not Generate Gen2 Compliance Pattern

The PCI Express MegaCore function does not generate the Gen2 compliance pattern for the hard IP implementation in Stratix IV GX devices because the hard IP reset circuitry is holding the transceiver in reset.

Affected Configurations

This issue affects the hard IP implementation of the PCI Express MegaCore function targeting Stratix IV GX devices that use reset scheme for <*variant*>**.v** or **.vhd** MegaCore function as described the "Reset and Clocks" chapter of the *PCI Express Compiler User Guide*. (It does not affect the <*variant*>**_plus.v** or **.vhd** MegaCore functions.)

Workaround

The workaround is to modify the definition of the `rx_digitalreset_serdes` signal in <*variant*>**.v** or **.vhd** file when running the compliance test. Example 20–2 shows the required modification for compliance testing and the definition for normal operation.

Example 20–2. Definition of rx_digitalreset_serdes for Compliance Testing and Normal Operation

```
// Use this assignment for compliance testing
assign rx_digitalreset_serdes = rc_rx_digitalreset;
// Use this assignment for operation in non-compliance mode
assign rx_digitalreset_serdes = rc_rx_digitalreset | rst_rxpcs;
```

In addition, the reserved `test_in` bit (`test_in[32]`) must be defined as an input to the reset circuit to indicate that the DUT is performing the compliance test. When `test_in[32]` is set to 1, the portion of the reset circuit which introduces the compliance bug is bypassed.When this bit is set to 0, the PCI Express MegaCore function works in normal operating mode.

Solution Status

This issue is fixed in version 10.1 of the PCI Express MegaCore function.

Arria II GX Missing PLL_powerdown Signal when Using Custom Quartus II Installation

PCI Express MegaCore functions that target the Arria II GX device are missing the `pll_powerdown` signal which connects to the <*variation*>**_serdes.v** or **.vhd** module.

Affected Configurations

This issue affects the hard IP implementation of the PCI Express MegaCore function targeting Arria II GX devices when using a custom Quartus II installation which does not include the Stratix IV device family.

Workaround

The workaround is to include the Stratix IV GX device family when you install the Quartus II 10.0 or 10.0 SP1 software.

Solution Status

This issue will be fixed in a future version of the Quartus II software.

Compilation Fails for Hard IP PCI Express MegaCore Function in Stratix IV GT Devices

For designs that target Stratix IV GT devices in downbonded packages, the Quartus II software version 10.0 incorrectly places PCI Express hard IP block at the bottom transciever block, which does not include the hard IP PCI Express MegaCore function. Compilation of the design fails with a message similar to the following:

```
Error: Can't assign I/O pad <"pad name"> to <pin name> because this causes
failure in the placement of the other atoms in its associated channel.
```

```
Error: The transceiver block has no associated PCI Express hard IP block.
```

Affected Configurations

This issue affects the hard IP implementation of the PCI Express MegaCore function targeting Stratix IV GT devices.

Workaround

The workaround is to install version 10.0 SP1 of the Quartus II software.

Solution Status

This issue is fixed in version 10.0 SP1 of the Quartus II software.

PCI Express Hard IP Compilation Is Disabled for Gen1 ×4 and ×8 in Some Devices

The PCI Express Compiler v10.0 does not support IP and MegaWizard generation or regeneration of PCIe Gen1 ×4 or ×8 designs targeting the Stratix IV GX, Stratix IV GT, and HardCopy IV device families.

Affected Configurations

This issue affects Gen1 ×4 or ×8 designs targeting the hard IP implementation of the PCI Express MegaCore function in Stratix IV and HardCopy IV device families in the Quartus II 10.0 release.

Workaround

The workaround is to download and install Quartus II software patch described in the following solution.

http:/www.altera.com/support/kdb/solutions/rd07012010_723.html.

A second alternative is to continue to use the Quartus II 9.1 SP2 release to generate the affected Gen1 PCI Express variant. After generating your variant using the Quartus II 9.1 SP2 software, you can compile your complete design using the either the 9.1 SP2 or 10.0 Quartus II 10.0 software release.

A third alternative is to parameterize the PCI Express MegaCore function to run at the Gen2 rate.

Solution Status

This issue is fixed in version 10.0 SP1 of the PCI Express MegaCore function.

PCI Express Design Example Does Always Not Close Timing in Stratix V GX and HardCopy IV GX in 250 MHz Modes

The PCI Express design example discussed in both the "*Getting Started*" and "*Testbench and Design Example*" chapters of the *PCI Express Compiler User Guide* does not always close timing in Stratix V GX and HardCopy IV GX devices running at 250 MHz.

Affected Configurations

This issue affects Stratix V GX and HardCopy IV GX devices running at 250 MHz in the Quartus II 10.0 release.

Workaround

There is no workaround.

Solution Status

This issue is fixed in version 10.0 SP1 of the PCI Express Compiler.

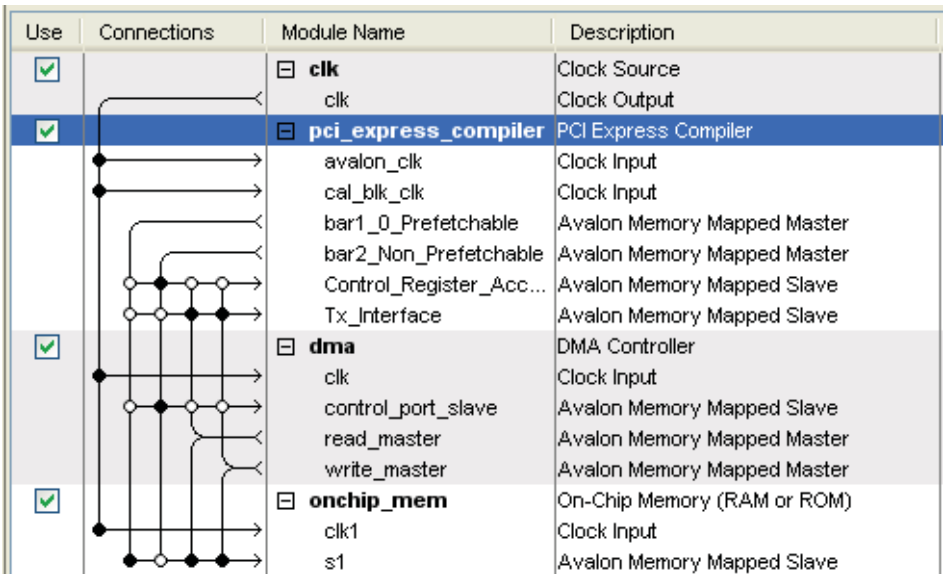
Incorrect Connections Shown in SOPC Builder Illustration

"*Figure 16-3 Port Connections*" in the *PCI Express Compiler User Guide* is missing a connection from the dma_0 `read_master` to the onchip_memory2_0 `s1`. In addition, it shows an incorrect connection from the pcie_compiler_0 `bar2_Non_Prefetchable` to onchip_memory2_0 `s1`.

Affected Configuration

This is a documentation error only. Figure 20–1 illustrates the correct connections.

Figure 20–1. System Port Connections



Workaround

No workaround is required. Make the connections described "Table 16-6 SOPC Builder Conections" of the *PCI Express Compiler User Guide*

Solution Status

This issue will be corrected in a future version of the *PCI Express Compiler User Guide*.

Incorrect HardCopy IV GX PCIe Gen2 ×8 Buffer Size Restriction Implementation

You must restrict the PCIe Gen2 ×8 variations that target the HardCopy IV GX device to use an 8 KBytes Rx Buffer and an 8 KByte Retry Buffer. The PCI Express Compiler does not implement this restriction correctly when you select **HardCopy IV GX** for the **PHY type**, **Gen2** for **Max rate** and **×8** for **Lanes**. Incorrect values are shown in the **Rx Buffer Space Allocation** table on the **Buffer Setup** page PCI Express Compiler MegaWizard. And, an incorrect value is reported on the `ko_cpl_spc_vc0` output signal. In addition, incorrect flow control credit values are reported on the PCIe link in both the IP Functional Simulation model of the variation and in Stratix IV GX compilations of the HardCopy IV GX compatible variation.

Affected configurations

HardCopy IV GX compatible Gen2 ×8 variations in the 9.1, 9.1 SP1, 9.1 SP2, and 10.0 releases of the Quartus II software. Gen2 ×1, Gen2 ×4, and all Gen1 variations are not affected.

Workaround

You can upgrade to the 10.0 release of the Quartus II software.

Status

This issue is fixed in the Quartus II 10.0 release.

refclk Cannot Be Used to Generate reconfig_clk

Due to changes to the dynamic reconfiguration IP, you can no longer use the `refclk` pin directly or indirectly to generate the reconfiguration clock (`reconfig_clk`). The example design generated by PCI Express Compiler in the affected versions incorrectly uses the `refclk`.

Affected Configurations

This issue affects implementations of the PCI Express MegaCore function in Stratix IV GX/GT and Arria II GX devices.

Workaround

There are two solutions to this issue:

- Use a free running clock from a non-transceiver I/O clock pin that is stable at device power up.
- Use a GPLL to generate the `reconfig_clk` sourced from an I/O clock pin.

For more information refer to *Altera Solution rd12172009_309*.

Solution Status

This issue is fixed in version 10.0 of the PCI Express Compiler.

Connecting r2c_err0 or r2c_err1 Output Ports to Your Application Causes Quartus II Compilation to Fail

Adding the speed negotiation signals, `r2c_err0` and `r2c_err1`, to your PCI Express MegaCore function causes Quartus II compilation to fail.

Affected Configurations

This issue affects PCI Express designs in Stratix IV GX, HardCopy IV GX, and Arria II GX devices.

Workaround

Leave the output signals, `r2c_err0` and `r2c_err1`, unconnected.

Solution Status

This issue is fixed in version 10.0 of the Quartus II Compiler.

Arria II GX Does Not Report ECC Error Correction and ECC Uncorrectable Error Detection

The ECC error reporting signals (`derr_*`, `r2c_err0`, and `rx_st_err[0]`) are always set to 0 for Arria II GX devices in the hard IP implementation. The Arria II GX implementation does not propagate these ECC correction/detection flags for the RX or Retry buffers. This issue only concerns error reporting. Single bit errors are corrected. Double-bit or greater errors are never correctable.

Affected Configurations

This is a documentation issue for the hard IP implementation of Arria II GX devices.

Workaround

Two possible workarounds are to target the Arria II GZ device and to use ECRC to mitigate the possibility of incurring an uncorrectable error.

Solution Status

This issue is fixed in version 10.0 of the *PCI Express Compiler User Guide*.

Link Training or Down Training Hardware Issues with Gen2 ×4 or ×8 in Stratix IV GX Hard IP

Hard IP implementations of Gen2 PCI Express ×4 or ×8 designs may have link training or down training issues.

Affected Configurations

This issue affects Gen2 ×4 and ×8 hard IP PCI Express MegaCore functions in Stratix IV GX devices.

Workaround

The workaround is to download and install the patch described in the following solution.

http://www.altera.com/support/kdb/solutions/rd03012010_867.html

Solution Status

This issue is fixed in version 9.1 SP2 of the PCI Express Compiler.

MSI Requests not Supported in Completer Only Mode

When you configure the PCI Express MegaCore function in **Completer Only** mode, if an MSI is sent by asserting an interrupt, any subsequent reads returns all zeros.

Affected Configuration

This issue affects variants that use the Avalon-MM interface and select **Completer Only** mode on the **Avalon Configuration** tab.

Workaround

Configure your MegaCore function in **Requester/Completer** mode.

Solution Status

This issue will be not fixed in a future version of the PCI Express MegaCore function.

Incorrect <variation>_serdes.v(hd) File Produced When Editing an Older PCI Express Variation File

If you use PCI Express Compiler version 9.1 or later to edit a PCI Express Compiler variation that was created with Quartus II version 9.0 SP2 or earlier, a corrupted **<*variation*>_serdes.v** (or **<*variation*>_serdes.vhd**) file is created. This corrupt file leads to errors when trying to simulate or compile the PCI Express variation.

Affected Configurations

PCI Express variants created in Quartus II version 9.0 SP2 or earlier and edited in Quartus II release 9.1 or later.

Workaround

Before editing the variation with the newer PCI Express Compile version, delete the **<*variation*>_serdes.v** (or **<*variation*>_serdes.vhd**) file. If you had modified any settings in the SERDES file, re-enter them in PCI Express Compiler using the **Configure Transceiver Block** button on the **System Settings** tab.

Solution Status

This issue will not be fixed in a future version of PCI Express Compiler.

Compilation Fails when Working Directory Name Has a Space

Compilation of the PCI Express Compiler MegaCore function fails if the working directory name includes a space.

Affected Configurations

This issue affects all versions of the PCI Express MegaCore function that are compiled using version 9.1 of the Quartus II software.

Workaround

Do not include spaces in the working directory name.

Solution Status

This issue is fixed in version 9.1 SP1 of the Quartus II software.

MSI-X Capability Structure Not Working in Hardware

The MSI-X capability structure simulates correctly but is incorrect in the actual hardware for hard IP implementations of the PCI Express MegaCore function.

Affected Configurations

This is an Assembler issue that affects all hard IP PCI Express MegaCore functions in Stratix IV GX, Arria II GX and Cyclone IV GX devices.

Workaround

The workaround is to download and install Quartus II 9.1 software patch described in the following solution.

http:/www.altera.com/support/kdb/solutions/rd11172009_89.html

Solution Status

This issue is fixed in version 9.1 SP1 of the Quartus II software.

PCI Express Compiler User Guide, Version 9.1 Error in Table 1-4, Hard IP Configurations

Table 1-4 in the *PCI Express Compiler User Guide* breaks across two pages. The Avalon-ST heading is erroneously repeated on the second page; however, the Avalon-MM applies to the devices listed on the second page of this table. The correct table is given below.

Table 20–3. PCI Express Hard IP Configurations for the PCI Express Compiler in 9.1

Device	Link Rate (Gbps)	×1	×4	×8
Avalon Streaming (Avalon-ST) Interface using MegaWizard Plug-In Manager Design Flow				
Stratix IV GX	2.5	yes	yes	yes
	5.0	yes	yes	yes
Arria II GX	2.5	yes	yes	yes *(1)*
	5.0	no	no	no
Cyclone IV GX	2.5	yes	yes	no
	5.0	no	no	no
HardCopy IV GX	2.5	yes	yes	yes
	5.0	yes	yes	yes
Avalon-MM Interface using SOPC Builder Design Flow				
Stratix IV GX	2.5	yes	yes	no
	5.0	yes	no	no
Arria II GX	2.5	yes	yes	no
	5.0	no	no	no
Cyclone IV GX	2.5	yes	yes	no
	5.0	no	no	no

Note to Table 20–3:

(1) The ×8 support uses a 128-bit bus at 125 MHz.

Affected Configurations

This is a documentation error only.

Workaround

No workaround is required.

Solution Status

This issue will be fixed in version 91. SP1 of the *PCI Express Compiler User Guide*.

21. POS-PHY Level 4

Revision History

Table 21–1 shows the revision history for the POS-PHY Level 4 MegaCore function.

For more information about the new features, refer to the *POS-PHY Level 4 MegaCore Function User Guide*.

Table 21–1. POS-PHY Level 4 MegaCore Function Revision History

Date	Version	Description
December 2010	10.1	Maintenance release.
July 2010	10.0	Maintenance release.
November 2009	9.1	Maintenance release.

Errata

The following sections addresses known errata and documentation issues for the POS-PHY Level 4 MegaCore function. Errata are functional defects or errors, which may cause the POS-PHY Level 4 MegaCore function to deviate from published specifications. Documentation issues include errors, unclear descriptions, or omissions from current published specifications or product documents.

Table 21–2 shows the issues that affect the POS-PHY Level 4 MegaCore function v10.1, v10.0, and v9.1.

Not all issues affect all versions of the POS-PHY Level MegaCore function.

Table 21–2. POS-PHY Level 4 MegaCore Function Errata

Added or Updated	Issue	Affected Version		
		10.1	10.0	9.1
15 Mar 11	Compilation Targeting a Stratix V Device Fails	✓	—	—
15 Dec 10	Import PLL Frequency Launches Incorrect Parameter Editor	✓	—	—
15 Sep 10	Cannot Edit ALTPLL Megafunction for Stratix V Devices	✓	✓	—
15 Jul 10	Incorrect LVDS Frequencies in Quartus II Compilation	✓	✓	—
15 May 08	Errors when Editing Transmitters v7.2 or Earlier in v8.0	✓	✓	✓
	Training Interval is Greater than Specified	✓	✓	✓
01 May 07	Irrelevant Signals: err_ry_msop* & err_ry_meop*	✓	✓	✓
	Warning Message: Pin “err_rd_dpa” Stuck at GND	✓	✓	✓
	IP Toolbench Error After Changing the Device Family	✓	✓	✓
	IP Toolbench Fails to Generate IP Functional Simulation Models for HardCopy Stratix Devices	✓	✓	✓
	IP Toolbench Generation Fails if the Generation Is Cancelled and Restarted	✓	✓	✓

Compilation Targeting a Stratix V Device Fails

Designs that include a POS-PHY Level 4 IP core and target a Stratix V device, do not compile even if you have a valid license for the IP core. Refer to Altera solution rd03082011_116 at www.altera.com/support/kdb/solutions/rd03082011_116.html.

Affected Configurations

POS-PHY Level 4 IP cores that target a Stratix V device.

Design Impact

Designs that include this IP core and target a Stratix V device cannot compile.

Workaround

To fix this issue, if you have a valid license for this IP core, follow these steps:

1. Upgrade your Quartus II software installation to the 10.1 Service Pack 1 version.
2. Apply Patch 1.19 to your Quartus II software installation.
3. Regenerate your IP core and any others in your design that are affected by this issue.
4. Recompile your design.

Solution Status

This issue will be fixed in a future version of the Quartus II software.

Import PLL Frequency Launches Incorrect Parameter Editor

If you click **Import PLL Frequency**, the ALTLVDS_TX parameter editor correctly starts, but you can incorrectly edit all parameters not just the **Frequency /PLL Settings** page parameters.

Affected Configurations

This issue affects all configurations.

Design Impact

There is no design impact.

Workaround

To work around this issue, when the ALTLVDS_TX parameter editor starts on the **General parameters** page, follow these steps:

1. Click **Next** to go to the **Frequency/PLL Settings** page.
2. Select desired input clock rate.
3. Click **Finish** twice to skip the remaining pages and close the ALTLVDS_TX parameter editor.

Solution Status

This issue will be fixed in a future version of the POS-PHY Level 4 MegaCore function.

Cannot Edit ALTPLL Megafunction for Stratix V Devices

You cannot edit the ALTPLL megafunction with the parameter editor.

Affected Configurations

This issue affects variations for Stratix V devices.

Design Impact

There is no design impact.

Workaround

To work around this issue, manually modify the ALTPLL variation to the desired parameters. The only parameter that generally requires modification is the phase shift, which is currently set to a quarter clock period.

Solution Status

This issue will be fixed in a future version of the POS-PHY Level 4 MegaCore function.

Incorrect LVDS Frequencies in Quartus II Compilation

For most of the data rates, the LVDS frequencies, which the Quartus II software reports after compilation in the Timequest Timing Analyzer under the **Clocks** section, are incorrect. Though, for some data rates (800 Mbps, 1000 Mbps, 1250 Mbps), the calculated frequencies are correct

Affected Configurations

This issue affects 64 and 128 bit RX and TX variations for Stratix V devices.

Design Impact

The Quartus II software uses incorrect clock frequencies during compilation.

Workaround

To work around this issue, use only the 800-Mbps, 1,000-Mbps or 1,250-Mbps data rates.

Solution Status

This issue will be fixed in a future version of the POS-PHY Level 4 MegaCore function.

Errors when Editing Transmitters v7.2 or Earlier in v8.0

If you edit a v7.2 or earlier 64 or 128-bit transmitter MegaCore variation in the v8.0 or later MegaWizard Plug-In, the PLL input frequency is set to 1 MHz, which is incorrect.

Affected Configurations

This issue affects 64- and 128-bit transmitters.

Design Impact

There is no design impact.

Workaround

To work around the issue, follow these steps:

1. Click in the **LVDS Data Rate** dialog box.
2. Press **Enter**.

The PLL input frequency parameter resets to the correct value—data rate divided by deserialization factor.

Solution Status

This issue will never be fixed.

Training Interval is Greater than Specified

In corner cases, for example with datapath is 256 and a high number of ports and low burst length (`BURSTLEN`), the maximum training interval (`MaxT`) is greater than you specify.

Affected Configurations

This issue affects all designs.

Design Impact

There is no design impact.

Workaround

Add (or subtract) another `BURSTLEN` to calculation, so `MaxT` is `SET_MaxT` + 2 × `BURSTLEN`.

Solution Status

This issue will never be fixed.

Irrelevant Signals: err_ry_msop* & err_ry_meop*

After generation, the MegaCore function may include the following irrelevant output signals, which you can safely ignore:

- `err_ry_msop*`

- err_ry_meop*

Affected Configurations

This issue affects all designs.

Design Impact

There is no design impact.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the POS-PHY Level 4 MegaCore function.

Warning Message: Pin “err_rd_dpa” Stuck at GND

During compilation, the Quartus II software issues the following warning, which you can safely ignore:

```
Pin "err_rd_dpa" Stuck at GND
```

Affected Configurations

This issue affects all non-Stratix GX receivers with dynamic phase alignment (DPA) enabled.

Design Impact

There is no design impact.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the POS-PHY Level 4 MegaCore function.

The Calendar Length Value Cannot Equal 256

If the transmitter’s status interpretation mode is set to pessimistic, the programmable calendar length support parameter must be less than the maximum number of ports (< 256), unless the asymmetric port support parameter is enabled.

Affected Configurations

This issue affects all transmitter variations of the MegaCore function that use the pessimistic mode for status interpretation, and that do not have the asymmetric port support parameter enabled.

Design Impact

The status first-in first-out (FIFO) buffer may lock up. The scheduler in individual buffers variations of the MegaCore function may also lock up.

Workaround

If you turn on the programmable calendar length support in your variation, make sure that you set the calendar length value—via a pin or the Avalon Memory-Mapped (Avalon-MM) register—to less than the maximum calendar length (that is, 256); unless asymmetric port support is enabled, in which case you select the maximum calendar length in IP Toolbench.

Solution Status

This issue will be fixed in a future version of the POS-PHY Level 4 MegaCore function.

IP Toolbench Error After Changing the Device Family

If you change the device family when editing an existing custom megafunction variation (POS-PHY Level 4 MegaCore function variation) without first changing the device family in the Quartus II project, an error may occur when generating the MegaCore function. This results in a MegaCore function generation error message.

This issue also applies when creating a new custom megafunction variation, if you use a different device family to that specified in the Quartus II project.

Affected Configurations

This issue can affect all configurations.

Design Impact

You may not be able to generate a MegaCore function.

Workaround

Before using the MegaWizard Plug-In Manager to create or edit a POS-PHY Level 4 custom megafunction variation, make sure that a Quartus II project exists and that the required device family is set in the project. To set the device family, in the Quartus II software, on the Assignments menu click **Device**.

When using the MegaWizard Plug-In Manager to create or edit the megafunction variation, set the device family to be the same as the device family set in the Quartus II project. You can set the device family in the **Basic Parameters** tab when parameterizing the MegaCore function.

Solution Status

This issue will be fixed in a future version of the POS-PHY Level 4 MegaCore function.

IP Toolbench Fails to Generate IP Functional Simulation Models for HardCopy Stratix Devices

If you select **HardCopy Stratix** in the MegaWizard Plug-In Manager and you turn on **Generate Simulation Model** and generate a MegaCore function variation, IP Toolbench fails with an error.

Affected Configurations

This issue affects all configurations.

Design Impact

You cannot generate an IP functional simulation model.

Workaround

Select the Stratix family in the MegaWizard Plug-In Manager.

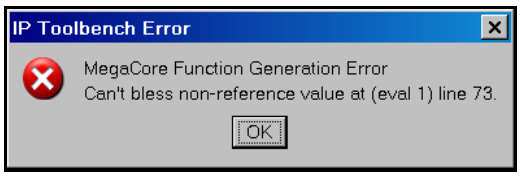
Solution Status

This issue will never be fixed.

IP Toolbench Generation Fails if the Generation Is Cancelled and Restarted

By clicking the IP Toolbench **Generate** button, you start generating a POS-PHY Level 4 MegaCore function variation. If, during generation, you click the **Cancel** button (Generation window) and click the IP Toolbench **Generate** button again to restart the generation, IP Toolbench fails and produces the following error message:

Figure 21–1. IP Toolbench Generation Error Message



Affected Configurations

This issue affects all variations of the MegaCore function.

Design Impact

IP Toolbench does not generate any files.

Workaround

To cancel a generation and avoid this error, follow these steps:

1. Click the **Cancel** button in the Generation window.
2. Close IP Toolbench by clicking the × in the upper right corner.
3. Relaunch IP Toolbench from the MegaWizard Plug-In Manager (Tools menu).

Refer to the Getting Started chapter of the *POS-PHY Level 4 MegaCore Function User Guide* for instructions on using IP Toolbench.

Solution Status

This issue will be fixed in a future version of the POS-PHY Level 4 MegaCore function.

Revision History

Table 22–1 shows the revision history for the QDRII SRAM MegaCore function.

For more information about the new features, refer to the *QDRII SRAM MegaCore Function User Guide*.

Table 22–1. QDRII SRAM MegaCore Function Revision History

Version	Date	Description
10.1	December 2010	Maintenance release.
10.0	July 2010	Maintenance release.
9.1	November 2009	Maintenance release.
9.0 SP2	July 2009	Maintenance release.
9.0 SP1	May 2009	Maintenance release.
9.0	March 2009	Maintenance release.
8.1	November 2008	Maintenance release.

Errata

Table 22–2 shows the issues that affect the QDRII SRAM MegaCore functionv10.1, 10.0, and 9.1.

Not all issues affect all versions of the QDRII SRAM MegaCore function.

Table 22–2. QDRII SRAM MegaCore Function Errata

Added or Updated	Issue	Affected Version		
		10.1	10.0	9.1
15 May 08	Termination Error When Compiling Design	✓	✓	✓
01 Dec 06	Incorrect IP Toolbench Latency Behavior	✓	✓	✓
01 Nov 06	Simulating with the VCS Simulator	✓	✓	✓
	TimeQuest Timing Analyzer Failure	✓	✓	✓
	PLL Placement	✓	✓	✓
01 Nov 05	Constraints Errors With Companion Devices	✓	✓	✓
	Supported Device Families	✓	✓	✓
	Compilation Error (Stratix II Series & HardCopy II Devices Only)	✓	✓	✓
	Gate-Level Simulation Filenames	✓	✓	✓
	The ModelSim Simulation Script Does Not Support Companion Devices	✓	✓	✓

Termination Error When Compiling Design

The Fitter reports the following error: "Error Bidirectional I/O "cq" uses the parallel termination but does not have dynamic termination control."

Affected Configurations

This issue affects designs using the QDRII SRAM Controller.

Design Impact

The design fails to fit.

Workaround

At top-level design, change the pin direction from inout to input for
- qdrii_cq_<index>; qdrii_cqn_<index>.

Solution Status

This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

Incorrect IP Toolbench Latency Behavior

When you open the IP Toolbench Parameterize window, you can select any latency for the default **QDRII**, but it only supports 1.5.

Affected Configurations

This issue affects all QDRII SRAM configurations.

Design Impact

IP Toolbench does not generate a variation and gives the following error message:

```
MegaCore Function Generation Error
IP Functional Simulation creation Failed. The following error was
returned:
Error: Top-level design entity
"qdr_auk_qdrii_sram_avalon_controller_ipfs_wrap" is undefined.
```

Workaround

For longer latency, select **QDRII+**.

Solution Status

This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

Simulating with the VCS Simulator

The QDRII SRAM Controller MegaCore function does not support the VCS simulator.

Affected Configurations

This issue affects all configurations.

Design Impact

The design does not simulate.

Workaround

There is no workaround for VHDL simulations. For Verilog HDL simulations. Change line 154 in the **qdrii_model.v** file to:

```
begin : f1
```

Also, change line 417 to:

```
begin : f2
```

Solution Status

This issue will not be fixed.

TimeQuest Timing Analyzer Failure

When you use the Quartus II TimeQuest timing analyzer, it reports a recovery issue, because the reset is not in the same clock domain as the system clock.

Affected Configurations

This issue affects all configurations.

Design Impact

This issue has no design impact.

Workaround

Change the reset sequence for the signals clocked on the CQ clock, before you run the TimeQuest timing analyzer.

Solution Status

This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

PLL Placement

The IP Toolbench-generated example design uses a PLL phase shift of 90°, which can cause the design to fail hold timing analysis. The source synchronous PLL for the read capture should have a location constraint to place it on the same side of the device as the Q pins; otherwise, the source synchronous compensation does not compensate for the expected delays.

Affected Configurations

This issue affects all configurations.

Design Impact

The design fails hold timing analysis.

Workaround

The PLL must be located on the same side of the device as the CQ/CQn groups, for the PLL to compensate properly.

Solution Status

This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

Constraints Errors With Companion Devices

When you change the device in your project or add a HardCopy II companion device to a Stratix II project and you reopen the variation with IP Toolbench, the constraints editor sometimes does not show all previously set byte groups in the floorplan. The constraints editor only shows the constraints applied to byte groups that are valid for the current device.

Affected Configurations

This issue affects all configurations.

Design Impact

The design fails.

Workaround

Reassign the byte groups for the new device in the constraints editor.

Solution Status

This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

Supported Device Families

The QDRII SRAM Controller MegaCore function only supports Stratix and Stratix II series, and HardCopy II devices. However, if you choose an unsupported device for your Quartus II project and subsequently start the MegaWizard Plug-In Manager, you can choose a different device family in the MegaWizard Plug-In Manager, which allows you to choose the QDRII SRAM Controller MegaCore function. There are no error messages when you perform this illegal operation.

Affected Configurations

This issue affects all configurations.

Design Impact

You cannot compile a design.

Workaround

Ensure you choose a supported device family for the Quartus II project.

Solution Status

This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

Compilation Error (Stratix II Series & HardCopy II Devices Only)

The IP Toolbench Constraints window allows the illegal situation where you can share DQ groups on the top and bottom banks for Stratix II series and HardCopy devices. When you compile your design the Quartus II software issues a no fit error.

Affected Configurations

This issue affects all DQS mode QDRII SRAM controllers on Stratix II series and HardCopy II devices.

Design Impact

When you choose **Start Compilation**, there is an error message and the design does not compile.

Workaround

If you are targeting Stratix II series or HardCopy II devices, in the Constraints window ensure you choose bytegroups on either the top or the bottom of the device, but not both.

Solution Status

This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

Gate-Level Simulation Filenames

Various Quartus II software options may cause it to generate a netlist with a different filename than that expected by the gate-level simulation script. The simulation script expects <*project name*>**.vho** or .**vo** and <*project name*>**_v** or **_vhd.sdo** files to be present.

Affected Configurations

This issue affects all configurations.

Design Impact

You cannot run gate-level simulations.

Workaround

For VHDL gate-level simulations, in the **simulation/modelsim** directory follow these steps:

1. Rename <*filename*>**.vho** file to <*project name*>**.vho.**

2. Rename <*filename*>**.sdo** file to <*project name*>**_vhd.sdo**.

For Verilog HDL gate-level simulations, in the **simulation/modelsim** directory follow these steps:

1. Rename the <*filename*>**.vo** file to <*project name*>**.vo.**
2. Rename the <*filename*>**.sdo** file to <*project name*>**_v.sdo**.
3. In the <*project name*>.**vo** file change the following line to point to the <*project name*>**_v.sdo** file:

```
initial $sdf_annotate("<project name>_v.sdo");
```

Solution Status

This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

The ModelSim Simulation Script Does Not Support Companion Devices

If you have a HardCopy II companion device in a Stratix II project, be aware that the ModelSim simulation scripts do not work if you change to your companion device.

Affected Configurations

This issue affects designs with companion devices.

Design Impact

The simulation script does not run.

Workaround

Edit the ModelSim script to include the correct libraries.

Solution Status

This issue will be fixed in a future version of the QDRII SRAM Controller MegaCore function.

23. QDR II and QDR II+ SRAM Controller with UniPHY

Revision History

Table 23–1 shows the revision history for the QDR II and QDR II+ SRAM Controller with UniPHY.

For more information about the new features, refer to the *QDR II and QDR II+ SRAM Controller with UniPHY User Guide*.

Table 23–1. QDR II and QDR II+ SRAM Controller with UniPHY Revision History

Date	Version	Description
December 2010	10.1	■ Added preliminary support for Arria II GZ and Stratix V. ■ Added new generated directory structure. ■ Added new OCT Sharing Interface feature. ■ Added External Memory Interface Toolkit.
September 2010	10.0 SP1	■ Maintenance release.
July 2010	10.0	■ Final support for Arria II GX devices. ■ Added width expansion feature. ■ Added variable latency feature.
November 2009	9.1	First release.

Errata

Table 23–2 shows the issues that affect the QDR II and QDR II+ SRAM Controller with UniPHY v10.1, v10.0 SP1, v10.0, and v9.1.

Not all issues affect all versions of the QDR II and QDR II+ SRAM Controller with UniPHY.

Table 23–2. QDR II and QDR II+ SRAM Controller with UniPHY Errata (Part 1 of 2)

Added or Updated	Issue	Affected Version			
		10.1	10.0 SP1	10.0	9.1
15 Mar 11	VHDL-only Simulation Not Supported	✓	—	—	—

Table 23–2. QDR II and QDR II+ SRAM Controller with UniPHY Errata (Part 2 of 2)

Added or Updated	Issue	Affected Version			
		10.1	10.0 SP1	10.0	9.1
15 Dec 10	NativeLink Simulation fails for VHDL Output	✓	—	—	—
	NativeLink Simulation fails for VHDL Output	—	✓	✓	—
	Timing-related Warning Messages When Sharing PLLs on Stratix V Devices	✓	—	—	—
	Reset Synchronizer May Cause Design to Fail Timing	✓	—	—	—
	Compilation Fails if Synthesis Fileset is Mixed with Example Project Files	✓	—	—	—
	Warning Messages Displayed When Compiling for Stratix V Devices	✓	—	—	—
	Cannot Launch MegaWizard Plug-In Manager by Opening Example Design	✓	—	—	—
	Example Design May Not Compile for IP Cores from Earlier Versions	✓	—	—	—
	Calibration Failure in Earlier Versions	✓	—	—	—
	SOPC Builder-generated Systems Cannot Serve as Top-Level Design	✓	—	—	—
	Higher Delays and Skews Expected for Corner I/Os in Stratix V Devices	✓	—	—	—
15 Sept 10	Simulation Fails—PLL Clocks Out of Synchronization	✓	✓	✓	—
15 Aug 10	Selecting VHDL Gives a Verilog HDL IP Core	✓	✓	✓	—
15 Jul 10	BSF File Not Generated	Fixed	✓	✓	—
	Global Signal Assignments Not Applied	✓	✓	✓	—
	Simulation Error	—	Fixed	✓	—
	Incorrect Clock Uncertainty	✓	✓	✓	—
	IP Core May Not Operate Below 167MHz	✓	✓	✓	—
15 Nov 09	UniPHY DQS Clock Buffer Location	✓	✓	✓	✓
	IP Functional Simulation Model	✓	✓	✓	✓
	No Link to User Guide from Wizard	✓	✓	✓	✓
	Incorrect Operation of Waitrequest Signal	—	—	Fixed	✓
	QDR II SRAM Emulated Mode	✓	✓	✓	✓

VHDL-only Simulation Not Supported

VHDL-only simulation is not supported in version 10.1 of the QDR II and QDR II+ SRAM Controller with UniPHY.

Affected Configurations

This issue affects all designs.

Design Impact

The simulation fails.

Workaround

The workaround for this issue is to use a mixed Verilog-VHDL simulator.

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

NativeLink Simulation fails for VHDL Output

In version 10.1 of the Quartus II software, when a user specifies VHDL output for the QDR II and QDR II+ SRAM Controller with UniPHY and attempts to simulate using NativeLink, NativeLink fails and reports that it cannot find the file <*design_name*>**.vho** in the top-level directory.

Affected Configurations

This issue affects all VHDL designs.

Design Impact

The simulation fails.

Workaround

The workaround for this issue is to not use NativeLink for simulations of VHDL designs, but to set up simulation manually instead.

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

NativeLink Simulation fails for VHDL Output

In version 10.0 of the Quartus II software, when a user specifies VHDL output for the QDR II and QDR II+ SRAM Controller with UniPHY and attempts to simulate using NativeLink, NativeLink fails and reports that it cannot find the file <*design_name*>**.vho** in the top-level directory.

Affected Configurations

This issue affects all VHDL designs.

Design Impact

The simulation fails.

Workaround

The workaround for this issue is to edit the <*design_name*>**.vhd** file and remove the line similar to the following:

```
-- IPFS_FILES : <design_name>.vho
```

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

Timing-related Warning Messages When Sharing PLLs on Stratix V Devices

When instantiating a design in PLL/DLL slave mode on a Stratix V device, the TimeQuest Timing Analyzer may display warning messages similar to the following:

```
Warning: Ignored filter at slave_report_timing_core.tcl(176):
slave_inst0|controller_phy_inst|memphy_top_inst|umemphy|uio_pads|
dq_ddio[1].ubidir_dq_dqs|altdq_dqs2_inst|thechain|clkin could not be
matched with a keeper or register or port or pin or cell or net
```

```
Warning: Command get_path failed
```

Affected Configurations

This issue affects Stratix V designs instantiated in PLL/DLL slave mode.

Design Impact

The resulting timing analysis is incorrect.

Workaround

This issue has no workaround. The warning messages can be safely ignored; however, do not rely on the accuracy of the resulting timing analysis.

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

Reset Synchronizer May Cause Design to Fail Timing

Systems generated with SOPC Builder or Qsys may fail timing closure due to paths that include a reset synchronizer.

Affected Configurations

This issue affects all configurations.

Design Impact

The design fails timing closure.

Workaround

A workaround for this issue is to apply the following constraint in the TimeQuest Timing Analyzer:

For SOPC Builder:

```
set_false_path -from {dut_sopc_top_reset_clk_0_domain_synch_module:
dut_sopc_top_reset_clk_0_domain_synch*}
```

For Qsys:

```
set_false_path -from *:rst_controller*|*:alt_rst_sync_uq1|
altera_reset_synchronizer_int_chain[*] -to *:controller_phy_inst|
*:memphy_top_inst|*:umemphy|*:ureset|*:ureset_*_clk|reset_reg[*]
```

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

Compilation Fails if Synthesis Fileset is Mixed with Example Project Files

Compilation fails if the **Files** list in the **Settings** dialog box in the Quartus II software includes files from both the example project located at <*working_dir*>/<*variation_name*>**_example_design_fileset/example_project/** and the synthesis fileset located at <*working_dir*>/<*variation_name*>.

Affected Configurations

This issue affects all configurations.

Design Impact

Compilation fails.

Workaround

A workaround for this issue is to perform the following steps:

1. In an editor, open the <*variation_name*>**_driver.sv** file, located in the <*working_dir*>/<*variation_name*>**_example_design_fileset/example_project/** directory.
2. In the <*variation_name*>**_driver.sv** file, change the entity name <*variation_name*>**_reset_sync** to <*variation_name*>_<*num*>**_reset_sync**, where *num* is the same value as in the <*variation_name*>_<*num*>**_reset_sync.v** filename in the <*working_dir*>/<*variation_name*>/ directory.

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

Warning Messages Displayed When Compiling for Stratix V Devices

When compiling a design for Stratix V devices, the system may display numerous PLL-related warning messages similar to the following:

```
Warning: PLL(s) placed in location FRACTIONALPLL_X0_Y1_N0 do not have a PLL
clock to compensate specified - the Fitter will attempt to compensate all
PLL

Warning: PLL(s) placed in location FRACTIONALPLL_X0_Y1_N0 use multiple
different clock network types - the PLL will compensate for output clocks

Warning: PLL cross checking found inconsistent PLL clock settings:

Warning: Node: mem_if|controller_phy_inst|memphy_top_inst|
pll1~FRACTIONAL_PLL|mcntout was found missing 1 generated clock that
corresponds to a base clock with a period of: 8.000
```

```
Warning: Clock: mem_if|ddr3_pll_write_clk was found on node:
mem_if|controller_phy_inst|memphy_top_inst|pll3|outclk with settings that
do not match the following PLL specifications:

Warning: -multiply_by (expected: 21, found: 4264000)

Warning: -divide_by (expected: 5, found: 1000000)

Warning: -phase (expected: 0.00, found: 90.00)
```

These warning messages are expected and can be ignored.

Affected Configurations

This issue affects all configurations targeting Stratix V devices.

Design Impact

This issue has no design impact.

Workaround

There is no workaround for this issue. You can safely ignore the error messages.

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

Cannot Launch MegaWizard Plug-In Manager by Opening Example Design

You cannot reopen your project in the MegaWizard Plug-In Manager by clicking on your generated IP instantiation **<***variation_name***>.v** in the **<***working_dir***>/<***variation_name***>_example_design_fileset/example_project/** directory.

Affected configurations

This issue affects all configurations.

Design Impact

This issue has no design impact.

Workaround

To reopen your project in the MegaWizard Plug-In Manager, follow these steps:

1. In the Quartus II software, click **MegaWizard Plug-In Manager** on the **Tools** menu.
2. Click **Edit an existing custom megafunction variation** and specify your project.

Solution Status

This issue will not be fixed.

Example Design May Not Compile for IP Cores from Earlier Versions

The example design provided with version 10.1 may not compile with IP cores migrated from earlier versions of the Quartus II software.

Affected configurations

This issue affects all configurations.

Design Impact

Attempting to compile the example design with IP cores migrated from earlier versions of the Quartus II software may fail with the following message:
`Error:instance “ureset_driver_clk” instantiates undefined entity “<variation_name>_reset_sync”`

Workaround

The workaround for this issue is to perform the following steps:

1. In the Quartus II software, open the **Settings** dialog box on the **Assignments** menu.
2. In the **Category** tree of the **Settings** dialog box, click **Files** to display the files list.
3. Remove all the UniPHY files, including the **.qip** file and example project files, from the migrated project assignments.
4. Add to the project the newly generated .**qip** file located in the **<***working_dir***>/<***variation_name***>_example_design_fileset** directory.
5. Add to the project all of the files except for the memory model, from the directory **<***working_dir***>/<***variation_name***>_example_design_fileset/example_project**.

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

Calibration Failure in Earlier Versions

Designs generated in version 10.0SP1 and earlier may experience calibration failure due to unreliable asynchronous signal transfer from the AFI clock domain to the read-capture clock domain.

Affected Configurations

This issue affects full-rate IP cores generated in version 10.0SP1 and earlier of the QDR II and QDR II+ SRAM Controller with UniPHY.

Design Impact

Designs fail in calibration.

Workaround

Open the design in version 10.1 of the QDR II and QDR II+ SRAM Controller with UniPHY and regenerate the design.

Solution Status

This issue is fixed in version 10.1 of the QDR II and QDR II+ SRAM Controller with UniPHY.

SOPC Builder-generated Systems Cannot Serve as Top-Level Design

Systems generated with SOPC Builder cannot serve as the top-level design, because SOPC Builder automatically exports the `parallelterminationcontrol` and `seriesterminationcontrol` OCT control signals as top-level ports, but these signals must not be exposed at the top level.

Affected configurations

This issue affects all configurations generated with SOPC Builder.

Design Impact

Compilation fails.

Workaround

Perform either of the following procedures to work around this issue:

- Create a top-level wrapper which instantiates the SOPC Builder-generated system, and does not make any connection to the `parallelterminationcontrol` or `seriesterminationcontrol` signals.

or

- Open the top-level SOPC Builder system file (for example, *system.v*), and delete the wire names from within the brackets for the `parallelterminationcontrol` and `seriesterminationcontrol` signals for all UniPHY cores. The resulting lines should appear as follows:

```
.parallelterminationcontrol ()
.seriesterminationcontrol ()
```

  The wire names that you delete from within the brackets must also be removed from all other locations in the top-level system file, including the top-level port list.

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

Higher Delays and Skews Expected for Corner I/Os in Stratix V Devices

In Stratix V devices, the corner I/O banks are expected to have higher core-to-I/O and I/O-to-core delay and skew values than the other I/O banks, and are unsuitable for interfacing with external memory at frequencies above 667 MHz.

The characteristics of the corner I/O banks are not yet reflected in the Stratix V timing models available in version 10.1 of the Quartus II software; consequently, timing analysis will not accurately characterize the performance of the corner I/Os.

Affected Configurations

This issue affects all configurations targeting Stratix V devices at frequencies above 667 MHz.

Design Impact

This issue can adversely affect timing.

Workaround

Avoid using the outer I/O banks at the upper and lower sides of the device.

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

Simulation Fails—PLL Clocks Out of Synchronization

During simulation, the PLL clocks lose synchronization.

Affected Configurations

This issue affects all designs.

Design Impact

This issue causes simulation failures.

Workaround

To work around this issue, follow these steps:

1. In text editor open the design file and remove the following line:

```
coverage exclude_file
```

In the ALTPLL MegaWizard interface, turn on **Create output files using the Advanced PLL parameters** and regenerate the PLL ().

Selecting VHDL Gives a Verilog HDL IP Core

If you select VHDL in the MegaWizard interface and generate a QDR II and QDR II+ SRAM Controller with UniPHY IP core, the generated core is in Verilog HDL.

Affected Configurations

This issue affects all VHDL designs.

Design Impact

The issue affects all VHDL designs.

Workaround

To generate a VHDL IP core follow these steps:

1. In a text editor open <*Quartus II directory*>**\ip\altera\uniphy\lib\altera_uniphy_qdrii_hw.tcl**.
2. Search for the string "LANGUAGE" that appears in the following code:

```
append param_str ",LANGUAGE=[get_generation_property HDL_LANGUAGE]"
```

3. Change this line to the following code:

```
append param_str ",LANGUAGE=vhdl"
```

4. Continue searching for the next occurence of the string "LANGUAGE" which appears in the following code:

```
if {[string compare -nocase [get_generation_property HDL_LANGUAGE]
verilog] == 0} {
   add_file ${outdir}/${outputname}.v {SYNTHESIS SUBDIR}
   puts $qipfile "set_global_assignment -name VERILOG_FILE \[file
join \$::quartus(qip_path) ${outputname}.v\]"
} else {
   add_file ${outdir}/${outputname}.vhd {SYNTHESIS SUBDIR}
   puts $qipfile "set_global_assignment -name VHDL_FILE \[file join
\$::quartus(qip_path) ${outputname}.vhd\]"
}
```

5. Comment out the if line, the else line, and the block of code in the conditional section so that the code in the "else" block always executes, similar to the following code:

```
# if {[string compare -nocase [get_generation_property HDL_LANGUAGE]
verilog] == 0} {
#    add_file ${outdir}/${outputname}.v {SYNTHESIS SUBDIR}
#   puts $qipfile "set_global_assignment -name VERILOG_FILE \[file
join \$::quartus(qip_path) ${outputname}.v\]"
# } else {
   add_file ${outdir}/${outputname}.vhd {SYNTHESIS SUBDIR}
   puts $qipfile "set_global_assignment -name VHDL_FILE \[file join
\$::quartus(qip_path) ${outputname}.vhd\]"
# }
```

6. Use the MegaWizard interface to generate a UniPHY-based IP core.

☞ To generate a Verilog HDL IP core, restore the original **altera_uniphy_qdrii_hw.tcl** file.

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY IP core.

BSF File Not Generated

The IP core does not generate a BSF file, and therefore is not compatible with workflows requiring a BSF file.

Affected Configurations

This issue affects all configurations.

Design Impact

Errors are likely to occur with workflows using the Schematic Editor or Symbol Editor.

Workaround

Do not use the Schematic Editor or the Symbol Editor with the IP core.

Solution Status

This issue is fixed in version 10.1 of the QDR II and QDR II+ SRAM Controller with UniPHY.

Global Signal Assignments Not Applied

The Fitter sometimes does not honor GLOBAL signal assignments applied by the `<variation_name>_pin_assignments.tcl` script.

Affected Configurations

This issue affects all configurations.

Design Impact

This issue has no impact on the correctness of the design, but can result in suboptimal resource placement and can contribute to difficulties in achieving timing closure.

Workaround

To determine whether GLOBAL assignments are properly applied, check the Fitter Report and verify whether any GLOBAL signal assignment referring to a PLL output port (for example, `...|auto_generated|clk[*]`) appears in the **Ignored Assignments** section.

If there is a GLOBAL assignment to a PLL output port listed in **Ignored Assignments**, you can correct the problem by running Analysis & Synthesis and then running the Fitter. You should then verify in the Fitter Report that the assignment is no longer ignored.

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

Simulation Error

Inconsistency between module definition and instantiation may cause some simulators to produce an error message.

Affected Configurations

This issues affects designs targeting Arria II GX devices.

Design Impact

Some simulators may issue an error message reporting that a given port is unknown.

Workaround

The workaround for this issue is to manually edit the `oct_control.v` and `clock_pair_generator_config.v` files, and remove specific port names from each, as described below:

Table 23–3. Port names to remove from `clock_pair_generator_config.v`

File:	<*variation_name*>/rtl/<*variation_name*>_clock_pair_generator_config.v
Module:	arriaii_pseudo_diff_out
Instance:	pseudo_diffa_0
Port names to remove:	.dtc .dtcbar .oebout .oeout .dtcin .oein

Table 23–4. Port names to remove from `oct_control.v`

File:	<*variation_name*>/rtl/<*variation_name*>_oct_control.v
Module:	arriaii_termination_logic
Instance:	sd2a_0
Port names to remove:	.scanout .s2pload .scanclk .scanenable .scanin .serdata

Solution Status

This issue is fixed in version 10.0SP1 of the QDR II and QDR II+ SRAM Controller with UniPHY.

Incorrect Clock Uncertainty

A clock uncertainty related to the read FIFO clocked by DQS can result in inaccurate setup and hold slack values.

Affected Configurations

This issue affects all configurations.

Design Impact

This issue can cause setup and hold slack values to be inaccurate.

Workaround

The workaround for this issue is to manually edit the PHY **.sdc** file located in the *<variation_name>*/constraints/ directory, and add the following two lines to the Multicycle Constraints section of the file:

```
set_max_delay -from *ddio_in_inst_regout* -0.05
set_min_delay -from *ddio_in_inst_regout* [expr -$tCYC + 0.05]
```

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

IP Core May Not Operate Below 167MHz

The IP core may not operate reliably at memory clock frequencies less than 167MHz.

Affected Configurations

This issue affects configurations targeting Stratix III or Stratix IV devices.

Design Impact

Designs targeting memory clock frequencies less than 167MHz may not function properly.

Workaround

Do not use the IP core at memory clock frequencies less than 167MHz for Stratix III or Stratix IV devices.

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

UniPHY DQS Clock Buffer Location

The DQS clock buffer location for the UniPHY can cause hold time violations when placed suboptimally. The Quartus II software may suboptimally place the DQS clock buffer on a global or dual-regional clock after reentering the FPGA, so that it can be routed to the write side of the read capture FIFO buffer.

Affected Configurations

The issue affects all configurations.

Design Impact

You may see hold time failures on the capture clocks in core logic.

Workaround

Create a location assignment on the buffer to the same edge as the memory interface (for example `EDGE_BOTTOM`).

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

IP Functional Simulation Model

The wizard-generated IP core functional simulation model (**.vho**) file for VHDL designs is functionally incorrect.

Affected Configurations

The issue affects all configurations.

Design Impact

You cannot use an IP core functional simulation model to simulate your design.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

No Link to User Guide from Wizard

The wizard does not have a link to the *QDR II and II+ SRAM Controller with UniPHY User Guide*.

Affected Configurations

The issue affects all configurations.

Design Impact

There is no design impact.

Workaround

Access the *QDR II and II+ SRAM Controller with UniPHY User Guide* from the Altera website.

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

Incorrect Operation of Waitrequest Signal

The IP core does not correctly assert the Avalon-MM `waitrequest` signal, when the interface is reset.

Affected Configurations

This issue affects designs that try and send Avalon-MM data to the interface while the interface is in reset.

Design Impact

As the interface does not assert `waitrequest` it does not observe Avalon-MM transactions sent to it while reset is asserted.

Workaround

The workaround for this issue is to not send Avalon-MM transactions to the interface while reset is asserted.

Solution Status

This issue is fixed in version 10.0 of the QDR II and QDR II+ SRAM Controller with UniPHY.

QDR II SRAM Emulated Mode

If you turn on **×36 emulated mode**, you must change the **CQ Width** to 2.

Affected Configurations

The issue affects all ×36 emualated designs.

Design Impact

There is no design impact.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the QDR II and QDR II+ SRAM Controller with UniPHY.

Revision History

Table 24–1 shows the revision history for the RapidIO MegaCore function.

For more information about the new features, refer to the *RapidIO MegaCore Function User Guide*.

Table 24–1. RapidIO MegaCore Function Revision History

Version	Date	Description
10.1 SP1	February 2011	Maintenance release
10.1	December 2010	■ Support for Qsys system integration tool ■ Read-only version of Port 0 Local AckID CSR
10.0 SP1	September 2010	Maintenance release
10.0	July 2010	■ Preliminary support for Cyclone IV GX devices. ■ Support for configurable number of link-request attempts to be sent before fatal error, after timeout on link-response ■ Support for order preservation between read and write requests that come in on the Avalon-MM interface ■ Removed support for Stratix GX devices
9.1 SP1	February 2010	Maintenance release
9.1	November 2009	■ Preliminary support for HardCopy IV GX and Cyclone III LS devices ■ Support for 5.0 Gbaud data rate ■ Support for order preservation between I/O write requests and DOORBELL requests ■ NWRITE_R completion indication ■ Post-reset ackID synchronization ■ Transceiver configuration using full transceiver MegaWizard interface

Errata

Table 24–2 shows the issues that affect the RapidIO MegaCore function v10.1 SP1, v10.1, v10.0 SP1, v10.0, v9.1 SP1, and v9.1.

Not all issues affect all versions of the RapidIO MegaCore function. Altera recommends upgrading to the latest available version of the MegaCore IP Library.

For Qsys and SOPC Builder errata, which might affect the RapidIO MegaCore function and other IP cores, refer to the *Quartus II Software Release Notes*.

Table 24–2. RapidIO MegaCore Function Errata (Part 1 of 2)

Added or Updated	Issue	Affected Version					
		10.1 SP1	10.1	10.0 SP1	10.0	9.1 SP1	9.1
15 Mar 11	Receive Buffer Can Overflow	✓	✓	✓	✓	—	—
15 Feb 11	Migration from SOPC Builder to Qsys Changes Port Names	✓	✓	—	—	—	—
	Warning Message Indicates Preliminary Support for Arria II GX Devices	Fixed	✓	—	—	—	—
	Parameter Values Modified in SOPC to Qsys Conversion	Fixed	✓	—	—	—	—
	Generation Stalls in Arria GX and Stratix II GX Designs	✓	✓	✓	✓	—	—
15 Jan 11	Cannot Regenerate RapidIO MegaCore Function with Read-only .qip File	✓	✓	✓	✓	✓	✓
15 Dec 10	Device and Assembly Register Values Might Lose MSBs	✓	✓	—	—	—	—
	Qsys Appears to Allow Larger Revision IDs Than are Implemented	✓	✓	—	—	—	—
	Some MegaCore Variations Return Incorrect Read Data	—	Fixed	✓	✓	✓	✓
	Some Cyclone III Designs Fail Hold Time Requirements in TimeQuest Timing Analyzer	—	Fixed	✓	✓	—	—
	Migrated Designs Automatically Set to Seven link-request Attempts	—	—	Fixed	✓	—	—
	Stratix II GX Transceiver Transmitter Buffer Power Does Not Regenerate Correctly	—	—	Fixed	✓	—	—
	Unsupported Input Clock Frequencies Available in RapidIO MegaWizard Interface	—	—	Fixed	✓	—	—
15 Aug 10	MegaWizard GUI Does Not Warn That Small Cyclone IV GX Devices Are Not Supported	✓	✓	✓	✓	—	—
15 Jul 10	The Demonstration Testbench May Fail for Some RapidIO Variations	✓	✓	✓	✓	—	—
	Incorrect cmu_pll_inclock_period in Stratix II GX and Arria GX Designs	✓	✓	✓	✓	—	—
	Critical Warning Displays if System Clock and Reference Clock Have Same Source	✓	✓	✓	✓	✓	✓
	Doorbell Response Packets are not Sent if Master Enable Bit is not Set	—	—	—	Fixed	✓	✓
	A link-request reset-device Sequence Can Be Ignored	—	—	—	Fixed	✓	✓
	Specific Variation With Transaction Ordering Enabled Requires Additional Logical Layer Modules	—	—	—	Fixed	✓	✓
	Some Variations Do Not Meet Timing Requirements	—	—	—	Fixed	✓	✓
1 Apr 10	Certain Changes Made in the RapidIO MegaWizard Interface are Ignored	✓	✓	✓	✓	✓	—
	Changes Made to the Reference Clock in the ALTGX MegaWizard Interface are Ignored	✓	✓	✓	✓	✓	✓
15 Feb 10	Starting Channel Number Resets When SOPC Builder is Closed	—	—	—	—	Fixed	✓
	Reception of a Small Packet Can Cause Counter Overflow in the Transport Layer Module	—	—	—	—	Fixed	✓

Table 24–2. RapidIO MegaCore Function Errata (Part 2 of 2)

Added or Updated	Issue	Affected Version					
		10.1 SP1	10.1	10.0 SP1	10.0	9.1 SP1	9.1
15 Nov 09	Some Variations With High Reference Clock Frequency Generate Critical Timing Warnings	✓	✓	✓	✓	✓	✓
01 Nov 08	Stratix IV Simulations May Fail With ModelSim 6.3g Compiler Optimizations Enabled	✓	✓	✓	✓	✓	✓

Receive Buffer Can Overflow

The Rx buffer in the Transport layer can overflow.

Affected Configurations

All RapidIO variations that instantiate a Transport layer.

Design Impact

Received packets may become corrupted in the Rx buffer.

Workaround

To avoid this issue, ensure that you do not fill the Rx buffer.

Solution Status

This issue will be fixed in a future version of the RapidIO MegaCore function.

Migration from SOPC Builder to Qsys Changes Port Names

When you migrate an SOPC Builder system that contains a RapidIO MegaCore function to a Qsys system, many of the RapidIO MegaCore function signal names change. Signal names that have the _<*variation*> suffix in the SOPC Builder system, instead have the suffix `_from_the_`<*variation*> or `_to_the_`<*variation*> in the Qsys system. The suffix for each signal depends on the signal direction.

The following signals are affected: `arxwlevel`, `atxovf`, `atxwlevel`, `buf_av0`, `buf_av1`, `buf_av2`, `buf_av3`, `char_err`, `ef_ptr`, `error_capture_destination_id`, `error_capture_ftype`, `error_capture_letter`, `error_capture_mbox`, `error_capture_msgseg_or_xmbox`, `error_capture_source_id`, `error_capture_ttype`, `error_detect_illegal_transaction_decode`, `error_detect_illegal_transaction_target`, `error_detect_message_error_response`, `error_detect_message_format_error`, `error_detect_message_request_timeout`, `error_detect_packet_response_timeout`, `error_detect_unsolicited_response`, `error_detect_unsupported_transaction`, `gxb_powerdown`, `gxbpll_locked`, `master_enable`, `multicast_event_rx`, `multicast_event_tx`, `packet_accepted`, `packet_cancelled`, `packet_crc_error`, `packet_not_accepted`, `packet_retry`, `packet_transmitted`, `port_error`, `port_initialized`, `rd`, `reconfig_clk`, `reconfig_fromgxb`, `reconfig_togxb`, `rx_errdetect`, `rx_packet_dropped`, `rxclk`, `rxgxbclk`, `symbol_error`, `td`, `txclk`.

Clock and reset signal renaming depends on the conduit names you provide in Qsys following the migration.

Affected Configurations

All RapidIO variations generated with the SOPC Builder flow and migrated to the Qsys system integration tool.

Design Impact

After migration of your design to the Qsys system integration tool, you must manually rename the affected signals in the RapidIO MegaCore function instantiation in the HDL code.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the RapidIO MegaCore function.

Warning Message Indicates Preliminary Support for Arria II GX Devices

The RapidIO MegaCore function v10.1 provides final support for Arria II GX devices. However, when your RapidIO MegaCore function targets an Arria II GX device, a warning message indicates support is only preliminary. This warning message is erroneous.

Affected Configurations

All RapidIO variations that target an Arria II GX device.

Design Impact

This issue has no design impact. You can ignore this warning message.

Workaround

This issue has no workaround.

Solution Status

This issue is fixed in version 10.1 SP1 of the RapidIO MegaCore function.

Parameter Values Modified in SOPC to Qsys Conversion

If you open an SOPC Builder system in Qsys to convert it to a Qsys system, every RapidIO MegaCore function instance in the system reverts to the default disabled value for the following parameters:

- **Port Write Tx Enable**
- **Port Write Rx Enable**
- **I/O read and write order preservation**

- **Prevent doorbell messages from passing write transactions**
- **Data Messages Source Operation**
- **Data Messages Destination Operation**

Affected Configurations

All RapidIO variations in a Qsys system created by converting an SOPC Builder system to Qsys, in which one or more of the preceding parameters is enabled.

Design Impact

A design based on a Qsys system created by conversion from an SOPC Builder system might not function correctly. It might have incorrect parameter values for these RapidIO MegaCore function parameters.

Workaround

To fix the problem in your system, after conversion, edit each RapidIO MegaCore function instance in your Qsys system, and set the parameters to the correct values.

Solution Status

This issue is fixed in version 10.1 SP1 of the RapidIO MegaCore function.

Generation Stalls in Arria GX and Stratix II GX Designs

When you attempt to generate a new RapidIO MegaCore function, or regenerate an existing RapidIO MegaCore function, generation stalls. A message indicates the MegaWizard is preparing to generate the MegaCore function. The issue is due to multiple running processes to generate transceiver IP cores.

Affected Configurations

RapidIO variations that target an Arria GX or Stratix II GX device.

Design Impact

These RapidIO variations do not generate or regenerate successfully.

Workaround

To avoid this issue, kill all your running `mega_altgxbq` processes, or reboot your computer.

Solution Status

This issue will be fixed in a future version of the RapidIO MegaCore function.

Cannot Regenerate RapidIO MegaCore Function with Read-only .qip File

If you try to edit or regenerate a RapidIO MegaCore function whose previously generated **.qip** file has permissions set to read-only, the MegaWizard Plug-in Manager hangs when trying to generate the new version of the MegaCore function.

Affected Configurations

This issue affects all RapidIO variations.

Design Impact

Under these circumstances, you cannot edit an existing RapidIO MegaCore function.

Workaround

To avoid this issue, modify the permissions for the RapidIO MegaCore function **.qip** file to ensure it is writable before editing the RapidIO MegaCore function.

Solution Status

This issue will be fixed in a future version of the RapidIO MegaCore function.

Device and Assembly Register Values Might Lose MSBs

In RapidIO variations that are generated with Qsys and target a device other than a Cyclone IV GX device, the device and assembly register (capability registers at offsets 0x00 to 0x0C) non-zero field values whose decimal (base 10) representation has four or fewer decimal digits are truncated such that the two most significant decimal digits are zeroed. Leftmost zero digits are ignored for purposes of this count. No warning message is generated.

In the case of the device revision ID field, the two leftmost decimal digits are truncated if the decimal representation has eight or fewer decimal digits, rather than four or fewer decimal digits.

For example, if the device revision ID is 0x5F54433, the decimal representation is 99,959,859. This representation has eight digits, so the two most significant digits are truncated, resulting in the decimal value 959859.

Affected Configurations

All RapidIO variations generated using Qsys that target a device other than a Cyclone IV GX device.

Design Impact

In an affected configuration, if a device or assembly register value has four or fewer significant decimal digits (leftmost zeroes are not counted), the actual configured register value is missing the two most significant decimal digits. In the case of the device revision ID, if the value has eight or fewer significant decimal digits, the actual configured register value is missing the two most significant decimal digits. In these cases, the device and assembly register values are incorrect.

Workaround

To correct this issue in your RapidIO MegaCore function, after you generate your Qsys system and before you compile, follow these steps:

1. Open the file <*sysdir*>**/synthesis/submodules/altera_rapidio_**<*variation_string*>**.v** in a text editor. <*sysdir*> is the output directory path you specify in Qsys, and <*variation_string*> is an arbitrary alphanumeric string generated by Qsys to specify your RapidIO variation.
2. Correct the values of the signals that correspond to the individual register fields according to the register-field signal-name correspondence shown in Table 24–3. Specify the correct hexadecimal value for each parameter.

Table 24–3. Signals that Correspond to Device and Assembly Register Fields

Register Field	Signal Name	Format of Corrected Value
Device ID	signal_wire10	16'hXXXX
Vendor ID	signal_wire11	16'hXXXX
Revision ID	signal_wire12	32'hXXXXXXXX
Assembly ID	signal_wire13	16'hXXXX
Assembly Vendor ID	signal_wire14	16'hXXXX
Assembly Revision ID	signal_wire15	16'hXXXX
Extended feature pointer	signal_wire16	16'hXXXX

Solution Status

This issue will be fixed in a future version of the RapidIO MegaCore function.

Qsys Appears to Allow Larger Revision IDs Than are Implemented

The RapidIO MegaCore function supports device revision ID values (values in the DEVICE_REV field of the Device Information CAR at offset 0x04 in the capability register space) from 0 to 0xFFFFFFFF, stored in a 32-bit word. The RapidIO parameter editor that appears when you include a RapidIO MegaCore function in your Qsys design shows the Revision ID as a 64-bit parameter. If you set the Revision ID to a value greater than 0xFFFFFFFF, only the least significant 32 bits are maintained, and no warning message is generated.

Affected Configurations

All RapidIO variations generated using Qsys.

Design Impact

If the user-configured device revision ID value is greater than 0xFFFFFFFF, the actual configured Revision ID value is different.

Workaround

Ensure that you configure the device revision ID parameter only with values between 0 and 0xFFFFFFFF, inclusive. However, refer to "Device and Assembly Register Values Might Lose MSBs" on page 24–6.

Solution Status

This issue will be fixed in a future version of the RapidIO MegaCore function.

Some MegaCore Variations Return Incorrect Read Data

When a 4× RapidIO MegaCore function at data rate 5.00 Gbaud with an 8-bit device ID responds to an Avalon-MM read request, it sets the value of `io_s_rd_readdata[63:48]` incorrectly.

Affected Configurations

All 4× RapidIO variations at data rate 5.00 Gbaud with an 8-bit device ID that implement an Input/Output Avalon-MM slave Logical layer module.

Design Impact

The two most significant bytes in each 8-byte read response datum from an affected RapidIO MegaCore function variation are not reliable.

Workaround

This issue has no known workaround.

Solution Status

This issue is fixed in version 10.1 of the RapidIO MegaCore function.

Some Cyclone III Designs Fail Hold Time Requirements in TimeQuest Timing Analyzer

RapidIO ×1 variations at data rate 3.125 Gbaud that target a Cyclone III device compile with a critical warning from the TimeQuest timing analyzer indicating that timing requirements are not met and worst-case hold slack is negative.

Affected Configurations

All RapidIO ×1 variations at data rate 3.125 Gbaud that target a Cyclone III device.

Design Impact

Because these variations do not meet timing requirements using the default place and route settings, a design that contains one of these variations does not operate properly.

Workaround

Turn on the fitter setting **Perform Clocking Topology Analysis During Routing** before compiling your RapidIO design.

Solution Status

This issue is fixed in version 10.1 of the RapidIO MegaCore function.

Migrated Designs Automatically Set to Seven link-request Attempts

The RapidIO MegaCore function provided with the Quartus II software release 9.1 SP2 and earlier declares a fatal error as soon as it detects a `link-request` to `link-response` timeout. The RapidIO MegaCore function provided starting with the Quartus II software release 10.0 allows you to specify the number of times such a timeout can be detected—and a subsequent `link-request reset-device` control symbol be sent— before declaring a fatal error. When an earlier RapidIO MegaCore function is migrated to version 10.0, the number of times the MegaCore function sends a `link-request reset-device` control symbol after detecting a timeout, before declaring a fatal error, should remain at its original default value of one, for backward compatibility. However, this number in migrated MegaCore functions erroneously defaults to seven.

Seven is the default number for a new RapidIO MegaCore function version 10.0, but should not be the number to which a migrated MegaCore function defaults.

Affected Configurations

All RapidIO variations in designs migrated from a previous release of the Quartus II software.

Design Impact

By default, migrated RapidIO MegaCore functions attempt to send the `link-request reset-device` control symbol as many as seven times following a `link-request` timeout. This setting can extend the duration of the error recovery process significantly.

Workaround

After you migrate your design, to change the number of `link-request` attempts to the expected value of one, open the MegaWizard interface for the RapidIO MegaCore function and set the **Link-request attempts** parameter to 1.

Solution Status

This issue is fixed in version 10.0 SP1 of the RapidIO MegaCore function.

Stratix II GX Transceiver Transmitter Buffer Power Does Not Regenerate Correctly

When you regenerate an existing RapidIO MegaCore function that use the high-speed transceivers on a Stratix II GX device, the transmitter buffer power (VCCH) reverts to the default value 1.2 V. The compiler complains about an invalid combination of I/O standard, common mode voltage, analog power voltage, and data rate.

Affected Configurations

All RapidIO variations that use the high-speed transceivers on a Stratix II GX device.

Design Impact

A design that contains one of these variations cannot compile successfully.

Workaround

To avoid this issue, perform the following workaround to regenerate the high-speed transceiver with the correct VCCH value:

1. In the Quartus II software, on the Tools menu, click **MegaWizard Plug-In Manager**.
2. In the MegaWizard Plug-In Manager, turn on **Edit an existing custom megafunction variation**.
3. Click **Next**.
4. In the File name field, select the file <*RapidIO_instance_name*>**.v**.
5. Click **Next**.
6. On the **Physical Layer** page, click **Configure Transceiver**.
7. In the transceiver MegaWizard interface, on the **Tx Analog** page, for **What is the transmitter buffer power (VCCH)?**, select the correct voltage.
8. Click **Finish**.
9. To regenerate the RapidIO MegaCore function high-speed transceiver with the issue resolved, click **Finish**.

   You can now compile your design without encountering this problem in your RapidIO MegaCore variation.

Solution Status

This issue is fixed in version 10.0 SP1 of the RapidIO MegaCore function.

Unsupported Input Clock Frequencies Available in RapidIO MegaWizard Interface

The RapidIO MegaWizard interface offers the following unsupported input clock frequencies for RapidIO MegaCore functions that target a Cyclone IV GX device:

- 78.125 MHz at data rate 1.250 Gbaud
- 78.125 MHz and 500 MHz at data rate 2.500 Gbaud
- 78.125 MHz, 97.65625 MHz, 195.3125 MHz, and 390.625 MHz at data rate 3.125 Gbaud

If you select one of these input clock frequencies, the closest supported input clock frequency is implemented in the RapidIO MegaCore function variation.

Affected Configurations

All RapidIO variations that target a Cyclone IV GX device.

Design Impact

The transceiver block in the RapidIO variation is configured with a different input clock frequency than the frequency you specified.

Workaround

Avoid selecting an unsupported input clock frequency in the RapidIO MegaWizard interface.

Solution Status

This issue is fixed in version 10.0 SP1 of the RapidIO MegaCore function.

MegaWizard GUI Does Not Warn That Small Cyclone IV GX Devices Are Not Supported

The RapidIO MegaCore function device support for Cyclone IV GX devices includes only the EP4CGX50, EP4CGX75, EP4CGX110, and EP4CGX150 devices. This restriction is not explained in the *RapidIO MegaCore Function User Guide*. In addition, the RapidIO MegaWizard interface does not enforce this restriction: if you specify another Cyclone IV GX device or allow the Quartus II software to automatically determine the device, RapidIO MegaCore function generation proceeds with no warning, but compilation fails.

Affected Configurations

RapidIO variations that target a Cyclone IV GX device, if the specific device is automatically determined by the Quartus II software, or is an EP4CGX15, EP4CGX22, or EP4CGX30 device.

Design Impact

These RapidIO variations do not compile successfully.

Workaround

To avoid this issue, target your Cyclone IV GX RapidIO MegaCore function to an EP4CGX50, EP4CGX75, EP4CGX110, or EP4CGX150 device.

Solution Status

The restriction is clarified in version 10.1 of the *RapidIO MegaCore Function User Guide*.

The Demonstration Testbench May Fail for Some RapidIO Variations

RapidIO variations that implement an Input/Output Avalon-MM master or slave Logical layer module and target a Stratix IV GX or Arria II GX device fail simulation with an error message indicating that a signal did not have expected value. The problem is due to an uninitialized RTL parameter in the IP functional simulation model.

Affected Configurations

RapidIO variations that implement an Input/Output Avalon-MM master or slave Logical layer module and target an Arria II GX or Stratix IV GX device.

Design Impact

These RapidIO variations cannot simulate successfully with the demonstration testbench.

Workaround

To avoid this issue, regenerate your IP functional simulation model with the `quartus_map` command-line option `SIMGEN_RAND_POWERUP_FFS=OFF`.

The following script provides this command for the DUT and the sister RIO in the testbench, for the case of a RapidIO MegaCore function variation that instantiates all modules. To use it to regenerate your IP functional simulation model, update the file names for your variation, modify the commands with the correct device and HDL, and remove the lines that reference modules your variation does not include.

Run the script, or enter the corresponding commands, in the directory that contains all the source files.

```
#!/bin/sh

#Modify the following lines with the correct device and HDL information.
#Parameter CBX_HDL_LANGUAGE=Verilog or VHDL
#Parameter --family is one of {stratixiv, arriaiigx, cycloneiv, arriagx,
stratixiigx}.

#Regenerate the IP functional simulation model for the DUT:
quartus_map --simgen \
          --simgen_parameter="CBX_HDL_LANGUAGE=Verilog,SIMGEN_RAND_POW
ER_UP_FFS=OFF" \
          --family=stratixiv \
          --source="./rio_rio.v" \
          --source="./rio_riophy_gxb.v" \
          --source="./rio_phy_mnt.v" \
          --source="./rio_riophy_xcvr.v" \
          --source="./rio_riophy_dcore.v" \
          --source="./rio_riophy_reset.v" \
          --source="./rio_concentrator.v" \
          --source="./rio_drbell.v" \
          --source="./rio_io_master.v" \
          --source="./rio_io_slave.v" \
          --source="./rio_maintenance.v" \
          --source="./rio_reg_mnt.v" \
          --source="./rio_transport.v" \
rio.v

# Continued on next page

#Regenerate the IP Functional Simulation Model for SISTER
cp rio_rio_sister.v rio_sister_rio.v
cp rio_riophy_gxb_sister.v rio_sister_riophy_gxb.v
quartus_map --simgen \
          --simgen_parameter="CBX_HDL_LANGUAGE=Verilog,SIMGEN_RAND_POW
ERUP_FFS=OFF" \
         --family=stratixiv \
         --source="./rio_sister_rio.v" \
         --source="./rio_sister_riophy_gxb.v" \
         --source="./rio_phy_mnt_sister.v" \
         --source="./rio_riophy_xcvr_sister.v" \
         --source="./rio_riophy_dcore_sister.v" \
         --source="./rio_riophy_reset_sister.v" \
         --source="./rio_concentrator_sister.v" \
         --source="./rio_drbell_sister.v" \
         --source="./rio_io_master_sister.v" \
```

```
        --source="./rio_io_slave_sister.v" \
        --source="./rio_maintenance_sister.v" \
        --source="./rio_reg_mnt_sister.v" \
        --source="./rio_transport_sister.v" \
rio_sister_rio.v
```

Solution Status

This issue will be fixed in a future version of the RapidIO MegaCore function.

Incorrect cmu_pll_inclock_period in Stratix II GX and Arria GX Designs

For RapidIO variations that use the high-speed transceivers on a Stratix II GX or Arria GX device, the transceiver `cmu_pll_inclock_period` value is set incorrectly.

Affected Configurations

RapidIO variations that use the high-speed transceivers on a Stratix II GX or Arria GX device.

Design Impact

Simulation and compilation fail for the affected configurations.

Workaround

In the file <*RapidIO instance name*>**_riophy_gxb.v**, in the assignment to the `alt2gxb_component.cmu_pll_inclock_period` signal, assign the value 10^6/<*`pll_inclk` frequency*> in place of the incorrect value.

To propagate the change to the IP functional simulation model, regenerate the model with the `quartus_map` command. Refer to the workaround for the erratum "The Demonstration Testbench May Fail for Some RapidIO Variations" on page 24–11 for the appropriate command-line options.

Solution Status

This issue will be fixed in a future version of the RapidIO MegaCore function.

Critical Warning Displays if System Clock and Reference Clock Have Same Source

If the system clock and the reference clock for your RapidIO MegaCore function are driven by the same source, the Quartus II software issues a critical warning.

Affected Configurations

All RapidIO variations in designs in which the RapidIO system clock and reference clock are driven by the same source.

Design Impact

This issue has no design impact. The critical warning can be ignored.

Workaround

You can avoid the critical warning by cutting some of the nodes in the Synopsys Design Constraints File (**.sdc**). To obtain an **.sdc** compatible list of the nodes to be cut, refer to Altera solution rd07132010_207 at www.altera.com/support/kdb/solutions/rd07132010_207.html.

Solution Status

This issue will be fixed in a future version of the RapidIO MegaCore function.

Doorbell Response Packets are not Sent if Master Enable Bit is not Set

If the Master Enable (`ENA`) bit of the `Port General Control` CSR (offset 0x13C) is not set, the Doorbell module does not send `DOORBELL` responses. The Doorbell module checks this signal before sending out any packets, including response packets.

Affected Configurations

All RapidIO variations that instantiate a Doorbell module.

Design Impact

All Doorbell requests sent to the RapidIO MegaCore function while the Master Enable bit is not set, receive no response and eventually time out.

Workaround

Ensure that the Master Enable (`ENA`) bit of the `Port General Control` CSR (offset 0x13C) is set.

Solution Status

This issue is fixed in version 10.0 of the RapidIO MegaCore function.

A link-request reset-device Sequence Can Be Ignored

If the third and fourth received `link-request` control symbols with `cmd` set to `reset-device` are separated by other incoming symbols such as a status control symbol or the IDLE sequence, the count of received `link-request reset-device` control symbols resets to zero, instead of triggering a device reset, with 50% probability.

Affected Configurations

All 4× RapidIO variations.

Design Impact

The RapidIO MegaCore function does not reset as expected.

Workaround

Send an additional four `link-request` control symbols with `cmd` set to `reset-device`.

Solution Status

This issue is fixed in version 10.0 of the RapidIO MegaCore function.

Specific Variation With Transaction Ordering Enabled Requires Additional Logical Layer Modules

Specific RapidIO variations with transaction ordering enabled (**Prevent doorbell messages from passing write transactions** is turned on in the RapidIO MegaWizard interface) require that the variation implement at least one of an Input/Output Avalon-MM master Logical layer module, or the receive functionality of the Doorbell module.

Affected Configurations

RapidIO ×4 variations at 5.0 Gbaud, for which you select **Prevent doorbell messages from passing write transactions** in the RapidIO MegaWizard interface, but for which you do not select **Doorbell Rx enable**, that do not implement an Input/Output Avalon-MM master Logical layer module.

Design Impact

A design that contains one of these variations does not operate properly.

Workaround

To avoid this issue, in the RapidIO MegaWizard interface, if you turn on **Prevent doorbell messages from passing write transactions**, you must also specify **Avalon-MM Master and Slave** in the **I/O Logical Layer Interfaces** field, or turn on **Doorbell Rx enable**.

Solution Status

This issue is fixed in version 10.0 of the RapidIO MegaCore function.

Some Variations Do Not Meet Timing Requirements

Some specific RapidIO MegaCore function variations that use the high-speed transceivers on an Arria II GX or Stratix IV GX device, cause the TimeQuest timing analyzer to issue critical timing warnings. For these variations, by default, the MegaWizard performs an incorrect internal parameter computation for the transceiver.

Affected Configurations

The following configurations have this issue:

- RapidIO ×4 variations at data rate 3.125 Gbaud with reference clock frequency 390.625 MHz, that use the high-speed transceivers on an Arria II GX or Stratix IV GX device.
- RapidIO ×1 and ×4 variations at data rate 5.0 Gbaud with reference clock frequency 500 MHz, that use the high-speed transceivers on a Stratix IV GX device.

Design Impact

Because these variations do not meet timing requirements, a design that contains one of these variations cannot compile successfully.

Workaround

To avoid this issue, perform the following workaround to regenerate the high-speed transceiver:

1. In the Quartus II software, on the Tools menu, click **MegaWizard Plug-In Manager**.
2. In the MegaWizard Plug-In Manager, turn on **Edit an existing custom megafunction variation**.
3. Click **Next**.
4. In the File name field, select the file <*RapidIO_instance_name*>**_riophy_gxb.v**.
5. Click **Next**.
6. To regenerate the RapidIO MegaCore function high-speed transceiver with the issue resolved, click **Finish**.

   You can now compile your design without encountering this problem in your RapidIO MegaCore variation.

Solution Status

This issue is fixed in version 10.0 of the RapidIO MegaCore function.

Certain Changes Made in the RapidIO MegaWizard Interface are Ignored

If you modify the data rate, reference clock frequency, or 1×/4× setting in an existing RapidIO MegaCore function using the RapidIO MegaWizard interface, and then generate the RapidIO MegaCore function, the transceiver is generated with the previous data rate, reference clock frequency, and 1×/4× setting. The change does not propagate to the ALTGX megafunction.

Affected Configurations

All RapidIO variations that use the built-in transceivers on the device they target.

Design Impact

The RapidIO MegaCore function data rate, reference clock frequency, and 1×/4× setting cannot be modified using the RapidIO MegaWizard interface.

Workaround

To change the data rate, reference clock frequency, or 1×/4× setting of an existing RapidIO MegaCore function, remove the existing RapidIO MegaCore function from your design, including deletion of its <*variation*>**_riophy_gxb.v** file, and then create a new RapidIO MegaCore function to replace it.

Solution Status

This issue will be fixed in a future version of the RapidIO MegaCore function.

Changes Made to the Reference Clock in the ALTGX MegaWizard Interface are Ignored

If you modify the reference clock frequency using the ALTGX MegaWizard interface, and then generate the RapidIO MegaCore function, the RapidIO MegaCore function is generated with the previous reference clock frequency.

Affected Configurations

All RapidIO variations that use the built-in transceivers on the device they target, except variations that target a Stratix GX device.

Design Impact

The RapidIO MegaCore function reference clock frequency cannot be set using the ALTGX MegaWizard interface.

Workaround

To avoid this issue in the RapidIO MegaCore function v9.1, set the reference clock frequency in the RapidIO MegaWizard interface. In the RapidIO MegaCore function v9.1 SP1, that solution is not available, and you must create a new RapidIO MegaCore function instead.

Solution Status

This issue will be fixed in a future version of the RapidIO MegaCore function.

Starting Channel Number Resets When SOPC Builder is Closed

If you regenerate an existing system in SOPC Builder, and that system includes a RapidIO MegaCore function with a non-default (non-zero) starting channel number, and you do not edit the RapidIO MegaCore function by configuring the transceiver to reset the starting channel number explicitly before you regenerate the SOPC Builder system, the RapidIO MegaCore function is generated with the default starting channel number 0.

Affected Configurations

All RapidIO variations that use the built-in transceivers on the device they target, except variations that target an Arria GX or a Stratix GX device.

Design Impact

The RapidIO MegaCore function starting channel number must be reset manually whenever you reopen your design in SOPC Builder, before you regenerate the SOPC Builder system.

Workaround

To reset the starting channel number for the transceiver in your RapidIO MegaCore function, after you open SOPC Builder and before you regenerate your SOPC Builder system, perform one of the following actions:

- In a text editor, open the file <*RapidIO instance_name*>**_riophy_gxb.v**, set the value of `starting_channel_number`, and save the file.
- Open the RapidIO MegaCore function in the SOPC Builder system by double-clicking the MegaCore function name, click **Configure Transceiver**, set the starting channel value to the desired value, and click **Finish**.

Solution Status

This issue is fixed in version 9.1 SP1 of the RapidIO MegaCore function.

Reception of a Small Packet Can Cause Counter Overflow in the Transport Layer Module

The reception of a 64-bit packet, such a response packet with 8-bit device IDs and without data, from the Physical layer, immediately after another packet, can cause the Transport layer packet counter to overflow and roll over to zero.

Affected Configurations

All RapidIO ×4 variations with 8-bit device IDs that implement a Transport layer and can receive 64-bit long packets.

Design Impact

If the counter rolls over to zero, the Rx buffer in the Transport layer appears empty until a new packet arrives. The empty indication may cause a temporary interruption in the transfer of a packet from the Transport layer to a Logical layer module. When the following packet arrives in the Transport layer, the packet-size information transmitted to the Logical layer modules is not synchronized correctly with the packet boundaries. The resulting erroneous packet sizes could cause Input/Output Avalon-MM Logical layer modules to reject valid packets, or to issue Avalon-MM transactions with incorrect burstcounts, among other possible events.

Workaround

To avoid this issue, perform the following workaround to modify the Transport layer counter behavior:

1. Generate the RapidIO MegaCore function using the MegaWizard interface.
2. In a text editor, open the generated Transport layer RTL file, <*variation_name*>**_transport.v**.
3. To increase the size of the counter, replace

```
reg [1:0] pktcnt, _Fpktcnt;
```

with

```
reg [2:0] pktcnt, _Fpktcnt;
```

4. To modify the Transport layer functionality to ensure it recognizes the counter value 4, perform one of the following actions to add `|| (pktcnt == 3'h4)` to the relevant condition:
   - If your RapidIO variation runs at 3.125 Gbaud per lane or slower, replace

```
if ((valid_data && srceop && (pktcnt == 2'h2 || just_got_eop)) ||
       (pktcnt == 2'h2 && (inc_pktcnt || inc_pktcnt_dly))      ||
       (pktcnt == 2'h3 && !(dec_pktcnt && !inc_pktcnt &&
!inc_pktcnt_dly))
) begin
```

   with

```
if ((valid_data && srceop && (pktcnt == 2'h2 || just_got_eop)) ||
       (pktcnt == 2'h2 && (inc_pktcnt || inc_pktcnt_dly))      ||
       (pktcnt == 2'h3 && !(dec_pktcnt && !inc_pktcnt &&
!inc_pktcnt_dly))
       || (pktcnt == 3'h4)
) begin
```

   - If your RapidIO variation runs at 5.0 Gbaud per lane, replace

```
if ((valid_data && srceop && (pktcnt_eq_2 || just_got_eop)) ||
       (pktcnt_eq_2 && pktcnt_flag1)                       ||
       (pktcnt_eq_3 && !(dec_pktcnt && pktcnt_flag2))
) begin
```

   with

```
if ((valid_data && srceop && (pktcnt_eq_2 || just_got_eop)) ||
       (pktcnt_eq_2 && pktcnt_flag1)                       ||
       (pktcnt_eq_3 && !(dec_pktcnt && pktcnt_flag2))
       || (pktcnt == 3'h4)
) begin
```

5. Save your changes and exit the text editor.

You can now compile and simulate your design without encountering this problem in your RapidIO MegaCore variation.

Solution Status

This issue is fixed in version 9.1 SP1 of the RapidIO MegaCore function.

Some Variations With High Reference Clock Frequency Generate Critical Timing Warnings

RapidIO MegaCore function variations with reference clock frequency higher than 260 MHz that target an Arria II GX or Stratix IV GX device cause the TimeQuest timing analyzer to issue the following critical warning:

```
Critical Warning: Found minimum pulse width or period violations. See
Report Minimum Pulse Width for details.
```

The warning occurs because the reference clock input pin is set to the 2.5 V I/O pin standard by default, and this I/O pin standard requires a minimum pulse width of 3.826 us, which corresponds to 260 MHz.

Affected Configurations

All RapidIO variations with reference clock frequency higher than 260 MHz that target an Arria II GX or Stratix IV GX device.

Design Impact

Designs that contain any of these RapidIO variations cannot compile with the default I/O standard assignments.

Workaround

To avoid this issue, in the Assignment Editor, assign the reference clock pin to the LVDS I/O standard.

Solution Status

This issue will be fixed in a future version of the RapidIO MegaCore function.

Stratix IV Simulations May Fail With ModelSim 6.3g Compiler Optimizations Enabled

Simulation of a RapidIO MegaCore function targeted to a Stratix IV device using ModelSim 6.3g with compiler optimizations enabled, may fail. Compiler optimizations are enabled by default in this version of ModelSim.

Affected Configurations

All RapidIO variations that target a Stratix IV device.

Design Impact

The IP functional simulation model of an affected configuration may produce data errors if simulated using ModelSim 6.3g.

Workaround

To avoid this issue, perform one of the following workarounds:

- Disable the ModelSim compiler optimizations by adding the `-novopt` switch to the `vsim` command, in the <*variant*>**_run_modelsim.tcl** script or when you call `vsim` from the command line.
- Use ModelSim 6.4a or later.

Solution Status

The issue is fixed in ModelSim 6.4a.

25. Reed-Solomon Compiler

Revision History

Table 25–1 shows the revision history for the Reed-Solomon Compiler.

For more information about the new features, refer to the *Reed-Solomon Compiler User Guide*.

Table 25–1. Reed-Solomon Compiler Revision History

Version	Date	Description
10.1	December 2010	■ Preliminary support for Arria II GZ devices. ■ Final support for Stratix IV GT devices.
10.0	July 2010	Preliminary support for Stratix V devices.
9.1	November 2009	■ Preliminary support for HardCopy IV GX, Stratix IV, and Cyclone III LS devices. ■ Withdrawn support for HardCopy family of devices.

Errata

Table 25–2 shows the issues that affect the Reed-Solomon Compiler v10.1, v10.0, and v9.1.

Not all issues affect all versions of the Reed-Solomon Compiler.

Table 25–2. Reed-Solomon Compiler Errata

Added or Updated	Issue	Affected Version		
		10.1	10.0	9.1
15 Mar 11	Compilation Targeting a Stratix V Device Fails	✓	—	—
01 Nov 08	Verilog HDL Simulation Fails	✓	✓	✓
	RS Decoder Fails When Number of Check Symbols and Symbols are Similar	✓	✓	✓

Compilation Targeting a Stratix V Device Fails

Designs that include a Reed-Solomon Compiler and target a Stratix V device, do not compile even if you have a valid license for the IP core. Refer to Altera solution rd03082011_116 at www.altera.com/support/kdb/solutions/rd03082011_116.html.

Affected Configurations

Reed-Solomon Compiler designs that target a Stratix V device.

Design Impact

Designs that include this IP core and target a Stratix V device cannot compile.

Workaround

To fix this issue, if you have a valid license for this IP core, follow these steps:

1. Upgrade your Quartus II software installation to the 10.1 Service Pack 1 version.
2. Apply Patch 1.19 to your Quartus II software installation.
3. Regenerate your IP core and any others in your design that are affected by this issue.
4. Recompile your design.

Solution Status

This issue will be fixed in a future version of the Quartus II software.

Verilog HDL Simulation Fails

Running a simulation with the Verilog HDL testbench results in an empty **summary_output.txt** file.

Affected Configurations

This issue affects all Verilog HDL configurations.

Design Impact

You cannot use the **summary_output.txt** file to evaluate the functionality of the design. But you can evaluate the functionality by looking at the simulation waveform.

Workaround

Run the simulation with a VHDL design and use the VHDL testbench.

Solution Status

This issue will be fixed in a future release of the Reed-Solomon Compiler.

RS Decoder Fails When Number of Check Symbols and Symbols are Similar

With the variable decoder, when the **Number of check symbols** and **Symbols per codeword** values are similar, for example, 5 and 6, respectively, the Avalon-ST interface on the source side fails and the `sop` and `eop` overlap.

Affected Configurations

This issue affects all Verilog HDL variable decoder designs.

Design Impact

The design fails simulation.

Workaround

To avoid this issue, create a VHDL design model and use the VHDL testbench.

Solution Status

This issue will be fixed in a future version of the Reed-Solomon Compiler.

26. Reed-Solomon II

Revision History

Table 26–1 shows the revision history for Reed-Solomon II.

For information about the new features, refer to the *Reed-Solomon II MegaCore Function User Guide*.

Table 26–1. Reed-Solomon II Revision History

Version	Date	Description
10.1	December 2010	First release.

Errata

Table 26–2 shows the issues that affect the Reed-Solomon II v10.1.

Not all issues affect all versions of the Reed-Solomon II.

Table 26–2. Reed-Solomon II Errata

Added or Updated	Issue	Affected Version
		10.1
15 December 2010	Backpressure Feature is Not Supported	✓
	Unsupported Variants	✓
	Unable to Support Invalid Avalon-ST Packets	✓

Backpressure Feature is Not Supported

Backpressure feature is not supported for 10.1 software release.

Affected Configurations

This issue affects all Reed-Solomon II encoder and decoder variations.

Design Impact

The core may generate erroneous output if it is backpressured. For example, `out_ready` signal is toggled.

Workaround

Set the `out_ready` signal high.

Solution Status

This issue will be fixed in a future version of the Reed-Solomon II MegaCore function.

Unsupported Variants

Variants other than the ones targeted for OTN (Optical Transport Network) applications are not fully supported in 10.1 software.

Affected Configurations

This issue affects all Reed-Solomon II encoder and decoder variations except for the following variants:

- N=255, CHECK=16, CHANNEL=1 IRRPOL=285
- N=255, CHECK=16, CHANNEL=2 IRRPOL=285
- N=255, CHECK=16, CHANNEL=8 IRRPOL=285

Design Impact

The core might generate erroneous output for all affected variants.

Workaround

Use non-affected configurations only.

Solution Status

This issue will be fixed in a future version of the Reed-Solomon II MegaCore function.

Unable to Support Invalid Avalon-ST Packets

The Reed-Solomon II encoder and decoder are unable to suppot Avalon-ST packets (codewords) that contain invalid data.

Affected Configurations

This issue affects all Reed-Solomon II encoder and decoder variations.

Design Impact

The core might generate erroneous output if `in_valid` signal is toggled during a codeword transmission.

Workaround

To avoid this problem, use only codewords with continuous valid data.

Solution Status

This issue will be fixed in a future version of the Reed-Solomon II MegaCore function.

27. RLDRAM II

Revision History

Table 27–1 shows the revision history for the RLDRAM II MegaCore function.

For more information about the new features, refer to the *RLDRAM II MegaCore Function User Guide*.

Table 27–1. RLDRAM II MegaCore Function Revision History

Version	Date	Description
10.1	December 2010	Maintenance release.
10.0	July 2010	Maintenance release.
9.1	November 2009	Maintenance release.
9.0 SP2	July 2009	Maintenance release.
9.0 SP1	May 2009	Maintenance release.
9.0	March 2009	Maintenance release.
8.1	15 November 2008	Maintenance release.

Errata

Table 27–2 shows the issues that affect the RLDRAM II MegaCore function v10.1, 10.0, and 9.1.

Not all issues affect all versions of the RLDRAM II MegaCore function.

Table 27–2. RLDRAM II MegaCore Function Errata

Added or Updated	Issue	Affected Version		
		10.1	10.0	9.1
15 Nov 09	The Quartus II Design Assistant Reports Critical Warning	✓	✓	✓
	Hold Timing Violation	✓	✓	✓
01 Dec 06	NativeLink Fails with the ModelSim Simulator	✓	✓	✓
01 Nov 06	Add an RLDRAM II Controller to a Project with Other Memory Controllers	✓	✓	✓
	Simulating with the NCSim Software	✓	✓	✓
	Simulating with the VCS Simulator	✓	✓	✓
	Multiple Instances of the auk_ddr_functions.vhd File	✓	✓	✓
	Gate-Level Simulation Filenames	✓	✓	✓
	Unpredictable Results for Gate-Level Simulations (HardCopy II Devices Only)	✓	✓	✓
	Editing the Custom Variation (non-DQS Mode)	✓	✓	✓

The Quartus II Design Assistant Reports Critical Warning

When you compile a design with the RLDRAM II controller, the Quartus II Design Assistant reports design the following warnings:

```
Critical Warning: (High) Rule R101: Combinational logic used as a reset signal should be synchronized. Found 1 node(s) related to this rule.
```

```
Warning: (Medium) Rule C104: Clock signal source should drive only clock input ports. Found 2 nodes related to this rule.
```

Affected Configurations

This issue affects all configurations.

Design Impact

There is no design impact.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller MegaCore function.

Hold Timing Violation

Hold timing violation occurs on the DQS clock reported in fast-corner timing report.

Affected Configurations

This issue affects all configurations.

Design Impact

There is no design impact.

Workaround

Disable the global clock promotion on `dqs_clk` by adding the following assignment in the Quartus II settings file (**.qsf**):

```
set_instance_assignment -name GLOBAL_SIGNAL OFF -to "<variation name>_wrapper:<variation name>|<variation name>_auk_rldramii_datapath:rldramii_io|<variation name>_auk_rldramii_dqs_group:auk_rldramii_dqs_group_*|dqs_clk[0]"
```

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller MegaCore function.

NativeLink Fails with the ModelSim Simulator

When using NativeLink to run VHDL gate-level simulations using the ModelSim software, the simulation fails with the following error message:

```
# ** Error: (vcom-19) Failed to access library 'altera' at "altera".
```

Affected Configurations

The issue affects VHDL gate-level simulations.

Design Impact

The design does not simulate.

Workaround

The following lines need to be added to the NativeLink-generated gate-level simulation script:

```
vlib vhdl_libs/altera
vmap altera vhdl_libs/altera
vcom -work altera <Quartus installation
directory>/libraries/vhdl/altera/altera_europa_support_lib.vhd
```

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller MegaCore function.

Add an RLDRAM II Controller to a Project with Other Memory Controllers

If you try to generate a new RLDRAM II controller in a project that already contains a DDR, DDR2, QDRII, or RLDRAM II controller, the example design gets corrupted and the compilation fails.

Affected Configurations

This issue affects all configurations.

Design Impact

The design does not compile.

Workaround

To work around this issue, follow these steps:

1. Generate the RLDRAM II controller in a new project and update the required project to instantiate the new RLDRAM II controller.
2. Copy the constraints from the new RLDRAM II project to the target project.
3. Copy the new RLDRAM II design files into the target project directory.

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller MegaCore function.

Simulating with the NCSim Software

The RLDRAM II Controller MegaCore function does not fully support the NCSim software.

Affected Configurations

This issue affects all configurations.

Design Impact

The design does not simulate.

Workaround

Set the `-relax` switch for all calls to the VHDL or Verilog HDL analyzer.

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller MegaCore function.

Simulating with the VCS Simulator

The RLDRAM II Controller MegaCore function does not fully support the VCS simulator.

Affected Configurations

This issue affects all configurations.

Design Impact

The design does not simulate.

Workaround

For VHDL simulations, in the <*variation name*>**_example_driver.vhd** file, change all `when` statements from:

```
when std_logic_vector'("<bit_pattern>")
```

to:

```
when "<bit_pattern>"
```

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller MegaCore function.

Multiple Instances of the auk_ddr_functions.vhd File

When a project contains multiple memory MegaCore functions, the Quartus II project has multiple instances of the **auk_ddr_functions.vhd** file (one per MegaCore function).

Affected Configurations

This issue affects all configurations.

Design Impact

The Quartus II project fails during compilation.

Workaround

Remove the **auk_ddr_functions.vhd** file associated with the RLDRAM II controller from the list of files added to the Quartus II project, by choosing **Add/Remove Files from Project** on the Project menu. Keep only the **auk_ddr_functions.vhd** file associated with the DDR or DDR2 SDRAM controller.

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller MegaCore function.

Gate-Level Simulation Filenames

Various Quartus II software options may cause the Quartus II software to generate a netlist with a different filename than that expected by the gate-level simulation script. The simulation script expects <*project name*>**.vho** or .**vo** and <*project name*>**_v** or **_vhd.sdo** files to be present.

Affected Configurations

This issue affects all configurations.

Design Impact

You cannot run gate-level simulations.

Workaround

For VHDL gate-level simulations, in the **simulation/modelsim** directory, follow these steps:

1. Rename <*filename*>**.vho** file to <*project name*>**.vho.**
2. Rename <*filename*>**.sdo** file to <*project name*>**_vhd.sdo**.

For Verilog HDL gate-level simulations, in the **simulation/modelsim** directory, follow these steps:

1. Rename the <*filename*>**.vo** file to <*project name*>**.vo.**
2. Rename the <*filename*>**.sdo** file to <*project name*>**_v.sdo**.
3. In the <*project name*>.**vo** file, change the following line to point to the <*project name*>**_v.sdo** file:

```
initial $sdf_annotate("<project name>_v.sdo");
```

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller MegaCore function.

Unpredictable Results for Gate-Level Simulations (HardCopy II Devices Only)

Gate-level simulations may not work as expected on HardCopy II devices, because HardCopy II timing is preliminary in the Quartus II software.

Affected Configurations

This issue affects all configurations on HardCopy II devices.

Design Impact

This issue has no design impact.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the Quartus II software.

Editing the Custom Variation (non-DQS Mode)

When you generate a non-DQS mode custom variation with large databus widths, you may encounter one of the following characteristics when you try to edit the custom variation:

- IP Toolbench does not reload
- IP Toolbench reloads, but the databus width and constraints are set to the default for the selected RLDRAM II device
- IP Toolbench reloads, but the databus width is set to the default value for the selected RLDRAM II device and the constraints floorplan shows no chosen byte groups

Affected Configurations

This issue affects non-DQS mode designs only.

Design Impact

This issue has no design impact if you implement the workaround.

Workaround

Use one of the following workarounds:

- If IP Toolbench does not reload, you must regenerate a new custom variation and re-enter your parameters

- If IP Toolbench reloads, but the databus width and constraints are set to the default, reselect the databus width and rechoose the byte groups in the constraints floorplan
- If IP Toolbench reloads, but the databus width is set to the default and the constraints floorplan shows no byte groups, reselect the databus width and rechoose the byte groups in the constraints floorplan

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller MegaCore function.

28. RLDRAM II Controller with UniPHY

Revision History

Table 28–1 shows the revision history for the RLDRAM II Controller with UniPHY.

For more information about the new features, refer to the *RLDRAM II Controller with UniPHY User Guide*.

Table 28–1. RLDRAM II Controller with UniPHY Revision History

Date	Version	Description
December 2010	10.1	■ Added preliminary support for Arria II GZ and Stratix V. ■ Added new generated directory structure. ■ Added new OCT Sharing Interface feature. ■ Added External Memory Interface Toolkit.
July 2010	10.0	■ Added width expansion feature. ■ Added error detection parity feature. ■ Added user-controlled refresh feature. ■ Added variable latency feature.
November 2009	9.1	First release.

Errata

Table 28–2 shows the issues that affect the RLDRAM II Controller with UniPHY v10.1, v10.0, and v9.1.

Not all issues affect all versions of the RLDRAM II Controller with UniPHY.

Table 28–2. RLDRAM II Controller with UniPHY Errata (Part 1 of 2)

Added or Updated	Issue	Affected Versions		
		10.1	10.0	9.1
15 Mar 11	VHDL-only Simulation Not Supported	✓	—	—

Table 28–2. RLDRAM II Controller with UniPHY Errata (Part 2 of 2)

Added or Updated	Issue	Affected Versions		
		10.1	10.0	9.1
15 Dec 10	NativeLink Simulation fails for VHDL Output	✓	—	—
	NativeLink Simulation fails for VHDL Output	—	✓	—
	Timing-related Warning Messages When Sharing PLLs on Stratix V Devices	✓	—	—
	Reset Synchronizer May Cause Design to Fail Timing	✓	—	—
	Compilation Fails if Synthesis Fileset is Mixed with Example Project Files	✓	—	—
	Warning Messages Displayed When Compiling for Stratix V Devices	✓	—	—
	Cannot Launch MegaWizard Plug-In Manager by Opening Example Design	✓	—	—
	Example Design May Not Compile for IP Cores from Earlier Versions	✓	—	—
	Calibration Failure in Earlier Versions	✓	—	—
	SOPC Builder-generated Systems Cannot Serve as Top-Level Design	✓	—	—
	Higher Delays and Skews Expected for Corner I/Os in Stratix V Devices	✓	—	—
15 Sept 10	Simulation Fails—PLL Clocks Out of Synchronization	✓	✓	—
15 Aug 10	Selecting VHDL Gives a Verilog HDL IP Core	✓	✓	—
	Incorrect Clock Uncertainty	✓	✓	—
15 Jul 10	BSF File Not Generated	Fixed	✓	—
	Global Signal Assignments Not Applied	✓	✓	—
15 Nov 09	UniPHY DQS Clock Buffer Location	✓	✓	✓
	IP Functional Simulation Model	Fixed	✓	✓
	No Link to User Guide from Wizard	✓	✓	✓
	Incorrect Operation of Waitrequest Signal	—	Fixed	✓
	User Guide States Support for ×72 Devices	—	Fixed	✓
	–18 Presets Give Errors	✓	✓	✓
	tQKH Parameter Incorrect	—	Fixed	✓

VHDL-only Simulation Not Supported

VHDL-only simulation is not supported in version 10.1 of the RLDRAM II Controller with UniPHY.

Affected Configurations

This issue affects all designs.

Design Impact

The simulation fails.

Workaround

The workaround for this issue is to use a mixed Verilog-VHDL simulator.

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller with UniPHY.

NativeLink Simulation fails for VHDL Output

In version 10.1 of the Quartus II software, when a user specifies VHDL output for the RLDRAM II Controller with UniPHY and attempts to simulate using NativeLink, NativeLink fails and reports that it cannot find the file **<***design_name***>.vho** in the top-level directory.

Affected Configurations

This issue affects all VHDL designs.

Design Impact

The simulation fails.

Workaround

The workaround for this issue is to not use NativeLink for simulations of VHDL designs, but to set up simulation manually instead.

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller with UniPHY.

NativeLink Simulation fails for VHDL Output

In version 10.0 of the Quartus II software, when a user specifies VHDL output for the RLDRAM II Controller with UniPHY and attempts to simulate using NativeLink, NativeLink fails and reports that it cannot find the file **<***design_name***>.vho** in the top-level directory.

Affected Configurations

This issue affects all VHDL designs.

Design Impact

The simulation fails.

Workaround

The workaround for this issue is to edit the **<***design_name***>.vhd** file and remove the line similar to the following:

```
-- IPFS_FILES : <design_name>.vho
```

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller with UniPHY.

Timing-related Warning Messages When Sharing PLLs on Stratix V Devices

When instantiating a design in PLL/DLL slave mode on a Stratix V device, the TimeQuest Timing Analyzer may display warning messages similar to the following:

```
Warning: Ignored filter at slave_report_timing_core.tcl(176):
slave_inst0|controller_phy_inst|memphy_top_inst|umemphy|uio_pads|
dq_ddio[1].ubidir_dq_dqs|altdq_dqs2_inst|thechain|clkin could not be
matched with a keeper or register or port or pin or cell or net
```

```
Warning: Command get_path failed
```

Affected Configurations

This issue affects Stratix V designs instantiated in PLL/DLL slave mode.

Design Impact

The resulting timing analysis is incorrect.

Workaround

This issue has no workaround. The warning messages can be safely ignored; however, do not rely on the accuracy of the resulting timing analysis.

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller with UniPHY.

Reset Synchronizer May Cause Design to Fail Timing

Systems generated with SOPC Builder or Qsys may fail timing closure due to paths that include a reset synchronizer.

Affected Configurations

This issue affects all configurations.

Design Impact

The design fails timing closure.

Workaround

A workaround for this issue is to apply the following constraint in the TimeQuest Timing Analyzer:

For SOPC Builder:

```
set_false_path -from {dut_sopc_top_reset_clk_0_domain_synch_module:
dut_sopc_top_reset_clk_0_domain_synch*}
```

For Qsys:

```
set_false_path -from *:rst_controller*|*:alt_rst_sync_uq1|
altera_reset_synchronizer_int_chain[*] -to *:controller_phy_inst|
*:memphy_top_inst|*:umemphy|*:ureset|*:ureset_*_clk|reset_reg[*]
```

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller with UniPHY.

Compilation Fails if Synthesis Fileset is Mixed with Example Project Files

Compilation fails if the **Files** list in the **Settings** dialog box in the Quartus II software includes files from both the example project located at <*working_dir*>/<*variation_name*>**_example_design_fileset/example_project/** and the synthesis fileset located at <*working_dir*>/<*variation_name*>.

Affected Configurations

This issue affects all configurations.

Design Impact

Compilation fails.

Workaround

A workaround for this issue is to perform the following steps:

1. In an editor, open the <*variation_name*>**_driver.sv** file, located in the <*working_dir*>/<*variation_name*>**_example_design_fileset/example_project/** directory.
2. In the <*variation_name*>**_driver.sv** file, change the entity name <*variation_name*>**_reset_sync** to <*variation_name*>**_**<*num*>**_reset_sync**, where *num* is the same value as in the <*variation_name*>**_**<*num*>**_reset_sync.v** filename in the <*working_dir*>/<*variation_name*>/ directory.

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller with UniPHY.

Warning Messages Displayed When Compiling for Stratix V Devices

When compiling a design for Stratix V devices, the system may display numerous PLL-related warning messages similar to the following:

```
Warning: PLL(s) placed in location FRACTIONALPLL_X0_Y1_N0 do not have a PLL
clock to compensate specified - the Fitter will attempt to compensate all
PLL

Warning: PLL(s) placed in location FRACTIONALPLL_X0_Y1_N0 use multiple
different clock network types - the PLL will compensate for output clocks

Warning: PLL cross checking found inconsistent PLL clock settings:

Warning: Node: mem_if|controller_phy_inst|memphy_top_inst|
pll1~FRACTIONAL_PLL|mcntout was found missing 1 generated clock that
corresponds to a base clock with a period of: 8.000
```

```
Warning: Clock: mem_if|ddr3_pll_write_clk was found on node:
mem_if|controller_phy_inst|memphy_top_inst|pll3|outclk with settings that
do not match the following PLL specifications:

Warning: -multiply_by (expected: 21, found: 4264000)

Warning: -divide_by (expected: 5, found: 1000000)

Warning: -phase (expected: 0.00, found: 90.00)
```

These warning messages are expected and can be ignored.

Affected Configurations

This issue affects all configurations targeting Stratix V devices.

Design Impact

This issue has no design impact.

Workaround

There is no workaround for this issue. You can safely ignore the error messages.

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller with UniPHY.

Cannot Launch MegaWizard Plug-In Manager by Opening Example Design

You cannot reopen your project in the MegaWizard Plug-In Manager by clicking on your generated IP instantiation **<***variation_name***>.v** in the **<***working_dir***>/<***variation_name***>_example_design_fileset/example_project/** directory.

Affected configurations

This issue affects all configurations.

Design Impact

This issue has no design impact.

Workaround

To reopen your project in the MegaWizard Plug-In Manager, follow these steps:

1. In the Quartus II software, click **MegaWizard Plug-In Manager** on the **Tools** menu.
2. Click **Edit an existing custom megafunction variation** and specify your project.

Solution Status

This issue will not be fixed.

Example Design May Not Compile for IP Cores from Earlier Versions

The example design provided with version 10.1 may not compile with IP cores migrated from earlier versions of the Quartus II software.

Affected configurations

This issue affects all configurations.

Design Impact

Attempting to compile the example design with IP cores migrated from earlier versions of the Quartus II software may fail with the following message:
`Error:instance "ureset_driver_clk" instantiates undefined entity "<variation_name>_reset_sync"`

Workaround

The workaround for this issue is to perform the following steps:

1. In the Quartus II software, open the **Settings** dialog box on the **Assignments** menu.
2. In the **Category** tree of the **Settings** dialog box, click **Files** to display the files list.
3. Remove all the UniPHY files, including the **.qip** file and example project files, from the migrated project assignments.
4. Add to the project the newly generated .**qip** file located in the **<***working_dir***>/<***variation_name***>_example_design_fileset** directory.
5. Add to the project all of the files except for the memory model, from the directory **<***working_dir***>/<***variation_name***>_example_design_fileset/example_project**.

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller with UniPHY.

Calibration Failure in Earlier Versions

Designs generated in version 10.0SP1 and earlier may experience calibration failure due to unreliable asynchronous signal transfer from the AFI clock domain to the read-capture clock domain.

Affected Configurations

This issue affects full-rate IP cores generated in version 10.0SP1 and earlier of the RLDRAM II Controller with UniPHY.

Design Impact

Designs fail in calibration.

Workaround

Open the design in version 10.1 of the RLDRAM II Controller with UniPHY and regenerate the design.

Solution Status

This issue is fixed in version 10.1 of the RLDRAM II Controller with UniPHY.

SOPC Builder-generated Systems Cannot Serve as Top-Level Design

Systems generated with SOPC Builder cannot serve as the top-level design, because SOPC Builder automatically exports the `parallelterminationcontrol` and `seriesterminationcontrol` OCT control signals as top-level ports, but these signals must not be exposed at the top level.

Affected configurations

This issue affects all configurations generated with SOPC Builder.

Design Impact

Compilation fails.

Workaround

Perform either of the following procedures to work around this issue:

- Create a top-level wrapper which instantiates the SOPC Builder-generated system, and does not make any connection to the `parallelterminationcontrol` or `seriesterminationcontrol` signals.

or

- Open the top-level SOPC Builder system file (for example, *system.v*), and delete the wire names from within the brackets for the `parallelterminationcontrol` and `seriesterminationcontrol` signals for all UniPHY cores. The resulting lines should appear as follows:

```
.parallelterminationcontrol ()
.seriesterminationcontrol ()
```

  The wire names that you delete from within the brackets must also be removed from all other locations in the top-level system file, including the top-level port list.

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller with UniPHY.

Higher Delays and Skews Expected for Corner I/Os in Stratix V Devices

In Stratix V devices, the corner I/O banks are expected to have higher core-to-I/O and I/O-to-core delay and skew values than the other I/O banks, and are unsuitable for interfacing with external memory at frequencies above 667 MHz.

The characteristics of the corner I/O banks are not yet reflected in the Stratix V timing models available in version 10.1 of the Quartus II software; consequently, timing analysis will not accurately characterize the performance of the corner I/Os.

Affected Configurations

This issue affects all configurations targeting Stratix V devices at frequencies above 667 MHz.

Design Impact

This issue can adversely affect timing.

Workaround

Avoid using the outer I/O banks at the upper and lower sides of the device.

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller with UniPHY.

Simulation Fails—PLL Clocks Out of Synchronization

During simulation, the PLL clocks lose synchronization.

Affected Configurations

This issue affects all designs.

Design Impact

This issue causes simulation failures.

Workaround

To work around this issue, follow these steps:

1. In text editor open the design file and remove the following line:

   ```
   coverage exclude_file
   ```

2. In the ALTPLL MegaWizard interface, turn on **Create output files using the Advanced PLL parameters** and regenerate the PLL ().

Selecting VHDL Gives a Verilog HDL IP Core

If you select VHDL in the MegaWizard interface and generate an RLDRAM II controller with UniPHY IP core, the generated core is in Verilog HDL.

Affected Configurations

This issue affects all VHDL designs.

Design Impact

The issue affects all VHDL designs.

Workaround

To generate a VHDL IP core follow these steps:

1. In a text editor open <*Quartus II directory*>**\ip\altera\uniphy\lib\altera_uniphy_rldramii_hw.tcl**.
2. Search for the string `"LANGUAGE"` that appears in the following code:

   ```
   append param_str ",LANGUAGE=[get_generation_property HDL_LANGUAGE]"
   ```

3. Change this line to the following code:

```
append param_str ",LANGUAGE=vhdl"
```

4. Continue searching for the next occurence of the string "LANGUAGE" which appears in the following code:

```
if {[string compare -nocase [get_generation_property HDL_LANGUAGE]
verilog] == 0} {
   add_file ${outdir}/${outputname}.v {SYNTHESIS SUBDIR}
   puts $qipfile "set_global_assignment -name VERILOG_FILE \[file
join \$::quartus(qip_path) ${outputname}.v\]"
} else {
   add_file ${outdir}/${outputname}.vhd {SYNTHESIS SUBDIR}
   puts $qipfile "set_global_assignment -name VHDL_FILE \[file join
\$::quartus(qip_path) ${outputname}.vhd\]"
}
```

5. Comment out the if line, the else line, and the block of code in the conditional section so that the code in the "else" block always executes, similar to the following code:

```
# if {[string compare -nocase [get_generation_property HDL_LANGUAGE]
verilog] == 0} {
#    add_file ${outdir}/${outputname}.v {SYNTHESIS SUBDIR}
#    puts $qipfile "set_global_assignment -name VERILOG_FILE \[file
join \$::quartus(qip_path) ${outputname}.v\]"
# } else {
   add_file ${outdir}/${outputname}.vhd {SYNTHESIS SUBDIR}
   puts $qipfile "set_global_assignment -name VHDL_FILE \[file join
\$::quartus(qip_path) ${outputname}.vhd\]"
# }
```

6. Use the MegaWizard interface to generate a UniPHY-based IP core.

☞ To generate a Verilog HDL IP core, restore the original **altera_uniphy_rldramii_hw.tcl** file.

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller with UniPHY IP core.

Incorrect Clock Uncertainty

A clock uncertainty related to the read FIFO clocked by DQS can result in inaccurate setup and hold slack values. The solution described in the 15 July 2010 version of the MegaCore IP Library Release Notes and Errata contained an error which this solution corrects.

Affected Configurations

This issue affects all configurations.

Design Impact

This issue can cause setup and hold slack values to be inaccurate.

Workaround

The workaround for this issue is to manually edit the PHY **.sdc** file located in the *<variation_name>*/constraints/ directory, and add the following two lines to the Multicycle Constraints section of the file:

```
set_max_delay -from *ddio_in_inst_regout* -0.05
set_min_delay -from *ddio_in_inst_regout* [expr -$t(CK) + 0.05]
```

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller with UniPHY.

BSF File Not Generated

The IP core does not generate a BSF file, and therefore is not compatible with workflows requiring a BSF file.

Affected Configurations

This issue affects all configurations.

Design Impact

Errors are likely to occur with workflows using the Schematic Editor or Symbol Editor.

Workaround

Do not use the Schematic Editor or the Symbol Editor with the IP core.

Solution Status

This issue is fixed in version 10.1 of the RLDRAM II Controller with UniPHY.

Global Signal Assignments Not Applied

The Fitter sometimes does not honor GLOBAL signal assignments applied by the *<variation_name>*_pin_assignments.tcl script.

Affected Configurations

This issue affects all configurations.

Design Impact

This issue has no impact on the correctness of the design, but can result in suboptimal resource placement and can contribute to difficulties in achieving timing closure.

Workaround

To determine whether GLOBAL assignments are properly applied, check the Fitter Report and verify whether any GLOBAL signal assignment referring to a PLL output port (for example, `...|auto_generated|clk[*]`) appears in the **Ignored Assignments** section.

If there is a GLOBAL assignment to a PLL output port listed in **Ignored Assignments**, you can correct the problem by running Analysis & Synthesis and then running the Fitter. You should then verify in the Fitter Report that the assignment is no longer ignored.

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller with UniPHY.

UniPHY DQS Clock Buffer Location

The DQS clock buffer location for the UniPHY can cause hold time violations when placed suboptimally. The Quartus II software may suboptimally place the DQS clock buffer on a global or dual-regional clock after reentering the FPGA, so that it can be routed to the write side of the read capture FIFO.

Affected Configurations

The issue affects all configurations.

Design Impact

You may see hold time failures on the capture clocks in core logic.

Workaround

Create a location assignment on the buffer to the same edge as the memory interface (for example `EDGE_BOTTOM`).

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller with UniPHY.

IP Functional Simulation Model

The wizard-generated IP core functional simulation model (**.vho**) file for VHDL designs is functionally incorrect.

Affected Configurations

The issue affects all configurations.

Design Impact

You cannot use an IP core functional simulation model to simulate your design.

Workaround

This issue has no workaround.

Solution Status

This issue is fixed in version 10.1 of the RLDRAM II Controller with UniPHY.

No Link to User Guide from Wizard

The wizard does not have a link to the *RLDRAM II Controller with UniPHY User Guide*.

Affected Configurations

The issue affects all configurations.

Design Impact

There is no design impact.

Workaround

Access the *RLDRAM II Controller with UniPHY User Guide* from the Altera website.

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller with UniPHY.

Incorrect Operation of Waitrequest Signal

The IP core does not correctly assert the Avalon-MM `waitrequest` signal, when the interface is reset.

Affected Configurations

This issue affects designs that try and send Avalon-MM data to the interface while the interface is in reset.

Design Impact

As the interface does not assert `waitrequest` it does not observe Avalon-MM transactions sent to it while reset is asserted.

Workaround

The workaround for this issue is to not send Avalon-MM transactions to the interface while reset is asserted.

Solution Status

This issue is fixed in version 10.0 of the RLDRAM II Controller with UniPHY.

User Guide States Support for ×72 Devices

The user guide states support for multiple devices with a combined interface width of up to ×72, which is incorrect.

Affected Configurations

The issue affects all configurations.

Design Impact

You cannot use multiple devices with a combined interface width of up to ×72.

Workaround

This issue has no workaround.

Solution Status

This issue is fixed in version 10.0 of the RLDRAM II Controller with UniPHY, which supports width expansion.

–18 Presets Give Errors

If you select any preset with –18 (for example, MT49H64M9-18, MT49H32M18-18, MT49H16M36-18), you see the following error:

```
Error: <variation>: Memory clock frequency must be between 170 MHz
and 500 MHz
```

Affected Configurations

The issue affects all –18 presets.

Design Impact

If you select a 533-MHz component, the FPGA device fails to meet timing.

Workaround

Ensure you change the frequency to a supported frequency.

Solution Status

This issue will be fixed in a future version of the RLDRAM II Controller with UniPHY.

tQKH Parameter Incorrect

In the wizard, the t_{QKH} parameter is defined as a "percentage of half of a clock period." However, in the generated timing constraints, the tQKH parameter is used as a "percentage of a full clock period." .

Affected Configurations

The issue affects all configurations.

Design Impact

The read hold margin, as defined in the timing constrants, is too optimistic

Workaround

Manually edit the following two files, to apply the t_{CKH} corrective factor to the equations where t_{QKH} is used:

- *<variaiton_name>*_**report_timing.tcl**

- *<variaiton_name>*.**sdc**

For example, change:

```
[ expr $tQKH * $tCK ]
```

to:

```
[ expr $tQKH * $tCK * 0.45 ]
```

where: `0.45` is an example value of the t_{CKH} parameter.

☞ You can obtain the t_{CKH} parameter for your memory device from the RLDRAM II datasheet.

Solution Status

This issue is fixed in version 10.0 of the RLDRAM II Controller with UniPHY.

29. SDI

Revision History

Table 29–1 shows the revision history for the SDI MegaCore function.

For more information about the new features, refer to the *SDI MegaCore Function User Guide*.

Table 29–1. SDI MegaCore Function Revision History

Version	Date	Description
10.1 SP1	February 2011	Maintenance release.
10.1	December 2010	■ Preliminary support for Arria II GZ devices. ■ Final support for Arria II GX and Stratix IV GT devices. ■ Added new GUI parameter: **Enable Spread Spectrum feature**.
10.0 SP1	September 2010	Added new GUI parameter: **Tolerance to consecutive missed EAV**.
10.0	July 2010	Added DPRIO with PLL Reconfiguration mode for Cyclone IV GX devices.
9.1 SP2	April 2010	Maintenance release.
9.1 SP1	February 2010	Maintenance release.
9.1	November 2009	■ Preliminary support for Cyclone III LS and Cyclone IV (soft SERDES) devices. ■ Dynamic generation of SDC and TCL scripts for all configurations. ■ Example simulation for triple standard cores.

Errata

Table 29–2 shows the issues that affect the SDI MegaCore function v10.1, 10.0, and 9.1.

Not all issues affect all versions of the SDI MegaCore function.

Table 29–2. SDI MegaCore Function Errata

Added or Updated	Issue	Affected Version			
		10.1 SP1	10.1	10.0	9.1
15 Feb 11	Duplex Operation Mode Does Not Support Spread Spectrum Clocking Feature	✓	—	—	—
	HD-SDI Dual Link RX Data Misaligns When Cable Connection is Interrupted	Fixed	✓	✓	—
	rx_status Signal Not Reliable in HD-SDI Dual Link Receiver	Fixed	✓	✓	—
15 Dec 10	The Quartus II Fitter Reports Error When Separate TX and Duplex TX Are Assigned in the Same Transceiver Quad	✓	✓	—	—
15 July 10	Pulse Width Violation in TimeQuest Report	✓	✓	✓	✓
01 Apr 10	Quartus II Fitter Reports Error When Multiple Channels in One Transceiver Quad Use More than One Reference Clock	✓	✓	✓	—
15 Nov 09	The Quartus II Design Assistant Reports Critical Warning	✓	✓	✓	✓

Table 29–2. SDI MegaCore Function Errata

Added or Updated	Issue	Affected Version			
		10.1 SP1	10.1	10.0	9.1
01 Nov 08	Quartus II Fitter Reports Error When PLL-Generated Clock of 67.5 MHz Is Used in Stratix GX Devices	✓	✓	✓	✓
15 May 08	NativeLink Fails With ModelSim Simulator	✓	✓	✓	✓
01 Mar 08	Timing Not Met in C5 Speed Grade Stratix II GX Devices	✓	✓	✓	✓

Duplex Operation Mode Does Not Support Spread Spectrum Clocking Feature

Designs targeting some Cyclone IV GX devices in duplex operation mode and with the **Enable Spread Spectrum** option turned on may fail to compile.

Affected Configurations

This issue affects all designs targeting Cyclone IV GX devices—EP4CGX30 (F484), EP4CGX50, and EP4CGX75—with the **Enable Spread Spectrum feature** option turned on.

Design Impact

The design fails to compile.

Workaround

Use separate SDI RX and TX instances if your design requires the spread spectrum clocking feature.

Solution Status

This issue will be fixed in a future version of the SDI MegaCore function.

HD-SDI Dual Link RX Data Misaligns When Cable Connection is Interrupted

The rx data from the HD-SDI dual link is not synchronized if either Link A or Link B's BNC cable connection is interrupted. When the rxdata is misaligned, the `rx_status[10]` signal remains high.

Affected Configurations

This issue affects all HD-SDI dual link receiver configurations.

Design Impact

HD-SDI Link A data (`rxdata[19:0]`) misaligns with HD-SDI Link B data (`rxdata[39:20]`)

Workaround

Apply hardware reset to the SDI MegaCore function if the cable connection is interrupted.

Solution Status

This issue is fixed in version 10.1 SP1 of the SDI MegaCore function.

rx_status Signal Not Reliable in HD-SDI Dual Link Receiver

The `rx_status[10]` signal is not reliable in the HD-SDI dual link receiver core if two incoming streams are synchronized ahead of the reception.

Affected Configurations

This issue affects all HD-SDI dual link receiver configurations.

Design Impact

The `rx_status[10]`signal toggles.

Workaround

None.

Solution Status

This issue fixed in version 10.1 SP1 of the SDI MegaCore function.

The Quartus II Fitter Reports Error When Separate TX and Duplex TX Are Assigned in the Same Transceiver Quad

For designs with the **Enable PLL Reconfiguration** option turned on and targeting Cyclone IV GX devices, the Quartus II Fitter reports an error when separate TX and duplex TX SDI instances are assigned in the same transceiver quad.

Affected Configurations

This issue affects all designs targeting Cyclone IV GX devices with the **Enable PLL Reconfiguration** option turned on.

Design Impact

The design cannot be fitted in the device.

Workaround

Uses separate RX and TX SDI instances to fit more than 1 SDI transmitter in a transceiver quad.

Solution Status

This issue will be fixed in a future version of the SDI MegaCore function.

Pulse Width Violation in TimeQuest Report

The TimeQuest report may show minimum pulse width violation when you run full compilation on a soft-SERDES design.

Affected Configurations

This issue affects all soft-SERDES designs.

Design Impact

Your design does not meet the timing requirements.

Workaround

Specify the I/O standard for the clock pins so that the clock pins perform better and runs with a higher speed. For example, if you see pulse width violation on the `rx_serial_clk` and `rx_serial_clk90` clock inputs, in the **.qsf** file add the following commands:

```
set_instance_assignment -name IO_STANDARD LVCMOS -to rx_serial_clk
set_instance_assignment -name IO_STANDARD LVCMOS -to rx_serial_clk90
```

Solution Status

This issue will be fixed in a future version of the SDI MegaCore function.

Quartus II Fitter Reports Error When Multiple Channels in One Transceiver Quad Use More than One Reference Clock

The Quartus II Fitter reports an error when multiple channels within one transceiver quad use more than one reference clock in Stratix II GX devices.

For example, four SDI transmitter core is instantiated four times for 4 video channels. These four channels reside within one transceiver quad of a Stratix II GX device. There are two reference clocks connected to this quad—two channels use the first reference clock, and the other two use the second reference clock.

Affected Configurations

This issue affects all designs targeting Stratix II GX devices.

Design Impact

The design cannot be fitted in the device.

Workaround

Apply the quartus variable in the design, by doing the following steps:

1. Create a **quartus.ini** file with content `farm_s2gx_dprio_bypass_pll_number_check=on`.
2. Place the **quartus.ini** file you creatd in your design folder, and compile the design in the Quartus II software version 9.1 SP2.

Solution Status

This issue will be fixed in a future version of the SDI MegaCore function.

The Quartus II Design Assistant Reports Critical Warning

When the **rx_protocol_clk** clock is used, the Quartus II Design Assistant reports the following error:

```
"Critical Warning: (High) Rule D103: Data bits are not correctly
synchronized when transferred between asynchronous clock domains."
```

This clock is not constrained in the SDC file.

Affected Configurations

This issue affects the dual link SDI in split protocol mode.

Design Impact

The design may fail to function properly on the hardware.

Workaround

Add the following constraints into the SDC file:

```
set rx_protocol_clk_name "rx_protocol_clk[1]"
```

```
create_clock -name $rx_protocol_clk_name -period 13.468 -waveform {0.000 6.734}
[get_ports $rx_protocol_clk_name]
```

Solution Status

This issue will be fixed in a future version of the Quartus II software.

Quartus II Fitter Reports Error When PLL-Generated Clock of 67.5 MHz Is Used in Stratix GX Devices

The Quartus II Fitter reports an error when you use PLL-generated clock inputs of 67.5 MHz frequency in SDI-SD MegaCore targeting Stratix GX devices.

Affected Configurations

This issue affects all Stratix GX SDI-SD MegaCore functions with PLL-generated clock inputs of 67.5 MHz frequency.

Design Impact

The design cannot be fitted in the device.

Workaround

Set the input clock to 29.7 MHz frequency so that the PLL generates the frequency of the output clock to 74.25 MHz.

Solution Status

This issue will be fixed in a future version of the SDI MegaCore function.

NativeLink Fails With ModelSim Simulator

When using NativeLink to run simulations with the ModelSim simulator, the testbench fails.

Affected Configurations

This issue affects all configurations.

Design Impact

The design does not simulate and the testbench reports a failure.

Workaround

Use the ModelSim simulation scripts provided by Altera or carry out the following steps:

1. Edit the NativeLink generated script to command "`vsim -t 100fs`".
2. Reexecute the script in ModelSim.

Solution Status

This issue will be fixed in a future version of the SDI MegaCore function.

Timing Not Met in C5 Speed Grade Stratix II GX Devices

The 3-Gbps and triple rate variants of the SDI MegaCore function may not meet the timing requirements in the C5 speed grade device of the Stratix II GX device family.

Affected Configurations

This issue affects the 3-Gbps and triple-rate SDI MegaCore functions.

Design Impact

Your design does not meet timing requirements.

Workaround

Use either a C4 or C3 speed grade device.

Solution Status

This issue will be fixed in a future version of the SDI MegaCore function.

30. SerialLite II

Revision History

Table 30–1 shows the revision history for the SerialLite II MegaCore function.

For more information about the new features, refer to the *SerialLite II MegaCore Function User Guide*.

Table 30–1. SerialLite II MegaCore Function Revision History

Version	Date	Description
10.1 SP1	February 2011	Maintenance release.
10.1	December 2010	Final support for Arria II GX and Stratix IV GT devices.
10.0	July 2010	Maintenance release.
9.1	November 2009	Preliminary support for HardCopy IV GX devices.

Errata

Table 30–2 shows the issues that affect the SerialLite II MegaCore v10.1, 10.0, 9.1, and 9.0.

Not all issues affect all versions of the SerialLite II MegaCore.

Table 30–2. SerialLite II MegaCore Function Errata

Added or Updated	Issue	Affected Version		
		10.1	10.0	9.1
15 Dec 10	The Quartus II Software Indicates Support for Arria II GX as Preliminary	✓	✓	—
15 Nov 09	Designs with Frequency Offset Tolerance Enabled Fail Testbench Simulation	✓	✓	✓
	The Quartus II Design Assistant Reports Critical Warning	✓	✓	✓

The Quartus II Software Indicates Support for Arria II GX as Preliminary

The Quartus II software version 10.1 issues an incorrect warning indicating that the support for Arria II GX devices is preliminary. The Arria II GX support for the SerialLite II MegaCore function is final.

Affected Configurations

This issue affects all configurations.

Design Impact

None.

Workaround

Ignore the warning.

Solution Status

This issue will be fixed in a future version of the Quartus II software.

Designs with Frequency Offset Tolerance Enabled Fail Testbench Simulation

Designs that have the **Frequency Offset Tolerance** option turned on to either 100 ppm or 300 ppm, using streaming or packet mode with an RX buffer size of zero with a non-default reference clock frequency, may fail the demonstration testbench simulation citing data mismatch errors.

This issue occurs because the utilities for the testbench monitor run at a different clock rate compared to the DUT's receive side's Atlantic clock rate.

Affected Configurations

This issue affects designs with the following settings:

- **Frequency Offset Tolerance** turned on to either 100 ppm or 300 ppm
- Streaming mode or Packet mode with RX buffer size = 0
- Reference clock frequency not equal to (data rate/(TSIZE*10))

Design Impact

There is no design impact. This is a demonstration testbench issue.

Workaround

To simulate the testbench successfully, perform the following steps:

1. Open the generated **<design>_tb.v**.
2. Search for the instantiation of **amon_dat_dut**, and replace the `trefclk` in the clock connection with `tx_coreclock`.

   For example,

   Original line: `.clk (trefclk & reset_done)`

   Replaced line: `.clk(tx_coreclock & reset_done)`
3. Repeat step 2 for **amon_dat_sis**, **amon_pri_dut**, and **amon_pri_sis** (if you have enabled Priority Port).
4. Search for the instantiation of **sbrd_dat_dut_to_sis**, and replace the `trefclk` in the `rclk` connection with `tx_coreclock`:

   For example,

   Original line: `,.rclk (trefclk)`

   Replaced line: `,.rclk (tx_coreclock)`

5. Repeat step 4 for **sbrd_pri_dut_to_sis**, **sbrd_dat_sis_to_dut**, and **sbrd_pri_sis_to_dut**.

Solution Status

This issue will be fixed in a future version of the SerialLite II MegaCore function.

The Quartus II Design Assistant Reports Critical Warning

When you compile a SerialLite II design that targets Stratix GX devices, the Quartus II Design Assistant reports the following error:

```
Critical Warning: (Critical) Rule C101: Gated clock should be
implemented according to the Altera standard scheme. Found 1 node(s)
related to this rule.

    Critical Warning: Node
"<design>_slite2_top|slite2_top_inst|slite2_xcvr:xcvr_inst|altgxb:altg
xb_component|rx_clkout_wire[0]
```

This warning, if targeted to the rx_clkout_wire[0], is erroneously issued by the Quartus II Design Assistant, and is not valid. You can ignore this warning.

Affected Configurations

This issue affects all designs that target Stratix GX devices.

Design Impact

There is no design impact.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the Quartus II software.

31. Triple Speed Ethernet

Revision History

Table 31–1 shows the revision history for the Triple Speed Ethernet MegaCore function.

For more information about the new features, refer to the *Triple Speed Ethernet MegaCore Function User Guide*.

Table 31–1. Triple Speed Ethernet MegaCore Function Revision History

Version	Date	Description
10.1	December 2010	■ Preliminary support for Arria II GZ devices. ■ Added a new parameter, **Starting Channel Number**.
10.0	July 2010	Preliminary support for Stratix V devices.
9.1 SP1	February 2009	Preliminary support for Cyclone IV E devices
9.1	November 2009	Preliminary support for Cyclone III LS and Cyclone IV devices.
9.0 SP2	July 2009	Maintenance release.
9.0 SP1	May 2009	Preliminary support for HardCopy III and HardCopy IV E devices.
9.0	March 2009	■ Preliminary support for Arria II GX device family. ■ Support for different speeds in multi-port MACs. ■ Option to extend the width of selected statistics counters to 64 bits. ■ Support for 64 Kbyte frame length. ■ Implemented 125-MHz clock enable signals in the physical coding sublayer (PCS) function to replace the internal SGMII clock generator blocks. ■ Added a new field, `disable_rd_timeout` (bit 27), in the `command_config` register. ■ Added a new parameter in the top-level file that specifies the depth of the synchronizer chain.

Errata

Table 31–2 shows the issues that affect the Triple Speed Ethernet MegaCore function v10.1, 10.0, and 9.1.

Not all issues affect all versions of the Triple Speed Ethernet MegaCore function.

Table 31–2. Triple Speed Ethernet MegaCore Function Errata

Added or Updated	Issue	Affected Version		
		10.1	10.0	9.1
15 Mar 11	Late Collision in Half-Duplex 10/100-Mbps Ethernet MAC	✓	✓	✓
	Packet Loss in 8-bit Internal FIFO Buffer	✓	✓	✓
	Speed Change Causes Corrupt Packet	✓	✓	✓
	Statistics Counters Issues	✓	✓	✓
	Continuous Data Transmission from MAC Function	✓	✓	✓
	Half-Duplex Mode Post Collision Issues	✓	✓	✓
	Transceiver Quad Sharing Failure	✓	✓	✓
	PLL Sharing Problem for LVDS Channels	✓	✓	✓
	Reset Synchronization Problem	✓	✓	✓
	MII Local Loopback Failure	✓	✓	✓
	Compilation Targeting a Stratix V Device Fails	✓	—	—
15 Dec 10	Simulation Fails for Hardcopy IV GX Designs	✓	✓	—
15 Sep 10	Corrupted Packets in 10/100-Mbps Designs with GXB Transceiver	✓	✓	—
15 July 10	Serial Loopback is Enabled by Default in Cyclone IV GX Devices	✓	✓	✓
	Unstable Designs with LVDS in Hardware	✓	✓	✓
15 Nov 09	Serial Loopback is Enabled by Default in Cyclone IV GX Devices	Fixed	Fixed	✓
15 Mar 09	Timing Not Met in Cyclone III Devices	✓	✓	✓
15 May 08	Non-Compliant Implementation of Bit PAGE_RECEIVE in PCS Register	✓	✓	✓
	Non-Compliant Implementation of aAlignmentError Statistics Counter	✓	✓	✓

Late Collision in Half-Duplex 10/100-Mbps Ethernet MAC

MAC function with 1000BASE-X/SGMII PCS may detect late collision when it is operating in 10/100-Mbps half-duplex mode. The external third party PYH and cables introduce latency in addition to the latency of the 1000BASE-X/SGMII PCS with embedded PMA. This issue arises when the total latency exceeds the 512-bit slotTime as defined in IEEE 802.3 Clause 4.4.

Affected Configuration

This issue affects MAC function designs that contain 10/100/1000-Mbps Ethernet MAC with 1000BASE-X/SGMII PCS operating in 10/100-Mbps half-duplex mode.

Workaround

Use 10/100/1000-Mbps Ethernet MAC only with GMII/MII or RGMII for 10/100-Mbps half-duplex mode operation.

Solution Status

This issue will be fixed in a future version of the Triple Speed Ethernet MegaCore function.

Packet Loss in 8-bit Internal FIFO Buffer

When you enable the SGMII on the MAC function with 8-bit internal FIFO buffer, the MAC function will not transmit the first packet into the FIFO buffer.

Affected Configuration

This issue affects MAC function designs with 8-bit internal FIFO buffer and SGMII PCS.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the Triple Speed Ethernet MegaCore function.

Speed Change Causes Corrupt Packet

When you switch the MAC speed from 10/100-Mbps to 1000-Mbps while the MAC function is transmitting data, the transmit packet gets corrupted. The MAC function continuously sends data out through the SGMII.

Affected Configuration

This issue affects all designs that contain MAC function with SGMII PCS.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the Triple Speed Ethernet MegaCore function.

Statistics Counters Issues

Statistics counters are registers that collect statistics on the transmit and receive datapaths in the MAC function. When statistics counters are enabled in any MAC variant, you may observe these issues in various configurations:

- `ifOutUcastPkts` and `ifOutBroadcastPkts` do not increase when the MAC function transmits erroneous unicast and broadcast frames.
- `aFramesReceivedOK` does not increase when the MAC function in 10/100-Mbps variation receives a pause frame.
- `ifInBroadcastPkts` increases when the MAC function in 1000-Mbps variation receives a pause frame.
- `aOctetsReceivedOK` and `etherStatsUndersizePkts` do not count the length of pause frame when you disable the pause frame forwarding on receive.
- `ifOutErrors`, `ifOutUcastPkts`, `ifOutMulticastPkts` and `ifOutBroadcastPkts` do not count the flushed packets when late collision or excessive collision occurs.
- `aFramesReceivedOK`, `aOtetsReceivedOK`, `etherStatsOctets`, `etherStatsPkts` and `etherStatsPkts64Octets` count an extra frame when the MAC function receives a pause frame.
- `aFrameReceivedOK` and `etherStatsUndersizePkts` increase by 1 when the MAC function receives magic packet and wakes up. These statistics counters should not increase in sleep mode.
- All statistics counters operate in normal mode when the MAC function operates in sleep mode.

Affected Configuration

This issue affects variants of MAC with enabled statistics counters.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the Triple Speed Ethernet MegaCore function.

Continuous Data Transmission from MAC Function

When you switch the MAC function from half-duplex to full-duplex mode while it is transmitting data, the MAC function continuously sends data out through the MII even when you are not sending any data to the MAC function.

Affected Configuration

This issue affects variants of MAC with internal FIFO buffer operating in half-duplex mode.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the Triple Speed Ethernet MegaCore function.

Half-Duplex Mode Post Collision Issues

When the MAC function operates in half-duplex mode, these issues are observed after collisions:

- The MAC function continuously sends data out through the MII even when you do not send any data to the MAC function.
- No retransmit frame is available on the MAC transmit datapath when collision happens on half-duplex 10Mbps MAC variant.
- The MAC function fails to copy the start of packet (SOP) of the subsequent frame after the retransmit frame into the retransmit buffer.

Affected Configuration

This issue affects variants of MAC function operating in half-duplex mode.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the Triple Speed Ethernet MegaCore function.

Transceiver Quad Sharing Failure

In designs containing multiple PMA blocks with GXB transceivers, the transceiver channels fail to share one transceiver quad when you instantiate the Triple Speed Ethernet MegaCore functions individually.

Affected Configuration

This issue affects designs that contain all transceiver family devices.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the Triple Speed Ethernet MegaCore function.

PLL Sharing Problem for LVDS Channels

In designs containing multiple PMA Blocks with LVDS I/O, the LVDS channels from different Triple Speed Ethernet MegaCore functions fail to share a common PLL.

Affected Configuration

This issue affects designs that contain the Stratix II, Stratix II GX, Stratix III and Stratix IV E/GX device families.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the Triple Speed Ethernet MegaCore function.

Reset Synchronization Problem

The `reset_rx_clk` and `reset_tx_clk` signals do not synchronize to `rx_clk` and `tx_clk`.

Affected Configuration

This issue affects variants of MAC function with 1000BASE-X/SGMII PCS and embedded PMA.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the Triple Speed Ethernet MegaCore function.

MII Local Loopback Failure

The MAC function receives corrupt data packet when you enable the local loopback on MII.

Affected Configuration

This issue affects designs that contain Triple Speed Ethernet MAC operating at 10/100-Mbps.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the Triple Speed Ethernet MegaCore function.

Compilation Targeting a Stratix V Device Fails

Designs that include a Triple Speed Ethernet MegaCore function and target a Stratix V device, do not compile even if you have a valid license for the IP core. Refer to Altera solution rd03082011_116 at www.altera.com/support/kdb/solutions/rd03082011_116.html.

Affected Configurations

This issue affects all Triple Speed Ethernet MegaCore function designs that target a Stratix V device.

Workaround

To fix this issue, if you have a valid license for this IP core, follow these steps:

1. Upgrade your Quartus II software installation to the 10.1 Service Pack 1 version.
2. Apply Patch 1.19 to your Quartus II software installation.
3. Regenerate your IP core and any others in your design that are affected by this issue.
4. Recompile your design.

Solution Status

This issue will be fixed in a future version of the Quartus II software.

Simulation Fails for Hardcopy IV GX Designs

Simulation may fail for designs that target Hardcopy IV GX devices.

Affected Configuration

This issue affects all Hardcopy IV GX designs.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the Triple Speed Ethernet MegaCore function.

Corrupted Packets in 10/100-Mbps Designs with GXB Transceiver

The rate match FIFO in the transceiver compensates for the frequency difference between the recovered clock and the receive clock by inserting or removing inter-packet gaps between packets. You may observe corrupted packets in variations of the MegaCore function operating at 10/100 Mbps with GXB transceiver for certain combinations of ppm difference and packet size. For 200 ppm difference, the largest supported ppm difference, you get corrupted packets if the packet size is greater than 160 bytes in 10-Mbps designs or 1600 bytes in 100-Mbps designs.

Affected Configuration

This issue affects all designs that contain SGMII PCS variations with GXB transceiver operating at 10/100 Mbps.

Workaround

Set the GXB transceiver to operate in basic mode. To do so, you must instantiate the MegaCore function with an external transceiver. The Instantiate TSE with External ALTGX / ALTLVDS page includes a design example that demonstrates this configuration and lists the required parameter settings.

Solution Status

This issue will be fixed in a future version of the Triple Speed Ethernet MegaCore function.

Serial Loopback is Enabled by Default in Cyclone IV GX Devices

The serial loopback option in designs that target Cyclone IV GX devices is always turned on by default, which is different from designs targeting other device families.

Affected Configuration

This issue affects all Cyclone IV GX designs that contain GXB transceiver blocks.

Workaround

Using the MegaWizard Plug-in Manager, edit the transceiver variation file for Cyclone IV GX, *<project directory>/triple_speed_ethernet-library/* **altera_tse_altgx_civgx_gige.v**. In the transceiver MegaWizard Interface, turn off the serial loopback option and click **Finish** to regenerate the transceiver variation.

Solution Status

This issue will be fixed in a future version of the Triple Speed Ethernet MegaCore function.

Unstable Designs with LVDS in Hardware

You may get unstable results when running designs that contain LVDS transceiver blocks in hardware. This is caused by the constraints provided with the MegaCore function.

Affected Configuration

This issue affects all configurations that contain LVDS transceiver blocks.

Workaround

Edit the constraint file, *<project directory>/<variation name>*_**constraint.sdc**, and replace lines 410 through 417 with the following lines:

```
set_clock_groups -asynchronous \
-group {altera_tse_mac_rx_clk_0} \
-group {altera_tse_mac_tx_clk_0} \
-group {altera_tse_rx_afull_clk} \
-group {altera_tse_sys_clk} \
-group {altera_tse_ref_clk \
altera_tse_multi_mac_pcs_pma_inst|the_altera_tse_pma_lvds_rx_0|altlvds_
rx_component|auto_generated|rx[0]|clk0 \
altera_tse_multi_mac_pcs_pma_inst|the_altera_tse_pma_lvds_rx_0|altlvds_
rx_component|auto_generated|pll|clk[0]}
```

Solution Status

This issue will be fixed in a future version of the Triple Speed Ethernet MegaCore function.

Timing Not Met in Cyclone III Devices

Designs targeted to Cyclone III devices may not meet timing when the skew optimization option is turned on by default.

Affected Configuration

This issue may affect variations in designs targeted to Cyclone III devices.

Workaround

Turn off the skew optimization option by adding the following assignment in the Quartus II settings file (**.qsf**):

```
set_global_assignment -name ENABLE_BENEFICIAL_SKEW OPTIMIZATION OFF
```

Solution Status

This issue will be fixed in a future version of the Triple Speed Ethernet MegaCore function.

Non-Compliant Implementation of Bit PAGE_RECEIVE in PCS Register

The Triple Speed Ethernet MegaCore function sets the `PAGE_RECEIVE` bit in the PCS register `an_expansion` to 1 when a /C/ ordered set is received. This behavior does not comply with the IEEE 802.3 Standard clause 37.

Affected Configuration

This issue affects all configurations that include the PCS function.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the Triple Speed Ethernet MegaCore function.

Non-Compliant Implementation of aAlignmentError Statistics Counter

The Triple Speed Ethernet MegaCore function increments the `aAlignmentError` statistics counter when an SFD error is encountered. This behavior does not comply with the IEEE 802.3 Standard clause 5.2.2.1.7.

Affected Configuration

This issue affects all configurations.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the Triple Speed Ethernet MegaCore function.

32. Video and Image Processing Suite

Revision History

Table 32–1 shows the revision history of the Video and Image Processing Suite MegaCore functions.

For information about the new features, refer to the *Video and Image Processing Suite User Guide*.

Table 32–1. Video and Image Processing Suite Revision History

Version	Date	Description
10.1 SP1	February 2011	Maintenance release.
10.1	December 2010	■ Added Scaler II MegaCore function. ■ Final support for Stratix IV GT devices.
10.0	July 2010	■ Added Interlacer MegaCore function. ■ Updated Clocked Video Output and Clocked Video Input MegaCore functions to insert and extract ancillary packets.

9.1	November 2009	■ Added the following new MegaCore functions:
		  ■ The Frame Reader
		  ■ The Control Synchronizer
		  ■ The Switch MegaCore function
		■ The Frame Buffer MegaCore function supports:
		  ■ Controlled frame dropping or repeating to keep the input and output frame rates locked together
		  ■ Triple buffering of interlaced video streams.
		  ■ The ability to discard invalid frames or fields, or both, by repeating the last video frame received.
		■ The Clipper, Frame Buffer, and Color Plane Sequencer MegaCore functions now support four channels in parallel.
		■ The Deinterlacer MegaCore function supports a new 4:2:2 motion-adaptive mode and an option to align read/write bursts on burst boundaries.
		■ The Clocked Video Input and Clocked Video Output MegaCore functions support synchronization signals and have revised control register maps.
		■ The Line Buffer Compiler MegaCore function is obsolete.
		■ Extended the Avalon-ST Video protocol to improve support for interlaced content. The change is backward compatible.

9.0 SP1	May 2009	Preliminary support for HardCopy III and HardCopy IV E devices.
9.0	March 2009	■ The Deinterlacer MegaCore function supports controlled frame dropping or repeating to keep the input and output frame rates locked together. ■ The Test Pattern Generator MegaCore function can generate a user-specified constant color that can be used as a uniform background. ■ Preliminary support for Arria II GX devices.

Errata

Table 32–2 shows the issues that affect the Video and Image Processing Suite MegaCore functions v10.1, 10.0, and v9.1.

Not all issues affect all versions of the Video and Image Processing Suite MegaCore functions.

Table 32–2. Video and Image Processing Suite Errata

Added or Updated	Issue	Affected Version		
		10.1	10.0	9.1
15 Mar 11	Compilation Targeting a Stratix V Device Fails	✓	—	—
	Signed Vertical Coefficients and Unsigned Horizontal Coefficients (or Vice Versa) with Sum of Coefficients More Than 1 Cause Scaler II to Generate Incorrect Output	✓	—	—
	Scaler II Generates Incorrect Output When Vertical Filter Taps is 3	✓	—	—
15 Dec 10	Scaler II Generates Incorrect Output When Receiving Empty Packets	✓	—	—
	Deinterlacer and Frame Buffer Connected to DDR3 May Not Work Properly	✓	✓	✓
	Compilation Fails on the Windows 7 or Vista Operating System	✓	✓	✓
15 Feb 10	Compilation Errors with the Frame Buffer	✓	✓	✓
15 Nov 09	Frame Buffer and Deinterlacer are Missing Entry in .sdc File	✓	✓	✓
	Clocked Video Output Incorrectly Aligns Start of Frame (vid_sof)	✓	✓	✓
	Scaler: Number of Colour Planes Incorrect	✓	✓	✓
15 Mar 09	RTL Simulation Reports Errors When Using Verilog HDL	✓	✓	✓
	Incorrect Simulation Models Created for Deinterlacer and Frame Buffer	✓	✓	✓
	Deinterlacer and Test Pattern Generator May Not Upgrade	✓	✓	✓
	The 2D Median Filter Does Not Support 7×7 Filter Size	✓	✓	✓
	Packets Sent to VIP Cores Must Have Non-Empty Payload	✓	✓	✓
15 May 08	SOPC Builder Avalon-ST Adapter Does Not Support Avalon-ST Video	✓	✓	✓
01 Oct 07	Scalar Coefficients Preview Window Cannot be Closed	✓	✓	✓
01 May 07	Precision Must be Set When Using Lanczos Coefficients in Scaler	✓	✓	✓
01 Dec 06	Cyclone II M4K Fails in Alpha Blending Mixer and Gamma Corrector	✓	✓	✓

Compilation Targeting a Stratix V Device Fails

Designs that include at least one of several IP cores from the Video and Image Processing Suite and target a Stratix V device, do not compile even if you have a valid license for the suite. Refer to Altera solution rd03082011_116 at www.altera.com/support/kdb/solutions/rd03082011_116.html.

Affected Configurations

This issue affects designs that target a Stratix V device and include at least one of the following IP cores from the Video and Image Processing Suite:

- 2D FIR Filter IP core
- 2D Median Filter IP core

- Alpha Blending Mixer IP core
- Chroma Resampler IP core
- Clipper IP core
- Color Plan Sequencer IP core
- Color Space Converter (CSC) IP core
- Deinterlacer IP core
- Frame Buffer IP core
- Gamma Corrector IP core
- Interlacer IP core
- Scaler IP core
- Test Pattern Generator IP core

Design Impact

Designs that include at least one of these IP cores and target a Stratix V device cannot compile.

Workaround

To fix this issue, if you have a valid license for the video and image processing IP cores, follow these steps:

1. Upgrade your Quartus II software installation to the 10.1 Service Pack 1 version.
2. Apply Patch 1.19 to your Quartus II software installation.
3. Regenerate your IP core and any others in your design that are affected by this issue.
4. Recompile your design.

Solution Status

This issue will be fixed in a future version of the Quartus II software.

Signed Vertical Coefficients and Unsigned Horizontal Coefficients (or Vice Versa) with Sum of Coefficients More Than 1 Cause Scaler II to Generate Incorrect Output

The Scaler II MegaCore function may generate incorrect output when you use signed vertical coefficients with unsigned horizontal coefficients (or vice versa) and the sum of the coefficients for one or more phases is more than 1.

Affected Configurations

This issue affects all configurations that use the polyphase and bicubic algorithms with the Scaler II MegaCore function.

Design Impact

The affected configuration may generate incorrect output.

Workaround

None.

Solution Status

This issue will be fixed in a future version of the Video and Image Processing Suite.

Scaler II Generates Incorrect Output When Vertical Filter Taps is 3

The Scaler II MegaCore function using polyphase algorithm may generate incorrect output when you set **Vertical Filter Taps** to 3.

Affected Configurations

This issue affects all configurations that use the polyphase algorithms with the Scaler II MegaCore function.

Design Impact

The affected configuration may generate incorrect output.

Workaround

None. If your design allows, set **Vertical Filter Taps** to 4.

Solution Status

This issue will be fixed in a future version of the Video and Image Processing Suite.

Scaler II Generates Incorrect Output When Receiving Empty Packets

The Scaler II MegaCore function generates incorrect output when it receives empty packets with only the header, start of packet (SOP), and end of packet (EOP) on the same clock cycle.

Affected Configurations

This issue affects all configurations that use the Scaler II MegaCore function.

Design Impact

The empty packets sent will be altered.

Workaround

None. You cannot deliberately send empty user packets through the Scaler II MegaCore function expecting unaltered outputs.

Solution Status

This issue will be fixed in a future version of the Video and Image Processing Suite.

Deinterlacer and Frame Buffer Connected to DDR3 May Not Work Properly

The Deinterlacer and Frame Buffer MegaCore functions may not work properly when connected to a DDR3 SDRAM High Performance Controller MegaCore function.

In some configurations and or with specific input resolutions, the Deinterlacer and Frame Buffer MegaCore functions may issue write and read bursts starting at odd addresses. The DDR3 SDRAM controller uses wrapping bursts for read accesses, consequently the wrong data may be read back from memory.

Affected Configurations

Systems connecting the Video and Image Processing MegaCore functions to DDR3 SDRAM.

Design Impact

This issue may have unpredictable effects. Typically, the output video is distorted.

Workaround

Turn on **Align read/write bursts with burst boundaries** in the Frame Buffer and Deinterlacer parameter editors.

Solution Status

This issue will be fixed in a future version of the Video and Image Processing Suite.

Compilation Fails on the Windows 7 or Vista Operating System

On the Windows 7 or Vista Operating System, when synthesizing the VIP Suite IP MegaCore functions in the Quartus II software, or generating an IP functional simulation model, compilation fails.

Affected Configurations

This issue affects all configurations.

Design Impact

For synthesis, you receive the following error:

```
Error: Node instance "scaler" instantiates undefined entity
"alt_vip_scl_GNRA6GTEAK" File: C:/work/testvip/db/scaler_GN.vhd Line:
52
```

For IP functional simulation model generation, you receive the following error:

```
Error:  Simulation model map command failed:
D:\altera\90sp2\quartus/bin/quartus_map scaler --simgen --
simgen_parameter="CBX_HDL_LANGUAGE=VHDL"
```

Workaround

You must run the Quartus II software as adminstrator to enable the VIP Suite IP generation and synthesis to complete successfully. To run Quartus II as adminstrator on the **Start menu**, point to **Programs**, then **Altera**, then right click on **Quartus II** *<version>*. Click **Run as adminstrator**.

Solution Status

This issue will be fixed in a future version of the Video and Image Processing Suite.

Compilation Errors with the Frame Buffer

The frame buffer may fail to generate and issues a compilation error when you turn on **Discard invalid frames/fields**.

Affected Configurations

This issue affects configurations that use the **Discard invalid frames/fields** option without turning on either the frame dropping or the support for interlaced fields.

Design Impact

The generation fails and you receive the following compilation errors:

```
Error: IP Generator Error: At end of source: error: expected a "}"
```

```
Error: IP Generator Error:
"C:/altera/91/ip/altera/frame_buffer/lib/vip_vfb_hwfast.hpp", line
756: error: expected "while"
```

Workaround

This issue has no workaround. However, enabling the support for interlaced video may be an acceptable solution for video systems where the frame buffer is only processing progressive frames.

Solution Status

This issue will be fixed in a future version of the Video and Image Processing Suite.

Frame Buffer and Deinterlacer are Missing Entry in .sdc File

You must manually add the Synopsis Design Constraint **(.sdc)** files to the Quartus II project for the following MegaCore functions:

- Deinterlacer
- Frame Buffer
- Clocked Video Input
- Clocked Video Output

Affected Configurations

All configurations that use any of these MegaCore functions.

Design Impact

These **.sdc** files declare false paths that the Quartus II software should not consider during timing analysis. Timing closure for valid critical paths may not be achievable if you do not include these files in your project, which results in a nonfunctioning system.

Workaround

Add the **.sdc** files manually from the project settings windows. In the Quartus II software, on the Project menu click **Add/Remove Files in Project**. Altera procides these **.sdc** files with your Quartus II installation and are in the following directory:

<*install_dir*>**\ip**<*megacore_function*>**\lib\alt_vip_**<*tla*>**.sdc**

where:

- <*megacore_function*> is **deinterlacer**, **frame_buffer**, **clocked_video_input**, or **clocked_video_output**
- <*tla*> is an acronym that identifies the MegaCore function

To verify that the Quartus II software corerctly adds the **.sdc** files, keep the **Settings** window open and click **Timing Analysis Settings** then **TimeQuest Timing Analyzer** in the tree menu.

Solution Status

This issue will be fixed in a future version of the Video and Image Processing Suite.

Clocked Video Output Incorrectly Aligns Start of Frame (vid_sof)

When you turn on frame locking in the **Clocked Video Output** it attempts to align its start of frame (output by the `vid_sof` signal) to the incoming start of frame signal (the `sof` signal). When it achieves this aligment, the IP core frame locks the output video (the start of frames are aligned) to the input video.

Affected Configurations

This issue affects systems enabling the frame locking functionality in the **Clocked Video Output**.

Design Impact

The output video frame lock is out by one cycle.

Workaround

To work around this issue, move the **Clocked Video Output** start of frame one cycle earlier. For example, if the start of frame required for **Mode 1** is at sample 10, write 9 into bits 2 to 15 of the `Mode1 SOF Sample` register.

Solution Status

This issue will be fixed in a future version of the Video and Image Processing Suite.

Scaler: Number of Colour Planes Incorrect

The **Scaler: Number of colour planes** should be 1 to 3.

Affected Configurations

This issue affects all configurations.

Design Impact

```
There is no design impact.
```

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the Video and Image Processing Suite.

RTL Simulation Reports Errors When Using Verilog HDL

EDA RTL simulation started from the Quartus II software reports errors in the ModelSim® simulator for designs containing Video and Image Processing Suite MegaCore functions when the output files are in Verilog HDL.

Affected Configurations

This issue affects configurations that use NativeLink to run a ModelSim simulation from Verilog HDL.

Design Impact

An error message reports that software cannot find the Altera library.

Workaround

Compile the file **db/alt_cusp90_package.vhd** to the Altera library. To perform this compilation, modify the top-level **.do** script in the **simulation/modelsim** directory.

Solution Status

This issue will be fixed in a future version of the Video and Image Processing Suite.

Incorrect Simulation Models Created for Deinterlacer and Frame Buffer

The Quartus II software may create incorrect functional simulation models for the Deinterlacer and Frame Buffer MegaCore functions.

Affected Configurations

This issue affects configurations that use a different clock domain for the Avalon Memory-Mapped (Avalon-MM) master interfaces.

Design Impact

The IP functional simulation models generated with the MegaWizard Plug-in may reset in an incorrect state. This issue may also affect simulation models generated with SOPC Builder.

Workaround

If possible, release the reset signals for the Avalon-MM interface ports before the reset signal for the MegaCore function. Alternatively, repeat the generation until the wizard produces a valid **.vo** or **.vho** file.

Solution Status

This issue will be fixed in a future version of the Video and Image Processing Suite.

Deinterlacer and Test Pattern Generator May Not Upgrade

The Deinterlacer and Test Pattern Generator MegaCore functions may not directly upgrade to v9.0 in SOPC Builder.

Affected Configurations

This issue affects the Quartus II v8.1 designs containing Deinterlacer or Test Pattern Generator MegaCore functions that were originally created in the Quartus II v8.0 software.

Design Impact

SOPC Builder reports an error when it tries to upgrade the MegaCore function if you do not change the parameterization.

Workaround

To workaroud this issue, follow these steps:

1. Open the v8.1 version of your design.
2. Make a change to the parameterization of any Deinterlacer or Test Pattern Generator MegaCore functions and apply your change.
3. Change back to the original parameterization, then save the SOPC Builder system.

Solution Status

This issue will be fixed in a future version of the Video and Image Processing Suite.

The 2D Median Filter Does Not Support 7×7 Filter Size

The 2D Median Filter MegaCore function does not support the 7×7 filter size.

Affected Configurations

This issue affects configurations that include the 2D Median Filter MegaCore function.

Design Impact

You can select a 7×7 filter size in pre-9.0 versions of the 2D Median Filter MegaCore function but the software issues an error message when generating the simulation model.

Workaround

There is no workaround. Do not select the 7×7 filter size.

Solution Status

The 7×7 filter size is not available in version 9.0 or later of the Video and Image Processing Suite.

Packets Sent to VIP Cores Must Have Non-Empty Payload

The packets sent to the Color Space Converter and 2D Median Filter MegaCore functions must have non-empty payload. If a packet is sent with a type but without any further information, the packet processing logic may enter an inconsistent state.

Affected Configurations

This issue affects configurations that include the Color Space Converter or 2D Median Filter MegaCore functions.

Design Impact

If the IP core receives a packet with an empty payload, it may not output correct data until it receives a few non-empty packets.

Workaround

If you intend to send an empty packet, send one symbol of data with it.

Solution Status

This issue is unlikely to be fixed as there is a simple workaround.

SOPC Builder Avalon-ST Adapter Does Not Support Avalon-ST Video

In SOPC Builder, the Avalon-ST data adapter does not support the Avalon-ST Video protocol. No error message is currently displayed when connecting the components.

Affected Configurations

This issue affects SOPC Builder configurations that connect an Avalon-ST adapter to a Video and Image Processing MegaCore function.

Design Impact

Connecting any of the Video and Image Processing Suite MegaCore functions to an Avalon-ST data adapter results in a generated system in which the Avalon-ST video protocol is corrupted.

Workaround

To connect Video and Image Processing MegaCore functions that have a different number of planes in parallel, use the Color Plane Sequencer. For example: to convert between 3 colors in parallel (3 symbols per beat) and 3 colors in sequence (1 symbol per beat).

Solution Status

You cannot connect unsupported Avalon-ST adapters in a future version of SOPC Builder and the Video and Image Processing Suite.

Scalar Coefficients Preview Window Cannot be Closed

You cannot close the Scalar Coefficients Preview window when you use it in SOPC Builder.

Affected Configurations

This issue affects the Scaler MegaCore Function when you use the SOPC Builder flow.

Design Impact

This issue does not prevent you from parameterizing the Scalar and therefore has no design impact.

Workaround

The Coefficient Preview window closes when you close the main Scalar parameterization interface.

Solution Status

This issue will be fixed in a future version of the Video and Image Processing Suite.

Precision Must be Set When Using Lanczos Coefficients in Scaler

When configuring the Scaler MegaCore function, you must choose the correct coefficient precision when using Lanczos coefficients.

Affected Configurations

This issue affects configurations of the Scaler MegaCore function using the polyphase algorithm with Lanczos coefficients.

Design Impact

The MegaCore function fails to generate.

Workaround

If you select polyphase mode with Lanczos coefficients, you must set the coefficient precision to be signed with one integer bit. Fraction bits can be set within the full range available in the MegaWizard interface.

Solution Status

The coefficient precision restriction will be enforced in future versions of the Video and Image Processing Suite.

Cyclone II M4K Fails in Alpha Blending Mixer and Gamma Corrector

M4K block write operations may fail for Cyclone II devices with the Alpha Blending Mixer and Gamma Corrector MegaCore functions.

Affected Configurations

This issue affects configurations using Cyclone II devices and the Alpha Blending Mixer or Gamma Corrector MegaCore function.

Design Impact

The Quartus II software issues the following error message:

```
Error: M4K memory block WYSIWYG primitive
"vhdl_gam:vhdl_gam_inst|TTA_X_smem_av:gamma_lut|altsyncram:\ds1:altsyn
cram_component|altsyncram_rvh1:auto_generated|ram_block1a0" utilizes
the dual-port dual-clock mode. However, this mode is not supported in
Cyclone II device family in this version of Quartus II software. Please
refer to the Cyclone II FPGA Family Errata Sheet for more information
on this feature.
```

Workaround

If you target any affected revision (Rev a or b of the 2c35 or Rev a of any other Cyclone II part), set the `CYCLONEII_SAFE_WRITE` variable to `RESTRUCTURE`. This setting causes the Quartus II software to fix the issue at a cost in M4Ks and F_{max}. If you are using a newer revision device, set the `CYCLONEII_SAFE_WRITE` variable to `VERIFIED_SAFE`, which turns off the error message.

Solution Status

This issue is fixed for the latest silicon devices but remains an issue if you are using the earlier silicon.

Refer to the *Cyclone II FPGA Family Errata Sheet* for more information about this issue.

33. Viterbi Compiler

Revision History

Table 33–1 shows the revision history for the Viterbi Compiler.

For more information about the new features, refer to the *Viterbi Compiler User Guide*.

Table 33–1. Viterbi Compiler Revision History

Version	Date	Description
10.1	December 2010	■ Preliminary support for Arria II GZ devices. ■ Final support for Stratix IV GT devices.
10.0	July 2010	Preliminary support for Stratix V devices.
9.1	November 2009	■ Preliminary support for HardCopy IV GX, Stratix IV, and Cyclone III LS devices. ■ Withdrawn support for HardCopy family of devices.

Errata

Table 33–2 shows the issues that affect the Viterbi Compiler v10.1, v10.0, and v9.1.

Not all issues affect all versions of the Viterbi Compiler.

Table 33–2. Viterbi Compiler Errata

Added or Updated	Issue	Affected Version		
		10.1	10.0	9.1
15 Mar 11	Compilation Targeting a Stratix V Device Fails	✓	—	—
15 Mar 09	Testbench ber_clear Signal is Not Connected	✓	✓	✓
	Gate-Level Simulation Fails	✓	✓	✓

Compilation Targeting a Stratix V Device Fails

Designs that include a Viterbi Compiler and target a Stratix V device, do not compile even if you have a valid license for the IP core. Refer to Altera solution rd03082011_116 at www.altera.com/support/kdb/solutions/rd03082011_116.html.

Affected Configurations

Viterbi Compiler designs that target a Stratix V device.

Design Impact

Designs that include this IP core and target a Stratix V device cannot compile.

Workaround

To fix this issue, if you have a valid license for this IP core, follow these steps:

1. Upgrade your Quartus II software installation to the 10.1 Service Pack 1 version.
2. Apply Patch 1.19 to your Quartus II software installation.
3. Regenerate your IP core and any others in your design that are affected by this issue.
4. Recompile your design.

Solution Status

This issue will be fixed in a future version of the Quartus II software.

Testbench ber_clear Signal is Not Connected

The `ber_clear` signal in the generated testbench is not connected correctly.

Affected Configurations

This issue affects all designs.

Design Impact

There is no design impact.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the Viterbi Compiler.

Gate-Level Simulation Fails

The Viterbi Compiler does not support gate-level simulations.

Affected Configurations

This issue affects all designs.

Design Impact

There is no design impact.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future version of the Viterbi Compiler.

34. XAUI PHY

Revision History

Table 34–1 shows the revision history for the XAUI PHY IP core.

For more information about the new features, refer to the "*XAUI PHY IP Core*" chapter in the *Altera Transceiver PHY IP Core User Guide*.

Table 34–1. XAUI PHY Revision History

Version	Date	Description
10.1	December 2010	Added support for Arria II GX and Cyclone IV GX with hard PCS
10.0 SP1	September 2010	Added simulation support.
10.0	July 2010	First release.

Errata

Table 34–2 shows the issues that affect the XAUI PHY IP core versions 10.1, 10.0 SP1, and 10.0.

Table 34–2. XAUI PHY Errata

Added or Updated	Issue	Affected Version		
		10.1	10.0 SP1	10.0
15 Dec 10	Mixed Language Simulation Fails when Optimization Is On	✓	—	—
15 Sept 10	TimeQuest Timing Analyzer Might Improperly Report Setup Violations	—	Fixed	✓
15 Aug 10	Incorrect Addresses for XAUI Reset, RX and TX Control and Status Registers	Fixed	✓	✓

Mixed Language Simulation Fails when Optimization Is On

Simulation fails when using ModelSim with mixed-languages.

Affected Configurations

This issue affects mixed language simulation including Verilog modules and VHDL entities when optimization is on.

Workaround

The workaround is to turn ModelSim optimization off by using the `-novpt` option to the `vsim` command.

Solution Status

This issue may be fixed in a future version of ModelSim.

TimeQuest Timing Analyzer Might Improperly Report Setup Violations

During timing analysis of a soft XAUI PHY MegaCore function, the TimeQuest Timing Analyzer might report setup violations within the mgmt_clk_clk domain and between the mgmt_clk_clk and another clock domain. The TimeQuest Timing Analyzer might also report hold time violations.

Affected Configurations

This issue affects the soft IP implementation of the XAUI PHY IP core in Stratix V devices.

Workaround

The majority of paths that show violations are between asynchronous signals and consequently are false timing paths. In addition, because there is no relationship between the mgmt_clk_clk and refclk_clk, these timing violations represent false paths. To eliminate timing errors for these false paths, you can add the statements in Example 34–1 to your Synopsis Design Constraints File (**.sdc**).

Example 34–1. False Timing Paths for the mgmt_clk_clk Clock Domain

```
set_false_path -from [get_clocks refclk_clk]   -to [get_clocks mgmt_clk_clk]
set_false_path -from [get_clocks mgmt_clk_clk] -to [get_clocks refclk_clk]
set_false_path -from [get_clocks
{*|alt_pma_0|alt_pma_sv_inst|sv_xcvr_generic_inst|channel_tx[0].duplex_pcs|ch[0].rx_pc
s|clocktopld}] -to   [get_clocks mgmt_clk_clk]
```

The timing paths in the mgmt_clk_clk domain shown in Example 34–2 are not false paths; however, you can ignore these errors or other errors that are within the soft XAUI IP core.

Example 34–2. Timing Violations for the mgmt_clk_clk Clock Domain

```
1. From Node
top:i|top_0002:top_inst|top_alt_xcvr_reconfig_0:alt_xcvr_reconfig_0|alt_xcvr_reconfig_
analog:analog_reconfig_instance|alt_xcvr_reconfig_analog_sv:reconfig_analog_sv|chnl_ad
dr_reg[7]
; To Node            ;
top:i|top_0002:top_inst|top_alt_xcvr_reconfig_0:alt_xcvr_reconfig_0|alt_xcvr_reconfig_
analog:analog_reconfig_instance|alt_xcvr_reconfig_analog_sv:reconfig_analog_sv|analog_
reconfig_readdata[2] ;

2. From Node          ;
top:i|top_0002:top_inst|top_alt_xcvr_reconfig_0:alt_xcvr_reconfig_0|alt_xcvr_reconfig_
analog:analog_reconfig_instance|alt_xcvr_reconfig_analog_sv:reconfig_analog_sv|chnl_ad
dr_reg[7]            ;

; To Node            ;
top:i|top_0002:top_inst|top_alt_xcvr_reconfig_0:alt_xcvr_reconfig_0|alt_xcvr_reconfig_
analog:analog_reconfig_instance|alt_xcvr_reconfig_analog_sv:reconfig_analog_sv|analog_
reconfig_readdata[3] ;
```

Finally, the soft IP implementation of the XAUI PHY might show hold time violations which may also be safely ignored.

No workaround is required.

Solution Status

This issue is fixed in release 10.0 SP1 of the soft XAUI PHY IP core.

Incorrect Addresses for XAUI Reset, RX and TX Control and Status Registers

The *XAUI IP Core* chapter of the *Altera Transceiver PHY IP Core User Guide* provides incorrect addresses for the XAUI reset, RX and TX control and status registers.

Affected Configurations

This is a documentation issue only. Table 34–1 gives the correct addresses.

Table 34–3. Reset, RX, TX Status and Simulation Registers (Part 1 of 2) **Addr: 0x200**

Offset	Register	Field	Description
0x004	RESET	RX_DIGITAL	Resets the Rx PCS clock domain.
		TX_DIGITAL	Resets the Tx PCS clock domain.
0x008	RX_CNTRL	INVPOLARITY[3:0]	Inverts the polarity of corresponding bit. This register is RW.
0x00C	TX_CNTRL	INVPOLARITY[3:0]	Inverts the polarity of corresponding bit. This register is RW.
0x010	RX_STATUS_0	PATTERNDETECT[7:0]	When asserted, indicates that the programmed word alignment pattern has been detected in the current word boundary. The Rx pattern detect signal is 2 bits wide per channel or 8 bits per XAUI link. Reading the value of the pattern detect registers clears the bits.
		SYNCSTATUS[7:0]	Records the synchronization status of the corresponding bit. There are 2 bits per channel for a total of 8 bits per XAUI link.
0x014	RX_STATUS_1	ERRDETECT[7:0]	When set, indicates that a received 10-bit code group has an 8B/10B code violation or disparity error. It is used along with Rx disparity to differentiate between a code violation error and a disparity error, or both. There are 2 bits per channel for a total of 8 bits per XAUI link. Reading the value of the errdetect register clears the bits.
		DISPERR[7:0]	Indicates that the received 10-bit code or data group has a disparity error. When set, the corresponding errdetect bits are also set. There are 2 bits wide per channel for a total of 8 bits per XAUI link. Reading the value of the errdetect register clears the bits.
0x018	RX_STATUS_2	RLV[3:0]	Indicates a run length violation. Asserted, if the number of continuous 1s and 0s exceeds the number that was set in the run-length option. Bits 0-3 correspond to lanes 0-3, respectively. Reading the value of the RLV register clears the bits.
		PHASE_COMP_FIFO_ERROR[3:0]	Indicates a Rx phase compensation FIFO overflow or underrun condition on the corresponding lane. Reading the value of the PHASE_COMP_FIFO_ERROR register clears the bits.

Table 34–3. Reset, RX, TX Status and Simulation Registers (Part 2 of 2) Addr: 0x200

Offset	Register	Field	Description
0x01C	RX_STATUS_3	RMFIFODATADELETED[7:0]	When asserted, indicates that the rate match block has deleted an ||R|| column. The flag goes high for one clock cycle per deleted ||R|| column. There are 2 bits for each lane. Reading the value of the RMFIFODATADELETED register clears the bits.
		RMFIFODATAINSERTED[7:0]	When asserted, indicates that the rate match block inserted a ||R|| column. Goes high for one clock cycle per inserted ||R|| column. cycle per deleted ||R|| column. Reading the value of the RMFIFODATAINSERTED register clears the bits.
0x020	RX_STATUS_4	RMFIFOFULL[3:0]	When asserted, indicates that rate match FIFO block is full (20 words). This bit is asserted as long as the FIFO is full and is asynchronous to the Rx data. Bits 0-3 correspond to lanes 0-3, respectively. Reading the value of the RMFIFOFULL register clears the bits.
		RMFIFOEMPTY[3:0]	When asserted, indicates that the rate match FIFO block is empty (5 words). This bit is asserted as long as the FIFO is empty and is asynchronous to the receiver. Bits 0-3 correspond to lanes 0-3, respectively. Reading the value of the RMFIFOEMPTY register clears the bits.
0x024	TX_STATUS_0	PHASE_COMP_FIFO_ERROR[2:0]	Indicates a Tx phase compensation FIFO overflow or underrun condition on the corresponding lane. Reading the value of the PHASE_COMP_FIFO_ERROR register clears the bits.

Workaround

No workaround is required.

Solution Status

This issue is fixed in version 10.1 of the *XAUI IP Core* chapter of the *Altera Transceiver PHY IP Core User Guide*.

This chapter provides additional information about the document and Altera.

How to Contact Altera

To locate the most up-to-date information about Altera products, refer to the following table.

Contact *(1)*	Contact Method	Address
Technical support	Website	www.altera.com/support
Technical training	Website	www.altera.com/training
	Email	custrain@altera.com
Product literature	Website	www.altera.com/literature
Non-technical support (General)	Email	nacomp@altera.com
(Software Licensing)	Email	authorization@altera.com

Note to Table:

(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

The following table shows the typographic conventions this document uses.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Indicate command names, dialog box titles, dialog box options, and other GUI labels. For example, **Save As** dialog box. For GUI elements, capitalization matches the GUI.
bold type	Indicates directory names, project names, disk drive names, file names, file name extensions, software utility names, and GUI labels. For example, **\qdesigns** directory, **D:** drive, and **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Indicate document titles. For example, *Stratix IV Design Guidelines*.
italic type	Indicates variables. For example, *n* + 1. Variable names are enclosed in angle brackets (< >). For example, *<file name>* and *<project name>*.**pof** file.
Initial Capital Letters	Indicate keyboard keys and menu names. For example, the Delete key and the Options menu.
"Subheading Title"	Quotation marks indicate references to sections within a document and titles of Quartus II Help topics. For example, "Typographic Conventions."

Visual Cue	Meaning
`Courier type`	Indicates signal, port, register, bit, block, and primitive names. For example, `data1`, `tdi`, and `input`. The suffix n denotes an active-low signal. For example, `resetn`. Indicates command line commands and anything that must be typed exactly as it appears. For example, `c:\qdesigns\tutorial\chiptrip.gdf`. Also indicates sections of an actual file, such as a Report File, references to parts of files (for example, the AHDL keyword `SUBDESIGN`), and logic function names (for example, `TRI`).
↵	An angled arrow instructs you to press the Enter key.
1., 2., 3., and a., b., c., and so on	Numbered steps indicate a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ■ ■	Bullets indicate a list of items when the sequence of the items is not important.
	The hand points to information that requires special attention.
	A question mark directs you to a software help system with related information.
	The feet direct you to another document or website with related information.
	A caution calls attention to a condition or possible situation that can damage or destroy the product or your work.
	A warning calls attention to a condition or possible situation that can cause you injury.
	The envelope links to the Email Subscription Management Center page of the Altera website, where you can sign up to receive update notifications for Altera documents.