Simulating the Reed-Solomon Model

with the Visual IP Software

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Introduction

Altera® intellectual property (IP) MegaCore™ functions are developed and pre-tested by Altera, and are optimized for specific Altera device architectures. You can test-drive these functions for free via the OpenCore™ feature by downloading the functions from the Altera web site and installing them on your PC or UNIX workstation. To help in your evaluation, Altera also provides Visual IP simulation models for these functions.

The Visual IP software from Innoveda lets you create simulation models that can be used in third-party VHDL and Verilog HDL simulation tools. Altera distributes the Visual IP software for the end user along with Visual IP models of Altera IP functions.

Altera's Visual IP models are parameterizable, RTL level, functional simulation models. The models let you instantiate Altera IP in your design and simulate it in your choice of simulation tool. This user guide describes how to install and use the Visual IP simulation model for the Altera Reed-Solomon Compiler function.

Before using the Reed-Solomon Compiler VIP model, you must download and install the Visual IP software, which is available for free from the Altera IP MegaStore site at **http://www.altera.com/IPmegastore**. Follow the instructions in the *Installing the Visual IP Software User Guide*.

Altera recommends that you also obtain the *Reed-Solomon Compiler MegaCore Function User Guide* from the Altera web site. This user guide describes the technical specifications of the Reed-Solomon Compiler function.

The Reed-Solomon Visual IP model contains the following elements:

Table 1. Reed-Solomon Visual IP Model Elements

Element	Description
rs_enc.*	The VHDL or Verilog HDL model file for the Reed-Solomon standard encoder.
rs_enc_vectors.*	A set of VHDL or Verilog HDL test vectors for the standard encoder.
rs_enc_vip_top.*	Top-level VHDL or Verilog HDL file that references the Reed-Solomon standard encoder model file and test vectors.
rs_var_enc.*	VHDL or Verilog HDL model files for the variable encoder.
rs_eras_cont.*	VHDL or Verilog HDL model files for the continuous decoder with erasures.
rs_eras_dsc.*	VHDL or Verilog HDL model files for the discrete decoder with erasures.
rs_eras_str.*	VHDL or Verilog HDL model files for the streaming decoder with erasures.
rs_std_cont.*	VHDL or Verilog HDL model files for the continuous decoder.
rs_std_dsc.*	VHDL or Verilog HDL model files for the discrete decoder.
rs_std_dsc_vectors.*	A set of VHDL or Verilog HDL test vectors for the discrete decoder.
rs_std_dsc_vip_top.*	Top-level VHDL or Verilog HDL file that references the Reed-Solomon discrete decoder model file and test vectors.
rs_std_str.*	VHDL or Verilog HDL model files for the streaming decoder.
rs_var_dsc.*	VHDL or Verilog HDL model files for the discrete variable decoder.
rs_var_str.*	VHDL or Verilog HDL model files for the streaming variable decoder.
rs_vera_str.*	VHDL or Verilog HDL model files for the streaming variable decoder with erasures.
rs_vera_dsc.*	VHDL or Verilog HDL model files for the discrete variable decoder with erasures.

Download the Models

If you have not already done so, download Visual IP models from Altera's web site at **http://www.altera.com** by following the instructions below.

1. Point your web browser to **http://www.altera.com/IPmegastore**.
2. Search in the IP MegaStore for the function / model you wish to obtain.
3. On the search results page, click the name of the function / model you wish to obtain.
4. Click the Free Test Drive icon and follow the on-line instructions to download the function and / or model.

PC Installation

Execute the **rs_vip_pc.exe** file and follow the on-line instructions to install the model. See the **readme.txt** file for a listing of the files that are installed.

Before using the Visual IP models, set the VIP_MODELS_DIR environment variable to <*installation path*>**/vip_models**. The installation process sets all other required environment variables in the system registry.

All Altera Visual IP models use the VIP_MODELS_DIR environment variable. If you only wish to use one Visual IP model, you can install the model into any directory and set up the variable to point to that directory. However, if you wish to use several models (e.g., both the Reed-Solomon Compiler and a8237 models) you should install all Visual IP models into the same directory (e.g., <*installation path*>**/vip_models** / <*function name*>).

Solaris Installation

The Reed-Solomon Compiler model is a tape archive file (**.tar**) that has been compressed using the **gzip** utility. To extract the files, move the **rs_vip_solaris.tar.gz** file to the location in which you would like to install the models and type the following commands at a UNIX prompt:

```
gunzip rs_vip_solaris.tar.gz ↵
tar xvf rs_vip_solaris.tar ↵
```

See the **readme.txt** file for a listing of the files that are installed. Before using the Visual IP models, perform the following steps:

1. Set the VIP_MODELS_DIR environment variable to <*installation path*>**/vip_models**.

All Altera Visual IP models use the VIP_MODELS_DIR environment variable. If you only wish to use one Visual IP model, you can install the model into any directory and set up the variable to point to that directory. However, if you wish to use several models (e.g., both the Reed-Solomon Compiler and a8237 models) you should install all Visual IP models into the same directory (e.g., <*installation path*>**/vip_models** / <*function name*>).

2. Set the VIP_EU_ROOT environment variable to the root directory in which you installed the Visual IP software.

3. Set the VIP_RS_HEXFILES environment variable to a temporary directory (e.g., **/tmp**).

4. Source the **setup.csh** file to complete the configuration of the Visual IP environment.

Running Test Vectors

The Reed-Solomon Compiler Visual IP model includes test vectors for the standard encoder and the discrete decoder. This section describes how to use the test vectors provided with the simulation model.

Verilog HDL

If you are using Verilog HDL, perform the following steps to simulate the standard encoder:

1. Set up the PLI interface to the Visual IP software as described in *Installing the Visual IP Software User Guide*.

2. Make sure the VIP_MODELS_DIR environment variable is set properly.

3. Change to the <*installation path*>**/vip_simulation/rs/verilog** directory.

4. Compile the **rs_enc.v** and **rs_enc_vectors.v** files. These modules attach to the appropriate Visual IP models using the Verilog-XL PLI interface.

5. Compile the **rs_enc_vip_top.v** file.

6. Simulate **rs_enc_vip_top**.

To simulate the discrete decoder, perform the steps above using the **rs_std_dsc.v**, **rs_std_dsc_vectors.v**, and **rs_std_dcs_vip_top.v** files.

VHDL

If you are using VHDL, perform the following steps to simulate the standard encoder:

1. Set up the C language interface to the Visual IP software as described in *Installing the Visual IP Software User Guide*.

2. Make sure the VIP_MODELS_DIR environment variable is set properly.

3. Change to the directory <*installation path*>**/vip_simulation/rs/vhdl/**<*simulator*>, where <*simulator*> is to the VHDL simulation tool you are using.

4. Compile the **rs_enc.vhd** and **rs_enc_vectors.vhd** files into your work library. These components attach to the appropriate Visual IP models using the C language interface of your VHDL simulator.

5. Compile the **rs_enc_vip_top.vhd** file into your work library.

6. Simulate **work.rs_enc_vip_top(struct)**.

To simulate the discrete decoder, perform the steps above using the **rs_std_dsc.vhd**, **rs_std_dsc_vectors.vhd**, and **rs_std_dcs_vip_top.vhd** files.

Using the Reed-Solomon Model

This section describes how to use the Reed-Solomon simulation model in your designs.

Verilog HDL

If you are using Verilog HDL, go through the following steps:

1. Set up the PLI interface to the Visual IP software as described in *Installing the Visual IP Software User Guide*.

2. Make sure the `VIP_MODELS_DIR` environment variable is set properly.

3. Go to the <*installation path*>**/vip_simulation/rs/verilog** directory

4. Compile the Verilog HDL model that corresponds to the Reed-Solomon function you wish to simulate (e.g., the continuous decoder). This module attachs to the appropriate Visual IP model using the Verilog-XL PLI interface. Refer to Table 1.

5. Instantiate the model in yourVerilog HDL design. When you instantiate the model, you can modify the parameters as needed for your application.

The output files generated by the Reed-Solomon MegaWizard® Plug-In contain a parameterized instance of the function. You can use the output files with the model file to simulate a function with custom parameters.

VHDL

If you are using VHDL, perform the following steps:

1. Set up the C language interface to the Visual IP software as described in *Installing the Visual IP Software User Guide*.
2. Make sure the `VIP_MODELS_DIR` environment variable is set properly.
3. Go to the<*installation path*>**/vip_simulation/rs/vhdl/**<*simulator*> directory, where <*simulator*> is the VHDL simulation tool you are using.
4. Compile the VHDL model that corresponds to the Reed-Solomon function you wish to simulate (e.g., the continuous decoder). This component attaches to the appropriate Visual IP model using the C language interface of your VHDL simulator. Refer to Table 1.
5. Instantiate the model in your VHDL design. When you instantiate the model, you can modify the parameters as needed for your application.

The output files generated by the Reed-Solomon MegaWizard Plug-In contain a parameterized instance of the function. You can use the output files with the model file to simulate a function with custom parameters.

Known Issues

Visual IP models do not support checkpoint/restart. Therefore, you must reload the simulation model to restart the simulation.

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