IEEE 1149.1 JTAG Boundary-Scan Testing
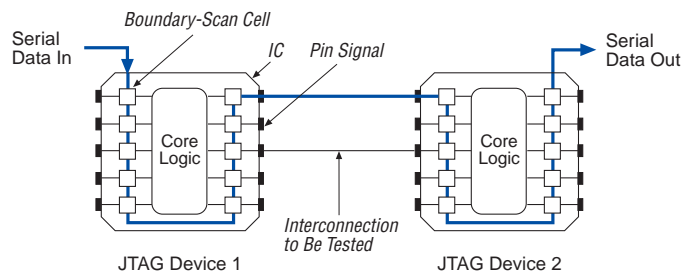
in Altera Devices

Introduction

As printed circuit boards (PCBs) become more complex, the need for thorough testing becomes increasingly important. Advances in surface-mount packaging and PCB manufacturing have resulted in smaller boards, making traditional test methods—external test probes and "bed-of-nails" test fixtures—harder to implement. As a result, cost savings from PCB space reductions are sometimes offset by cost increases in traditional testing methods.

In the 1980s, the Joint Test Action Group (JTAG) developed a specification for boundary-scan testing that was later standardized as the IEEE Std. 1149.1 specification. This boundary-scan test (BST) architecture offers the capability to efficiently test components on PCBs with tight lead spacing.

This BST architecture can test pin connections without using physical test probes and capture functional data while a device is operating normally. Boundary-scan cells (BSCs) in a device can force signals onto pins, or capture data from pin or core logic signals. Forced test data is serially shifted into the BSCs. Captured data is serially shifted out and externally compared to expected results. Figure 1 illustrates the concept of boundary-scan testing.

Figure 1. IEEE Std. 1149.1 Boundary-Scan Testing

Table 1 summarizes the Altera® devices that comply with the IEEE Std. 1149.1 specification by providing BST capability for input, output, and dedicated configuration pins.

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Table 1. Altera Devices with BST Capability	
Family	**Devices Supporting BST**
HardCopy® II	All devices
HardCopy Stratix®	All devices
Stratix	All devices
Stratix GX	All devices
Cyclone™	All devices
Mercury™	All devices
APEX™ II	All devices
APEX™ 20K, APEX 20KE	All devices
ACEX® 1K	All devices
FLEX® 10K, FLEX 10KE	All devices
FLEX 8000	EPF8282A, EPF8282AV, EPF8636A, EPF8820A, EPF81500A
FLEX 6000	All devices
MAX® 9000 (including MAX 9000A)	All devices
MAX 7000S *(1)*	EPM7128S, EPM7160S, EPM7192S, EPM7256S
MAX 7000A	All devices
MAX 7000B	All devices
MAX 3000A	All devices
Configuration Devices	EPC2, EPC4, EPC8, EPC16

Note to Table 1:

(1)   Although EPM7032S and EPM7064S devices contain circuitry to support the Test Access Port (TAP) controller, these devices do not offer the BSCs required to support the EXTEST and SAMPLE/PRELOAD instructions. When the instruction register is updated with these instructions, the BYPASS register is selected. Therefore, you can place EPM7032S and EPM7064S devices in a chain of boundary-scan test (BST) devices.

This application note discusses how to use the IEEE Std. 1149.1 BST circuitry in Altera devices. The topics are as follows:

- IEEE Std. 1149.1 BST architecture
- IEEE Std. 1149.1 boundary-scan register for each Altera device family
- IEEE Std. 1149.1 BST operation control
- Enabling IEEE Std. 1149.1 BST circuitry for each Altera device family
- Guidelines for IEEE Std. 1149.1 boundary-scan testing
- Boundary-Scan Description Language (BSDL) support
- References

In addition to BST, you can use the IEEE Std. 1149.1 controller for in-system programming or for in-circuit reconfiguration for Altera devices with that feature. The MAX 3000A, MAX 7000AE, MAX 7000B, and enhanced configuration devices support IEEE 1532 programming, which utilizes the IEEE Std. 1149.1 TAP interface. This application note only discusses the BST feature of the IEEE Std. 1149.1 circuitry.

For more information on using IEEE Std. 1149.1 circuitry for in-system programming and in-circuit reconfiguration, see the following documents:

■ *Stratix Handbook Chapter: Configuring Stratix and Stratix GX Devices*
■ *Cyclone Handbook Chapter: Configuring Cyclone Devices*
■ *Application Note 33 (Configuring FLEX 8000 Devices)*
■ *Application Note 38 (Configuring Multiple FLEX 8000 Devices)*
■ *Application Note 95 (In-System Programmability in MAX Devices)*
■ *Configuration Handbook Chapter: Enhanced Configuration Devices Data Sheet*
■ *Configuration Handbook Chapter: Configuration Devices for SRAM-based LUT Devices Data Sheet*

IEEE Std. 1149.1 BST Architecture

A device operating in IEEE Std. 1149.1 BST mode uses four required pins, TDI, TDO, TMS, and TCK, and one optional pin, TRST. Table 2 summarizes the functions of each of these pins.

Table 2. IEEE Std. 1149.1 Pin Descriptions (Part 1 of 2)		
Pin	**Description**	**Function**
TDI	Test data input	Serial input pin for instructions as well as test and programming data. Data is shifted in on the rising edge of TCK.
TDO	Test data output	Serial data output pin for instructions as well as test and programming data. Data is shifted out on the falling edge of TCK. The pin is tri-stated if data is not being shifted out of the device.
TMS	Test mode select	Input pin that provides the control signal to determine the transitions of the TAP controller state machine. Transitions within the state machine occur at the rising edge of TCK. Therefore, TMS must be set up before the rising edge of TCK. TMS is evaluated on the rising edge of TCK.
TCK	Test clock input	The clock input to the BST circuitry. Some operations occur at the rising edge, while others occur at the falling edge.

| Table 2. IEEE Std. 1149.1 Pin Descriptions (Part 2 of 2)		
Pin	**Description**	**Function**
TRST	Test reset input (optional)	Active-low input to asynchronously reset the boundary-scan circuit. (TRST is optional according to IEEE Std. 1149.1). This pin should be driven low when not in boundary scan operation and for non-JTAG users the pin should be permanently tied to GND. It is not supported by all families.

Altera devices either have pins dedicated for IEEE Std. 1149.1 operation or the IEEE Std. 1149.1 pins are dual purpose; they can either be used for JTAG only or as regular I/O pins. For the families that support it, you can use the four JTAG pins as I/O pins by turning off the JTAG option with the MAX+PLUS® II or Quartus® II software (see "Enabling IEEE Std. 1149.1 BST Circuitry" on page 32 of this application note). Go to the appropriate device family data sheet for specific information on device and package combinations.

The IEEE Std. 1149.1 BST circuitry requires the following registers:

- The instruction register, which is used to determine the action to be performed and the data register to be accessed.
- The bypass register, which is a 1-bit-long data register used to provide a minimum-length serial path between TDI and TDO.
- The boundary-scan register, which is a shift register composed of all the BSCs of the device.

Figure 2 shows a functional model of the IEEE Std. 1149.1 circuitry.

Figure 2. IEEE Std. 1149.1 Circuitry
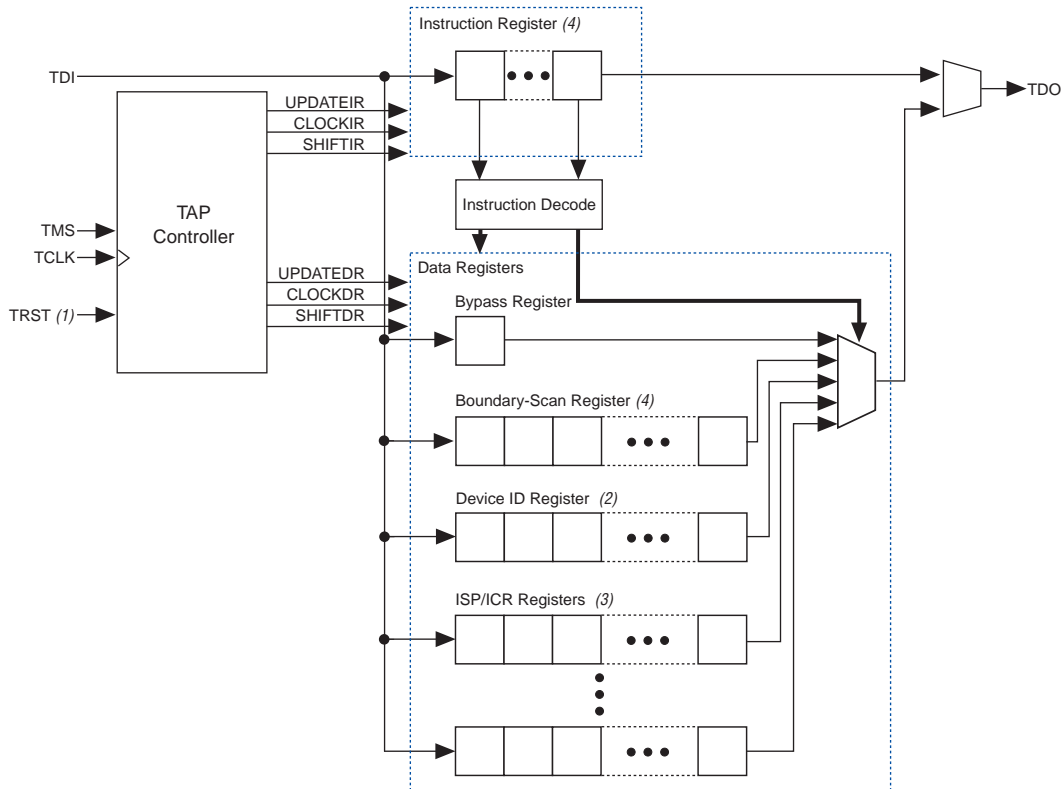
Notes to Figure 2:
(1)   The TRST pin is optional. Check the data sheet and pin tables for individual device support.
(2)   The device ID register is available in all JTAG-compliant families except EPM9320 and EPM9560 devices.
(3)   The private registers are used for in-system programmability (ISP) in MAX 9000 (including MAX 9000A),
      MAX 7000A, MAX 7000B, MAX 7000S, and MAX 3000A devices and for in-circuit reconfigurability (ICR) in Stratix,
      Mercury, APEX II, APEX 20K, ACEX 1K, and FLEX 10K devices.
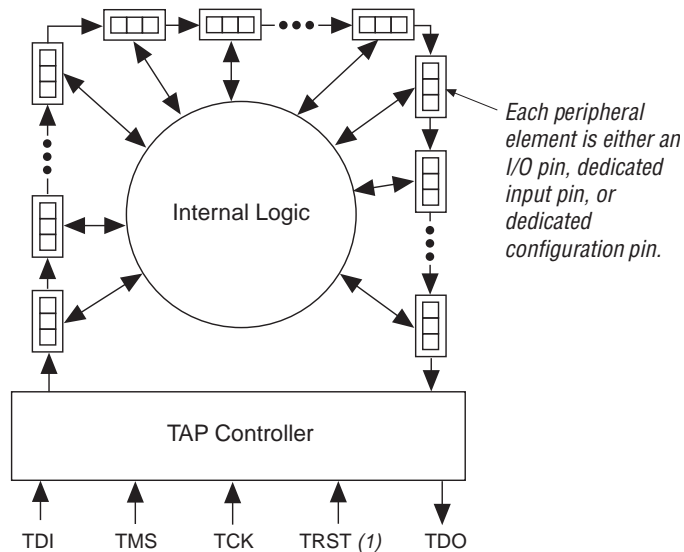(4)   Refer to the appropriate device family data sheet for register lengths.

IEEE Std. 1149.1 boundary-scan testing is controlled by a TAP controller, which is described in "IEEE Std. 1149.1 Std. Operation Control" on page 22 of this application note. The TMS, TRST, and TCK pins operate the TAP controller, and the TDI and TDO pins provide the serial path for the data registers. The TDI pin also provides data to the instruction register, which then generates control logic for the data registers.

IEEE Std. 1149.1 Boundary-Scan Register

The boundary-scan register is a large serial shift register that uses the TDI pin as an input and the TDO pin as an output. The boundary-scan register consists of 3-bit peripheral elements that are either I/O pins, dedicated inputs, or dedicated configuration pins. You can use the boundary-scan register to test external pin connections or to capture internal data. Figure 3 shows how test data is serially shifted around the periphery of the IEEE Std. 1149.1 device.

Figure 3. Boundary-Scan Register

Each peripheral element is either an I/O pin, dedicated input pin, or dedicated configuration pin.

Note to Figure 3:
(1)   Refer to the appropriate device family data sheet for TRST pin availability.

Altera Device I/O Pins

The 3-bit BSC consists of a set of capture registers and a set of update registers for each I/O pin. The capture registers connect to internal device data via the OUTJ, OEJ, and I/O pin signals, while the update registers connect to external data through the PIN_OUT, PIN_OE, and/or INJ signals. The global control signals for the IEEE Std. 1149.1 BST registers (for example, SHIFT, CLOCK, and UPDATE) are generated internally by the TAP controller; the MODE signal is generated by a decode of the instruction register. The HIGH-Z signal and connections are only available in some of the device families (for example, Stratix or Cyclone devices). See figures for specific device family details. The data signal path for the boundary-scan register runs from the serial data in (SDI) signal to the serial data out (SDO) signal. The scan register begins at the TDI pin and ends at the TDO pin of the device.

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Altera Device Dedicated Inputs

The boundary-scan register also includes dedicated input pins. Because these pins have special functions, some bits of the boundary-scan register are internally connected to V_{CC} or ground, or are used only for device configuration; these bits are either forced to a static high (1) or low (0), or used internally for configuration. The BSDL file may preclude test ability on some of these pins.

Altera Device Dedicated Clock Input Pins

The boundary-scan register also includes dedicated clock input pins. Because these pins have special functions, some bits of the boundary-scan register are internally connected to V_{CC} or ground before configuration; these bits are thus forced to a static high (1) or low (0) state.

These pins continue to clock internal user registers, but the capture register associated with the pin can be used for external pin connectivity tests. The pin can receive data but cannot force data onto external connections. The data values associated with the other two capture registers should be ignored.

Altera Device Dedicated Clock Output Pins

The boundary-scan register also includes dedicated clock output pins. Because these pins have special output functions, the input update register cannot drive to the core logic or user registers. The capture register associated with the pin can be used for external pin connectivity tests. The pin can force and capture data (to the capture register).

Altera Device Dedicated Configuration Pins

The boundary-scan register includes dedicated configuration pins for FPGA devices. These include dedicated bidirectional and output configuration pins. Because these pins have special functions, some bits of the boundary-scan register are internally connected to V_{CC} or ground, or are used only for device configuration; these bits are either forced to a static high (1) or low (0) state, or used internally for configuration.

These pins are used only during FPGA configuration, but the capture register associated with the pin can be used for external pin connectivity tests. The pin can receive data but cannot force data onto external connections. The data values associated with the other two capture registers should be ignored.

JTAG Pins (TDI, TDO, TMS, TCK & TRST)

Altera devices do not have BSCs for the dedicated JTAG pins: TDI, TDO, TMS, TCK, or TRST (if available).

Altera Device Family Specific BSCs

The following sections show the I/O BSC diagram for each device family. Within each section, device specific tables describe the BSC for pins other than I/O pins (dedicated clock input, dedicated function pins, and dedicated configuration pins).

HardCopy II, HardCopy Stratix, Stratix, Stratix GX, Cyclone & APEX II Boundary Scan Cells

Figure 4 shows the user I/O BSC for HardCopy II, HardCopy Stratix, Stratix, Stratix GX, Cyclone, and APEX II devices.

Figure 4. HardCopy II, HardCopy Stratix, Stratix, Stratix GX, Cyclone & APEX II User I/O BSC with IEEE Std. 1149.1 BST Circuitry
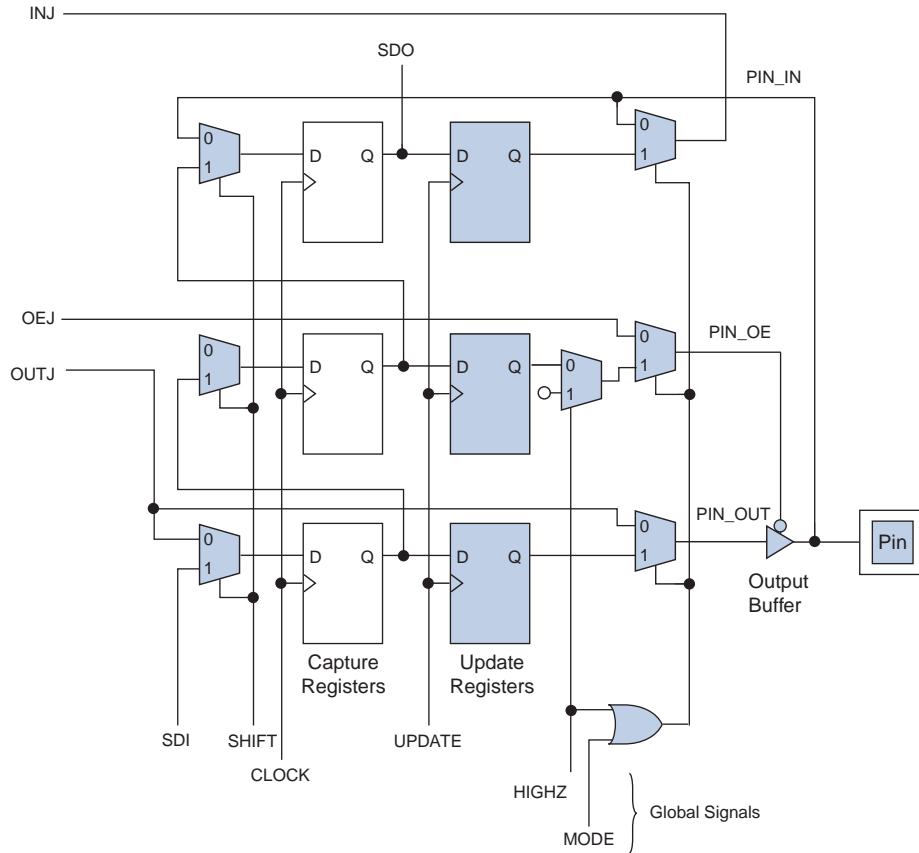
Tables 3 and 4 describe the capture and update register capabilities of all BSCs within HardCopy II, HardCopy Stratix, Stratix, Stratix GX, Cyclone, and APEX II devices. They describe user I/O pins (that match Figure 4 exactly), dedicated clock input, dedicated inputs, dedicated bidirectional, and dedicated outputs cells.

Table 3. HardCopy II, HardCopy Stratix, Stratix, Stratix GX & Cyclone Device BSC Descriptions						*Note (1)*
Pin Type	**Output Capture Register**	**OE Capture Register**	**Input Capture Register**	**Output Update Register**	**OE Update Register**	**Input Update Register**	**Notes**
	Captures			**Drives**			
User I/O pin	OUTJ	OEJ	PIN_IN	PIN_OUT	PIN_OE	INJ	
Dedicated clock input	0	1	PIN_IN	N.C. *(5)*	N.C. *(5)*	N.C. *(5)*	PIN_IN drives to clock network or core logic
Dedicated input *(2)*	0	1	PIN_IN	N.C. *(5)*	N.C. *(5)*	N.C. *(5)*	PIN_IN drives to control logic
Dedicated bidirectional *(3)*	0	OEJ	PIN_IN	N.C. *(5)*	N.C. *(5)*	N.C. *(5)*	PIN_IN drives to configuration control
Dedicated output *(4)*	OUTJ	0	0	N.C. *(5)*	N.C. *(5)*	N.C. *(5)*	OUTJ drives to output buffer

Notes to Table 3:
(1)   All VCC, VREF, GND, GX_RX, GX_TX, RREF, REFCLK, and TEMP_DIODE pins do not have BSCs.
(2)   For Stratix and Stratix GX this includes pins PLL_ENA, nCONFIG, MSEL0, MSEL1, MSEL2, DCLK, nCE, VCCSEL, PORSEL, nIO_PULLUP. For Cyclone, this includes nCONFIG, MSEL0, MSEL1, DCLK, and nCE.
(3)   This includes pins CONF_DONE and nSTATUS.
(4)   This includes pin nCEO.
(5)   N.C.: No Connect.

Table 4. APEX II Device BSC Descriptions *Note (1)*

Pin Type	Output Capture Register	OE Capture Register	Input Capture Register	Output Update Register	OE Update Register	Input Update Register	Detail
	Captures			Drives			
User I/O pin	OUTJ	OEJ	PIN_IN	PIN_OUT	PIN_OE	INJ	
Dedicated clock input *(2)*	0	1	PIN_IN	N.C. *(7)*	N.C. *(7)*	N.C. *(7)*	PIN_IN drives to core logic
Dedicated input *(3)*	0	1	PIN_IN	N.C. *(7)*	N.C. *(7)*	N.C. *(7)*	PIN_IN drives to control logic
Dedicated clock output *(4)*	OUTJ	OEJ	PIN_IN	PIN_OUT	PIN_OE	N.C. *(7)*	OUTJ and OEJ driven from PLL
Dedicated bidirectional *(5)*	0	OEJ	PIN_IN	N.C. *(7)*	N.C. *(7)*	N.C. *(7)*	PIN_IN drives to configuration control
Dedicated output *(6)*	OUTJ	0	0	N.C. *(7)*	--	N.C. *(7)*	OUTJ drives to output buffer

Notes to Table 4:
(1)   TDI, TDO, TMS, TCK, and TRST pins and all VCC and GND pin types do not have BSCs.
(2)   Includes CLKp and CLKLK_FBINp pins.
(3)   Includes pins PLL_ENA, DATA0, nCONFIG, MSEL0, MSEL1, DCLK, nCE, VCCSEL, and nIO_PULLUP.
(4)   Includes CLKLK_OUTp pins.
(5)   Includes pins CONF_DONE and nSTATUS.
(6)   Includes pin nCEO.
(7)   N.C.: No Connect.

Mercury BSCs

Figure 5 shows the user I/O BSC for Mercury devices.

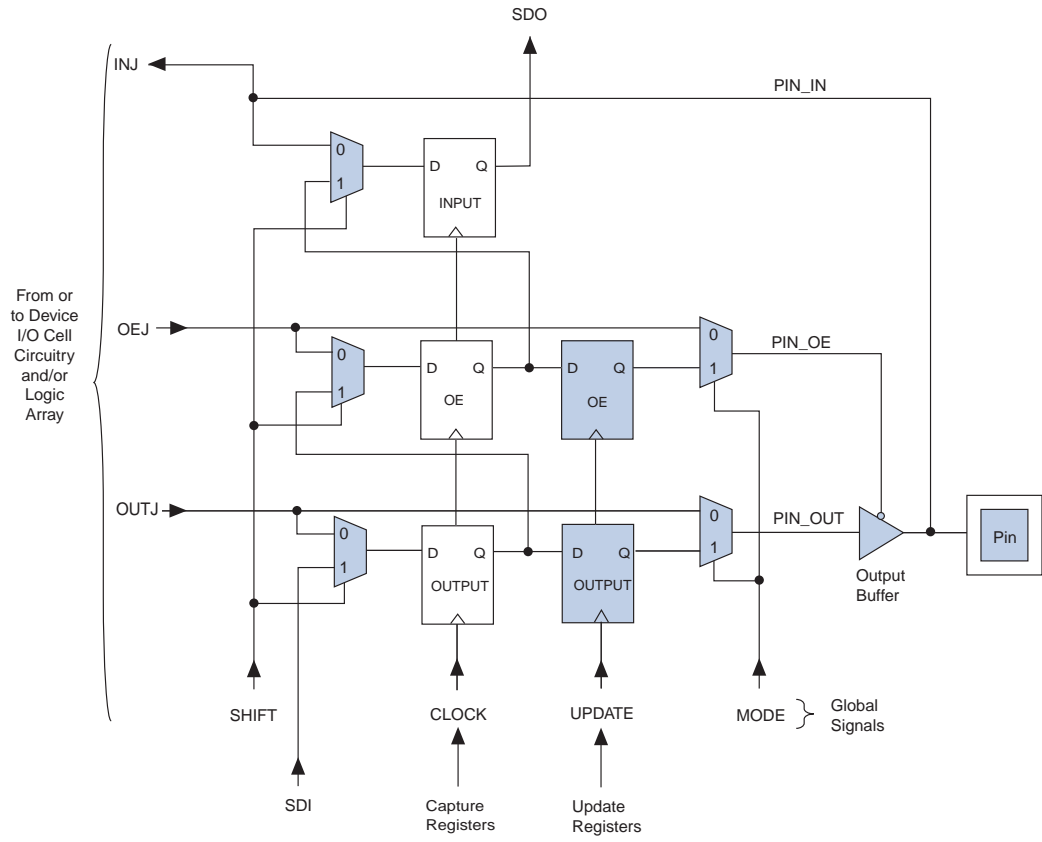*Figure 5. A Mercury User I/O BSC with IEEE Std. 1149.1 BST Circuitry*

Table 5 describes the capture and update register capabilities of all BSCs within Mercury devices. It describes user I/O pins (will match Figure 5 exactly), dedicated clock input, dedicated inputs, dedicated bidirectional and dedicated outputs cells.

Table 5. Mercury Device BSC Descriptions   *Note (1)*

Pin Type	Output Capture Register	OE Capture Register	Input Capture Register	Output Update Register	OE Update Register	Input Update Register	Details
	Captures			Drives			
User I/O pins	OUTJ	OEJ	PIN_IN	PIN_OUT	PIN_OE	N.C. *(7)*	
Dedicated clock input *(2)*	0	1	PIN_IN	N.C. *(7)*	N.C. *(7)*	N.C. *(7)*	PIN_IN drives to core logic
Dedicated input *(3)*	0	1	PIN_IN	N.C. *(7)*	N.C. *(7)*	N.C. *(7)*	PIN_IN drives to control logic
Dedicated clock output *(4)*	OUTJ	OEJ	PIN_IN	PIN_OUT	PIN_OE	N.C. *(7)*	OUTJ and OEJ driven from PLL
Dedicated bidirectional *(5)*	0	OEJ	PIN_IN	N.C. *(7)*	N.C. *(7)*	N.C. *(7)*	PIN_IN drives to configuration control
Dedicated output *(6)*	OUTJ	0	0	N.C. *(7)*	N.C. *(7)*	N.C. *(7)*	OUTJ drives to output buffer

Notes to Table 5:

(1) All VCC and GND pin types do not have BSCs.
(2) Includes CLKp/n, HSDI_CLKp/n, and CLKLK_FBINp/n pins.
(3) Includes pins PLL_ENA, DATA0, nCONFIG, MSEL0, MSEL1, DCLK, nCE, VCCSEL, nIO_PULLUP.
(4) Includes CLKLK_OUTp/n and HSDI_TXCLKOUTp/n pins.
(5) Includes pins CONF_DONE and nSTATUS.
(6) Includes pin nCEO and PLLRDY.
(7) N.C.: No Connect.

APEX 20K, ACEX 1K, FLEX 10K, FLEX 6000 & FLEX 8000 BSCs

Figure 6 shows the user I/O BSC for APEX 20K, ACEX 1K, FLEX 10K, FLEX 6000, and FLEX 8000 devices.

Figure 6. An APEX 20K, ACEX 1K, FLEX 10K, FLEX 6000 & FLEX 8000 User I/O BSC with IEEE Std. 1149.1 BST Circuitry
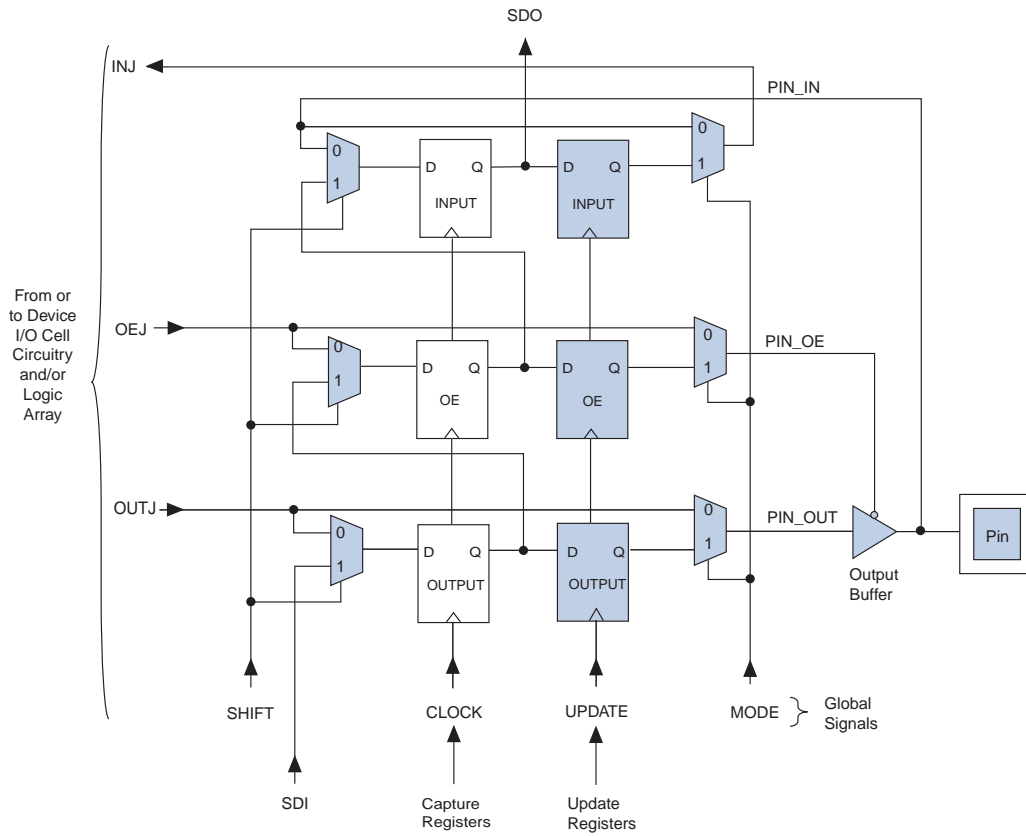
Table 6 describes the capture and update register capabilities of all BSCs within APEX 20K, ACEX 1K, FLEX 10K, FLEX 6000, and FLEX 8000 devices. It describes user I/O pins (will match Figure 4 exactly), dedicated clock input, dedicated inputs, dedicated bi-directional, and dedicated outputs cells.

Table 6. APEX 20K, ACEX 1K, FLEX 10K, FLEX 6000 & FLEX 8000 Device BSC Descriptions							*Note (1)*
Pin Type	**Output Capture Register**	**OE Capture Register**	**Input Capture Register**	**Output Update Register**	**OE Update Register**	**Input Update Register**	**Detail**
	Captures			**Drives**			
User I/O pin	OUTJ	OEJ	PIN_IN	PIN_OUT	PIN_OE	INJ	
Dedicated clock input *(2)*	0	1	PIN_IN	N.C. *(8)*	N.C. *(8)*	N.C. *(8)*	PIN_IN drives to clock network or core logic
Dedicated input *(3)*	0	1	PIN_IN	N.C. *(8)*	N.C. *(8)*	INJ	PIN_IN drives to core logic
Dedicated clock output *(4)*	OUTJ	OEJ	PIN_IN	PIN_OUT	PIN_OE	N.C. *(8)*	OUTJ and OEJ driven from PLL
Dedicated configuration input	0	1	PIN_IN	N.C. *(8)*	N.C. *(8)*	N.C. *(8)*	PIN_IN drives to configuration control
Dedicated open-drain configuration *(5)*	0	OEJ	PIN_IN	N.C. *(8)*	N.C. *(8)*	N.C. *(8)*	PIN_IN drives to configuration control
Dedicated bidirectional *(6)*	INJ	OEJ	PIN_IN	N.C. *(8)*	N.C. *(8)*	N.C. *(8)*	PIN_IN drives to configuration control
Dedicated output *(7)*	OUTJ	0	0	N.C. *(8)*	N.C. *(8)*	N.C. *(8)*	OUTJ drives to output buffer

Notes to Table 6:
(1) All VCC and GND pin types do not have BSCs.
(2) For APEX 20KE devices, these pins include CLKp/n, HSDI_CLKp/n, and CLKLK_FBINp/n pins; for APEX 20K and FLEX devices, these pins include CLK pins.
(3) For APEX 20KE devices, this includes pins PLL_ENA, DATA0, nCONFIG, MSEL0, MSEL1, DCLK, nCE; for APEX 20K, ACEX, and FLEX 10K devices, these pins include nCONFIG, MSEL0, MSEL1, nCE, and DCLK; for FLEX 8000 devices, these pins include nCONFIG, nSP, MSEL0, MSEL1; for FLEX 6000 devices, these pins include nCONFIG, MSEL, nCE, and DCLK.
(4) For APEX 20KE devices, these pins include CLKLK_OUTp/n.
(5) These pins include CONF_DONE and nSTATUS.
(6) For FLEX 8000 devices, these pins include DCLK and DATA.
(7) For APEX, ACEX, FLEX 10K, and FLEX 6000 devices, these pins include nCEO and PLLRDY.
(8) N.C.: No Connect.

MAX 9000 BSCs

Figure 7 shows the user I/O BSC for MAX 9000 devices.

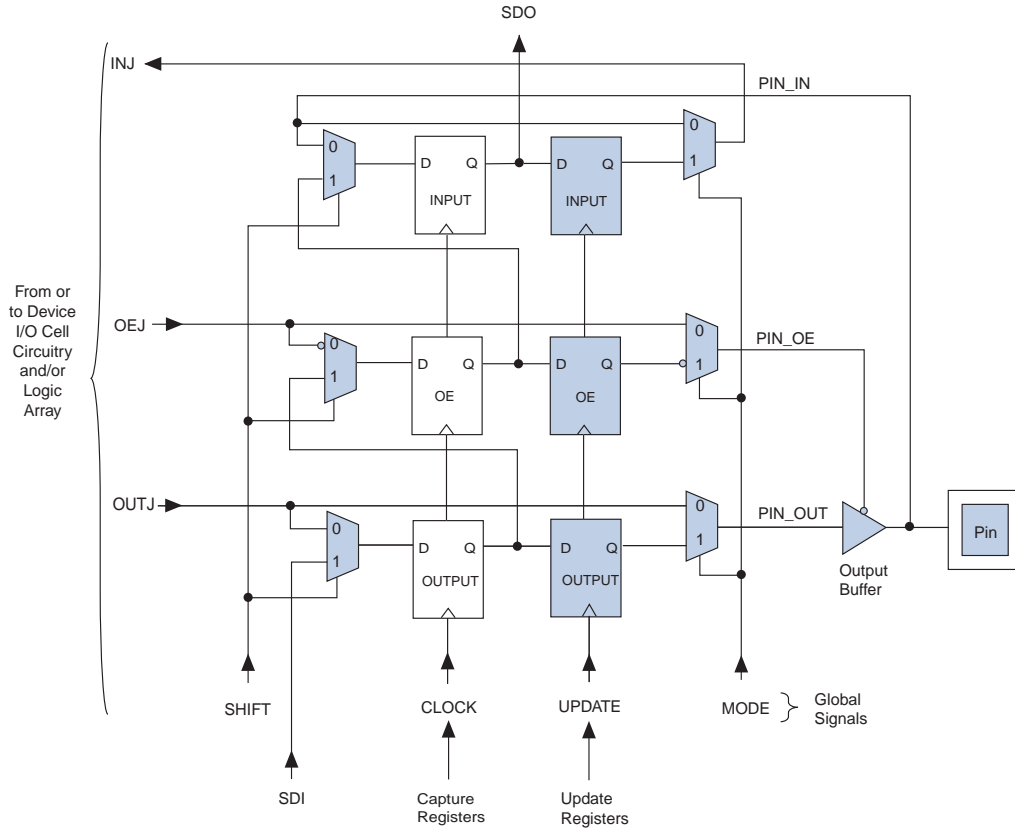*Figure 7. A MAX 9000 User I/O BSC with IEEE Std. 1149.1 BST Circuitry*

Table 7 describes the capture and update register capabilities of all BSCs within MAX 9000 devices. It describes user I/O pins (will match Figure 7 exactly), and dedicated inputs.

Table 7. MAX 9000 Device BSC Descriptions						*Note (1)*
Pin Type	**Output Capture Register**	**OE Capture Register**	**Input Capture Register**	**Output Update Register**	**OE Update Register**	**Input Update Register**	**Detail**
	Captures			**Drives**			
User I/O pin	`OUTJ`	`OEJ`	`PIN_IN`	`PIN_OUT`	`PIN_OE`	`INJ`	
Dedicated input *(2)*	0	0	`PIN_IN`	N.C.*(3)*	N.C.*(3)*	N.C.*(3)*	`PIN_IN` drives to core logic

Notes to Table 7:
(1)   All `VCC` and `GND` pins do not have BSCs.
(2)   These pins include `DIN1`, `DIN2`, `DIN3`, and `DIN4`.
(3)   N.C.: No Connect.

MAX 7000S, MAX 7000A, MAX 7000B & MAX 3000A BSCs

Figure 8 shows the user I/O BSC for MAX 7000S, MAX 7000A, MAX 7000B, and MAX 3000A devices.

Figure 8. A MAX 7000S, MAX 7000A, MAX 7000B & MAX 3000A User I/O BSC with IEEE Std. 1149.1 BST Circuitry
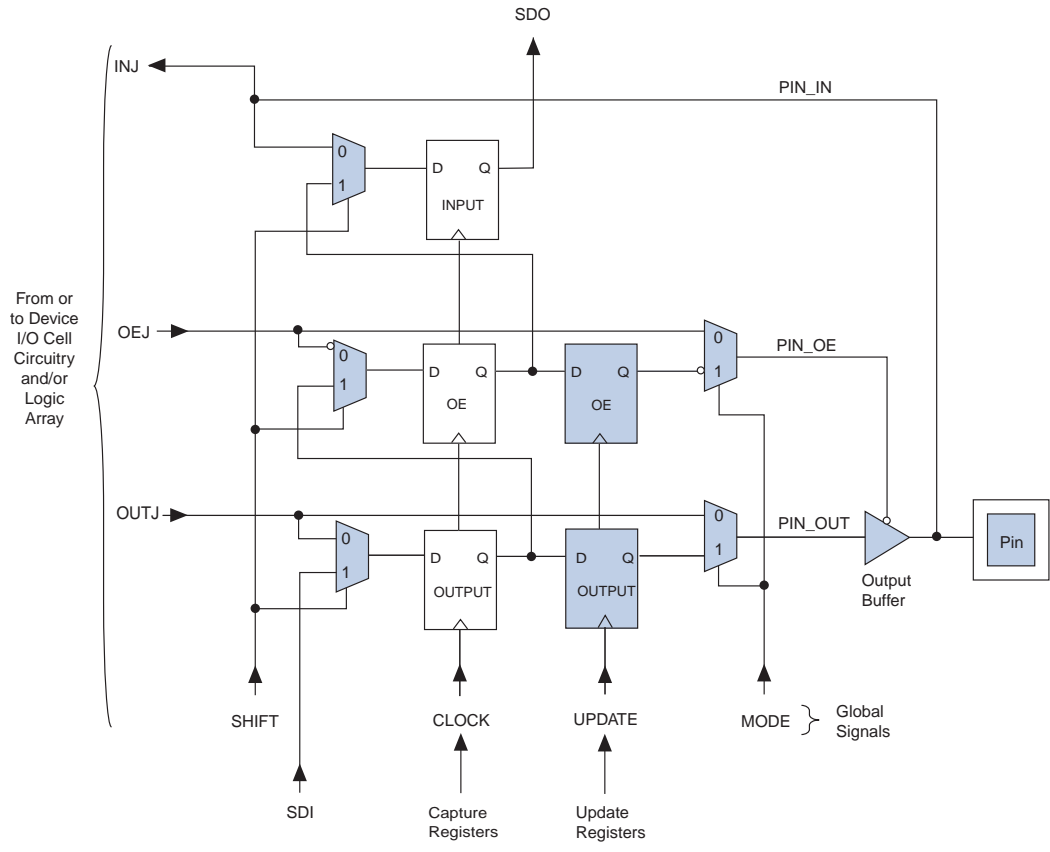

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Table 8 describes the capture and update register capabilities of all BSCs within MAX 7000S, MAX 7000A, MAX 7000B, and MAX 3000A devices. It describes user I/O pins (will match Figure 7 exactly), and dedicated inputs.

| *Table 8. MAX 7000S, MAX 7000A, MAX 7000B & MAX 3000A Device BSC Descriptions*							*Note (1)*
Pin Type	**Output Capture Register**	**OE Capture Register**	**Input Capture Register**	**Output Update Register**	**OE Update Register**	**Input Update Register**	**Detail**
	Captures			**Drives**			
User I/O pins	OUTJ	OEJ	PIN_IN	PIN_OUT	PIN_OE	INJ	
Dedicated input *(2)*	0	0	PIN_IN	N.C. *(3)*	N.C. *(3)*	N.C. *(3)*	PIN_IN drives to core logic

Notes to Table 8:
(1) All VCC and GND pins do not have BSCs.
(2) These pins include all four dedicated inputs.
(3) N.C. No Connect.

EPC16, EPC8, EPC4 & EPC2 BSCs

Figure 9 shows the user I/O BSC for EPC16, EPC8, EPC4, and EPC2 configuration devices.

Figure 9. An EPC16, EPC8, EPC4 & EPC2 I/O BSC with IEEE Std. 1149.1 BST Circuitry   *Note (1)*
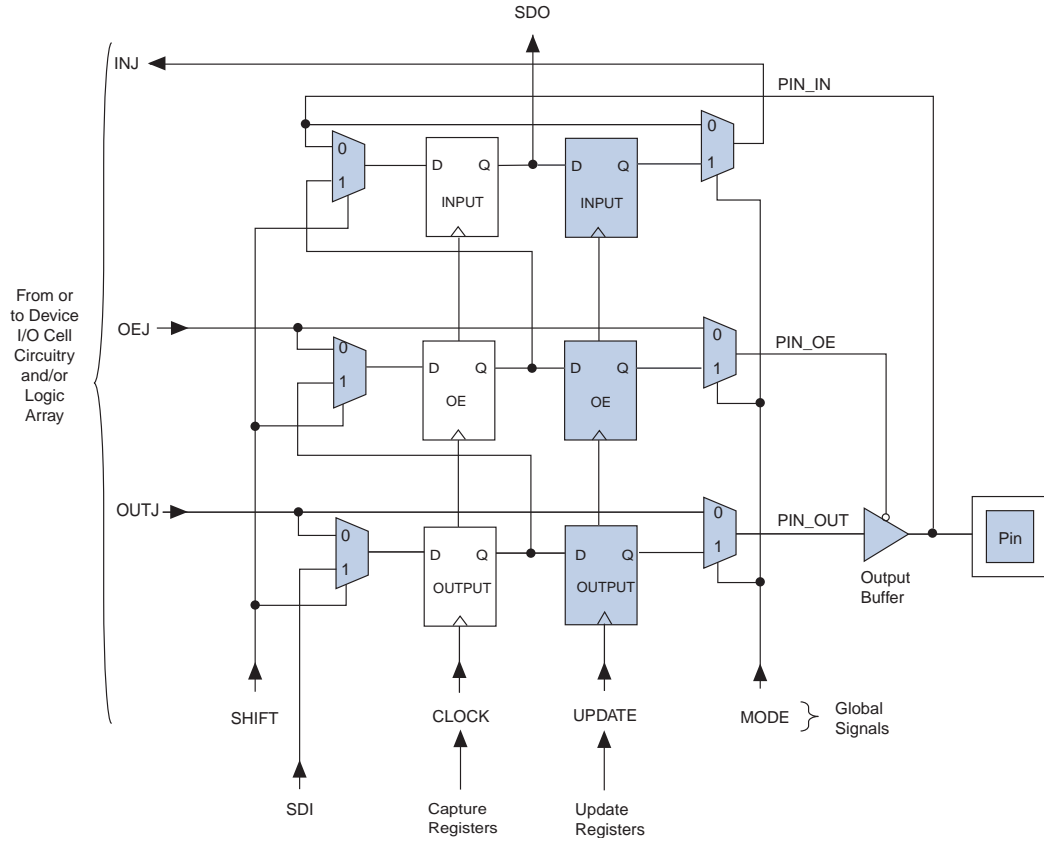
Note to Figure 9:
(1)   The EPC2 tri-state buffer is active-high.

Tables 9 and 10 describe the capture and update register capabilities of all BSCs within EPC16, EPC8, EPC4, and EPC2 configuration devices. They describe I/O pins (will match Figure 8 exactly), and dedicated input and open-drain pins.

Table 9. EPC16, EPC8 & EPC4 Device BSC Descriptions   Note (1)

Pin Type	Output Capture Register	OE Capture Register	Input Capture Register	Output Update Register	OE Update Register	Input Update Register	Detail
	Captures			Drives			
I/O pin (2)	OUTJ	OEJ	PIN_IN	PIN_OUT	PIN_OE	INJ	
Input only (3)	0	1	PIN_IN	N.C. (5)	N.C. (5)	INJ	PIN_IN also drives to core logic
Open-drain pins (4)	0	OEJ	PIN_IN	N.C. (5)	PIN_OE	INJ	OEJ driven from core

Notes to Table 9:
(1) All VCC and GND pin types do not have BSCs.
(2) These pins include DCLK, DATA, DQ, C_WE, C_RP, OEN, and some C_A, and A pins. Check the BSDL file for more information.
(3) These pins include nCS, EXTCLK, PORSEL, PGM0, PGM1, and PGM2.
(4) This pin includes nINIT_CONF.
(5) N.C.: No Connect

Table 10. EPC2 Device BSC Descriptions   Note (1)

Pin Type	Output Capture Register	OE Capture Register	Input Capture Register	Output Update Register	OE Update Register	Input Update Register	Detail
	Captures			Drives			
I/O pin (2)	OUTJ	OEJ	PIN_IN	PIN_OUT	PIN_OE	INJ	
Input only (3)	0	0	PIN_IN	N.C. (5)	N.C. (5)	INJ	PIN_IN also drives to core logic
Open-drain pins (4)	0	OEJ	PIN_IN	N.C. (5)	PIN_OE	INJ	OEJ driven from core

Notes to Table 10:
(1) All VCC and GND pin types do not have BSCs.
(2) These pins include DCLK, DATA, and nCASC pins.
(3) These pins include pins nCS, VPPSEL, and VCCSEL. The MODE signal is permanently tied low for VPPSEL and VCCSEL BSCs.
(4) These pins include nINIT_CONF.
(5) N.C.: No Connect.

IEEE Std. 1149.1 Std. Operation Control

Altera IEEE Std. 1149.1 devices implement the following BST instructions: SAMPLE/PRELOAD, EXTEST, BYPASS, USERCODE, IDCODE, CLAMP, and HIGHZ. Table 11 summarizes the BST instructions, which are described in detail later in this application note. Instructions that are available for specific devices can be found in the device-specific BSDL file on the Altera Web site.

Table 11. Boundary Scan Instructions & Descriptions	
Mode	**Description**
SAMPLE/ PRELOAD	Allows a snapshot of the signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins.
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through the selected device to adjacent devices during normal device operation.
IDCODE	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
USERCODE	Selects the USERCODE register and places it between TDI and TDO, allowing the USERCODE to be serially shifted out of TDO.
CLAMP *(1)*	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation, while holding I/O pins to a state defined by the data in the boundary scan register.
HIGHZ *(1)*	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation, while tri-stating all of the I/O pins.

Note to Table 11:
(1)   Bus hold and weak pull-up features override the high-impedance state of HIGHZ, CLAMP, and EXTEST.

The IEEE Std. 1149.1 TAP controller, a 16-state state machine clocked on the rising edge of TCK, uses the TMS pin to control IEEE Std. 1149.1 operation in the device. Figure 10 shows the TAP controller state machine.

Figure 10. IEEE Std. 1149.1 TAP Controller State Machine
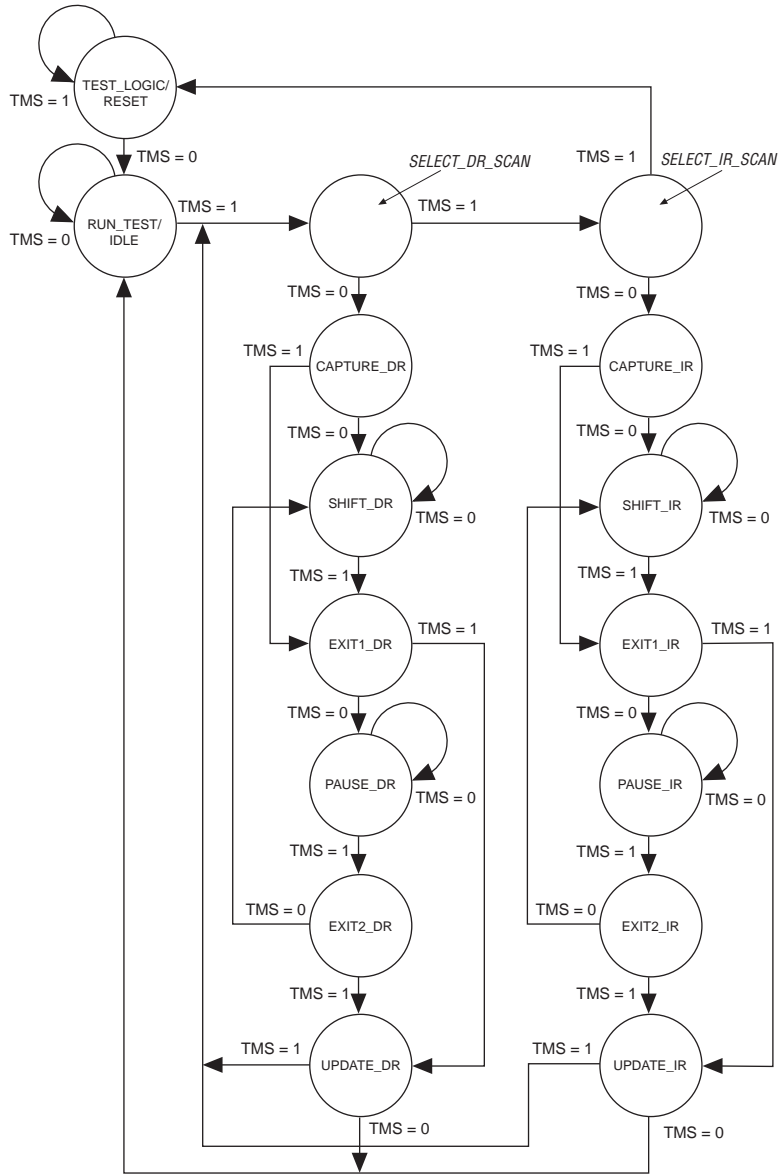
When the TAP controller is in the TEST_LOGIC/RESET state, the BST circuitry is disabled, the device is in normal operation, and the instruction register is initialized. If the device supports IDCODE, this initial instruction is IDCODE; otherwise, it is BYPASS. At device power-up, the TAP controller starts in this TEST_LOGIC/RESET state.

In addition, the TAP controller may be forced to the TEST_LOGIC/RESET state by holding TMS high for five TCK clock cycles or by holding the TRST pin low (if the optional TRST pin is supported). Once in the TEST_LOGIC/RESET state, the TAP controller remains in this state as long as TMS continues to be held high while TCK is clocked or TRST continues to be held low. Figure 11 shows the timing requirements for the IEEE Std. 1149.1 signals.

Figure 11. IEEE Std. 1149.1 Timing Waveforms
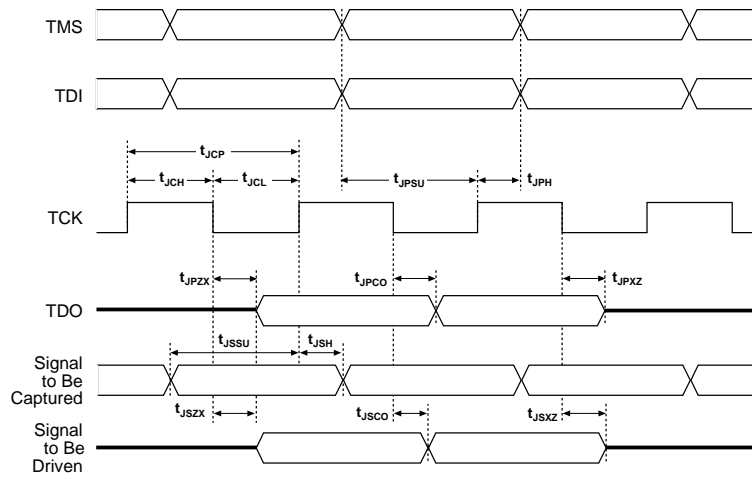
The timing values for each Altera device are provided in the appropriate device family data sheet.

To start IEEE Std. 1149.1 operation, select an instruction mode by advancing the TAP controller to the shift instruction register (SHIFT_IR) state and shift in the appropriate instruction code on the TDI pin. The waveform diagram in Figure 12 represents the entry of the instruction code into the instruction register. It shows the values of TCK, TMS, TDI, and TDO and the states of the TAP controller. From the RESET state, TMS is clocked with the pattern 01100 to advance the TAP controller to SHIFT_IR.

Figure 12. Selecting the Instruction Mode
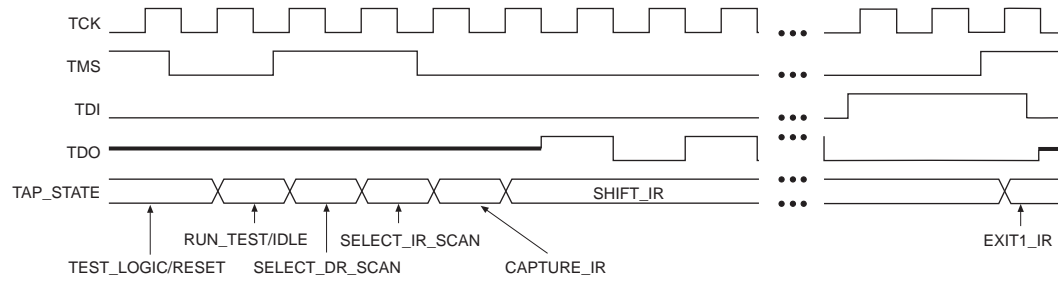
The TDO pin is tri-stated in all states except in the SHIFT_IR and SHIFT_DR states. The TDO pin is activated at the first falling edge of TCK after entering either of the shift states and is tri-stated at the first falling edge of TCK after leaving either of the shift states.

When the SHIFT_IR state is activated, TDO is no longer tri-stated, and the initial state of the instruction register is shifted out on the falling edge of TCK. TDO continues to shift out the contents of the instruction register as long as the SHIFT_IR state is active. The TAP controller remains in the SHIFT_IR state as long as TMS remains low.

During the SHIFT_IR state, an instruction code is entered by shifting data on the TDI pin on the rising edge of TCK. The last bit of the opcode must be clocked at the same time that the next state, EXIT1_IR, is activated; EXIT1_IR is entered by clocking a logic high on TMS. Once in the EXIT1_IR state, TDO becomes tri-stated again. TDO is always tri-stated except in the SHIFT_IR and SHIFT_DR states. After an instruction code is entered correctly, the TAP controller advances to perform the serial shifting of test data in one of three modes—SAMPLE/PRELOAD, EXTEST, or BYPASS—that are described below.

SAMPLE/PRELOAD Instruction Mode

The SAMPLE/PRELOAD instruction mode allows you to take a snapshot of device data without interrupting normal device operation. However, this instruction mode is most often used to preload the test data into the update registers prior to loading the EXTEST instruction. Figure 13 shows the capture, shift, and update phases of the SAMPLE/PRELOAD mode.

Figure 13. IEEE Std. 1149.1 BST SAMPLE/PRELOAD Mode

Capture Phase

In the capture phase, the signals at the pin, OEJ and OUTJ, are loaded into the capture registers. The register CLOCK signal is supplied by the TAP Controller's CLOCKDR output. The data retained in these registers consists of signals from normal device operation.
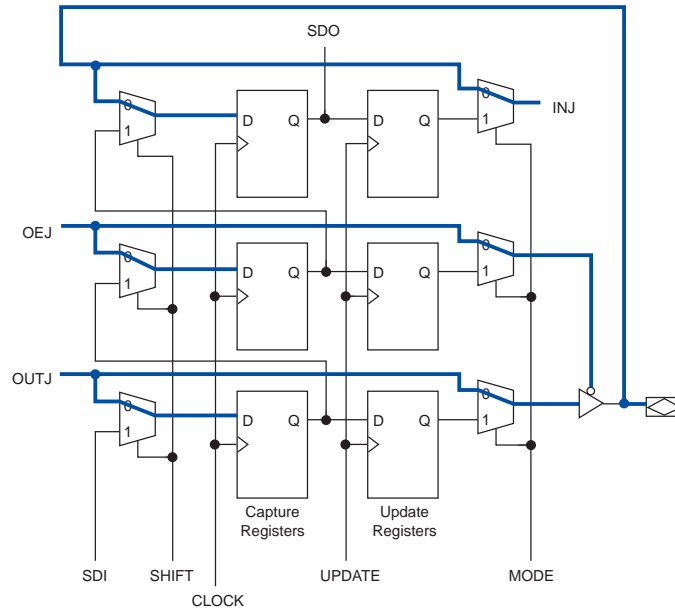
Shift & Update Phases

In the shift phase, the previously captured signals at the pin, OEJ and OUTJ, are shifted out of the boundary-scan register via the TDO pin using CLOCK. As data is shifted out, the patterns for the next test can be shifted in via the TDI pin.

In the update phase, data is transferred from the capture registers to the UPDATE registers using the UPDATE Clock. The data stored in the UPDATE registers can be used for the EXTEST instruction.
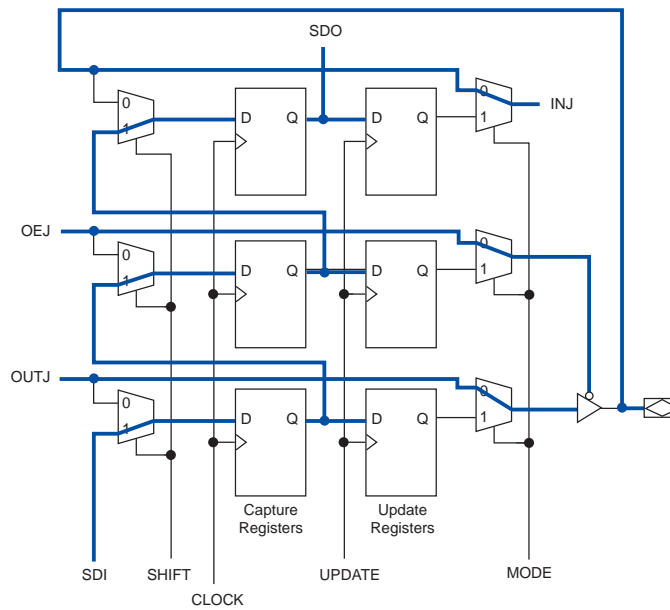
During the capture phase, multiplexers preceding the capture registers select the active device data signals; this data is then clocked into the capture registers. The multiplexers at the outputs of the update registers also select active device data to prevent functional interruptions to the device.

During the shift phase, the boundary-scan shift register is formed by clocking data through capture registers around the device periphery and then out of the TDO pin. New test data can simultaneously be shifted into TDI and replace the contents of the capture registers. During the update phase, data in the capture registers is transferred to the update registers. This data can then be used in the EXTEST instruction mode. Refer to "BYPASS Instruction Mode" on page 30 for more information.

Figure 14 shows the SAMPLE/PRELOAD waveforms. The SAMPLE/PRELOAD instruction code is shifted in through the TDI pin. The TAP controller advances to the CAPTURE_DR state and then to the SHIFT_DR state, where it remains if TMS is held low. The data shifted out of the TDO pin consists of the data that was present in the capture registers after the capture phase.

New test data shifted into the TDI pin appears at the TDO pin after being clocked through the entire boundary-scan register. Figure 14 shows that the instruction code at TDI does not appear at the TDO pin until after the capture register data is shifted out. If TMS is held high on two consecutive TCK clock cycles, the TAP controller advances to the UPDATE_DR state for the update phase.

Figure 14. SAMPLE/PRELOAD Shift Data Register Waveforms

EXTEST Instruction Mode

The EXTEST instruction mode is used primarily to check external pin

connections between devices. Unlike the SAMPLE/PRELOAD mode, EXTEST allows test data to be forced onto the pin signals. By forcing known logic high and low levels on output pins, opens and shorts can be detected at pins of any device in the scan chain.

Figure 15 shows the capture, shift, and update phases of the EXTEST mode.

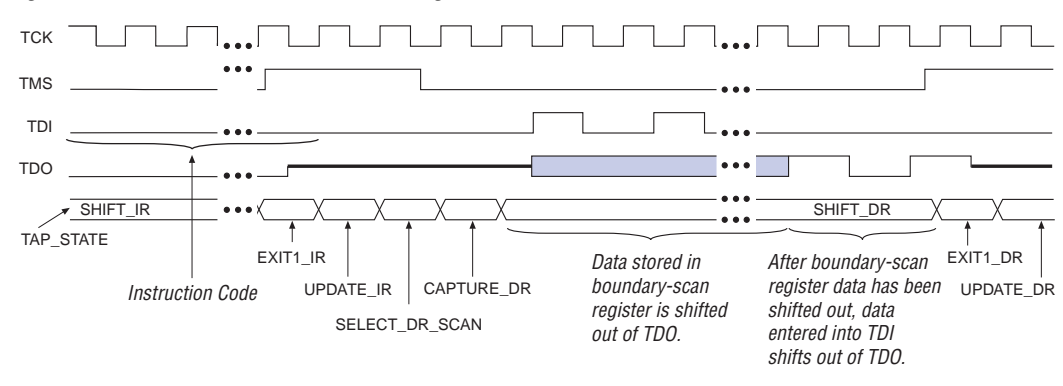*Figure 15. IEEE Std. 1149.1 BST EXTEST Mode*

Capture Phase

In the capture phase, the signals at the pin, OEJ and OUTJ, are loaded into the capture registers. The register CLOCK signal is supplied by the TAP Controller's CLOCKDR output. Previously retained data in the update registers drives the IOC input, INJ, and allows the I/O pin to tri-state or drive a signal out.

A "1" in the OEJ update register tri-states the output buffer.
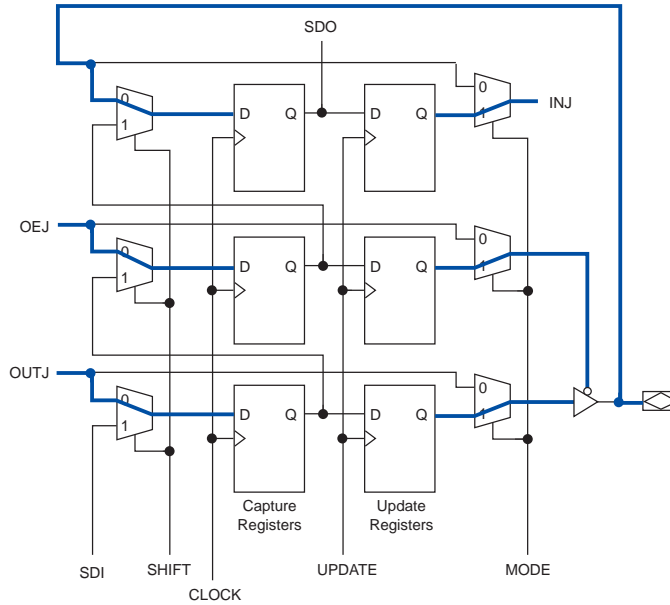
Shift & Update Phases

In the shift phase, the previously captured signals at the pin, OEJ and OUTJ, are shifted out of the boundary-scan register via the TDO pin using CLOCK. As data is shifted out, the patterns for the next test can be shifted in via the TDI pin.

In the update phase, data is transferred from the capture registers to the update registers using the UPDATE Clock. The update registers then drive the IOC input, INJ, and allow the I/O pin to tri-state or drive a signal out.
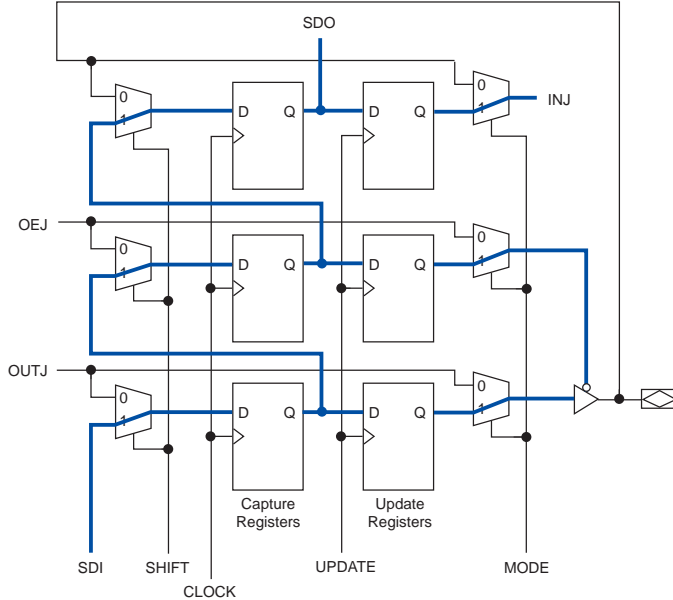
EXTEST selects data differently than SAMPLE/PRELOAD. EXTEST chooses data from the update registers as the source of the INJ, output, and output enable signals. Once the EXTEST instruction code is entered, the multiplexers select the update register data; thus, data stored in these registers from a previous EXTEST or SAMPLE/PRELOAD test cycle can be forced onto the pin signals. In the capture phase, the results of this test data are stored in the capture registers and then shifted out of TDO during the shift phase. New test data can then be stored in the update registers during the update phase.

The waveform diagram in Figure 16 resembles the SAMPLE/PRELOAD waveform diagram, except that the instruction code for EXTEST is different. The data shifted out of TDO consists of the data that was present in the capture registers after the capture phase. New test data shifted into the TDI pin appears at the TDO pin after being clocked through the entire boundary-scan register.

Figure 16. EXTEST Shift Data Register Waveforms
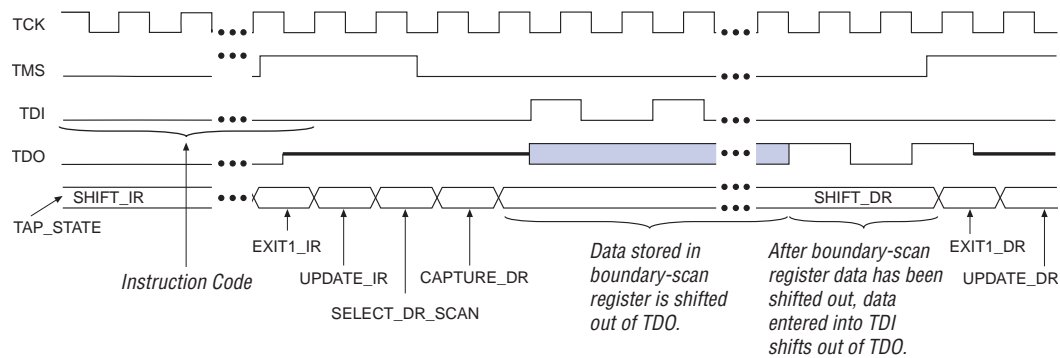
BYPASS Instruction Mode

The BYPASS instruction mode is activated with an instruction code made up of only 1's. The waveforms in Figure 17 show how scan data passes through a device once the TAP controller is in the SHIFT_DR state. In this state, data signals are clocked into the bypass register from TDI on the rising edge of TCK and out of TDO on the falling edge of the same clock pulse.

Figure 17. BYPASS Shift Data Register Waveforms
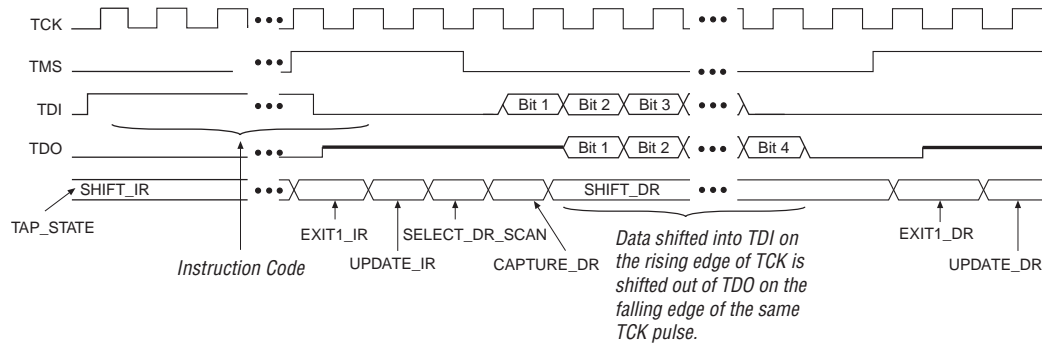
IDCODE Instruction Mode

The IDCODE instruction mode is used to identify the devices in an IEEE Std. 1149.1 chain. When IDCODE is selected, the device identification register is loaded with the 32-bit vendor-defined identification code and connected between the TDI and TDO ports. The 32-bit vendor-defined identification register for Altera devices is listed in the appropriate device family data sheet.

USERCODE Instruction Mode

The USERCODE instruction mode is used to examine the user electronic signature (UES) within the devices along an IEEE Std. 1149.1 chain. When this instruction is selected, the device identification register is connected between the TDI and TDO ports and the user-defined UES is shifted out through the device ID register.

☞ MAX 7000S devices offer an alternative method of providing the ability to read out user-defined 16-bit UES.

☞ The Quartus II software has an Auto Usercode option that sets the UES of EPC2, EPC4, EPC8, or EPC16 devices to the checksum of its programming file. See Quartus II Help for more information.

Enabling IEEE Std. 1149.1 BST Circuitry

The IEEE Std. 1149.1 BST circuitry for Altera devices is enabled upon device power-up. Because this circuitry may be used for BST, ISP, or ICR (depending on the device), this circuitry must be enabled only at specific times. In the device sections you will find a description of how to enable the IEEE Std. 1149.1 circuitry when needed and to ensure that the circuitry is not inadvertently enabled when it is not needed.

Table 12 shows the pin connections necessary for disabling JTAG in device families that have dedicated IEEE Std. 1149.1 pins. Some families (for example, FLEX 8000, FLEX 6000, and MAX 3000A devices) have optional IEEE Std. 1149.1 pins that can be disabled through Compiler Options/Settings.

Table 12. Disabling IEEE Std. 1149.1 Circuitry						
Devices	**Compiler Option**	**JTAG Pins** *(1)*				
		TMS	**TCK**	**TDI**	**TDO**	**TRST**
Stratix Stratix GX HardCopy II HardCopy Stratix	*(4)*	VCC	GND *(2)*	VCC	Leave open	GND
Cyclone	*(4)*	VCC	GND *(2)*	VCC	Leave open	–
Mercury	*(4)*	VCC	GND *(2)*	VCC	Leave open	GND
APEX II	*(4)*	VCC	GND *(2)*	VCC	Leave open	GND
APEX 20K, APEX 20KE	*(4)*	VCC	GND *(2)*	VCC	Leave open	GND
ACEX 1K	*(4)*	VCC	GND *(2)*	VCC	Leave open	GND
FLEX 10K, FLEX 10KE	*(4)*	VCC	GND *(2)*	VCC	Leave open	GND
FLEX 8000	JTAG Disabled	User I/O pin *(3)*	User I/O pin *(3)*	User I/O pin *(3)*	User I/O pin	GND *(3)*
	JTAG Enabled	VCC	GND *(2)*	VCC	Leave open	GND
FLEX 6000	JTAG Disabled	User I/O pin	User I/O pin	User I/O pin	User I/O pin	–
	JTAG Enabled	VCC	GND *(2)*	VCC	Leave open	–
MAX 9000	*(4)*	VCC	GND *(2)*	VCC	Leave open	–
MAX 7000S, MAX 7000A, MAX 7000B, MAX 3000A	JTAG Disabled	User I/O pin	User I/O pin	User I/O pin	User I/O pin	–
	JTAG Enabled	VCC	GND *(2)*	VCC	Leave open	–
EPC2, EPC4, EPC8, EPC16	*(4)*	VCC	GND (2)	VCC	Leave open	

Notes to Table 12:

(1) If the design has been compiled with IEEE Std. 1149.1 circuitry enabled, tying the IEEE Std. 1149.1 pins to the appropriate state will deactivate the IEEE Std. 1149.1 circuitry.

(2) The TCK signal may also be tied high. If TCK is tied high, power-up conditions must ensure that TMS is pulled high before TCK. Pulling TCK low avoids this power-up condition.

(3) For EPF81500A devices, these pins are dedicated JTAG pins and are not available as user I/O pins. If JTAG BST is not used, TMS, TCK, TDI, and TRST should be tied to GND.

(4) There is no software option to disable JTAG in these device families, the JTAG pins are dedicated.

HardCopy II, HardCopy Stratix, Stratix, Stratix GX, Cyclone, APEX, ACEX, FLEX 10K & MAX 9000 Devices

The IEEE Std 1149.1 BST circuitry for these Altera devices are dedicated and enabled upon device power-up. You can use this IEEE Std. 1149.1 BST circuitry both before and after device programming or configuration. However, the nCONFIG pin on the FPGA families must be held low when you perform JTAG boundary-scan testing before configuration.

MAX 7000S, MAX 7000A, MAX 7000B & MAX 3000A Devices

The IEEE Std. 1149.1 BST circuitry of MAX 7000S, MAX 7000A, MAX 7000B, and MAX 3000A devices is enabled by an IEEE Std. 1149.1 enable bit within the device. A blank device always has the BST circuitry enabled. The Altera MPU or a third-party programmer can set the state of this enable bit when programming the device. The state of the JTAG enable bit may not be changed using ISP via the IEEE Std. 1149.1 port.

Because these devices have four pins that can be used as either JTAG pins or user I/O pins, you must enable or disable the JTAG circuitry before compilation. For a design that has been compiled with JTAG pins enabled, the four pins operate as dedicated pins only. If these devices are not using the IEEE Std. 1149.1 circuitry, tying the pins to the appropriate state (shown in Table 12) disables the circuitry.

In the MAX+PLUS II software, by choosing **Device Options** from the **Device** dialog box (Assign menu), you can enable or disable IEEE Std. 1149.1 support for applicable devices on a device-by-device basis with the Enable JTAG Support option. You can also enable JTAG support for all devices in a project by choosing **Global Project Device Options** (Assign menu) and selecting the *Enable JTAG Support* option.

In the Quartus II software, by choosing **Device & Pin Options** from the Settings dialog box (Assign menu), you can enable or disable IEEE Std. 1149.1 support for applicable devices on a device-by-device basis with the *Enable JTAG Support* checkbox under the **General** tab.

FLEX 8000 & FLEX 6000 Devices

The IEEE Std. 1149.1 BST circuitry for Altera devices is enabled upon device power-up. You can use the IEEE Std. 1149.1 BST circuitry both before and after device configuration. In FLEX 8000 and FLEX 6000 devices, the nCONFIG pin must be held low when you perform boundary-scan testing before configuration.

Because these devices have four pins that can be used as either JTAG pins or user I/O pins, you must enable or disable the JTAG circuitry before compilation. For a design that has been compiled with JTAG pins enabled, the four pins operate as dedicated pins only. If these devices are not using the IEEE Std. 1149.1 circuitry, tying the pins to the appropriate state (shown in Table 12) disables the circuitry.

In the MAX+PLUS II software, by choosing **Device Options** from the **Device** dialog box (Assign menu), you can enable or disable IEEE Std. 1149.1 support for applicable devices on a device-by-device basis with the *Enable JTAG Support* option. You can also enable JTAG support for all devices in a project by choosing **Global Project Device Options** (Assign menu) and selecting the *Enable JTAG Support* option.

In the Quartus II software, by choosing **Device & Pin Options** for FLEX 6000 projects from the Settings dialog box (Assign menu), you can enable or disable IEEE Std. 1149.1 support for applicable devices on a device-by-device basis with the **Enable JTAG Support** checkbox under the **General** tab.

Guidelines for IEEE Std. 1149.1 Boundary-Scan Testing

Use the following guidelines when performing boundary-scan testing with IEEE Std. 1149.1 devices:

■ Performing boundary-scan testing on open-drain pins requires an external pull-up resistor. For information about the value of the resistor, refer to the specific device data sheet.
■ If a certain pin has a weak pull-up resistor feature enabled before boundary-scan testing, the value of the resistor can be found in the specific device data sheet in the *Device DC Operating Conditions* section.

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- If internal termination is enabled for a specific pin, it can only function after device configuration. Therefore, Altera recommends postponing device configuration until after boundary-scan testing is complete.
- If the "10..." pattern does not shift out of the instruction register via the TDO pin during the first clock cycle of the SHIFT_IR state, the proper TAP controller state has not been reached. To solve this problem, try one of the following procedures:
    - Verify that the TAP controller has reached the SHIFT_IR state correctly. To advance the TAP controller to the SHIFT_IR state, return to the RESET state and clock the code 01100 on the TMS pin.
    - Check the connections to the VCC, GND, JTAG, and dedicated configuration pins on the device.
    - For all FLEX 10K, FLEX 10KE, FLEX 8000, FLEX 6000, MAX 7000S, MAX 7000A, MAX 7000B, and MAX 3000A devices, if the device is in user mode, make sure that you have turned on the *Enable JTAG Support* option in the MAX+PLUS II or Quartus II software.
- Perform a SAMPLE/PRELOAD test cycle prior to the first EXTEST test cycle to ensure that known data is present at the device pins when the EXTEST mode is entered. If the OEJ update register contains the value that enables the tri-state buffer, the data in the OUTJ update register will be driven out. The state must be known and correct to avoid contention with other devices in the system.
- Do not perform EXTEST and SAMPLE/PRELOAD tests during ISP or ICR. These instructions are supported before and after ISP/ICR but not during ISP and ICR.
- For devices that support differential signaling (LVDS, LVPECL, etc.), after configuration any pins that constitute part of a differential pin pair cannot be tested; therefore, to perform BST after configuration, the BSC group definitions that correspond to these differential pin pairs must be edited. The BSC group should be redefined as an internal cell. See the BSDL file for more information on editing.
- In FLEX 8000 devices, do not execute a BYPASS shift cycle before an EXTEST test cycle that requires preloaded test data. The bypass and boundary-scan registers shift simultaneously when the TAP controller is in the SHIFT_DR state. Therefore, using the BYPASS mode will shift test data out of the capture registers.

If problems persist, contact Altera Applications at (800) 800-EPLD.

Boundary-Scan Description Language Support

The Boundary-Scan Description Language (BSDL)—a subset of VHDL—provides a syntax that allows you to describe the features of an IEEE Std. 1149.1 BST-capable device that can be tested. Test software development systems then use the BSDL files for test generation, analysis, failure diagnostics, and in-system programming. For more information, or to receive BSDL files for IEEE Std. 1149.1-compliant Altera devices, visit the Altera web site at **www.altera.com**.

Following is a partial example of a BSDL file. Important things to note are:

- Make sure the revision of the file you are using is the latest BSDL version.
- Check that the part number and package are correct.
- Find the instruction length and OPCODE under INSTRUCTIONS AND REGISTER ACCESS
- Find the boundary scan length and the description of every BSC in the boundary scan register under BOUNDARY SCAN CELL INFORMATION
- Check the DESIGN WARNINGS section for helpful hints (this information is not available in all BSDL files).

```
-- Copyright (C) 1998-2003 Altera Corporation
--
-- File Name    : EP1S25F672.BSD
-- Device       : EP1S25F672
-- Package      : 672-Pin FineLine Ball Grid Array
-- BSDL Version : 3.01
-- BSDL Status  : Preliminary
-- Date Created : 08/22/2002
-- Created by   : Altera BSDL Generation Program Ver. 1.20
-- Verification : Software syntax checked on:
--                 Agilent Technologies 3070 BSDL Compiler
--                 ASSET ScanWorks ver. 3.1.1
--                 Corelis ScanPlus TPG ver. 4.12
--                 Genrad BSDL syntax checker ver. 4.01, a component
--                   of Scan Pathfinder(tm) and BasicSCAN(tm)
--                 GOEPEL Electronics' CASCON-GALAXY(R) ver. 4.0
--                 JTAG Technologies BSDL Converter ver. 2.4
--
-- Documentation : Stratix Family Datasheet
--                 AN39: JTAG Boundary Scan Testing for Altera Devices

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--
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```
-- writing by Altera Corporation. Altera customers are advised to
-- obtain the latest version of device specifications before relying
-- on any published information and before placing orders for products
-- or services.
--
--                    **Testing Differential Pin Pairs**
-- This file supports boundary scan testing (BST) before device
-- configuration.  After configuration any pins that constitute part
-- of a differential pin pair are untestable; therefore, to perform
-- BST after configuration, the boundary scan cell (BSC) group
-- definitions that correspond to these differential pin pairs must
-- be edited.  The bsc group should be redefined as an internal
-- cell. Make the following edits to this file:
--     a) Under the Entity Definitions With Ports section, change
--        the definition of the differential pins from inout bit, in
--        bit, or out bit to linkage bit.
--     b) Edit the corresponding bsc group definitions as shown in
--        the example below.
--
--         BSC group 278 for I/O pin H12
--         "834 (BC_1, IOH12, input, X)," &
--         "835 (BC_1, *, control, 1)," &
--         "836 (BC_1, IOH12, output3, X, 835, 1, Z)," &
-- Redefined as internal bsc group:
--
--         BSC group 278 for I/O pin H12
--         "834 (BC_4, *, internal, X)," &
--         "835 (BC_4, *, internal, 1)," &
--         "836 (BC_4, *, internal, X)," &
--
-- BSC groups for CLKp, CLKn, PLL_OUTp, PLL_OUTn, PLL_FBp,
-- PLL_FBn, DIFFIO_RXp, DIFFIO_RXn, DIFFIO_TXp, DIFFIO_TXn,
-- FPLLCLKp and FPLLCLKn pins will require the edits listed
-- above if differential signaling is used.
--
--                    **Testing PLL_ENA**
-- Please note that toggling the PLL_ENA pin after configuration
-- will cause the PLLs utilizing this enable pin to drive all output
-- clocks low.  The PLLs will also need to relock to their respective
-- input clocks when PLL_ENA returns to its active level.
--
--
-- ***********************************************************************
-- *                    ENTITY DEFINITION WITH PORTS                     *
-- ***********************************************************************
entity EP1S25F672 is
  generic (PHYSICAL_PIN_MAP : string := "FBGA672");

port (
--I/O Pins
    IOC1   , IOD2   , IOE3   , IOE4   , IOE1   , IOE2   , IOF3   ,
    IOF4   , IOF1   , IOF2   , IOG5   , IOG6   , IOG1   , IOG2   ,
    IOG3   , IOG4   , IOH1   , IOH2   , IOH3   , IOH4   , IOH6   ,
    IOH5   , IOJ7   , IOH7   , IOJ4   , IOJ3   , IOJ2   , IOJ1   ,
    IOJ6   , IOJ5   , IOK4   , IOK3   , IOK2   , IOK1   , IOK9   ,
    IOJ8   , IOK6   , IOK5   , IOK8   , IOK7   , IOL3   , IOL2   ,
    IOL5   , IOL4   , IOL7   , IOL6   , IOM6   , IOM7   , IOM4   ,
    IOM5   , ION6   , ION7   , IOM8   , IOM9   , IOP8   , ION8   ,
    IOP6   , IOP7   , IOR6   , IOR7   , IOR8   , IOR9   , IOR4   ,
    IOR5   , IOT3   , IOT2   , IOT7   , IOT6   , IOT5   , IOT4   ,
    IOU6   , IOU5   , IOU2   , IOU1   , IOU8   , IOU7   , IOU4   ,
    IOU3   , IOU9   , IOV8   , IOV6   , IOV5   , IOV1   , IOV2   ,
    IOW5   , IOW6   , IOV3   , IOV4   , IOW7   , IOW8   , IOW1   ,
    IOW2   , IOY3   , IOY4   , IOW3   , IOW4   , IOY6   , IOY5   ,
    IOY2   , IOY1   , IOAA6  , IOAA5  , IOAA2  , IOAA1  , IOAA4  ,
    IOAA3  , IOAB2  , IOAB1  , IOAB4  , IOAB3  , IOAC2  , IOAD1  ,
    IOAC4  , IOAC3  , IOAD5  , IOAC5  , IOAD2  , IOAE2  , IOAD3  ,
    IOAE4  , IOAD4  , IOAE3  , IOAB5  , IOAF3  , IOAB6  , IOAC6  ,
    IOAC7  , IOAD6  , IOAE7  , IOAF5  , IOAB7  , IOAD7  , IOAE6  ,
    IOAA7  , IOAF7  , IOAF6  , IOAC8  , IOAB8  , IOAD8  , IOAE8  ,
    IOAF8  , IOY9   , IOY8   , IOW9   , IOAA8  , IOAC9  , IOAD9  ,
```

```
        IOAB9   , IOAF9   , IOAD10  , IOAE10  , IOAA9   , IOAC10  , IOY10   ,
        IOAA10  , IOW10   , IOAB10  , IOAF10  , IOAB11  , IOAE11  , IOAC11  ,
        IOY11   , IOAD11  , IOAA11  , IOAD12  , IOAF12  , IOAB12  , IOAA12  ,
        IOAB14  , IOAA14  , IOAB13  , IOAA13  , IOW15   , IOAC15  , IOY16   ,
        IOAD15  , IOAA16  , IOAC16  , IOAB16  , IOAD16  , IOW17   , IOAE16  ,
        IOY17   , IOAF17  , IOAA17  , IOY18   , IOAE17  , IOW18   , IOAB17  ,
        IOAA18  , IOY19   , IOAF18  , IOAC17  , IOAD17  , IOAE18  , IOAF19  ,
        IOY20   , IOAA19  , IOAD18  , IOAB19  , IOAD19  , IOAC18  , IOAC19  ,
        IOAE19  , IOAF20  , IOAE20  , IOAA20  , IOAB20  , IOAE21  , IOAC20  ,
        IOAA21  , IOAB21  , IOAE21  , IOAD20  , IOAC21  , IOAE25  , IOAF22  ,
        IOAF24  , IOAE22  , IOAD23  , IOAB22  , IOAE23  , IOAD24  , IOAC23  ,
        IOAC22  , IOAD22  , IOAE24  , IOAC24  , IOAD26  , IOAC25  ,
        IOAB24  , IOAB23  , IOAB26  , IOAB25  , IOAA24  , IOAA23  , IOAA26  ,
        IOAA25  , IOAA22  , IOY22   , IOY26   , IOY25   , IOY24   , IOY23   ,
        IOW23   , IOW24   , IOW21   , IOW22   , IOW25   , IOW26   , IOW19   ,
        IOW20   , IOV23   , IOV24   , IOV21   , IOV22   , IOV25   , IOV26   ,
        IOU24   , IOU23   , IOV19   , IOU20   , IOU26   , IOU25   , IOU19   ,
        IOU18   , IOU22   , IOU21   , IOT21   , IOT20   , IOT25   , IOT24   ,
        IOT19   , IOR19   , IOT23   , IOT22   , IOR22   , IOR23   , IOP20   ,
        IOP21   , IOR20   , IOR21   , IOP19   , ION19   , ION20   , ION21   ,
        IOM18   , IOM19   , IOM20   , IOM21   , IOM22   , IOM23   , IOL22   ,
        IOL23   , IOL21   , IOL20   , IOK20   , IOK19   , IOL25   , IOL24   ,
        IOK22   , IOK21   , IOK24   , IOK23   , IOJ20   , IOJ19   , IOK26   ,
        IOK25   , IOJ22   , IOJ21   , IOH20   , IOH19   , IOJ26   , IOJ25   ,
        IOJ24   , IOJ23   , IOH22   , IOH21   , IOH24   , IOH23   , IOG21   ,
        IOG22   , IOH25   , IOH26   , IOG23   , IOG24   , IOG25   , IOG26   ,
        IOF23   , IOF24   , IOF25   , IOF26   , IOE23   , IOE24   , IOE25   ,
        IOE26   , IOD24   , IOC25   , IOD25   , IOC26   , IOB24   , IOB25   ,
        IOD23   , IOD22   , IOC24   , IOB23   , IOE22   , IOC23   , IOB22   ,
        IOA24   , IOA22   , IOC22   , IOC20   , IOD21   , IOD20   , IOB21   ,
        IOA21   , IOC21   , IOB20   , IOE21   , IOA20   , IOF21   , IOC19   ,
        IOD19   , IOE20   , IOB19   , IOE19   , IOA19   , IOC18   , IOB18   ,
        IOD18   , IOF20   , IOG19   , IOE18   , IOG20   , IOA18   , IOF19   ,
        IOC17   , IOG18   , IOB17   , IOE17   , IOF17   , IOD17   , IOG17   ,
        IOA17   , IOH18   , IOD16   , IOC16   , IOE16   , IOB16   , IOF16   ,
        IOC15   , IOH16   , IOF15   , IOF13   , IOE13   , IOF14   , IOE14   ,
        IOF12   , IOE12   , IOA12   , IOC12   , IOE11   , IOB11   , IOG11   ,
        IOH10   , IOC11   , IOD11   , IOA10   , IOE10   , IOG10   , IOF10   ,
        IOG9    , IOF9    , IOD10   , IOC10   , IOB10   , IOA9    , IOE9    ,
        IOB9    , IOC9    , IOG7    , IOA8    , IOA7    , IOB8    , IOE8    ,
        IOF7    , IOB7    , IOC8    , IOD8    , IOE7    , IOB6    , IOA6    ,
        IOF6    , IOF5    , IOD6    , IOE6    , IOA5    , IOE5    , IOC7    ,
        IOC6    , IOB5    , IOC3    , IOA3    , IOD5    , IOB4    , IOC2    ,
        IOB3    , IOD4    , IOC4    , IOC5    , IOD3    : inout bit;
--Stratix Family-Specific Pins
        CLK0p         , CLK0n         , CLK1p         , CLK2p          ,
        CLK2n         , CLK3p         , CLK4p         , CLK5p          ,
        CLK6p         , CLK7p         , CLK8p         , CLK9p          ,
        CLK9n         , CLK10p        , CLK11p        , CLK11n         ,
        CLK12p        , CLK13p        , CLK14p        , CLK15p         ,
        PLL_ENA       , DCLK          , MSEL0         , MSEL1          ,
        MSEL2         , PORSEL        , NIO_PULLUP    , VCCSEL
        : in bit;
        VREF2B1       , VREF1B1       , VREF0B1       , VREF1B2        ,
        VREF0B2       , VREF2B3       , VREF1B3       , VREF0B3        ,
        VREF2B4       , VREF1B4       , VREF0B4       , VREF1B5        ,
        VREF0B5       , VREF2B6       , VREF1B6       , VREF0B6        ,
        VREF2B7       , VREF1B7       , VREF0B7       , VREF2B8        ,
        VREF1B8       , VREF0B8       , CONF_DONE     , NCE            ,
        NCEO          , NCONFIG       , NSTATUS       , TEMPDIODEp     ,
        TEMPDIODEn : linkage bit;
--JTAG Ports
        TCK     , TMS     , TDI     , TRST   : in bit;
        TDO     : out bit;
--Power Pins
        VCC     : linkage bit_vector (1 to 74);
--Ground Pins
        GND     : linkage bit_vector (1 to 83)
);

use STD_1149_1_1994.all;
```

```
attribute COMPONENT_CONFORMANCE of EP1S25F672 :
        entity is "STD_1149_1_1993";

-- ***************************************************************************
-- *                          PIN MAPPING                                    *
-- ***************************************************************************
attribute PIN_MAP of EP1S25F672 : entity is PHYSICAL_PIN_MAP;
constant FBGA672 : PIN_MAP_STRING :=
--I/O Pins
    "IOC1   : C1  , IOD2   : D2  , IOE3   : E3  , IOE4   : E4  , "&
    "IOE1   : E1  , IOE2   : E2  , IOF3   : F3  , IOF4   : F4  , "&
    "IOF1   : F1  , IOF2   : F2  , IOG5   : G5  , IOG6   : G6  , "&
    "IOG1   : G1  , IOG2   : G2  , IOG3   : G3  , IOG4   : G4  , "&
    "IOH1   : H1  , IOH2   : H2  , IOH3   : H3  , IOH4   : H4  , "&
    "IOH6   : H6  , IOH5   : H5  , IOJ7   : J7  , IOH7   : H7  , "&
    "IOJ4   : J4  , IOJ3   : J3  , IOJ2   : J2  , IOJ1   : J1  , "&
    "IOJ6   : J6  , IOJ5   : J5  , IOK4   : K4  , IOK3   : K3  , "&
    "IOK2   : K2  , IOK1   : K1  , IOK9   : K9  , IOJ8   : J8  , "&
    "IOK6   : K6  , IOK5   : K5  , IOK8   : K8  , IOK7   : K7  , "&
    "IOL3   : L3  , IOL2   : L2  , IOL5   : L5  , IOL4   : L4  , "&
    "IOL7   : L7  , IOL6   : L6  , IOM6   : M6  , IOM7   : M7  , "&
    "IOM4   : M4  , IOM5   : M5  , ION6   : N6  , ION7   : N7  , "&
    "IOM8   : M8  , IOM9   : M9  , IOP8   : P8  , ION8   : N8  , "&
    "IOP6   : P6  , IOP7   : P7  , IOR6   : R6  , IOR7   : R7  , "&
    "IOR8   : R8  , IOR9   : R9  , IOR4   : R4  , IOR5   : R5  , "&
    "IOT3   : T3  , IOT2   : T2  , IOT7   : T7  , IOT6   : T6  , "&
    "IOT5   : T5  , IOT4   : T4  , IOU6   : U6  , IOU5   : U5  , "&
    "IOU2   : U2  , IOU1   : U1  , IOU8   : U8  , IOU7   : U7  , "&
    "IOU4   : U4  , IOU3   : U3  , IOU9   : U9  , IOV8   : V8  , "&
    "IOV6   : V6  , IOV5   : V5  , IOV1   : V1  , IOV2   : V2  , "&
    "IOW5   : W5  , IOW6   : W6  , IOV3   : V3  , IOV4   : V4  , "&
    "IOW7   : W7  , IOW8   : W8  , IOW1   : W1  , IOW2   : W2  , "&
    "IOY3   : Y3  , IOY4   : Y4  , IOW3   : W3  , IOW4   : W4  , "&
    "IOY6   : Y6  , IOY5   : Y5  , IOY2   : Y2  , IOY1   : Y1  , "&
    "IOAA6  : AA6 , IOAA5  : AA5 , IOAA2  : AA2 , IOAA1  : AA1 , "&
    "IOAA4  : AA4 , IOAA3  : AA3 , IOAB2  : AB2 , IOAB1  : AB1 , "&
    "IOAB4  : AB4 , IOAB3  : AB3 , IOAC2  : AC2 , IOAD1  : AD1 , "&
    "IOAC4  : AC4 , IOAC3  : AC3 , IOAD5  : AD5 , IOAC5  : AC5 , "&
    "IOAD2  : AD2 , IOAE2  : AE2 , IOAD3  : AD3 , IOAE4  : AE4 , "&
    "IOAD4  : AD4 , IOAE3  : AE3 , IOAB5  : AB5 , IOAF3  : AF3 , "&
    "IOAB6  : AB6 , IOAC6  : AC6 , IOAC7  : AC7 , IOAD6  : AD6 , "&
    "IOAE7  : AE7 , IOAF5  : AF5 , IOAB7  : AB7 , IOAD7  : AD7 , "&
    "IOAE6  : AE6 , IOAA7  : AA7 , IOAF7  : AF7 , IOAF6  : AF6 , "&
    "IOAC8  : AC8 , IOAB8  : AB8 , IOAD8  : AD8 , IOAE8  : AE8 , "&
    "IOAF8  : AF8 , IOY9   : Y9  , IOY8   : Y8  , IOW9   : W9  , "&
    "IOAA8  : AA8 , IOAC9  : AC9 , IOAD9  : AD9 , IOAB9  : AB9 , "&
    "IOAF9  : AF9 , IOAD10 : AD10, IOAE10 : AE10, IOAA9  : AA9 , "&
    "IOAC10 : AC10, IOY10  : Y10 , IOAA10 : AA10, IOW10  : W10 , "&
    "IOAB10 : AB10, IOAF10 : AF10, IOAB11 : AB11, IOAE11 : AE11, "&
    "IOAC11 : AC11, IOY11  : Y11 , IOAD11 : AD11, IOAA11 : AA11, "&
    "IOAD12 : AD12, IOAF12 : AF12, IOAB12 : AB12, IOAA12 : AA12, "&
    "IOAB14 : AB14, IOAA14 : AA14, IOAB13 : AB13, IOAA13 : AA13, "&
    "IOW15  : W15 , IOAC15 : AC15, IOY16  : Y16 , IOAD15 : AD15, "&
    "IOAA16 : AA16, IOAC16 : AC16, IOAB16 : AB16, IOAD16 : AD16, "&
    "IOW17  : W17 , IOAE16 : AE16, IOY17  : Y17 , IOAF17 : AF17, "&
    "IOAA17 : AA17, IOY18  : Y18 , IOAE17 : AE17, IOW18  : W18 , "&
    "IOAB17 : AB17, IOAA18 : AA18, IOY19  : Y19 , IOAF18 : AF18, "&
    "IOAC17 : AC17, IOAD17 : AD17, IOAE18 : AE18, IOAF19 : AF19, "&
    "IOY20  : Y20 , IOAA19 : AA19, IOAD18 : AD18, IOAB19 : AB19, "&
    "IOAD19 : AD19, IOAC18 : AC18, IOAC19 : AC19, IOAE19 : AE19, "&
    "IOAF20 : AF20, IOAE20 : AE20, IOAA20 : AA20, IOAB20 : AB20, "&
    "IOAF21 : AF21, IOAC20 : AC20, IOAA21 : AA21, IOAB21 : AB21, "&
    "IOAE21 : AE21, IOAD20 : AD20, IOAC21 : AC21, IOAE25 : AE25, "&
    "IOAF22 : AF22, IOAF24 : AF24, IOAE22 : AE22, IOAD23 : AD23, "&
    "IOAB22 : AB22, IOAE23 : AE23, IOAD24 : AD24, IOAC23 : AC23, "&
    "IOAC22 : AC22, IOAD22 : AD22, IOAE24 : AE24, IOAD25 : AD25, "&
    "IOAC24 : AC24, IOAD26 : AD26, IOAC25 : AC25, IOAB24 : AB24, "&
    "IOAB23 : AB23, IOAB26 : AB26, IOAB25 : AB25, IOAA24 : AA24, "&
    "IOAA23 : AA23, IOAA26 : AA26, IOAA25 : AA25, IOAA22 : AA22, "&
    "IOY22  : Y22 , IOY26  : Y26 , IOY25  : Y25 , IOY24  : Y24 , "&
    "IOY23  : Y23 , IOW23  : W23 , IOW24  : W24 , IOW21  : W21 , "&
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         "IOW22  : W22 , IOW25  : W25 , IOW26  : W26 , IOW19  : W19 , "&
         "IOW20  : W20 , IOV23  : V23 , IOV24  : V24 , IOV21  : V21 , "&
         "IOV22  : V22 , IOV25  : V25 , IOV26  : V26 , IOU24  : U24 , "&
         "IOU23  : U23 , IOV19  : V19 , IOU20  : U20 , IOU26  : U26 , "&
         "IOU25  : U25 , IOU19  : U19 , IOU18  : U18 , IOU22  : U22 , "&
         "IOU21  : U21 , IOT21  : T21 , IOT20  : T20 , IOT25  : T25 , "&
         "IOT24  : T24 , IOT19  : T19 , IOR19  : R19 , IOT23  : T23 , "&
         "IOT22  : T22 , IOR22  : R22 , IOR23  : R23 , IOP20  : P20 , "&
         "IOP21  : P21 , IOR20  : R20 , IOR21  : R21 , IOP19  : P19 , "&
         "ION19  : N19 , ION20  : N20 , ION21  : N21 , IOM18  : M18 , "&
         "IOM19  : M19 , IOM20  : M20 , IOM21  : M21 , IOM22  : M22 , "&
         "IOM23  : M23 , IOL22  : L22 , IOL23  : L23 , IOL21  : L21 , "&
         "IOL20  : L20 , IOK20  : K20 , IOK19  : K19 , IOL25  : L25 , "&
         "IOL24  : L24 , IOK22  : K22 , IOK21  : K21 , IOK24  : K24 , "&
         "IOK23  : K23 , IOJ20  : J20 , IOJ19  : J19 , IOK26  : K26 , "&
         "IOK25  : K25 , IOJ22  : J22 , IOJ21  : J21 , IOH20  : H20 , "&
         "IOH19  : H19 , IOJ26  : J26 , IOJ25  : J25 , IOJ24  : J24 , "&
         "IOJ23  : J23 , IOH22  : H22 , IOH21  : H21 , IOH24  : H24 , "&
         "IOH23  : H23 , IOG21  : G21 , IOG22  : G22 , IOH25  : H25 , "&
         "IOH26  : H26 , IOG23  : G23 , IOG24  : G24 , IOG25  : G25 , "&
         "IOG26  : G26 , IOF23  : F23 , IOF24  : F24 , IOF25  : F25 , "&
         "IOF26  : F26 , IOE23  : E23 , IOE24  : E24 , IOE25  : E25 , "&
         "IOE26  : E26 , IOD24  : D24 , IOC25  : C25 , IOD25  : D25 , "&
         "IOC26  : C26 , IOB24  : B24 , IOB25  : B25 , IOD23  : D23 , "&
         "IOD22  : D22 , IOC24  : C24 , IOB23  : B23 , IOE22  : E22 , "&
         "IOC23  : C23 , IOB22  : B22 , IOA24  : A24 , IOA22  : A22 , "&
         "IOC22  : C22 , IOC20  : C20 , IOD21  : D21 , IOD20  : D20 , "&
         "IOB21  : B21 , IOA21  : A21 , IOC21  : C21 , IOB20  : B20 , "&
         "IOE21  : E21 , IOA20  : A20 , IOF21  : F21 , IOC19  : C19 , "&
         "IOD19  : D19 , IOE20  : E20 , IOB19  : B19 , IOE19  : E19 , "&
         "IOA19  : A19 , IOC18  : C18 , IOB18  : B18 , IOD18  : D18 , "&
         "IOF20  : F20 , IOG19  : G19 , IOE18  : E18 , IOG20  : G20 , "&
         "IOA18  : A18 , IOF19  : F19 , IOC17  : C17 , IOG18  : G18 , "&
         "IOB17  : B17 , IOE17  : E17 , IOF17  : F17 , IOD17  : D17 , "&
         "IOG17  : G17 , IOA17  : A17 , IOH18  : H18 , IOD16  : D16 , "&
         "IOC16  : C16 , IOE16  : E16 , IOB16  : B16 , IOF16  : F16 , "&
         "IOC15  : C15 , IOH16  : H16 , IOF15  : F15 , IOF13  : F13 , "&
         "IOE13  : E13 , IOF14  : F14 , IOE14  : E14 , IOF12  : F12 , "&
         "IOE12  : E12 , IOA12  : A12 , IOC12  : C12 , IOE11  : E11 , "&
         "IOB11  : B11 , IOG11  : G11 , IOH10  : H10 , IOC11  : C11 , "&
         "IOD11  : D11 , IOA10  : A10 , IOE10  : E10 , IOG10  : G10 , "&
         "IOF10  : F10 , IOG9   : G9  , IOF9   : F9  , IOD10  : D10 , "&
         "IOC10  : C10 , IOB10  : B10 , IOA9   : A9  , IOE9   : E9  , "&
         "IOB9   : B9  , IOC9   : C9  , IOG7   : G7  , IOA8   : A8  , "&
         "IOA7   : A7  , IOB8   : B8  , IOE8   : E8  , IOF7   : F7  , "&
         "IOB7   : B7  , IOC8   : C8  , IOD8   : D8  , IOE7   : E7  , "&
         "IOB6   : B6  , IOA6   : A6  , IOF6   : F6  , IOF5   : F5  , "&
         "IOD6   : D6  , IOE6   : E6  , IOA5   : A5  , IOE5   : E5  , "&
         "IOC7   : C7  , IOC6   : C6  , IOB5   : B5  , IOC3   : C3  , "&
         "IOA3   : A3  , IOD5   : D5  , IOB4   : B4  , IOC2   : C2  , "&
         "IOB3   : B3  , IOD4   : D4  , IOC4   : C4  , IOC5   : C5  , "&
         "IOD3   : D3  , "&
--Stratix Family-Specific Pins
         "CLK0p          : N3  , CLK0n          : N2  , CLK1p          : M1  , "&
         "CLK2p          : R1  , CLK2n          : R2  , CLK3p          : R3  , "&
         "CLK4p          : AE12, CLK5p          : AC12, CLK6p          : AF15, "&
         "CLK7p          : AE15, CLK8p          : P24 , CLK9p          : R26 , "&
         "CLK9n          : P25 , CLK10p         : M26 , CLK11p         : M24 , "&
         "CLK11n         : M25 , CLK12p         : B15 , CLK13p         : A15 , "&
         "CLK14p         : B12 , CLK15p         : D12 , PLL_ENA        : W12 , "&
         "DCLK           : G12 , MSEL0          : Y12 , MSEL1          : Y13 , "&
         "MSEL2          : W13 , PORSEL         : W16 , NIO_PULLUP     : AA15, "&
         "VCCSEL         : Y15 , VREF2B1        : Y7  , VREF1B1        : V7  , "&
         "VREF0B1        : T8  , VREF1B2        : L8  , VREF0B2        : H8  , "&
         "VREF2B3        : D7  , VREF1B3        : D9  , VREF0B3        : F11 , "&
         "VREF2B4        : G16 , VREF1B4        : F18 , VREF0B4        : F22 , "&
         "VREF1B5        : J18 , VREF0B5        : L19 , VREF2B6        : R18 , "&
         "VREF1B6        : V20 , VREF0B6        : Y21 , VREF2B7        : AD21, "&
         "VREF1B7        : AB18, VREF0B7        : AB15, VREF2B8        : W11 , "&
         "VREF1B8        : AE9 , VREF0B8        : AE5 , CONF_DONE      : H11 , "&
         "NCE            : Y14 , NCEO           : W14 , NCONFIG        : H12 , "&
```

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       "NSTATUS       : H13 , TEMPDIODEp   : H14 , TEMPDIODEn   : G13 , "&
--JTAG ports
       "TCK   : G15 , TMS   : E15 , TDI   : H15 , TRST   : D15 , "&
       "TDO   : G14 , "&
--Power Pins
       "VCC   : (M3  , M2  , P5  , P4  , AE13, AD14, AD13, P23 , "&
                "P22 , N24 , N25 , D14 , C14 , D13 , D1  , L1  , "&
                "L9  , T1  , AC1 , T9  , AF4 , AF11, V11 , V12 , "&
                "V15 , V16 , AF16, AF23, T18 , AC26, T26 , L26 , "&
                "L18 , D26 , A23 , A16 , J15 , J16 , A4  , A11 , "&
                "J11 , J12 , K11 , M15 , P17 , U10 , K13 , M17 , "&
                "R10 , U12 , K15 , N10 , R12 , U14 , K17 , N12 , "&
                "R14 , U16 , L10 , N14 , R16 , L12 , N16 , T11 , "&
                "L14 , P11 , T13 , L16 , P13 , T15 , M11 , P15 , "&
                "T17 , M13 ), "&
--Ground Pins
       "GND   : (N5  , N4  , P3  , P2  , AC14, AE14, R25 , R24 , "&
                "N22 , N23 , B14 , B13 , F8  , A13 , B1  , J17 , "&
                "L17 , N17 , P26 , U11 , V18 , A14 , B2  , K10 , "&
                "M10 , N18 , R11 , U13 , A2  , AF25, J14 , L15 , "&
                "N15 , P18 , T16 , V17 , A25 , B26 , K12 , M12 , "&
                "N26 , R13 , U15 , AE1 , G8  , K14 , M14 , P1  , "&
                "R15 , U17 , AE26, H9  , K16 , M16 , P9  , R17 , "&
                "V9  , AF2 , H17 , K18 , N1  , P10 , T10 , V10 , "&
                "AF13, J9  , L11 , N9  , P12 , T12 , V13 , AF14, "&
                "J10 , L13 , N11 , P14 , T14 , V14 , J13 , N13 , "&
                "P16 , C13 , AC13)";


-- *************************************************************************
-- *                      IEEE 1149.1 TAP PORTS                            *
-- *************************************************************************

attribute TAP_SCAN_IN of TDI     : signal is true;
attribute TAP_SCAN_MODE of TMS   : signal is true;
attribute TAP_SCAN_OUT of TDO    : signal is true;
attribute TAP_SCAN_CLOCK of TCK  : signal is (10.00e6,BOTH);
attribute TAP_SCAN_RESET of TRST : signal is true;


-- *************************************************************************
-- *               INSTRUCTIONS AND REGISTER ACCESS                        *
-- *************************************************************************
attribute INSTRUCTION_LENGTH of EP1S25F672 : entity is 10;
attribute INSTRUCTION_OPCODE of EP1S25F672 : entity is
  "BYPASS          (1111111111), "&
  "EXTEST          (0000000000), "&
  "SAMPLE          (0000000101), "&
  "IDCODE          (0000000110), "&
  "USERCODE        (0000000111), "&
  "CLAMP           (0000001010), "&
  "HIGHZ           (0000001011)";

attribute INSTRUCTION_CAPTURE of EP1S25F672 : entity is "0101010101";

attribute IDCODE_REGISTER of EP1S25F672 : entity is
  "0000"&               --4-bit Version
  "0010000000000011"&   --16-bit Part Number (hex 2003)
  "00001101110"&        --11-bit Manufacturer's Identity
  "1";                  --Mandatory LSB
attribute USERCODE_REGISTER of EP1S25F672 : entity is
  "XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX";  --All 32 bits are programmable
attribute REGISTER_ACCESS of EP1S25F672 : entity is
  "DEVICE_ID       (IDCODE)";


-- *************************************************************************
-- *               BOUNDARY SCAN CELL INFORMATION                         *
-- *************************************************************************

attribute BOUNDARY_LENGTH of EP1S25F672 : entity is 2157;
attribute BOUNDARY_REGISTER of EP1S25F672 : entity is
  --BSC group 0 for I/O pin D4
  "0   (BC_1, IOD4, input, X)," &
```

```
"1   (BC_1, *, control, 1)," &
"2   (BC_1, IOD4, output3, X, 1, 1, Z)," &

--BSC group 1 for I/O pin C5
"3   (BC_1, IOC5, input, X)," &
"4   (BC_1, *, control, 1)," &
"5   (BC_1, IOC5, output3, X, 4, 1, Z)," &
:
:
--BSC group 67 for I/O pin H10
"201 (BC_1, IOH10, input, X)," &
"202 (BC_1, *, control, 1)," &
"203 (BC_1, IOH10, output3, X, 202, 1, Z)," &

--BSC group 68 for unused pad
"204 (BC_4, *, internal, X)," &
"205 (BC_4, *, internal, 1)," &
"206 (BC_4, *, internal, X)," &

--BSC group 69 for unused pad
"207 (BC_4, *, internal, X)," &
"208 (BC_4, *, internal, 1)," &
"209 (BC_4, *, internal, X)," &
:
:
--BSC group 697 for I/O pin H6
"2091 (BC_1, IOH6, input, X)," &
"2092 (BC_1, *, control, 1)," &
"2093 (BC_1, IOH6, output3, X, 2092, 1, Z)," &

--BSC group 698 for unused pad
"2094 (BC_4, *, internal, X)," &
"2095 (BC_4, *, internal, 1)," &
"2096 (BC_4, *, internal, X)," &

--BSC group 699 for I/O pin H2
"2097 (BC_1, IOH2, input, X)," &
"2098 (BC_1, *, control, 1)," &
"2099 (BC_1, IOH2, output3, X, 2098, 1, Z)," &

-- **********************************************************************
-- *                         DESIGN WARNING                             *
-- **********************************************************************
attribute DESIGN_WARNING of EP1S25F672 : entity is
  "This EP1S25 BSDL file supports 1149.1 testing before device"&
  "configuration.  Boundary scan testing with differential pin"&
  "pairs after configuration requires changes to this file.  Please"&
  "read the comments at the top of the file for further instruction.";

end EP1S25F672;
```

Conclusion

The IEEE Std. 1149.1 BST circuitry available in Altera devices provides a cost-effective and efficient way to test systems that contain devices with tight lead spacing. Circuit boards with Altera and other IEEE Std. 1149.1-compliant devices can use the EXTEST, SAMPLE/PRELOAD, and BYPASS modes to create serial patterns that internally test the pin connections between devices and check device operation.

References

Bleeker, H., P. van den Eijnden, and F. de Jong. *Boundary-Scan Test: A Practical Approach*. Eindhoven, The Netherlands: Kluwer Academic Publishers, 1993.

Institute of Electrical and Electronics Engineers, Inc. *IEEE Standard Test Access Port and Boundary-Scan Architecture* (IEEE Std 1149.1-1990). New York: Institute of Electrical and Electronics Engineers, Inc., 1990.

Maunder, C. M., and R. E. Tulloss. *The Test Access Port and Boundary-Scan Architecture*. Los Alamitos: IEEE Computer Society Press, 1990.

Revision History

The information contained in version 6.0 of *AN 39: JTAG Boundary-Scan Testing in Altera Devices* supersedes information published in previous versions.

Version 6.0

The following changes were made to *AN 39: JTAG Boundary-Scan Testing in Altera Devices* version 6.0:

■   Added HardCopy II information throughout the document.
■   Minor textual changes.

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