PowerPlay Early Power Estimator User Guide

For Cyclone II FPGAs

101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
www.altera.com

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Contents

About this User Guide

Revision History

The table below displays the revision history for the chapters in this User Guide.

Date	Version	Changes Made
May 2006	1.1	Updated cross references to match Quartus II 6.0 chapter title changes.
December 2005	1.0	First publication.

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Typographic Conventions

This document uses the typographic conventions shown below.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Command names, dialog box titles, checkbox options, and dialog box options are shown in bold, initial capital letters. Example: **Save As** dialog box.
bold type	External timing parameters, directory names, project names, disk drive names, filenames, filename extensions, and software utility names are shown in bold type. Examples: $\mathbf{f_{MAX}}$, **\qdesigns** directory, **d:** drive, **chiptrip.gdf** file.

Visual Cue	Meaning
Italic Type with Initial Capital Letters	Document titles are shown in italic type with initial capital letters. Example: *AN 75: High-Speed Board Design.*
Italic type	Internal timing parameters and variables are shown in italic type. Examples: t_{PIA}, $n + 1$. Variable names are enclosed in angle brackets (< >) and shown in italic type. Example: *<file name>*, *<project name>***.pof** file.
Initial Capital Letters	Keyboard keys and menu names are shown with initial capital letters. Examples: Delete key, the Options menu.
"Subheading Title"	References to sections within a document and titles of on-line help topics are shown in quotation marks. Example: "Typographic Conventions."
`Courier type`	Signal and port names are shown in lowercase Courier type. Examples: `data1`, `tdi`, `input`. Active-low signals are denoted by suffix `n`, e.g., `resetn`. Anything that must be typed exactly as it appears is shown in Courier type. For example: `c:\qdesigns\tutorial\chiptrip.gdf`. Also, sections of an actual file, such as a Report File, references to parts of files (e.g., the AHDL keyword `SUBDESIGN`), as well as logic function names (e.g., `TRI`) are shown in Courier.
1., 2., 3., and a., b., c., etc.	Numbered steps are used in a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ● •	Bullets are used in a list of items when the sequence of the items is not important.
✓	The checkmark indicates a procedure that consists of one step only.
☞	The hand points to information that requires special attention.
CAUTION	The caution indicates required information that needs special consideration and understanding and should be read prior to starting or continuing with the procedure or process.
	The warning indicates information that should be read prior to starting or continuing the procedure or processes
↵	The angled arrow indicates you should press the Enter key.
	The feet direct you to more information on a particular topic.

Chapter 1. About the Cyclone II PowerPlay Early Power Estimator

Release Information

Table 1–1 provides information on the version of the PowerPlay Early Power Estimator spreadsheet documented in this User Guide.

Table 1–1. PowerPlay Early Power Estimator Spreadsheet Versions

Device Family	PowerPlay Early Power Estimator Spreadsheet Version
Cyclone II	6.0 and later

Device Family Support

The Cyclone II™ PowerPlay Early Power Estimator spreadsheet provides full support for the target Altera device families listed in Table 1–2.

Table 1–2. Device Family Support

Device Family	Support
Cyclone II	Full

General Description

As designs grow larger and processes continue to shrink, power becomes an increasing concern. Printed circuit board (PCB) designers need an accurate estimate of the amount of power the device will consume to develop an appropriate power budget, design the power supplies, voltage regulators, heat sink and cooling system. You can calculate a Cyclone II device's power using the Microsoft Excel-based PowerPlay Early Power Estimator spreadsheet available from the Altera website or the PowerPlay power analyzer in the Quartus® II software. You need to enter the device resources, operating frequency, toggle rates, and other parameters in the PowerPlay Early Power Estimator spreadsheet.

This user guide explains how to use the Cyclone II PowerPlay Early Power Estimator spreadsheet to estimate device power consumption.

These calculations should only be used as an estimation of power, not as a specification. Be sure to verify the actual power during device operation, as the information is sensitive to the actual device design and the environmental operating conditions.

For more information about available device resources, I/O standard support, and other device features, refer to the appropriate device family handbook.

Features

The features of the PowerPlay Early Power Estimator spreadsheet include:

- Estimate your design's power usage before creating the design, during the design process, or after the design is complete
- Import device resource information from the Quartus II software into the PowerPlay Early Power Estimator spreadsheet with the use of the Quartus II-generated power estimation file
- Perform preliminary thermal analysis of your design

Chapter 2. Setting Up the Cyclone II PowerPlay Early Power Estimator

System Requirements

The PowerPlay Early Power Estimator spreadsheet requires:

- A PC running the Windows NT/2000/XP operating system
- Microsoft Excel 2002 or higher
- Quartus II software version 6.0 or higher if generating a file for import

Download & Install the PowerPlay Early Power Estimator Spreadsheet

The Cyclone II PowerPlay Early Power Estimator spreadsheet is available from the Altera website (**www.altera.com**). After reading the terms and conditions and clicking **I Agree**, you can download the Microsoft Excel file to your hard drive.

By default, the Microsoft Excel 2002 macro security level is set to **High**. When the macro security level is set to **High**, macros are automatically disabled. To change the macro security level in Microsoft Excel 2002, click **Options** on the Tools menu. On the **Security** tab of the **Options** window, click **Macro Security**. On the **Security Level** tab of the **Security** dialog box, chose **Medium**. When the macro security level is set to **Medium**, a pop-up window asks you whether to enable macros or disable macros each time you open a spreadsheet that contains macros. After changing the macro security level, you will have to close the spreadsheet and re-open it in order to use the macros.

Estimating Power

You can estimate power at any point in your design cycle. You can use the PowerPlay Early Power Estimator spreadsheet to estimate the power consumption if you have not begun your design, or if your design is not complete. After completing your design, you can use the PowerPlay power analyzer in the Quartus II software or the PowerPlay Early Power Estimator spreadsheet to estimate the power consumption.

For more information on the power estimation feature in the Quartus II software, refer to the *PowerPlay Power Analysis* chapter in volume 3 of the *Quartus II Handbook*.

To use the PowerPlay Early Power Estimator spreadsheet, enter the device resources, operating frequency, toggle rates and other parameters in the PowerPlay Early Power Estimator spreadsheet. If you do not have

an existing design, then you need to estimate the number of device resources your design will use in order to enter the information into the PowerPlay Early Power Estimator spreadsheet.

Estimating Power Before Starting the FPGA Design

FPGAs provide the convenience of a shorter design cycle and faster time-to-market than ASICs or ASSPs. This means that the board design often takes places during the FPGA design cycle, and the power planning for the device can happen before any of the FPGA design is complete.

Table 2–1 shows the advantages and disadvantages of using the PowerPlay Early Power Estimator spreadsheet before you begin the FPGA design.

Table 2–1. Power Estimation Before Designing FPGA

Advantages	Disadvantages
Power estimation can be done before any FPGA design is complete	• Accuracy depends on user input and estimate of the device resources • Process can be time consuming

To estimate power usage with the PowerPlay Early Power Estimator spreadsheet if you have not started your FPGA design, perform the following steps.

1. Download the PowerPlay Early Power Estimator spreadsheet from the Altera website (**www.altera.com**).
2. Select the target device and package from the PowerPlay Early Power Estimator spreadsheet's **Device** section.
3. Enter values in the fields on each section of the PowerPlay Early Power Estimator spreadsheet. Different worksheets in the file display different power sections, such as clocks and PLLs. Power is calculated automatically, and subtotals are given for each section.
4. The calculator displays the estimated power usage in the **Total** section.

Estimating Power While Creating the FPGA Design

When the FPGA design is partially complete, you can use the power estimation file (<*revision name*>**_early_pwr.csv**) generated by the Quartus II software to supply information to the PowerPlay Early Power Estimator spreadsheet. After importing the power estimation file

information into the PowerPlay Early Power Estimator spreadsheet, you can edit the PowerPlay Early Power Estimator spreadsheet to reflect the device resource estimates for the final design.

For more information on generating the power estimation file in the Quartus II software, refer to the *PowerPlay Power Analysis* chapter in volume 3 of the *Quartus II Handbook*.

Table 2–2 shows the advantages and disadvantages when using the PowerPlay Early Power Estimator spreadsheet for an FPGA design that is partially complete.

Table 2–2. Power Estimation When FPGA Design Is Partially Complete

Advantages	Disadvantages
• Power estimation can be done early in the FPGA design cycle • Provides the flexibility to automatically fill in the PowerPlay Early Power Estimator spreadsheet based on Quartus II software compilation results	Accuracy is dependent on user input and estimate of the final design device resources

Use the following steps to estimate power usage with the PowerPlay Early Power Estimator spreadsheet if your FPGA design is partially complete.

1. Compile the partial FPGA design in the Quartus II software.
2. Generate the PowerPlay Early Power Estimator file (<*revision name*>**_early_pwr.csv**) in the Quartus II software by clicking **Generate PowerPlay Early Power Estimator File** on the Project menu.
3. Download the PowerPlay Early Power Estimator spreadsheet from the Altera website.
4. Import the PowerPlay Early Power Estimator file into the PowerPlay Early Power Estimator spreadsheet to automatically populate the entries.
5. After importing the file to populate the PowerPlay Early Power Estimator spreadsheet, you can manually edit the cells to reflect final device resource estimates.

Estimating Power After Completing the FPGA Design

When you complete your FPGA design in the Quartus II software, the PowerPlay Power Analyzer provides the most accurate estimate of device power consumption. The PowerPlay power analyzer uses user mode and default assignments in addition to place-and-route information to determine power consumption. The Quartus II PowerPlay power analyzer supports power estimation for Cyclone II devices.

Table 2–3 shows the advantages and disadvantages when using the PowerPlay Early Power Estimator spreadsheet when the FPGA design is complete.

Table 2–3. Power Estimation When FPGA Design Is Complete

Advantages	Disadvantages
Provides more accurate power estimation since the design is complete	• Power estimation done later in the FPGA design cycle • Results will not be as accurate as those obtained using the Quartus II PowerPlay power analyzer

For more information about how to use the PowerPlay Power Analyzer in the Quartus II software, refer to the *PowerPlay Power Analysis* chapter in volume 3 of the *Quartus II Handbook*.

Entering Information into the PowerPlay Early Power Estimator

You can either manually enter power information into the PowerPlay early power estimator or load a power estimation file generated by the Quartus II software version 5.1. You can also clear all the values currently in the PowerPlay early power estimator.

Clearing All Values

All user entered values can be reset in the PowerPlay early power estimator by clicking **Reset**.

In order to use the Reset EPE feature, you must enable macros for the spreadsheet. If you have not enabled macros for the spreadsheet you will need to reset all user-entered values manually.

Manually Entering Information

You can manually enter values into the PowerPlay early power estimator in the appropriate section. White, unshaded cells are input cells and may be modified. Each section contains a column that allows you to specify a module name based on your design.

Importing a File

If you already have an existing design or a partially completed design, the power estimation report file generated by the Quartus II software contains the device resource information. You can import this device resource information from the Quartus II software power estimation file into the PowerPlay early power estimator. Importing a file saves you time and effort otherwise spent manually entering information into the PowerPlay early power estimator. You can also manually change any of the values after importing a file.

To generate the power estimation file, you must first compile your design in the Quartus II software. After compiling the design, click **Generate PowerPlay Early Power Estimator File** (Project menu). The Quartus II software creates a power estimation file with the name <*revision name*>**_early_pwr.csv**.

For more information on generating the power estimation file in the Quartus II software, refer to the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

To import data into the PowerPlay early power estimator, perform the following steps:

1. Click **Import Quartus II File** in the PowerPlay early power estimator.
2. Browse to a power estimation file generated from the Quartus II software and click **Open**. The file has a name <*revision name*>**_early_pwr.csv**.
3. Click **OK** in the confirmation window to proceed.
4. When the file is imported, click **OK**. Clicking OK acknowledges the import is complete. If there are any errors during the import, an .err file is generated with details.

After importing a file, you must verify all your information.

Importing a file from the Quartus II software populates all input parameters on the main page that were specified in the Quartus II software. These parameters include:

- Device
- Package
- Temperature grade
- Power characteristics
- Ambient temperature
- Airflow
- Heat sink
- Custom θ_{SA}
- Board thermal model
- Custom θ_{JB}
- Board temp T_B

The airflow, heat sink, custom θ_{SA}, board thermal model, custom θ_{JB}, and board temperature T_B parameters are optional. Refer to "Main Input Parameters" on page 3–1 for more information on these parameters.

The f_{MAX} values imported into the PowerPlay early power estimator are the same as the f_{MAX} values specified by the designer in the Quartus II software. You can manually edit the f_{MAX} and the toggle percentage in the PowerPlay early power estimator to suit your system requirements.

Importing Information from Early Power Estimator Version 5.1

If you already have an existing version 5.1 PowerPlay Early Power Estimator file, you can import the data directly into version 6.0 of the PowerPlay early power estimator using the Import EPE v.51 feature. This can save time and effort otherwise spent manually entering information into the PowerPlay early power estimator.

To import data from version 2.1 of the PowerPlay early power estimator, perform the following steps.

1. Click **Import EPE v5.1**.
2. Browse to the EPE and click **Open**.
3. Click **OK**.

Clicking OK, acknowledges that the import is complete.

Clicking OK clears any user-entered values and populates the PowerPlay early power estimator with device resource information from the specified PowerPlay early power estimator version 5.1 file.

After importing legacy Early Power Estimator spreadsheets, you must manually ensure that all the information is correct.

Chapter 3. Using the Cyclone II PowerPlay Early Power Estimator

Introduction

The PowerPlay Early Power Estimator spreadsheet provides the ability to enter information into sections based on architectural features. The PowerPlay Early Power Estimator spreadsheet also provides a subtotal of power consumed by each architectural feature and is reported in each section in Watts (W).

PowerPlay Early Power Estimator Spreadsheet Inputs

The following sections of the user guide explain what values you need to enter for each section of the PowerPlay Early Power Estimator spreadsheet. The different Excel worksheets of the PowerPlay Early Power Estimator spreadsheet are referred to as sections. Sections in the PowerPlay Early Power Estimator spreadsheet calculate power representing architectural features of the device, such as clocks, RAM blocks, or embedded multiplier blocks.

Main Input Parameters

Different Cyclone II devices consume different amounts of power for the same design. The larger the device, the more power it will consume because of the larger die and longer interconnects in the device.

In the **Main** section, you must enter the following parameters for the device and design:

- Device
- Package
- Temperature grade
- Power characteristics
- Ambient temperature
- Airflow
- Heat sink used
- Custom heat sink information
- Board thermal model
- Custom board thermal model information
- Board temperature

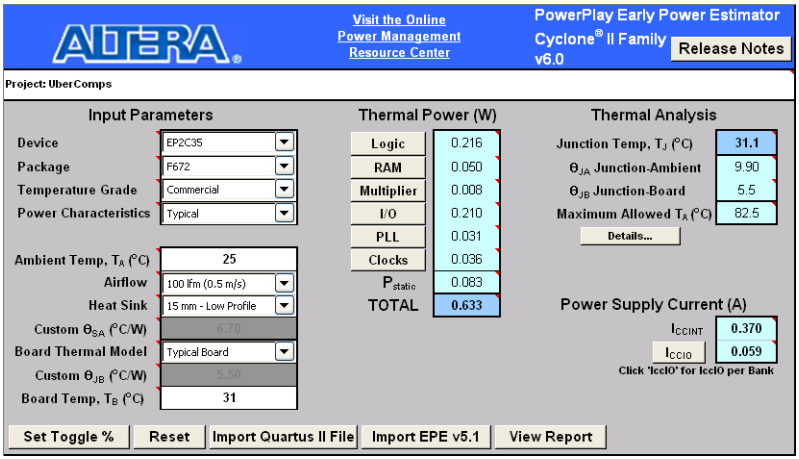
Table 3–1 describes the values that need to be specified in the **Main** section of the PowerPlay Early Power Estimator spreadsheet.

Table 3–1. Main Section Information

Input Parameter	Description
Device	Select the appropriate Cyclone II device.
Package	Select the appropriate package. The package options are dependant on the device selected.
Temperature Grade	Select whether a commercial or industrial device is being used.
Power Characteristics	Select whether you would like to estimate typical or maximum power for the design.
Ambient Temp, T_A (°C)	Enter the ambient temperature the device will be operating at. This value can range from –40 °C to 100 °C.
Airflow	Select an ambient airflow from the options of still air, 100 linear feet per minute (lfm, 0.5 m/s), 200 lfm (1 m/s), or 400 lfm (2 m/s).
Heat sink	Select the heat sink being used. You can specify no heat sink, a heat sink with set parameters or specify a custom solution. The heat sink selection will update the θ_{SA} Heatsink-Ambient parameter under Thermal Analysis. If a custom solution is selected the value will be what is entered for Custom θ_{SA} (°C/W).
Custom θ_{SA} (°C/W)	Enter a value for a custom heat sink setting. This value is only used if you set the Heat Sink parameter to "Custom Solution."
Board Thermal Model	Select the type of board to be used in thermal analysis. If no heat sink has been selected, the Altera-provided θ_{JA} value includes the board thermal pathway. If a board thermal model is selected, you must enter a board temperature in the **Board Temp** field. This field is only available when **Auto Compute T_J** is selected. Board thermal resistance is a function of device package, number of signal and power layers, % metallization at each layer, inter-layer thickness, and many other parameters. θ_{JB} values for a typical customer board stack (based on selected device and package) are provided for estimation purposes. Users should perform a detailed thermal simulation of their system to determine final junction temperature. This two-resistor thermal model is for early estimation only.
Custom θ_{JB} (°C/W)	Enter the junction-to-board thermal resistance obtained from thermal simulation if **Custom** is selected under Board Thermal Model. This field is only available when **Auto Compute T_J** is selected.
Board Temp, T_B (°C)	Enter the temperature on the PCB at the back-side of the device. This temperature is combined with the θ_{JB} value of the board to compute the junction temperature for the FPGA. This field is only available when **Auto Compute T_J** is selected. If the entered board temperature is less than ambient, the tool assumes ambient temperature in its thermal analysis since it is not possible for the board to be below ambient. Similarly, board temperatures in excess of the computed junction temperature are capped to the junction temperature.

Figure 3–1 shows the **Main** section of the Cyclone II PowerPlay Early Power Estimator spreadsheet.

Figure 3–1. Cyclone II PowerPlay Early Power Estimator Spreadsheet Main Section



Logic

A design is a combination of several design modules operating at different frequencies and toggle rates. Each design module can have a different amount of logic. For the most accurate power estimation, partition the design into different design modules. You can partition your design by grouping modules by clock frequency, location, hierarchy, or entities.

Each row in the **Logic** section represents a separate design module. You must enter the following parameters for each design module

- Clock frequency (f_{MAX}) in MHz
- Number of look-up tables (LUTs)
- Number of registers
- Toggle percentage

Table 3–2 describes the values that need to be entered in the **Logic** section of the PowerPlay Early Power Estimator spreadsheet.

Table 3–2. Logic Section Information

Column Heading	Description
Module	Enter a name for the module in this column. This is an optional value.
Clock Freq	Enter the clock frequency for the module in MHz. This value is limited by the maximum frequency specification for the device family.
# of LUTs	Enter the number of LUTs used in the whole design as reported in the Quartus II software Compilation Report in the Fitter > Resource Section > Resource Usage Summary section. For the number of LUTs used, add the values from the following rows in the Fitter Resource Usage Summary: ● -- 4 input functions ● -- 3 input functions ● -- 2 input functions ● -- Combinational cells for routing
# of FFs	Enter the number of registers used in the whole design as reported in the Quartus II software Compilation Report. The number of registers used in Cyclone II devices is reported in the Total registers row in the Fitter > Resource Section > Resource Usage Summary.
Toggle %	The average percentage of logic toggling on each clock cycle. The toggle percentage ranges from 0 to 100%. Typically, the toggle percentage is 12.5%, which is the toggle percentage of a 16-bit counter. To ensure you do not underestimate the toggle percentage, you can use a higher toggle percentage. For example, a TFF with its input tied to V_{CC} has a toggle rate of 100% because its output is changing logic states on every clock cycle. Refer to Figure 3–2 for an example. Figure 3–3 shows an example of a 4-bit counter. The first TFF with least significant bit (LSB) output `cout0` has a toggle rate of 100% because `cout0` toggles on every clock cycle. The toggle rate for the second TFF with output `cout1` is 50% since `cout1` only toggles on every two clock cycles. Consequently, the toggle rate for the third TFF with output `cout2` and fourth TFF with output `cout3` are 25% and 12.5%, respectively. Therefore, the average toggle percentage for this 4-bit counter is (100 + 50 + 25 + 12.5)/4 = 46.875%.
Thermal Power (W), Routing	This shows the estimated power consumed by the routing in W. This value is calculated automatically.
Thermal Power (W), Block	This shows the estimated power consumed by the logic elements (LEs) in W. This value is calculated automatically.
Thermal Power (W), Total	This shows the estimated power in W, based on the inputs you entered. It is the total power consumed by logic and is equal to the routing power and the block power. This value is calculated automatically.
User Comments	Enter any comments. This is an optional entry.

Figure 3–2. TFF Example

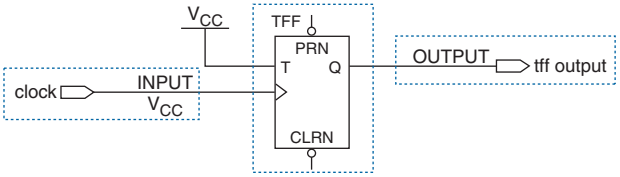


Figure 3–3. 4-Bit Counter Example

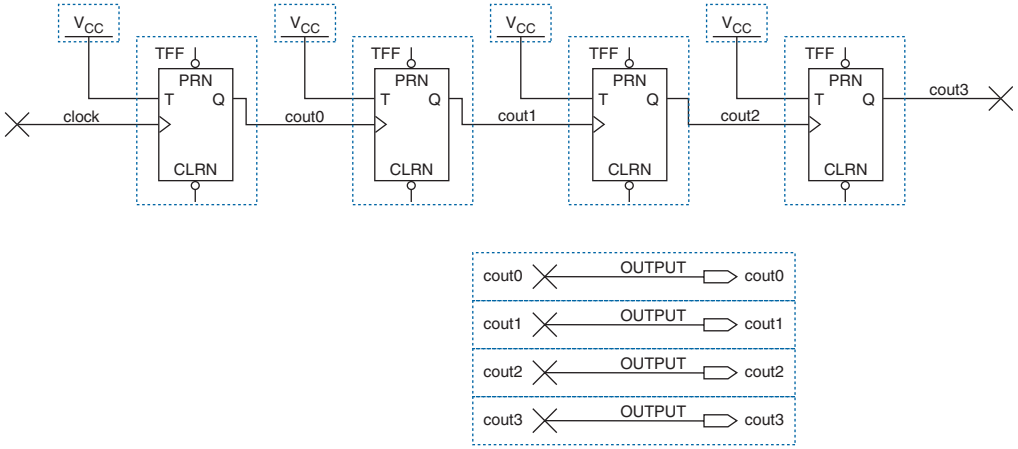


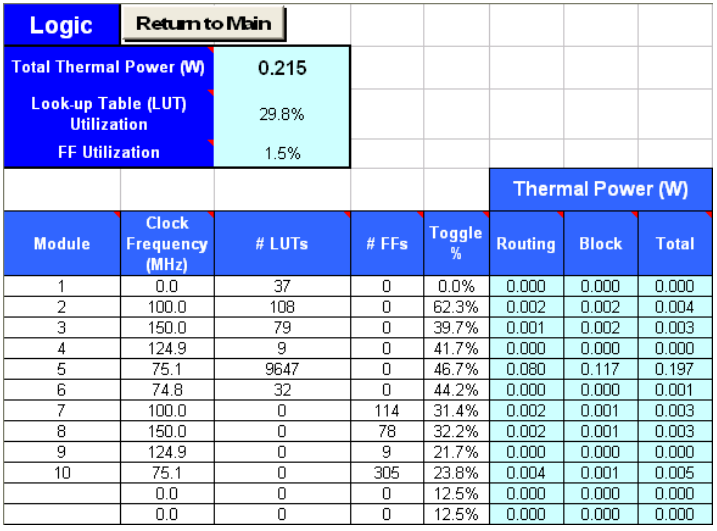
Figure 3–4 shows the Resource Usage Summary in the Quartus II software Compilation Report for a design targeting the Cyclone II device family. The Compilation Report provides the total number of LUTs and registers used by the design.

Figure 3–4. Cyclone II Resource Usage Summary in Compilation Report

Total logic elements	10,595 / 33,216 (31 %)
-- Combinational with no register	9391
-- Register only	157
-- Combinational with a register	1047
Logic element usage by number of LUT inputs	
-- 4 input functions	1648
-- 3 input functions	8008
-- <=2 input functions	782
-- Register only	157
-- Combinational cells for routing	145
Logic elements by mode	
-- normal mode	5265
-- arithmetic mode	5173
Total registers	1,204 / 33,216 (3 %)
Total LABs	863 / 2,076 (41 %)
User inserted logic elements	0
Virtual pins	0
I/O pins	131 / 475 (27 %)
-- Clock pins	4 / 8 (50 %)
Global signals	8
M4Ks	20 / 105 (19 %)
Total memory bits	90,112 / 483,840 (18 %)
Total RAM block bits	92,160 / 483,840 (19 %)
Embedded Multiplier 9-bit elements	6 / 70 (8 %)
Global clocks	8 / 16 (50 %)
Maximum fan-out node	LPLL:inst5|altpll:altpll_component|_clk0~clkctrl
Maximum fan-out	1014
Total fan-out	35425
Average fan-out	2.96

Figure 3–5 shows the Cyclone II device PowerPlay Early Power Estimator spreadsheet and the estimated power consumed by the logic in this design.

Figure 3–5. Logic Section in the PowerPlay Early Power Estimator Spreadsheet



Logic | Return to Main

Total Thermal Power (W)	0.215
Look-up Table (LUT) Utilization	29.8%
FF Utilization	1.5%

					Thermal Power (W)		
Module	Clock Frequency (MHz)	# LUTs	# FFs	Toggle %	Routing	Block	Total
1	0.0	37	0	0.0%	0.000	0.000	0.000
2	100.0	108	0	62.3%	0.002	0.002	0.004
3	150.0	79	0	39.7%	0.001	0.002	0.003
4	124.9	9	0	41.7%	0.000	0.000	0.000
5	75.1	9647	0	46.7%	0.080	0.117	0.197
6	74.8	32	0	44.2%	0.000	0.000	0.001
7	100.0	0	114	31.4%	0.002	0.001	0.003
8	150.0	0	78	32.2%	0.002	0.001	0.003
9	124.9	0	9	21.7%	0.000	0.000	0.000
10	75.1	0	305	23.8%	0.004	0.001	0.005
	0.0	0	0	12.5%	0.000	0.000	0.000
	0.0	0	0	12.5%	0.000	0.000	0.000

RAM Blocks

Cyclone II devices feature M4K RAM blocks.

Each row in the **RAM** section represents a design module where the RAM block(s) have the same data width, RAM mode, port parameters and output toggle rate. If some or all of the RAM blocks in your design have different configurations, enter the information in different rows. For each design module, you need to enter the number of RAM blocks, the data width, the RAM mode and the output toggle rate. You must also enter the following parameters for each port:

- Clock frequency, in MHz
- The percentage of time the RAM clocks are enabled
- The percentage of time the port is writing compared to reading

When selecting the RAM block mode, you must know how your RAM will be implemented by the Quartus II Compiler. For example, if a ROM is implemented with two ports, it will be considered a true dual-port memory and not a ROM. Single-port and ROM implementations only use port A. Simple dual-port and true dual-port implementations will use port A and port B.

Table 3–3 describes the parameters in the **RAM** section of the PowerPlay Early Power Estimator spreadsheet.

Table 3–3. RAM Section Information (Part 1 of 2)

Column Heading	Description
Module	Enter a name for the RAM module in this column. This is an optional value.
# RAM Blocks	Enter the number of RAM blocks in the module that have the same data width, RAM mode, port parameters, and output toggle rate. The parameters for each port are: clock frequency in MHz, the percentage of time the RAM clocks are enabled, and the percentage of time the port is writing as opposed to reading. The number of RAM blocks reported can be found in the M4K row of the Quartus II Compilation Report under Fitter > Resource Section > Resource Usage Summary.
Data Width	Enter the width of the data for the RAM block. This value must be between 1 and 18 for RAM blocks in true dual-port mode. This value must be between 1 and 36 for all other RAM modes. For RAM blocks that have different widths for port A and port B, use the larger of the two widths. The width of the RAM block can be found in the Port A Width or the Port B Width column of the Quartus II Compilation Report under Fitter > Resource Section > RAM Summary.
RAM Mode	Select from the following modes: Single-Port, Simple Dual-Port, True Dual-Port, ROM. The mode is based on how the Quartus II Compiler will implement the RAM. If you are unsure how your memory module will be implemented it is best to compile a test case in the required configuration in the Quartus II software. The RAM mode can be found in the Mode column of the Quartus II Compilation Report under Fitter > Resource Section > RAM Summary.
Port A – Clock Freq	Enter the clock frequency for port A of the RAM block(s) in MHz. This value is limited by the maximum frequency specification for the RAM type and device family.
Port A – Enable %	Enter the average percentage of time the input clock enable for port A is active, regardless of activity on RAM data and address inputs. The enable percentage ranges from 0 to 100%. The default is set to 25%.
Port A – Write %	Enter the average percentage of time port A of the RAM block is in write mode versus read mode. This is ignored for RAM blocks in ROM mode.
Port B – Clock Freq	Enter the clock frequency for port B of the RAM block(s) in MHz. This value is limited by the maximum frequency specification for the RAM type and device family. Port B is ignored for RAM blocks in ROM or single-port mode.
Port B – Enable %	Enter the average percentage of time the input clock enable for port B is active, regardless of activity on RAM data and address inputs. The enable percentage ranges from 0 to 100%. The default is set to 25%. Port B is ignored for RAM blocks in ROM or single-port mode.
Port B – R/W %	For RAM blocks in true dual-port mode, enter the average percentage of time port B of the RAM block is in write mode versus read mode. For RAM blocks in simple dual-port mode, enter the percentage of time port B of the RAM block is reading. You cannot write to port B in simple dual-port mode. Port B is ignored for RAM blocks in ROM or single-port mode.

Table 3–3. RAM Section Information (Part 2 of 2)

Column Heading	Description
Toggle %	Average percentage of clock cycles that each block output signal changes value. Multiplied by clock frequency to determine number of transitions per second. 50% corresponds to a randomly changing signal. A random signal changes states only half the time.
Valid Width/Mode	This check will fail if the entered data width exceeds that allowed by the RAM mode. See the description of the data width column for details.
Thermal Power (W), Routing	This shows the estimated power consumed by the routing in W. This value is calculated automatically.
Thermal Power (W), Block	This shows the estimated power consumed by the RAM blocks in W. This value is calculated automatically.
Thermal Power (W), Total	This shows the estimated power in W, based on the inputs you entered. It is the total power consumed by RAM blocks and is equal to the routing power and the block power. This value is calculated automatically.
User Comments	Enter any comments. This is an optional entry.

Figure 3–6 shows the Resource Usage Summary section in the Quartus II software Compilation Report for a design targeting the Cyclone II device family. The Compilation Report provides the number of RAM resources being used. Figure 3–7 shows the RAM Summary in the Quartus II software Compilation Report for a design targeting the Cyclone II device family. The Compilation Report provides the RAM mode and the data width.

Figure 3–6. Resource Usage Summary

Total logic elements	10,595 / 33,216 (31 %)
-- Combinational with no register	9391
-- Register only	157
-- Combinational with a register	1047
Logic element usage by number of LUT inputs	
-- 4 input functions	1648
-- 3 input functions	8008
-- <=2 input functions	782
-- Register only	157
-- Combinational cells for routing	145
Logic elements by mode	
-- normal mode	5265
-- arithmetic mode	5173
Total registers	1,204 / 33,216 (3 %)
Total LABs	863 / 2,076 (41 %)
User inserted logic elements	0
Virtual pins	0
I/O pins	131 / 475 (27 %)
-- Clock pins	4 / 8 (50 %)
Global signals	8
M4Ks	20 / 105 (19 %)
Total memory bits	90,112 / 483,840 (18 %)
Total RAM block bits	92,160 / 483,840 (19 %)
Embedded Multiplier 9-bit elements	6 / 70 (8 %)
Global clocks	8 / 16 (50 %)
Maximum fan-out node	LPLL:inst5|altpll:altpll_component|_clk0~clkctrl
Maximum fan-out	1014
Total fan-out	35425
Average fan-out	2.96

Figure 3–7. RAM Summary in Compilation Report

Fitter RAM Summary

	Name	Type	Mode	Port A Depth	Port A Width	Port B Depth	Port B Width	Port A Input Registers	Port A Output Registers	Port B Input Registers	Port B Output Registers	Size	Implementation Bits	M4Ks
1	Case2:inst4|altsyncram:altsyncram_component|altsyncram_pdv:auto_generated|ALTSYNCRAM	AUTO	Single Port	512	36	--	--	yes	yes	--	--	49152	49152	11
2	Case3:inst23|altsyncram:altsyncram_component|altsyncram_voe1:auto_generated|ALTSYNCRAM	M4K	Simple Dual Port	256	36	256	36	yes	no	yes	yes	9216	9216	2
3	Case3:inst|altsyncram:altsyncram_component|altsyncram_voe1:auto_generated|ALTSYNCRAM	M4K	Simple Dual Port	256	36	256	36	yes	no	yes	yes	9216	9216	2
4	Case4:inst20|altsyncram:altsyncram_component|altsyncram_n9q1:auto_generated|ALTSYNCRAM	M4K	True Dual Port	512	36	512	36	yes	yes	yes	yes	18432	18432	4
5	Case7:inst13|altsyncram:altsyncram_component|altsyncram_v6u:auto_generated|ALTSYNCRAM	M4K	ROM	512	8	--	--	yes	yes	--	--	4096	4096	1

Figure 3–8 shows the Cyclone II device PowerPlay Early Power Estimator spreadsheet and the estimated power consumed by RAM blocks in this design.

Figure 3–8. RAM Section in the PowerPlay Early Power Estimator Spreadsheet

RAM | Return to Main

Total Thermal Power (W)	0.050
M4K Utilization	23.8%

				Port A			Port B					Thermal Power (W)		
Module	# RAM Blocks	Data Width	RAM Mode	Clock Freq (MHz)	Enable %	Write %	Clock Freq (MHz)	Enable %	R/W %	Toggle %	Valid Width/ Mode	Routing	Block	Total
1	1	6	Single-Port	75.1	100%	50%	0.0	0%	0%	50.0%	Yes	0.000	0.001	0.001
2	2	18	Simple Dual-Port	100.0	100%	50%	100.0	100%	100%	50.0%	Yes	0.001	0.003	0.005
3	9	4	True Dual-Port	100.0	100%	50%	150.0	100%	50%	50.0%	Yes	0.003	0.022	0.025
4	1	8	ROM	124.9	100%	0%	0.0	0%	0%	50.0%	Yes	0.000	0.001	0.002
5	10	9	Single-Port	75.1	100%	50%	0.0	0%	0%	50.0%	Yes	0.003	0.008	0.011
6	2	18	Simple Dual-Port	150.0	100%	50%	150.0	100%	100%	50.0%	Yes	0.002	0.005	0.007
	0	1	Simple Dual-Port	0.0	25%	50%	0.0	25%	50%	50.0%	Yes	0.000	0.000	0.000
	0	1	Simple Dual-Port	0.0	25%	50%	0.0	25%	50%	50.0%	Yes	0.000	0.000	0.000

Multiplier Blocks

Cyclone II devices implement DSP functions in embedded multipliers. These embedded multiplier blocks are optimized for multiplier-intensive low-cost (DSP) applications. The **Multiplier** section in the Cyclone II PowerPlay Early Power Estimator spreadsheet provides power information for Cyclone II multiplier blocks.

Each row in the **Multiplier** section represents a multiplier design module where all instances of the module have the same configuration, clock frequency, toggle percentage and register usage. If some (or all) multiplier instances have different configurations, you need to enter the information in different rows. You must enter the following information for each multiplier module:

- Configuration
- Clock frequency (f_{MAX}) in MHz
- Number of instances
- Toggle percentage of the data outputs
- Whether or not the inputs and outputs are registered

For more information on Cyclone II embedded multiplier configurations, see the *Embedded Multipliers in Cyclone II Devices* chapter in Volume 1 of the *Cyclone II Device Handbook*.

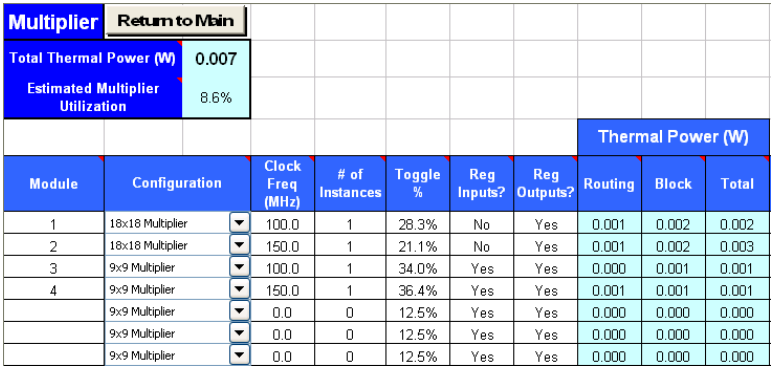
Table 3–4 describes the values that need to be entered in the **Multiplier** section of the PowerPlay Early Power Estimator spreadsheet.

Table 3–4. Multiplier Section Information

Column Heading	Description
Module	Enter a name for the embedded multiplier module in this column. This is an optional value.
Configuration	Select the multiplier block configuration. Cyclone II embedded multiplier blocks offer the following configurations: • 9 × 9 multiplier • 18 × 18 multiplier
Clock Freq	Enter the clock frequency for the module in MHz. This value is limited by the maximum frequency specification for the device family.
# of Instances	Enter the number of instances that have the same configuration, clock frequency, toggle percentage and register usage. This value is independent of the number of multiplier blocks being used.
Toggle %	Enter the average percentage of the multiplier block data outputs toggling on each clock cycle. The toggle percentage ranges from 0 to 50%. Typically the toggle percentage is 12.5%. For a more conservative power estimate, you can use a higher toggle percentage.
Reg Inputs?	Select whether the input to the multiplier block is registered using the dedicated input registers. If the dedicated input registers in the multiplier block are being used, select **Yes**. If the inputs are registered using registers in LEs, then select **No**.
Reg Outputs?	Select whether the input to the multiplier block is registered using the dedicated output registers. If the dedicated output registers in the multiplier block are being used, select **Yes**. If the outputs are registered using registers in LEs, then select **No**.
Thermal Power (W), Routing	This shows the estimated power consumed by the routing in W. This value is calculated automatically.
Thermal Power (W), Block	This shows the estimated power consumed by the multipliers in W. This value is calculated automatically.
Thermal Power (W), Total	This shows the estimated power in W, based on the inputs you entered. It is the total power consumed by multiplier blocks and is equal to the routing power and the block power. This value is calculated automatically.
User Comments	Enter any comments. This is an optional entry.

Figure 3–9 shows the Cyclone II device PowerPlay Early Power Estimator spreadsheet and the estimated power consumed by the multiplier blocks in this design.

Figure 3–9. Multiplier Section in the PowerPlay Early Power Estimator Spreadsheet



Multiplier | Return to Main

Total Thermal Power (W)	0.007
Estimated Multiplier Utilization	8.6%

							Thermal Power (W)		
Module	Configuration	Clock Freq (MHz)	# of Instances	Toggle %	Reg Inputs?	Reg Outputs?	Routing	Block	Total
1	18x18 Multiplier	100.0	1	28.3%	No	Yes	0.001	0.002	0.002
2	18x18 Multiplier	150.0	1	21.1%	No	Yes	0.001	0.002	0.003
3	9x9 Multiplier	100.0	1	34.0%	Yes	Yes	0.000	0.001	0.001
4	9x9 Multiplier	150.0	1	36.4%	Yes	Yes	0.001	0.001	0.001
	9x9 Multiplier	0.0	0	12.5%	Yes	Yes	0.000	0.000	0.000
	9x9 Multiplier	0.0	0	12.5%	Yes	Yes	0.000	0.000	0.000
	9x9 Multiplier	0.0	0	12.5%	Yes	Yes	0.000	0.000	0.000

General I/O Pins

Cyclone II devices feature programmable I/O pins that support a wide range of industry I/O standards for increased design flexibility. The **I/O** section in the PowerPlay Early Power Estimator spreadsheet allows you to estimate the I/O pin power consumption based on the pin's I/O standards.

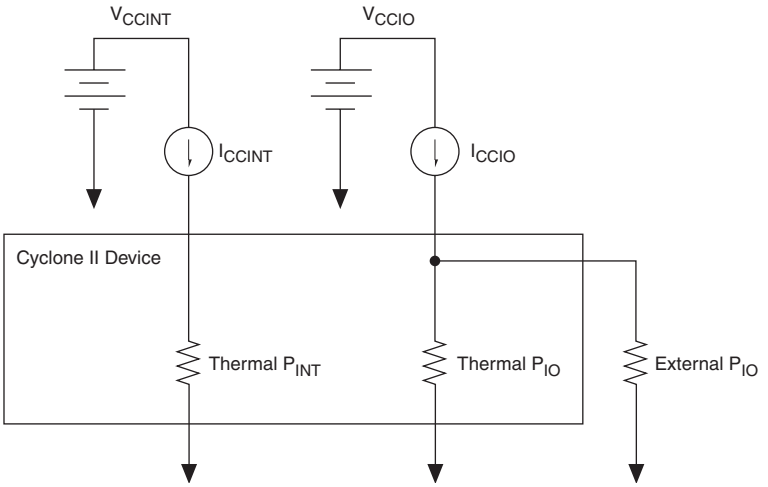
The PowerPlay Early Power Estimator spreadsheet assumes you are using external termination resistors when you design with I/O standards that recommend termination resistors (e.g., SSTL and HSTL). If your design does not use external termination resistors, you should choose the LVTTL I/O standard with the same V_{CCIO} and similar drive strength as the terminated I/O standard. For example, if you are using the SSTL-2 class II I/O standard without termination resistors (using a point-to-point connection), you should select **LVTTL/LVCMOS 2.5-V** as your I/O standard and **16mA** as the Drive Strength in the PowerPlay Early Power Estimator spreadsheet.

The power reported for I/O signals includes thermal and external I/O power. The total thermal power is the sum of the thermal power consumed by the device based on each power rail.

thermal power = thermal P_{INT} + thermal P_{IO}

Figure 3–10 shows a graphical representation of the I/O power consumption. The I_{CCIO} rail power includes both the thermal P_{IO} and the external P_{IO}.

Figure 3–10. I/O Power Representation



The V_{REF} pins consume minimal current (less than 10 µA) and is negligible when compared to the power consumed by the general purpose I/O pins. Therefore, the PowerPlay Early Power Estimator spreadsheet does not include the current for V_{REF} pins in the calculations.

Each row in the **I/O** section represents a design module where the I/O pins have the same frequency, toggle percentage, average capacitive load, I/O standard, data rate, and I/O bank. You must enter the following parameters for each design module:

- I/O standard
- Clock frequency (f_{MAX}) in MHz
- Number of output, input, and bidirectional pins
- I/O bank
- Pin toggle percentage
- Output enable percentage
- Average capacitance of the load
- I/O data rate

Table 3–5 describes the I/O bank parameters in the I/O section of the PowerPlay Early Power Estimator spreadsheet.

Table 3–5. I/O Bank Information in the I/O Section

Column Heading	Description
V_{CCIO}	Select the V_{CCIO} voltage for each bank. Used to cross-check selected I/O standards in table below for warning purposes.
I_{CCIO} (A)	This shows the total supply current due to the I/O pins in each I/O bank. This may be higher than the thermal power due to current supplied to off-chip termination resistors.
Unassigned	This represents the I_{CCIO} of all I/O modules not assigned to an I/O bank.

Figure 3–11 shows how the V_{CCIO} level is listed for each I/O bank. The PowerPlay Early Power Estimator spreadsheet shows the I_{CCIO} listed for each bank. Select the V_{CCIO} voltage in the V_{CCIO} column.

Figure 3–11. V_{CCIO} Listed for Each I/O Bank

	V_{CCIO}	I_{CCIO} (A)
I/O Bank 1	3.3	0.0054
I/O Bank 2	2.5	0.0077
I/O Bank 3	1.8	0.0000
I/O Bank 4	3.3	0.0339
I/O Bank 5	3.3	0.0068
I/O Bank 6	3.3	0.0014
I/O Bank 7	3.3	0.0012
I/O Bank 8	3.3	0.0025
Unassigned		0.0000

Table 3–6 describes the parameters in the **I/O** section of the PowerPlay Early Power Estimator spreadsheet.

Table 3–6. I/O Section Information (Part 1 of 2)

Column Heading	Description
Module	Enter a name for the module in this column. This is an optional value.
I/O Standard	Select the I/O standard used for the input, output or bidirectional pins in this module from the list. The calculated I/O power varies based on the I/O standard. For I/O standards that recommend termination (SSTL and HSTL), the PowerPlay Early Power Estimator spreadsheet assumes you are using external termination resistors. If you are not using external termination resistors, you should choose the LVTTL I/O standard with the same voltage and similar drive strength as the terminated I/O standard. There are up and down scroll bars to view all the I/O standards in the drop-down list.
Clock Freq	Enter the clock frequency for the module in MHz. This is the frequency of the clock used to feed the I/O registers or the registers that feed the I/O pins. This value is limited by the maximum I/O pin frequency specification for the device family.
# Output Pins	Enter the number of output pins used in this module. A differential pair of pins should be considered as one pin.
# Input Pins	Enter the number of input pins used in this module. A differential pair of pins should be considered as one pin.
# Bidir Pins	Enter the number of bidirectional pins used in this module.
I/O Bank	Select the I/O bank the module will be located in. If you do not know which I/O bank the pins will be assigned to, leave the value as "?."
Toggle %	Enter the average percentage of output and bidirectional pins toggling on each clock cycle. The toggle percentage ranges from 0 to 200%. If the pin uses a double data rate (DDR), you can set the data rate to single data rate (SDR) and double the toggle percentage. The Quartus II software will often use this method to output information. Typically the toggle percentage is 12.5%. To be more conservative, you can use a higher toggle percentage.
OE %	Enter the average percentage of time that the output pin is enabled. This is only applicable for bidirectional pins or in cases when output pins require an output enable.
Load (pF)	Enter the average external capacitive load in pico-Farads (pF) for the output and bidirectional pins in this clock domain.
Data Rate	Select either **SDR** or **DDR** as the I/O data rate. If the data rate of the pin is DDR, it is possible to set the data rate to SDR and double the toggle percentage. The Quartus II software will often use this method to output information.
Bank I/O Std Check	This indicates whether the selected I/O standard is available on the selected I/O bank. Not all I/O banks can implement every I/O standard.
Bank Voltage Check	This indicates whether or not the selected I/O bank has a voltage compatible with the selected I/O standard.
Thermal Power (W), Routing	This shows the estimated I/O power consumed by the routing in W. This value is calculated automatically.

Table 3–6. I/O Section Information (Part 2 of 2)

Column Heading	Description
Thermal Power (W), Block	This shows the estimated power consumed by the I/O elements (IOEs) in W. This value is calculated automatically.
Thermal Power (W), Total	This shows the estimated power in W, based on the inputs you entered. It is the total power consumed by the I/O pin and is equal to the routing power and the block power. This value is calculated automatically.
Supply Current (A), I_{CCINT}	This shows the internal supply current required for the module. This value is calculated automatically.
Supply Current (A), I_{CCIO}	This shows the I/O supply current required for the module. The total I_{CCIO} value for an I/O bank is listed based on the I/O bank section. This value is calculated automatically.
User Comments	Enter any comments. This is an optional entry.

Figure 3–12 shows the PowerPlay Early Power Estimator spreadsheet **I/O** section.

Figure 3–12. PowerPlay Early Power Estimator Spreadsheet I/O Section

													Thermal Power (W)			Supply Current (A)	
Module	I/O Standard	Clock Freq (MHz)	# Output Pins	# Input Pins	# Bidir Pins	I/O Bank	Toggle %	OE %	Load (pF)	Data Rate	Bank I/O Std Check	Bank Voltage Check	Routing	Block	Total	I_{CCINT}	I_{CCIO}
1	3.3 V 24mA	100.0	1	0	0	1	248.6%	100%	0	SDR	PASS	PASS	0.000	0.014	0.014	0.000	0.004
2	3.3 V 24mA	0.0	1	0	0	6	0.0%	100%	0	SDR	PASS	PASS	0.000	0.000	0.000	0.000	0.000
3	3.3 V 24mA	0.0	0	1	0	7	0.0%	100%	0	SDR	PASS	PASS	0.000	0.000	0.000	0.000	0.000
4	1.8 V 12mA	0.0	36	0	0	3	0.0%	100%	0	SDR	PASS	PASS	0.000	0.003	0.003	0.003	0.000
5	3.3 V 24mA	175.0	0	1	0	6	200.0%	100%	0	SDR	PASS	PASS	0.000	0.001	0.002	0.000	0.000
6	3.3 V 24mA	150.0	0	2	0	4	22.8%	100%	0	SDR	PASS	PASS	0.000	0.000	0.001	0.000	0.000
7	3.3 V 24mA	150.0	30	0	0	4	36.1%	100%	0	SDR	PASS	PASS	0.000	0.112	0.112	0.004	0.033
8	3.3 V 24mA	0.0	0	2	0	4	0.0%	100%	0	SDR	PASS	PASS	0.000	0.000	0.000	0.000	0.000
9	3.3 V 24mA	75.0	0	1	0	4	200.0%	100%	0	SDR	PASS	PASS	0.000	0.001	0.001	0.000	0.000
10	3.3 V 24mA	99.8	0	1	0	2	200.0%	100%	0	SDR	PASS	PASS	0.000	0.001	0.001	0.000	0.000
11	3.3 V 24mA	99.8	0	1	0	8	200.0%	100%	0	SDR	PASS	PASS	0.000	0.001	0.001	0.000	0.000
12	3.3 V 24mA	150.0	6	0	0	5	37.0%	100%	0	SDR	PASS	PASS	0.000	0.020	0.020	0.001	0.006
13	3.3 V 24mA	74.8	1	0	0	8	80.5%	100%	0	SDR	PASS	PASS	0.000	0.004	0.004	0.000	0.001
14	3.3 V 24mA	0.0	0	1	0	2	0.0%	100%	0	SDR	PASS	PASS	0.000	0.000	0.000	0.000	0.000
15	3.3 V 24mA	100.0	0	2	0	4	49.5%	100%	0	SDR	PASS	PASS	0.000	0.001	0.001	0.000	0.000
16	3.3 V 24mA	75.1	0	1	0	8	65.9%	100%	0	SDR	PASS	PASS	0.000	0.000	0.000	0.000	0.000
17	2.5 V 8mA	0.0	0	2	0	2	0.0%	100%	0	SDR	PASS	PASS	0.000	0.000	0.000	0.000	0.000
18	3.3 V 24mA	175.0	8	0	0	7	0.0%	100%	0	SDR	PASS	PASS	0.000	0.001	0.001	0.001	0.000
19	2.5 V 8mA	100.0	0	0	36	2	33.8%	50%	0	SDR	PASS	PASS	0.001	0.025	0.026	0.006	0.007
	3.3 V 24mA	0.0	0	0	0	?	12.5%	100%	0	SDR	N/A	N/A	0.000	0.000	0.000	0.000	0.000

The PowerPlay Early Power Estimator spreadsheet verifies whether or not the I/O standard selected is available in the selected I/O bank. If there is a discrepancy, it is displayed in the **Bank I/O Std Check** column, as shown in Figure 3–13. The PowerPlay Early Power Estimator spreadsheet

also verifies that the V_{CCIO} levels match the I/O standards for each I/O bank. If there is a discrepancy, it is displayed in the **Bank Voltage Check** column, as shown in Figure 3–14.

Figure 3–13. I/O Standard Verification

Bank I/O Std Check
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS

Figure 3–14. PowerPlay Early Power Estimator Spreadsheet Checks for V_{CCIO} Inconsistencies

Bank Voltage Check
PASS
PASS
FAIL?
PASS
PASS
PASS
PASS
PASS
PASS
FAIL?
PASS
PASS

The PowerPlay early power estimator shows the I_{CCIO} listed for each bank. Select the V_{CCIO} in the V_{CCIO} column. The PowerPlay early power estimator checks whether or not your selected V_{CCIO} is acceptable based on the I/O standard and I/O bank combination in the listed modules. If

the I/O standard, I/O bank, and I/O bank V_{CCIO} correspond correctly for a design module, the V_{CCIO} Check value shows **OK**. If there is a discrepancy, the V_{CCIO} Check value shows **FAIL?**.

Importing the Quartus II estimation file automatically populates the V_{CCIO} voltages. However, certain designs may have discrepancies. This occurs most often if I/O standards that are listed as different voltages in the PowerPlay Early Power Estimator spreadsheet can actually be in the same I/O bank on the device.

For more information on I/O standard guidelines, see the *Selectable I/O Standards in Cyclone II Devices* chapter in volume 1 of the *Cyclone II Device Handbook*. If there are discrepancies between the V_{CCIO} voltages in banks, the PowerPlay Early Power Estimator spreadsheet displays the following message:

> *** Bank and I/O voltage selection inconsistent with I/O bank voltage. See 'Bank Voltage Check' column.***

Ensure that the correct V_{CCIO} is selected for the bank.

Figure 3–15 shows an example of the **Output Pins** report in the Quartus II software Compilation Report for a design targeting a Cyclone II device. The Compilation Report lists the I/O standard used on each pin. Figure 3–12 shows the Cyclone II PowerPlay Early Power Estimator spreadsheet and the estimated power consumed by the I/O pins.

Figure 3–15. Output Pins Report in Compilation Report

Output Pins

	Name	Pin #	I/O Bank	X coordinate	Y coordinate	Cell number	Output Register	Output Enable Register	Power Up High	PCI I/O Enabled	Open Drain	TRI Primitive	Bus Hold	Weak Pull Up	I/O Standard	Current Strength	Termination	Location assigned by	Load
1	LogicOut	W11	8	18	0	1	no	no	no	no	no	no	no	Off	LVTTL	24mA	Off	Fitter	0 pF
2	c3out[0]	F11	3	18	36	1	no	no	no	no	no	no	no	Off	1.8 V	12mA	Off	Fitter	0 pF
3	c3out[10]	G11	3	22	36	1	no	no	no	no	no	no	no	Off	1.8 V	12mA	Off	Fitter	0 pF
4	c3out[11]	D9	3	16	36	3	no	no	no	no	no	no	no	Off	1.8 V	12mA	Off	Fitter	0 pF
5	c3out[12]	B6	3	3	36	1	no	no	no	no	no	no	no	Off	1.8 V	12mA	Off	Fitter	0 pF
6	c3out[13]	A6	3	3	36	0	no	no	no	no	no	no	no	Off	1.8 V	12mA	Off	Fitter	0 pF
7	c3out[14]	F10	3	14	36	1	no	no	no	no	no	no	no	Off	1.8 V	12mA	Off	Fitter	0 pF
8	c3out[15]	G12	3	27	36	2	no	no	no	no	no	no	no	Off	1.8 V	12mA	Off	Fitter	0 pF
9	c3out[16]	H10	3	7	36	1	no	no	no	no	no	no	no	Off	1.8 V	12mA	Off	Fitter	0 pF
10	c3out[17]	D12	3	24	36	2	no	no	no	no	no	no	no	Off	1.8 V	12mA	Off	Fitter	0 pF
11	c3out[18]	B8	3	16	36	1	no	no	no	no	no	no	no	Off	1.8 V	12mA	Off	Fitter	0 pF
12	c3out[19]	A7	3	11	36	0	no	no	no	no	no	no	no	Off	1.8 V	12mA	Off	Fitter	0 pF
13	c3out[1]	J9	3	5	36	0	no	no	no	no	no	no	no	Off	1.8 V	12mA	Off	Fitter	0 pF
14	c3out[20]	D10	3	20	36	0	no	no	no	no	no	no	no	Off	1.8 V	12mA	Off	Fitter	0 pF
15	c3out[21]	J14	3	24	36	0	no	no	no	no	no	no	no	Off	1.8 V	12mA	Off	Fitter	0 pF
16	c3out[22]	G9	3	7	36	0	no	no	no	no	no	no	no	Off	1.8 V	12mA	Off	Fitter	0 pF
17	c3out[23]	J11	3	27	36	0	no	no	no	no	no	no	no	Off	1.8 V	12mA	Off	Fitter	0 pF
18	c3out[24]	C11	3	29	36	3	no	no	no	no	no	no	no	Off	1.8 V	12mA	Off	Fitter	0 pF
19	c3out[25]	J10	3	27	36	1	no	no	no	no	no	no	no	Off	1.8 V	12mA	Off	Fitter	0 pF
20	c3out[26]	B11	3	29	36	2	no	no	no	no	no	no	no	Off	1.8 V	12mA	Off	Fitter	0 pF
21	c3out[27]	C12	3	29	36	1	no	no	no	no	no	no	no	Off	1.8 V	12mA	Off	Fitter	0 pF

Phase-Locked Loops

Cyclone II devices feature fast Phase-Locked Loops (PLLs).

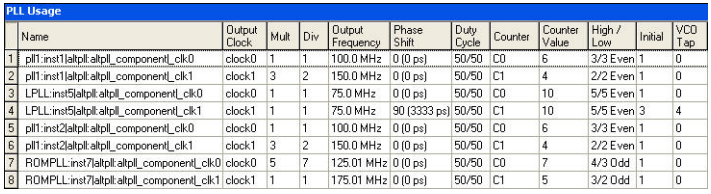
Each row in the **PLL** section represents one or more PLLs in the device. You need to enter the maximum output frequency and the VCO frequency for each PLL. Table 3–7 describes the values that need to be entered in the **PLL** section of the PowerPlay Early Power Estimator spreadsheet.

Table 3–7. PLL Section Information

Column Heading	Description
Module	Enter a name for the PLL in this column. This is an optional value.
# PLL Blocks	Enter the number of PLL blocks with the same specific output frequency and VCO frequency combination.
Output Freq	Enter the maximum output frequency (f_{MAX}) of the PLL in MHz. The maximum output frequency is reported in the PLL Usage column of the Quartus II Compilation Report under Fitter > Resource Section > PLL Usage > Output Frequency. If there are multiple clock outputs from the PLL, choose the maximum output frequency listed.
VCO Freq	Enter the frequency of the voltage controlled oscillator in MHz. The VCO frequency is reported in the Nominal VCO frequency row of the Quartus II Compilation Report under Fitter > Resource Section > PLL Summary > Nominal VCO frequency.
Total Power	This shows the estimated combined power for V_{CCA} and V_{CCD} in W, based on the maximum output frequency and the VCO frequency you entered. This value is calculated automatically.
User Comments	Enter any comments. This is an optional entry.

Figure 3–16 shows the PLL Usage section in the Quartus II software Compilation Report for a design targeting a Cyclone II device. The Compilation Report provides the maximum frequency a PLL outputs.

Figure 3–16. PLL Usage in Compilation Report



PLL Usage

	Name	Output Clock	Mult	Div	Output Frequency	Phase Shift	Duty Cycle	Counter	Counter Value	High / Low	Initial	VCO Tap
1	pll1:inst1|altpll:altpll_component|_clk0	clock0	1	1	100.0 MHz	0 (0 ps)	50/50	C0	6	3/3 Even	1	0
2	pll1:inst1|altpll:altpll_component|_clk1	clock1	3	2	150.0 MHz	0 (0 ps)	50/50	C1	4	2/2 Even	1	0
3	LPLL:inst5|altpll:altpll_component|_clk0	clock0	1	1	75.0 MHz	0 (0 ps)	50/50	C0	10	5/5 Even	1	0
4	LPLL:inst5|altpll:altpll_component|_clk1	clock1	1	1	75.0 MHz	90 (3333 ps)	50/50	C1	10	5/5 Even	3	4
5	pll1:inst2|altpll:altpll_component|_clk0	clock0	1	1	100.0 MHz	0 (0 ps)	50/50	C0	6	3/3 Even	1	0
6	pll1:inst2|altpll:altpll_component|_clk1	clock1	3	2	150.0 MHz	0 (0 ps)	50/50	C1	4	2/2 Even	1	0
7	ROMPLL:inst7|altpll:altpll_component|_clk0	clock0	5	7	125.01 MHz	0 (0 ps)	50/50	C0	7	4/3 Odd	1	0
8	ROMPLL:inst7|altpll:altpll_component|_clk1	clock1	1	1	175.01 MHz	0 (0 ps)	50/50	C1	5	3/2 Odd	1	0

Figure 3–17 shows the PLL Summary in the Quartus II software Compilation Report for a design targeting a Cyclone II device. The Compilation Report provides the VCO frequency of a PLL.

Figure 3–17. PLL Summary in Compilation Report

PLL Summary

	Name	pll1:inst1|altpll:altpll_component|pll	LPLL:inst5|altpll:altpll_component|pll	pll1:inst2|altpll:altpll_component|pll	ROMPLL:inst7|altpll:altpll_component|pll
1	PLL mode	Normal	Normal	Normal	Normal
2	Compensate clock	clock0	clock0	clock0	clock0
3	Gate lock counter	--	--	--	--
4	Input frequency 0	100.0 MHz	75.0 MHz	100.0 MHz	175.01 MHz
5	Input frequency 1	--	--	--	--
6	Nominal PFD frequency	100.0 MHz	75.0 MHz	100.0 MHz	175.0 MHz
7	Nominal VCO frequency	599.9 MHz	750.2 MHz	599.9 MHz	874.9 MHz
8	VCO post scale	--	--	--	--
9	VCO multiply	--	--	--	--
10	VCO divide	--	--	--	--
11	Freq min lock	83.33 MHz	50.0 MHz	83.33 MHz	100.0 MHz
12	Freq max lock	166.67 MHz	100.0 MHz	166.67 MHz	200.0 MHz
13	M VCO Tap	0	0	0	0
14	M Initial	1	1	1	1
15	M value	6	10	6	5
16	N value	1	1	1	1
17	Preserve counter order	Off	Off	Off	Off
18	PLL location	PLL_1	PLL_3	PLL_4	PLL_2
19	Inclk0 signal	clkab	lclk	clkfreq	romclk
20	Inclk1 signal	--	--	--	--

Figure 3–18 shows the Cyclone II device PowerPlay Early Power Estimator spreadsheet and the estimated power consumed by PLLs in this design.

Figure 3–18. PLL Section in the PowerPlay Early Power Estimator Spreadsheet

PLL | Return to Main

Total Thermal Power (W)	0.031
PLL Utilization	4 / 4

This section only estimates power from the PLL Control Blocks and does not include the power from the PLL clock output networks. Please enter additional parameters in the "Clocks" section.

Module	# PLL Blocks	Output Freq (MHz)	VCO Freq (MHz)	Total Power (W)	User Comments
1	2	150.0	599.9	0.013	
2	1	75.0	750.2	0.008	
3	1	175.0	874.9	0.010	
	0	0.0	0.0	0.000	

Clocks

Cyclone II devices have a total of 16 global clock networks. Cyclone II devices do not have regional clock networks.

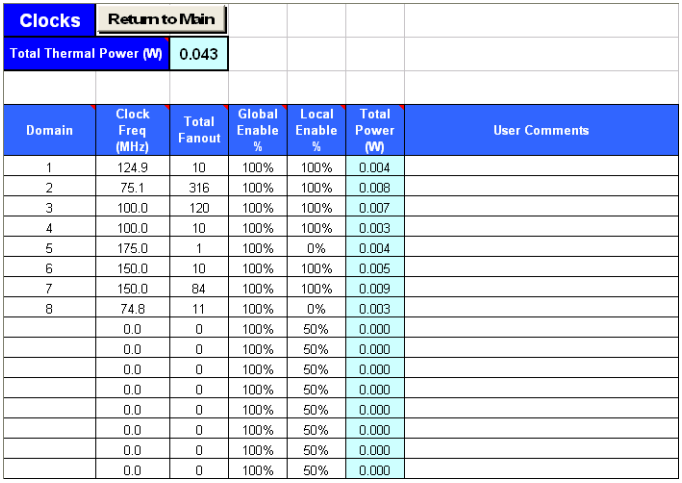
Each row in the **Clocks** section represents a clock network or a separate clock domain. You must enter the clock frequency (f_{MAX}) in MHz and the total fanout for each clock network used. Table 3–8 describes the parameters in the **Clock** section of the PowerPlay Early Power Estimator spreadsheet.

Table 3–8. Clock Section Information

Column Heading	Description
Domain	Enter a name for the clock network in this column. This is an optional value.
Clock frequency (MHz)	Enter the clock frequency for the clock network. This value is limited by the maximum frequency specification.
Total Fanout	Enter the number of registers, multiplier blocks, and memory blocks driven by the clock network. The number of resources driven by every global clock and regional clock signal is reported in the Fan-out column of the Quartus II Compilation Report under Fitter > Resource Section > Global & Other Fast Signals > Fan-out.
Global Enable %	Enter the average % of time that the entire clock tree is enabled. Each global clock buffer has an enable signal that can be used to dynamically shut down the entire clock tree.
Local Enable %	Enter the average % of time that clock enable is high for destination flip flops. Local clock enables for flip flops in the LEs are promoted to logic array block (LAB)-wide signals. When a given flip flop is disabled, the LAB-wide clock is also disabled, cutting clock power in addition to power for down-stream logic. This sheet models only the impact on clock tree power.
Total Power	This shows the estimated power in W, based on the f_{MAX} and total fan-out you entered. This value is calculated automatically.
User Comments	Enter any comments. This is an optional entry.

Figure 3–19 shows the Cyclone II PowerPlay Early Power Estimator spreadsheet and the estimated power consumed by clocks for this design.

Figure 3–19. Clocks Section in the PowerPlay Early Power Estimator Spreadsheet



Clocks | Return to Main

Total Thermal Power (W) 0.043

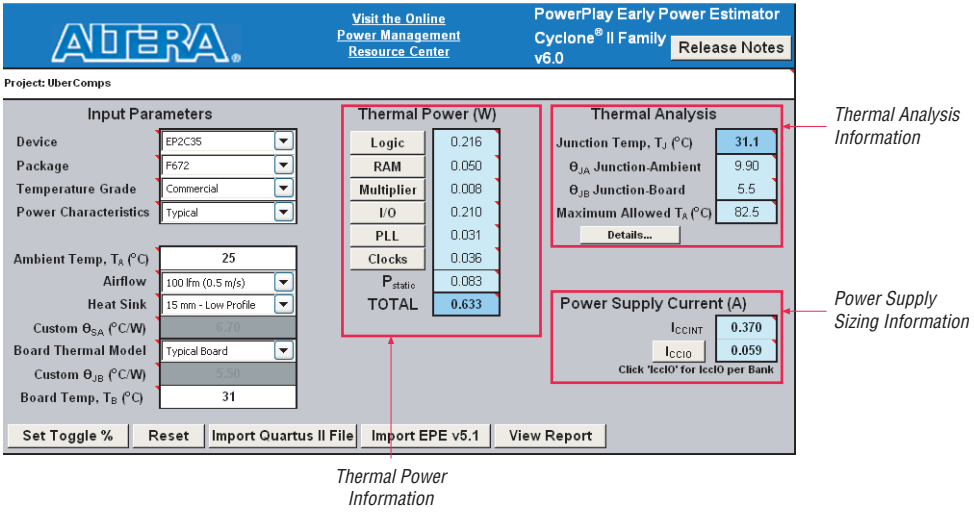
Domain	Clock Freq (MHz)	Total Fanout	Global Enable %	Local Enable %	Total Power (W)	User Comments
1	124.9	10	100%	100%	0.004	
2	75.1	316	100%	100%	0.008	
3	100.0	120	100%	100%	0.007	
4	100.0	10	100%	100%	0.003	
5	175.0	1	100%	0%	0.004	
6	150.0	10	100%	100%	0.005	
7	150.0	84	100%	100%	0.009	
8	74.8	11	100%	0%	0.003	
	0.0	0	100%	50%	0.000	
	0.0	0	100%	50%	0.000	
	0.0	0	100%	50%	0.000	
	0.0	0	100%	50%	0.000	
	0.0	0	100%	50%	0.000	
	0.0	0	100%	50%	0.000	
	0.0	0	100%	50%	0.000	
	0.0	0	100%	50%	0.000	

Power Analysis

The **Main** section of the PowerPlay Early Power Estimator spreadsheet summarizes the power and current estimates for the design. The **Main** section displays the total thermal power, thermal analysis, and power supply sizing information. The accuracy of the information depends on the information entered. The power consumed can also vary greatly depending on the toggle rates entered. The following sections provide a description of the results of the PowerPlay Early Power Estimator spreadsheet.

Figure 3–20 shows the Thermal Power, Thermal Analysis, and Power Supply Sizing areas in the **Main** section.

Figure 3–20. Power Areas in Main Section



Thermal Power

Thermal power is the power dissipated in the Cyclone II device. The total thermal power is shown in Watts and is a sum of the thermal power of all the resources being used in the device. The total thermal power includes the maximum power from standby and dynamic power.

The total thermal power only includes the thermal component for the **I/O** section and does not include the external power dissipation, such as from voltage referenced termination resistors.

Figure 3–21 shows the total thermal power in Watts. The thermal power for each section is also displayed. To see how the thermal power for a section was calculated, click on the section to view the inputs entered for that section.

Figure 3–21. Thermal Power in the PowerPlay Early Power Estimator Spreadsheet

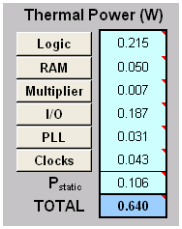


Table 3–9 describes the thermal power parameters in the PowerPlay Early Power Estimator spreadsheet.

Table 3–9. Thermal Power Section Information

Column Heading	Description
Logic	This shows the dynamic power consumed by LUTs and associated routing. Click **Logic** to see details.
RAM	This shows the dynamic power consumed by RAMs blocks and associated routing. Click **RAM** to see details.
Multiplier	This shows the dynamic power consumed by embedded multiplier blocks and associated routing. Click **Multiplier** to see details.
I/O	This shows the dynamic power consumed by I/O pins and associated routing. Also includes static power dissipated in terminated I/O standards on chip. Click **I/O** to see details.
PLL	This shows the dynamic power consumed by PLLs. Click **PLL** to see details.
Clocks	This shows the dynamic power consumed by clock networks. Click **Clocks** to see details.
P_{static}	This shows the static power consumed irrespective of clock frequency. Does not include static I/O current due to termination resistors, which is included in the I/O power above. P_{static} is affected by junction temperature, selected device, and power characteristics.
TOTAL	This shows the total power dissipated as heat from the FPGA. Does not include power dissipated in off-chip termination resistors. See Power Supply Current for current draw from the FPGA supply rails. This may differ due to currents supplied to off-chip components and thus not dissipated as heat in the FPGA.

Thermal Analysis

In the thermal analysis section, the device's ambient temperature, the airflow, the heat sink solution and the board thermal model are considered to determine the junction temperature (T_J) in degrees Celsius. T_J is the maximum recommended operating junction temperature based on your device and thermal conditions.

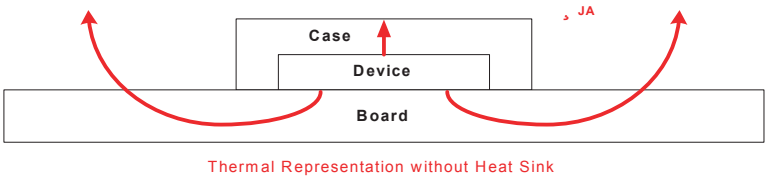
The device can be considered a heat source and the junction temperature is the temperature at the device. For simplicity, we can assume that the temperature of the device is constant regardless of where it is being measured. In reality, the temperature varies across the device.

Power can be dissipated from the device through many paths. Different paths become significant depending on the thermal properties of the system. In particular, the significance of power dissipation paths varies depending on whether or not a heat sink is being used for the device.

Not Using a Heat Sink

When a heat sink is not used the major paths of power dissipation are from the device to the air. This can be referred to as a junction-to-ambient thermal resistance (θ_{JA}). In this case there are two significant junction-to-ambient thermal resistance paths. The first is from the device through the case to the air and the second is from the device through the board to the air. Figure 3–22 shows the thermal representation without a heat sink.

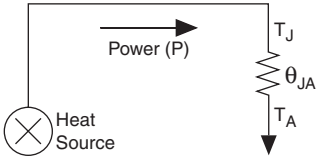
Figure 3–22. Thermal Representation without Heat Sink



Thermal Representation without Heat Sink

In the model used in the PowerPlay Early Power Estimator spreadsheet, power is dissipated through the case and board. Values of θ_{JA} have been calculated for differing air flow options accounting for the paths through the case and through the board. Figure 3–26 shows the thermal model for the PowerPlay Early Power Estimator spreadsheet without a heat sink.

Figure 3–23. Thermal Model in EPE without a Heat Sink



The ambient temperature does not change, but the junction temperature changes depending on the thermal properties. Since a change in junction temperature affects the thermal device properties used to calculate junction temperature, calculating junction temperature is an iterative process.

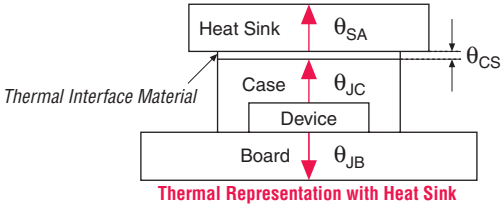
The total power is calculated based on the device properties which provide θ_{JA} and the ambient, board and junction temperatures using the following equation:

$$P = (T_J - T_A) / \theta_{JA}$$

Using a Heat Sink

When a heat sink is used the major paths of power dissipation are from the device through the case, thermal interface material, and heat sink. There is also a path of power dissipation through the board. The path through the board has much less impact than the path to air. Figure 3–24 shows the thermal representation with a heat sink.

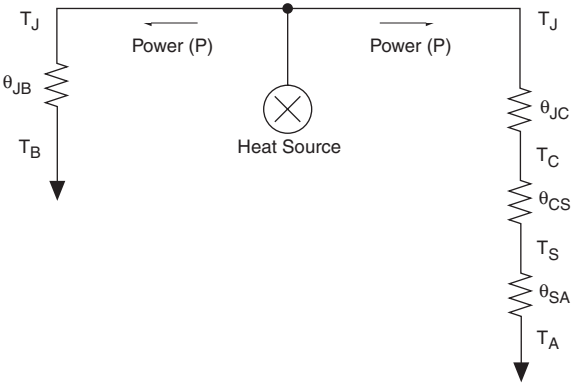
Figure 3–24. Thermal Representation with Heat Sink



In the model used in the early power estimator, power can be dissipated through the board or through the case and heat sink. The thermal resistance of the path through the board is referred to as the junction-to-board thermal resistance (θ_{JB}). The thermal resistance of the path through

the case, thermal interface material and heat sink is referred to as the junction-to-ambient thermal resistance (θ_{JA}). Figure 3–25 shows the thermal model for the PowerPlay Early Power Estimator spreadsheet.

Figure 3–25. Thermal Model for EPE with a Heat Sink



If you want the PowerPlay Early Power Estimator spreadsheet thermal model to take the junction-to-board thermal resistance (θ_{JB}) into consideration, set the Board Thermal Model to either "Typical" or "Custom." A Typical board thermal model sets θ_{JB} to a value based on the package and device selected. If you choose a Custom board thermal model, you must specify a value for θ_{JB}. If you do not want the PowerPlay Early Power Estimator spreadsheet thermal model to take the θ_{JB} resistance into consideration, set the Board Thermal Model to "None (conservative)." In this case, the path through the board is not considered and for power dissipation and a more conservative thermal power estimate is obtained.

The junction-to-ambient thermal resistance (θ_{JA}) is determined by the addition of the junction-to-case thermal resistance (θ_{JC}), the case-to-heat sink thermal resistance (θ_{CS}) and the heat sink-to ambient thermal resistance (θ_{SA}).

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

Based on the device, package, airflow, and the heat sink solution selected in the main input parameters, the PowerPlay Early Power Estimator spreadsheet determines the junction-to-ambient thermal resistance (θ_{JA}).

If you are using a low, medium, or high profile heat sink, select the airflow from the options of still air and air flow rates of 100 lfm (0.05 m/s), 200 lfm (1.0 m/s), and 400 lfm (2.0 m/s). If you are using a custom heat sink, enter the heat sink-to-ambient thermal resistance (θ_{SA}). The airflow should also be incorporated into θ_{SA}. Therefore, the Airflow parameter is not applicable in this case. Obtain these values from the heat sink manufacturer.

The ambient temperature does not change, but the junction temperature changes depending on the thermal properties. Since a change in junction temperature affects the thermal device properties used to calculate junction temperature, calculating junction temperature is an iterative process.

The total power is calculated based on the device properties which provide θ_{JA}, θ_{JB}, and the ambient, board and junction temperature using the following equation:

$$P = \frac{(T_J - T_A)}{\theta_{JA}} + \frac{(T_J - T_B)}{\theta_{JB}}$$

Figure 3–26 shows the thermal analysis, including the junction temperature (T_J), total θ_{JA}, θ_{JB}, and the maximum allowed T_A values. For details on the values of the thermal parameters not listed, click **Details**.

Figure 3–26. Thermal Analysis in the PowerPlay Early Power Estimator Spreadsheet

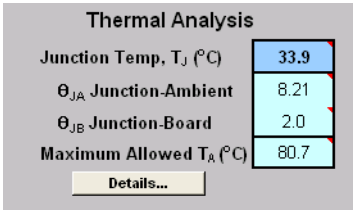


Table 3–10 describes the thermal analysis parameters in the PowerPlay Early Power Estimator spreadsheet.

Table 3–10. Thermal Analysis Section Information

Column Heading	Description
Junction Temp, T_J (°C)	This shows the device junction temperature estimated based on supplied thermal parameters. The junction temperature is determined by dissipating the total thermal power through the top of the chip and through the board (if selected). See **Details** for detailed calculations used.
θ_{JA} Junction-Ambient	This shows the junction-to-ambient thermal resistance between the device and ambient air, in °C/W. This represents the increase in temperature between ambient and junction for every Watt of additional power dissipation.
θ_{JB} Junction-Board	This shows the junction-to-board thermal resistance, in °C/W. This is used in conjunction with the board temperature, as well as the top-of-chip θ_{JA} and ambient temperatures, to compute junction temperature.
Maximum Allowed T_A (°C)	This shows a guideline for the maximum ambient temperature (in °C) that the device can be subjected to without violating maximum junction temperature, based on the supplied cooling solution and device temperature grade.

Power Supply Sizing (A)

The Power Supply Sizing section provides the estimated current drawn from power supplies. The I_{CCINT} current is the supply current drawn from V_{CCINT}. The total I_{CCIO} current is the supply current drawn from V_{CCIO} power supplies. For estimates of I_{CCIO} based on I/O banks, refer to the **I/O** section of the PowerPlay Early Power Estimator spreadsheet.

Figure 3–27 shows the power supply sizing estimation. I_{CCINT} and total I_{CCIO} are displayed.

Figure 3–27. Power Supply Sizing in the PowerPlay Early Power Estimator Spreadsheet

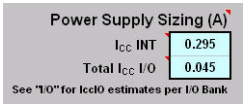


Table 3–11 describes the parameters in the Power Supply Current parameters of the PowerPlay Early Power Estimator spreadsheet.

Table 3–11. Power Supply Current Information

Column Heading	Description
I_{CC}INT	This shows the total current drawn from the I_{CCINT} supply (in A).
I_{CC}IO	This shows the total current drawn from the I_{CCIO} power rail(s). See the **I/O** sheet for details on the current drawn from each I/O rail. I_{CCIO} includes any current drawn through the I/O into off-chip termination resistors. This can result in I_{CCIO} values that are higher than the reported I/O thermal power, since this off-chip current is dissipated as heat elsewhere and does not factor into the calculation of device temperature.