Migration Between Stratix V GX and Stratix V GT Devices

AN-644-1.0 Application Note

This application note provides guidelines for designing cross-family migration (also known as vertical migration) between Altera® Stratix® V GX and Stratix V GT devices. With advance planning that takes into account the different power supply voltages and available packages in both families, you can design a PCB that can be assembled with either a Stratix V GX or a Stratix V GT device in the same package.

Follow these guidelines to use either device in your PCB design. Altera recommends using these guidelines throughout your PCB design process to ensure a seamless migration of designs between Stratix V GX and GT devices. Cross-family migration between Stratix V GX and GT FPGAs allows you to design with Stratix V GT FPGAs and test the system with Stratix V GX FPGAs.

Supported Migration Device Packages

Table 1 lists the devices that can migrate between the Stratix V GX and GT device packages. The four devices listed in Table 1 allow cross-family migration. The major difference between Stratix V GX and Stratix V GT devices is the transceivers. 5SGXA5 and 5SGXA7 devices offer 48 integrated 14.1-Gbps GX transceivers. 5SGTC5 and 5SGTC7 devices replace four GX transceivers in the Stratix V GX device with 28-Gbps GT transceivers. To support ultra-high bandwidth, Stratix V GT devices also replace the package pins of 12 transceivers in a Stratix V GX device with power pins.

You can use both Stratix V GT and GX devices in PCB designs based on a Stratix V GT device pin-out. However, PCB designs based on a Stratix V GX device pin-out only use GX devices.

Table 1. Cross-Family Migration for Stratix V GX and Stratix V GT Devices

Device	Package *(1)*	F1517 40 x 40 (mm) 1.0-mm pitch		
		User I/Os *(2)*	LVDS Count	28-Gbps Channels / 14.1-Gbps Channels
5SGXA5	NF40	600	150	0/48
5SGXA7	NF40	600	150	0/48
5SGTC5	KF40	600	150	4/32
5SGTC7	KF40	600	150	4/32

Notes to Table 1:

(1) For each package, N indicates 48 transceiver channels, K indicates 36 transceiver channels, F stands for FineLine BGA package type, and 40 indicates the 1517 pins and the 40 × 40 mm package dimension.

(2) The user I/O count includes all general purpose I/Os, dedicated clock pins, and dual-purpose configuration pins. Dedicated configuration pins are not included in the user I/O count.

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Differences Between Stratix V GX and Stratix V GT Devices

A Stratix V GT device replaces four GX transceiver channels on the right side of a Stratix V GX device with GT transceiver channels. Table 2 lists the migrated pin locations. To use a GT transceiver channel, the PCB trace design of these pins must meet 28-Gbps requirements.

Table 2. Migrated Pin Locations and Functions of Stratix V GX and GT Device Transceiver Pins

Pin Location	Stratix V GX Device Pin Name GX Transceivers	Stratix V GT Device Pin Name GT Transceivers
AM1	GXB_RX_R3n, GXB_REFCLK_R3n	GTB_RX_R0n
AM2	GXB_RX_R3p, GXB_REFCLK_R3p	GTB_RX_R0p
AB1	GXB_RX_R9n, GXB_REFCLK_R9n	GTB_RX_R1n
AB2	GXB_RX_R9p, GXB_REFCLK_R9p	GTB_RX_R1p
P1	GXB_RX_R15n, GXB_REFCLK_R15n	GTB_RX_R2n
P2	GXB_RX_R15p, GXB_REFCLK_R15p	GTB_RX_R2p
F1	GXB_RX_R21n, GXB_REFCLK_R21n	GTB_RX_R3n
F2	GXB_RX_R21p, GXB_REFCLK_R21p	GTB_RX_R3p
AP1	GXB_TX_R3n	GTB_TX_R0n
AP2	GXB_TX_R3p	GTB_TX_R0p
AD1	GXB_TX_R9n	GTB_TX_R1n
AD2	GXB_TX_R9p	GTB_TX_R1p
T1	GXB_TX_R15n	GTB_TX_R2n
T2	GXB_TX_R15p	GTB_TX_R2p
H1	GXB_TX_R21n	GTB_TX_R3n
H2	GXB_TX_R21p	GTB_TX_R3p

A Stratix V GT device also replaces the receiver pins of eight Stratix V GX transceivers with GT transceiver power pins in order to provide a clean power supply to the GT transceivers. Table 3 lists the migrated pin locations. During the PCB design, these pins must be bonded to power planes.

If a Stratix V GX device is used in the GX and GT device-compatible PCB, connect the pins in Table 3 to the dedicated 1.0 V GT power supplies; do not leave them floating.

Stratix V GT transceivers have their own power supplies: VCCR_GTBR, VCCT_GTBR, VCCL_GTBR, and VCCA_GTBR. To design a PCB for both GX and GT devices, you must consider the power supply requirements. You have many options for designing the power supplies of the migration PCBs. The following power supply design guidelines give an example of PCB design that includes all the data rate options:

- VCCR_GTBR, VCCL_GTBR, and VCCT_GTBR are 1.0 V power supplies. They may share the same power regulator. However, they must be isolated from each other by at least 60 dB.
- Keep VCCR_GXB on its own regulator that is adjustable from 0.85 V to 1.0 V.
- Keep VCCT_GXB on its own regulator that is adjustable from 0.85 V to 1.0 V.

- Keep VCCA_GXBL on one power regulator and VCCA_GXBR and VCCA_GTBR on a different power regulator. Use regulators that can be adjusted between 2.5 V and 3.0 V.

For updated power supply designs, refer to the *Stratix V GT Device Family Pin Connection Guidelines*.

Table 3. Migrated Pin Locations and Functions of Stratix V GX Device Receiver Pins and GT Device Power Pins

Pin Location	Stratix V GX Device Pin Name GX Receiver Channels	Stratix V GT Device Pin Name GT Transceivers
AL3	GXB_RX_R2n, GXB_REFCLK_R2n	VCCL_GTBR0
AL4	GXB_RX_R2p, GXB_REFCLK_R2p	VCCL_GTBR0
AE3	GXB_RX_R8n, GXB_REFCLK_R8n	VCCL_GTBR1
AE4	GXB_RX_R8p, GXB_REFCLK_R8p	VCCL_GTBR1
U3	GXB_RX_R14n, GXB_REFCLK_R14n	VCCL_GTBR2
U4	GXB_RX_R14p, GXB_REFCLK_R14p	VCCL_GTBR2
G3	GXB_RX_R20n, GXB_REFCLK_R20n	VCCL_GTBR3
G4	GXB_RX_R20p, GXB_REFCLK_R20p	VCCL_GTBR3
AK1	GXB_RX_R4n, GXB_REFCLK_R4n	VCCR_GXBR0
AK2	GXB_RX_R4p, GXB_REFCLK_R4p	VCCR_GXBR0
AC3	GXB_RX_R10n, GXB_REFCLK_R10n	VCCR_GXBR1
AC4	GXB_RX_R10p, GXB_REFCLK_R10p	VCCR_GXBR1
R3	GXB_RX_R16n, GXB_REFCLK_R16n	VCCR_GXBR2
R4	GXB_RX_R16p, GXB_REFCLK_R16p	VCCR_GXBR2
D1	GXB_RX_R22n, GXB_REFCLK_R22n	VCCR_GXBR3
D2	GXB_RX_R22p, GXB_REFCLK_R22p	VCCR_GXBR3
AT1	GXB_RX_R1n, GXB_REFCLK_R1n	VCCT_GXBR0
AT2	GXB_RX_R1p, GXB_REFCLK_R1p	VCCT_GXBR0
AF1	GXB_RX_R7n, GXB_REFCLK_R7n	VCCT_GXBR1
AF2	GXB_RX_R7p, GXB_REFCLK_R7p	VCCT_GXBR1
V1	GXB_RX_R13n, GXB_REFCLK_R13n	VCCT_GXBR2
V2	GXB_RX_R13p, GXB_REFCLK_R13p	VCCT_GXBR2
K1	GXB_RX_R19n, GXB_REFCLK_R19n	VCCT_GXBR3
K2	GXB_RX_R19p, GXB_REFCLK_R19p	VCCT_GXBR3

The transmitter pins of the eight Stratix V GX transceiver channels are not connected in Stratix V GT devices. Table 4 lists these pin locations. Leave these pins floating; do not use in your PCB design.

Table 4. Migrated Pin Locations and Functions of Stratix V GX Device Receiver Pins and GT Device Floating Pins

Pin Location	Stratix V GX Device Pin Name GX Receiver Channels	Stratix V GT Device Pin Name
AR3	GXB_TX_R1n	Not Connected (NC)
AR4	GXB_TX_R1p	NC
AN3	GXB_TX_R2n	NC
AN4	GXB_TX_R2p	NC
AK5	GXB_TX_R4n	NC
AK6	GXB_TX_R4p	NC
AF5	GXB_TX_R7n	NC
AF6	GXB_TX_R7p	NC
AD5	GXB_TX_R8n	NC
AD6	GXB_TX_R8p	NC
AB5	GXB_TX_R10n	NC
AB6	GXB_TX_R10p	NC
V5	GXB_TX_R13n	NC
V6	GXB_TX_R13p	NC
T5	GXB_TX_R14n	NC
T6	GXB_TX_R14p	NC
P5	GXB_TX_R16n	NC
P6	GXB_TX_R16p	NC
K5	GXB_TX_R19n	NC
K6	GXB_TX_R19p	NC
J3	GXB_TX_R20n	NC
J4	GXB_TX_R20p	NC
E3	GXB_TX_R22n	NC
E4	GXB_TX_R22p	NC

Table 5 lists the pin map of the package migration between a Stratix V GX device and a Stratix V GT device. The migrated pins in Table 2 on page 2 are highlighted in pink. The migrated pins in Table 3 on page 3 are highlighted in gray. The migrated pins in Table 4 on page 4 are highlighted in light blue.

Table 5. Pin Map of Stratix V GX and Stratix V GT Migration (Part 1 of 2)

Stratix V GX Pin Map

	1	2	3	4	5	6
A	—	GND	GND	—	GND	—
B	GXB_RX_R23n	GXB_RX_R23p	GND	GND	GND	GND
C	GND	GND	GXB_TX_R23n	GXB_TX_R23p	GND	—
D	GXB_RX_R22n	GXB_RX_R22p	GND	GND	GND	—
E	GND	GND	GXB_TX_R22n	GXB_TX_R22p	GND	—
F	GXB_RX_R21n	GXB_RX_R21p	GND	GND	GND	—
G	GND	GND	GXB_RX_R20n	GXB_RX_R20p	GND	—
H	GXB_TX_R21n	GXB_TX_R21p	GND	GND	GND	—
J	GND	GND	GXB_TX_R20n	GXB_TX_R20p	GND	GND
K	GXB_RX_R19n	GXB_RX_R19p	GND	GND	GXB_TX_R19n	GXB_TX_R19p
L	GND	GND	GXB_RX_R18n	GXB_RX_R18p	GND	GND
M	GXB_RX_R17n	GXB_RX_R17p	GND	GND	GXB_TX_R18n	GXB_TX_R18p
N	GND	GND	GXB_TX_R17n	GXB_TX_R17p	GND	GND
P	GXB_RX_R15n	GXB_RX_R15p	GND	GND	GXB_TX_R16n	GXB_TX_R16p
R	GND	GND	GXB_RX_R16n	GXB_RX_R16p	GND	GND
T	GXB_TX_R15n	GXB_TX_R15p	GND	GND	GXB_TX_R14n	GXB_TX_R14p
U	GND	GND	GXB_RX_R14n	GXB_RX_R14p	GND	GND
V	GXB_RX_R13n	GXB_RX_R13p	GND	GND	GXB_TX_R13n	GXB_TX_R13p
W	GND	GND	GXB_TX_R12n	GXB_TX_R12p	GND	GND
Y	GXB_RX_R12n	GXB_RX_R12p	GND	GND	GXB_TX_R11n	GXB_TX_R11p
AA	GND	GND	GXB_RX_R11n	GXB_RX_R11p	GND	GND
AB	GXB_RX_R9n	GXB_RX_R9p	GND	GND	GXB_TX_R10n	GXB_TX_R10p
AC	GND	GND	GXB_RX_R10n	GXB_RX_R10p	GND	GND
AD	GXB_TX_R9n	GXB_TX_R9p	GND	GND	GXB_TX_R8n	GXB_TX_R8p
AE	GND	GND	GXB_RX_R8n	GXB_RX_R8p	GND	GND
AF	GXB_RX_R7n	GXB_RX_R7p	GND	GND	GXB_TX_R7n	GXB_TX_R7p
AG	GND	GND	GXB_TX_R6n	GXB_TX_R6p	GND	GND
AH	GXB_RX_R6n	GXB_RX_R6p	GND	GND	GXB_TX_R5n	GXB_TX_R5p
AJ	GND	GND	GXB_RX_R5n	GXB_RX_R5p	GND	GND
AK	GXB_RX_R4n	GXB_RX_R4p	GND	GND	GXB_TX_R4n	GXB_TX_R4p
AL	GND	GND	GXB_RX_R2n	GXB_RX_R2p	GND	GND
AM	GXB_RX_R3n	GXB_RX_R3p	GND	GND	GND	GND

Stratix V GT Pin Map

	1	2	3	4	5	6
A	—	GND	GND	—	GND	—
B	GXB_RX_R23n	GXB_RX_R23p	GND	GND	GND	GND
C	GND	GND	GXB_TX_R23n	GXB_TX_R23p	GND	—
D	GXB_VCCR	GXB_VCCR	GND	GND	GND	—
E	GND	GND	NC	NC	GND	—
F	GTB_RX_R3n	GTB_RX_R3p	GND	GND	GND	—
G	GND	GND	GTB_VCCL	GTB_VCCL	GND	—
H	GTB_TX_R3n	GTB_TX_R3p	GND	GND	GND	—
J	GND	GND	NC	NC	GND	GND
K	GXB_VCCT	GXB_VCCT	GND	GND	NC	NC
L	GND	GND	GXB_RX_R18n	GXB_RX_R18p	GND	GND
M	GXB_RX_R17n	GXB_RX_R17p	GND	GND	GXB_TX_R18n	GXB_TX_R18p
N	GND	GND	GXB_TX_R17n	GXB_TX_R17p	GND	GND
P	GTB_RX_R2n	GTB_RX_R2p	GND	GND	NC	NC
R	GND	GND	GXB_VCCR	GXB_VCCR	GND	GND
T	GTB_TX_R2n	GTB_TX_R2p	GND	GND	NC	NC
U	GND	GND	GTB_VCCL	GTB_VCCL	GND	GND
V	GXB_VCCT	GXB_VCCT	GND	GND	NC	NC
W	GND	GND	GXB_TX_R12n	GXB_TX_R12p	GND	GND
Y	GXB_RX_R12n	GXB_RX_R12p	GND	GND	GXB_TX_R11n	GXB_TX_R11p
AA	GND	GND	GXB_RX_R11n	GXB_RX_R11p	GND	GND
AB	GTB_RX_R1n	GTB_RX_R1p	GND	GND	NC	NC
AC	GND	GND	GXB_VCCR	GXB_VCCR	GND	GND
AD	GTB_TX_R1n	GTB_TX_R1p	GND	GND	NC	NC
AE	GND	GND	GTB_VCCL	GTB_VCCL	GND	GND
AF	GXB_VCCT	GXB_VCCT	GND	GND	NC	NC
AG	GND	GND	GXB_TX_R6n	GXB_TX_R6p	GND	GND
AH	GXB_RX_R6n	GXB_RX_R6p	GND	GND	GXB_TX_R5n	GXB_TX_R5p
AJ	GND	GND	GXB_RX_R5n	GXB_RX_R5p	GND	GND
AK	GXB_VCCR	GXB_VCCR	GND	GND	NC	NC
AL	GND	GND	GTB_VCCL	GTB_VCCL	GND	GND
AM	GTB_RX_R0n	GTB_RX_R0p	GND	GND	GND	GND

Table 5. Pin Map of Stratix V GX and Stratix V GT Migration (Part 2 of 2)

Stratix V GX Pin Map

	1	2	3	4	5	6
AN	GND	GND	GXB_TX_R2n	GXB_TX_R2p	GND	—
AP	GXB_TX_R3n	GXB_TX_R3p	GND	GND	GND	—
AR	GND	GND	GXB_TX_R1n	GXB_TX_R1p	GND	—
AT	GXB_RX_R1n	GXB_RX_R1p	GND	GND	GND	—
AU	GND	GND	GXB_TX_R0n	GXB_TX_R0p	GND	—
AV	GXB_RX_R0n	GXB_RX_R0p	GND	GND	GND	GND
AW	—	GND	GND	—	—	—

Stratix V GT Pin Map

	1	2	3	4	5	6
AN	GND	GND	NC	NC	GND	—
AP	GTB_TX_R0n	GTB_TX_R0p	GND	GND	GND	—
AR	GND	GND	NC	NC	GND	—
AT	GXB_VCCT	GXB_VCCT	GND	GND	GND	—
AU	GND	GND	GXB_TX_R0n	GXB_TX_R0p	GND	—
AV	GXB_RX_R0n	GXB_RX_R0p	GND	GND	GND	GND
AW	—	GND	GND	—	—	—

Document Revision History

Table 6 lists the revision history for this application note.

Table 6. Document Revision History

Date	Version	Changes
May 2011	1.0	Initial release.