8. Configuring Mixed Altera FPGA Chains

CF52008-2.3

Introduction

A mixture of Stratix® series, Cyclone® series, APEX™ II, Mercury™, APEX 20K, ACEX® 1K and FLEX® 10K devices can be configured in the same configuration chain, provided that all devices in the chain support the selected configuration method, such as passive serial (PS). This chapter discusses guidelines you should follow when combining different device families in the same configuration chain.

General Guidelines

If any devices in your configuration chain require 10-kΩ pull-up resistors, external 10-kΩ pull-up resistors should be used to support all devices in the chain. The pull-up resistors should be tied to a supply that provides an acceptable input voltage high level for all devices in the chain.

The DCLK, DATA0, nCONFIG, nSTATUS, and CONF_DONE signals should be tied together for every device in the configuration chain. For concurrent configuration using enhanced configuration devices, each device or chain of devices is fed a separate DCLK line, while DCLK, nCONFIG, nSTATUS, and CONF_DONE are shared. This ensures that configuration begins and ends at the same time for each device. Additionally, if one device detects an error and pulls nSTATUS low, all devices in the chain will reset and restart configuration.

For more information about connecting the configuration control signals together, refer to "*Board Layout Tips & Debugging Techniques*" on page IV–1 in the *Configuration Handbook*.

Any FPGA or configuration device that supports JTAG programming can be placed in the same JTAG chain. For multi-device JTAG chains, external 1-kΩ resistors should be used on the TCK, TDI, and TMS pins. The pull-up resistors on TDI and TMS should be pulled up to a supply that provides an acceptable input voltage high level for all devices in the chain.

To interface the TDI and TDO signals of the JTAG pins of Altera devices that have different V_{CCIO} levels, you may need to insert level shifters. You will need to insert level shifters if the TDI pin is not tolerant to the voltage driven out by the previous device's TDO pin. For example, if the TDO of the first device in the JTAG chain is in a back where the V_{CCIO} is set to 5.0-V and the TDI of the second device is in a bank where the V_{CCIO} is set to 1.8-V and cannot accept 5.0-V inputs, you need to insert a level shifter in-between the devices' TDO-TDI interface.

Additionally, you will need to insert level shifters if the TDI pin will not recognize the voltage driven out by the previous device's TDO pin as an input voltage high level (V_{IH}). For example, if the TDO of the first device in the JTAG chain is in a back where the V_{CCIO} is set to 1.8-V and the TDI of the second device is in a bank where the V_{CCIO} is set to 5.0-V and does not recognize 1.8-V as a logic high level, you need to insert a level shifter in-between the devices' TDO-TDI interface.

Guidelines for Configuration Chains with APEX 20KE Devices

If your configuration chain contains an APEX 20KE device(s), you must follow the APEX 20KE power sequencing requirement as outlined in the *Configuring APEX 20KE and APEX 20KC Devices* Chapter of the Configuration Handbook. The guidelines below should be followed for successful configuration of your configuration chain with APEX 20KE Devices:

- For all configuration schemes, use 10-kΩ pull-up resistors on nCONFIG, nSTATUS, and CONF_DONE.
- For all configuration schemes, ensure nCONFIG is held low upon power-up until both the V_{CCINT} and V_{CCIO} power supplies are stable.
- If you are using a configuration device, nCONFIG must be pulled-up to V_{CCINT} of the APEX 20KE device.
- If you are using the nINIT_CONF pin of the enhanced configuration device or EPC2 device, you need to isolate the 1.8-V V_{CCINT} from the configuration device's 3.3-V supply by adding a diode between the nCONFIG pin and the nINIT_CONF pin.

Document Revision History

Table 8–1 shows the revision history for this document.

Table 8–1. Document Revision History

Date and Revision	Changes Made	Summary of Changes
October 2008, version 2.3	■ Updated new document format.	—
April 2007, version 2.2	■ Added "Document Revision History".	—
August 2005 version 2.1	■ Removed active cross references refering to document outside Chapter 8.	—
July 2004, version 2.0	■ Added Stratix II and Cyclone II device information throughout chapter.	—
September 2003, version 1.0	■ Initial Release.	—