8. Implementing 10-Gigabit Ethernet Using Stratix & Stratix GX Devices

S52010-2.0

Introduction

Ethernet has evolved to meet ever-increasing bandwidth demands and is the most prevalent local-area network (LAN) communications protocol. 10-Gigabit Ethernet extends that protocol to higher bandwidth for future high-speed applications. The accelerated growth of network traffic and the resulting increase in bandwidth requirements is driving service providers and enterprise network architects towards high-speed network solutions. Potential applications for 10-Gigabit Ethernet include private campus or LAN backbones, high-speed access links between service providers and enterprises, and aggregation and transport in metropolitan area networks (MANs).

The I/O features of Stratix® and Stratix GX devices enable support for 10-Gigabit Ethernet, supporting 10-Gigabit 16-bit interface (XSBI) and 10-Gigabit medium independent interface (XGMII). Stratix GX devices can additionally support the 10-gigabit attachment unit interface (XAUI) using the embedded 3.125-Gbps transceivers. You can find more information on XAUI support in Section II, *Stratix GX Transceiver User Guide*, of the *Stratix GX Device Handbook, Volume 1*.

This chapter discusses the following topics:

- Fundamentals of 10-Gigabit Ethernet
- Description and implementation of XSBI
- Description and implementation of XGMII
- Description of XAUI
- I/O characteristics of XSBI, XGMII, and XAUI

Related Links

- 10-Gigabit Ethernet Alliance at **www.10gea.org**
- The *Stratix Device Family Data Sheet* section of the *Stratix Device Handbook, Volume 1* and the *Stratix GX Device Family Data Sheet* section of the *Stratix GX Device Handbook, Volume 1*
- The *High-Speed Differential I/O Interfaces in Stratix Devices* chapter

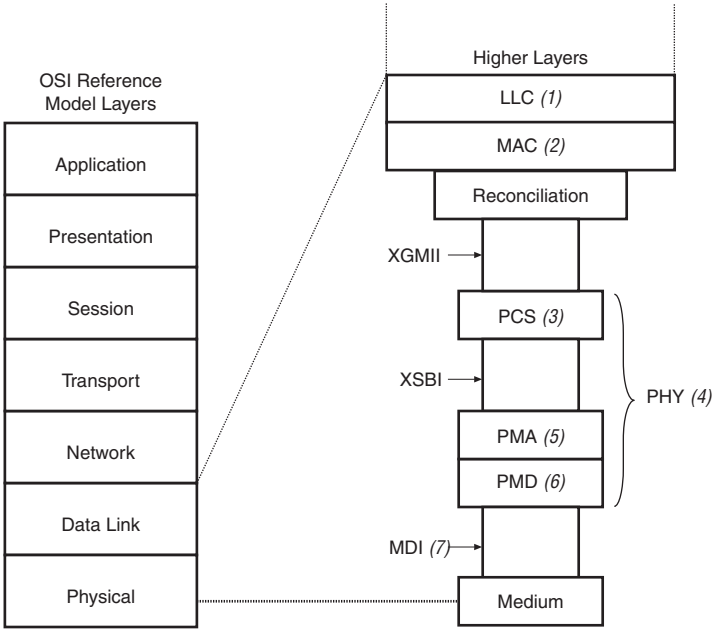
10-Gigabit Ethernet

Ethernet speed has increased to keep pace with demand, initially to 10 megabits per second (Mbps), later to 100 Mbps, and recently to 1 gigabit per second (Gbps). Ethernet is the dominant network technology in LANs, and with the advent of 10-Gigabit Ethernet, it is entering the MAN and wide area network (WAN) markets.

The purpose of the 10-Gigabit Ethernet proposed standard is to extend the operating speed to 10 Gbps defined by protocol IEEE 802.3 and include WAN applications. These additions provide a significant increase in bandwidth while maintaining maximum compatibility with current IEEE 802.3 interfaces.

Since its inception in March 1999, the 10-Gigabit Ethernet Task Force has been working on the IEEE 802.3ae Standard. Some of the information in the following sections is derived from Clauses 46, 47, 49, and 51 of the IEEE Draft P802.3ae/D3.1 document. A fully ratified standard is expected in the first half of 2002. Figure 8–1 shows the relationship of 10-Gigabit Ethernet to the Open Systems Interconnection (OSI) protocol stack.

Figure 8–1. 10-Gigabit Ethernet Protocol in Relation to OSI Protocol Stack

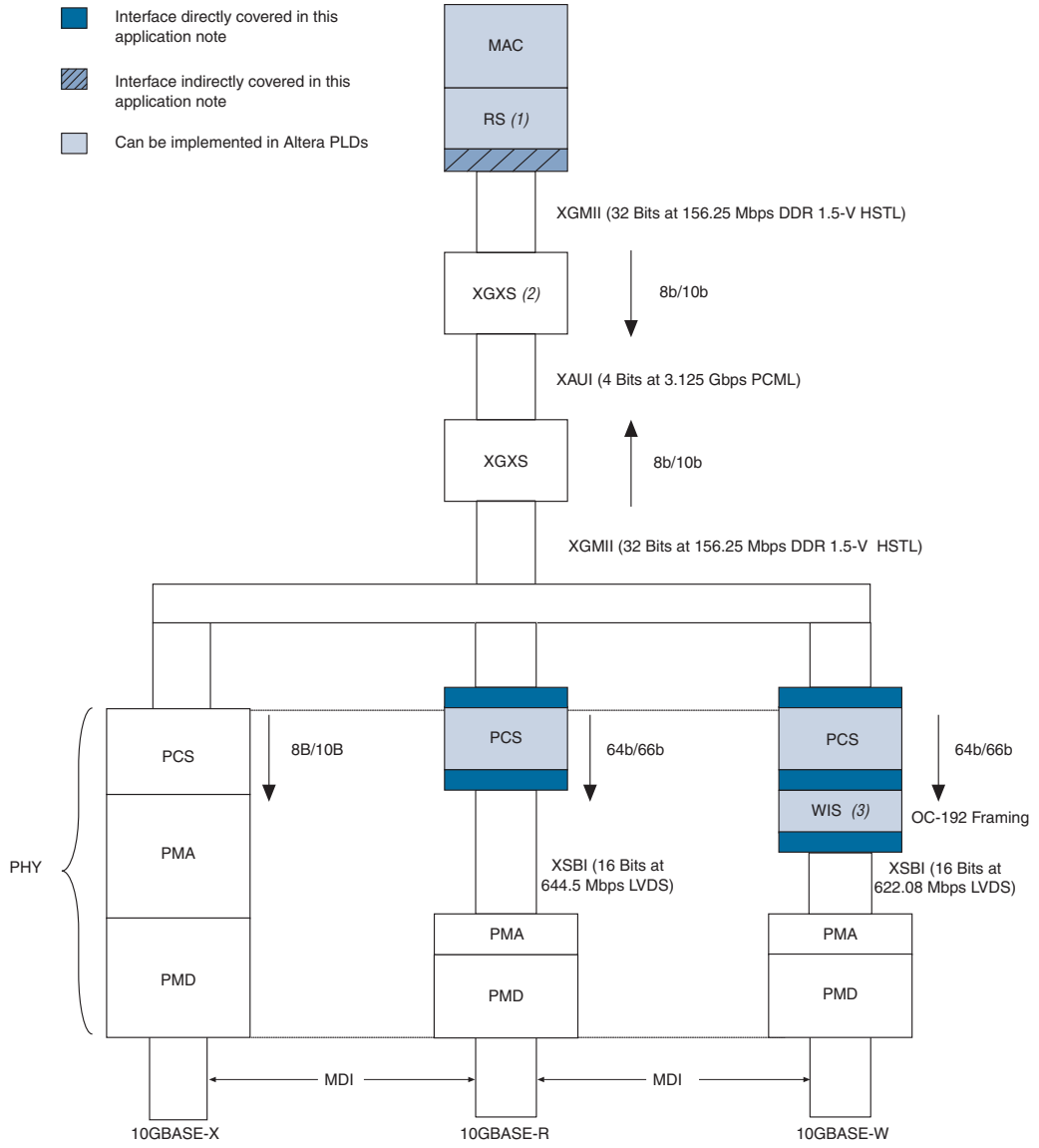


Notes to Figure 8–1:
(1) LLC: logical link controller
(2) MAC: media access controller
(3) PCS: physical coding sublayer
(4) PHY: physical layer
(5) PMA: physical medium attachment
(6) PMD: physical medium dependent
(7) MDI: medium dependent interface

The Ethernet PHY (layer 1 of the OSI model) connects the media (optical or copper) to the MAC (layer 2). The Ethernet architecture further divides the PHY (layer 1) into a PMD sublayer, a PMA sublayer, and a PCS. For example, optical transceivers are PMD sublayers. The PMA converts the data between the PMD sublayer and the PCS sublayer. The PCS is made up of coding (e.g., 8b/10b, 64b/66b) and serializer or multiplexing functions. Figure 8–2 shows the components of 10-Gigabit Ethernet and how Altera implements certain blocks and interfaces.

10-Gigabit Ethernet has three different implementations for the PHY: 10GBASE-X, 10GBASE-R, and 10GBASE-W. The 10GBASE-X implementation is a PHY that supports the XAUI interface. The XAUI interface used in conjunction with the XGMII extender sublayer (XGXS) allows more separation in distance between the MAC and PHY. 10GBASE-X PCS uses four lanes of 8b/10b coded data at a rate of 3.125 Gbps. 10GBASE-X is a wide wave division multiplexing (WWDM) LAN PHY. 10GBASE-R and 10GBASE-W are serial LAN PHYs and serial WAN PHYs, respectively. Unlike 10GBASE-X, 10GBASE-R and 10GBASE-W implementations have a XSBI interface and are described in more detail in the following section.

Figure 8–2. 10-Gigabit Ethernet Block Diagram



Notes to Figure 8–2:

(1) The reconciliation sublayer (RS) interfaces the serial MAC data stream and the parallel data of XGMII.

(2) The XGMII extender sublayer (XGXS) extends the distance of XGMII when used with XUAI and provides the data conversion between XGMII and XAUI.

(3) The WAN interface sublayer (WIS) implements the OC-192 framing and scrambling functions.

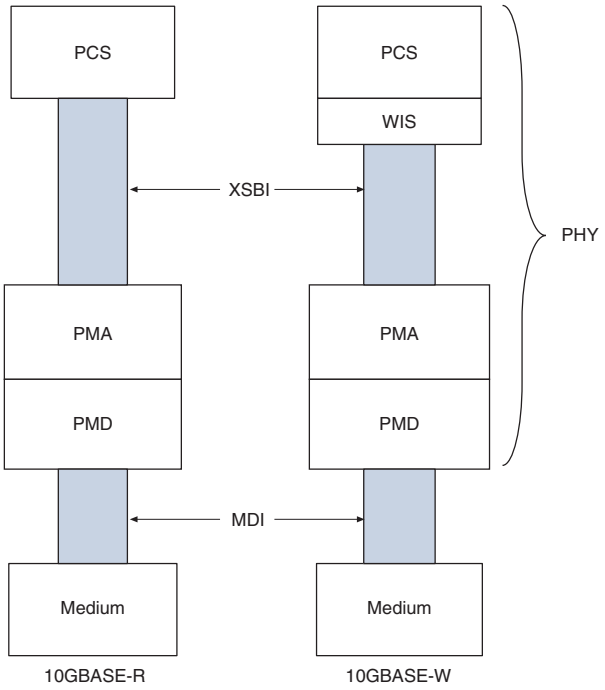
Interfaces

The following sections discuss XSBI, PCS, XGMII, and XAUI.

XSBI

One of the blocks of 10-Gigabit Ethernet is the XSBI interface. XSBI is the interface between the PCS and the PMA sublayers of the PHY layer of the OSI model. XSBI supports two types of PHY layers, LAN PHY and WAN PHY. The LAN PHY is part of 10GBASE-R, and supports existing Gigabit Ethernet applications at ten times the bandwidth. The WAN PHY is part of 10GBASE-W, and supports connections to existing and future installations of SONET/SDH circuit-switched access equipment. 10GBASE-R is a physical layer implementation that is comprised of the PCS sublayer, the PMA, and the PMD. 10GBASE-R is based upon 64b/66b data coding. 10GBASE-W is a PHY layer implementation that is comprised of the PCS sublayer, the WAN interface sublayer (WIS), the PMA, and the PMD. 10GBASE-W is based on STS-192c/SDH VC-4-64c encapsulation of 64b/66b encoded data. Figure 8–3 shows the construction of these two PHY layers.

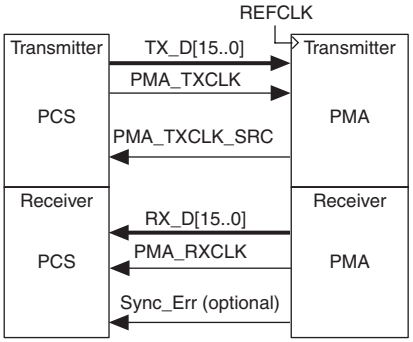
Figure 8–3. XSBI Interface for the Two PHY Layers



Functional Description

XSBI uses 16-bit LVDS data to interface between the PCS and the PMA sublayer. Figure 8–4 shows XSBI between these two sublayers.

Figure 8–4. XSBI Functional Block Diagram



On the transmitter side, the transmit data (TX_D[15..0]) is output by the PCS and input at the PMA using the transmitter clock (PMA_TXCLK), which is derived from the PMA source clock (PMA_TXCLK_SRC). The PMA source clock is generated from the PMA with its reference clock (REFCLK). On the receiver side, the receiver data (RX_D[15..0]) is output by the PMA and input at the PCS using the PMA-generated receiver clock (PMA_RXCLK). The SYNC_ERR optional signal is sent to the PCS by the PMA if the PMA fails to recover the clock from the serial data stream.

The ratios for these two clocks and data are dependent on the type of PHY used. Table 8–1 shows the rates for both PHY types.

Table 8–1. XSBI Clock & Data Rates for WAN & LAN PHY

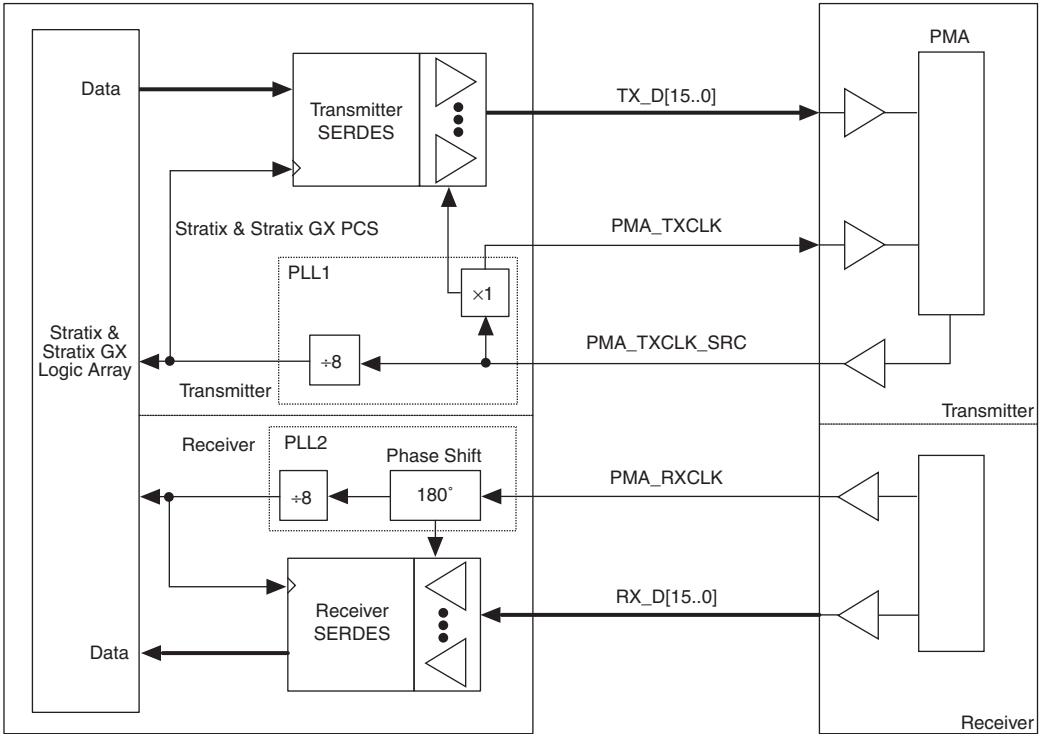
Parameter	WAN PHY	LAN PHY	Unit
TX_D[15..0]	622.08	644.53125	Mbps
PMA_TXCLK	622.08	644.53125	MHz
PMA_TXCLK_SRC	622.08	644.53125	MHz
RX_D[15..0]	622.08	644.53125	Mbps
PMA_RXCLK	622.08	644.53125	MHz

Implementation

The 16-bit full duplex LVDS implementation of XSBI in Stratix devices is shown in Figure 8–5.

The source-synchronous I/O implemented in Stratix GX devices optionally includes dynamic phase alignment (DPA). DPA automatically and continuously tracks fluctuations caused by system variations and self-adjusts to eliminate the phase skew between the multiplied clock and the serial data, allowing for data rates of 1 Gbps. In non DPA mode the I/O behaves similarly to that of the Stratix I/O. This document assumes that DPA is disabled. However, it is simple to implement the same system with DPA enabled to take advantage of its features. For more information on DPA, see the *Stratix GX Transceivers* chapter in the *Stratix GX Device Handbook, Volume 1*.

Figure 8–5. Stratix & Stratix GX Device XSBI Implementation



The transmit serializer/deserializer (SERDES) clock comes from the transmitter clock source (PMA_TXCLK_SRC). The receiver SERDES clock comes from the PMA receiver recovered clock (PMA_RXCLK).

Figure 8–6 shows the transmitter output of the XSBI core. Data transmitted from the PCS to the PMA starts at the core of the Stratix or Stratix GX device and travels to the Stratix or Stratix GX transmitter SERDES block. The transmitter SERDES block converts the parallel data to serial data for 16 individual channels (TX_D[15..0]). The PMA source clock (PMA_TXCLK_SRC) is used to clock out the signal data. PMA_TXCLK is generated from the same phase-locked loop (PLL) as the data, and it travels to the PMA at the same rate as the data. By using one of the data channels in the middle of the bus as the clock (in this case, the eighth channel CH8), the clock-to-data skew improves.

Figure 8–6. Stratix & Stratix GX Device XSBI Transmitter Implementation

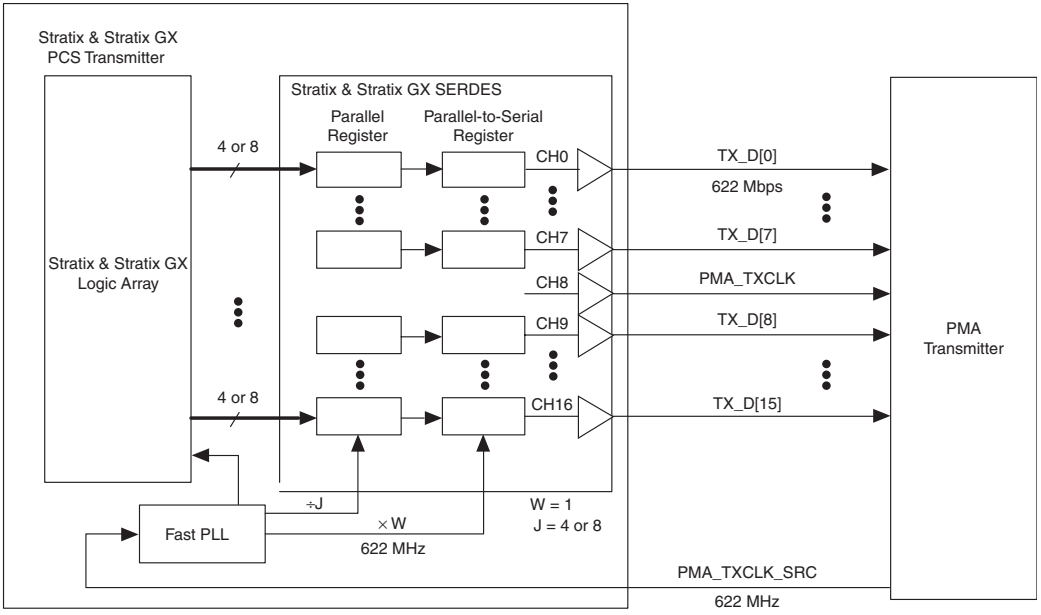
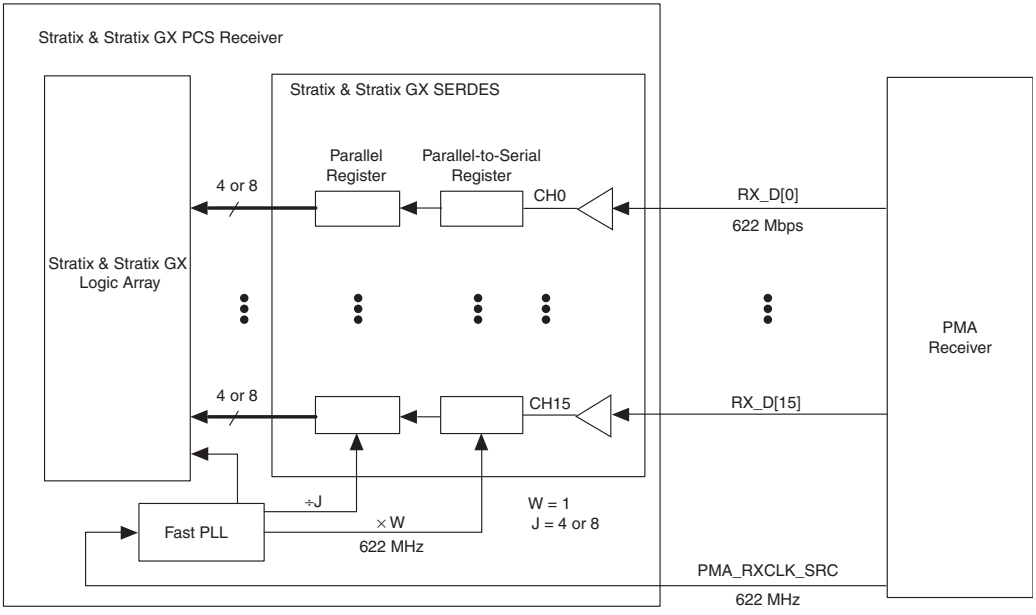


Figure 8–7 shows the receiver input of the XSBI core. From the receiver side, data (RX_D[15..0]) comes from the PMA to the Stratix or Stratix GX receiver SERDES block along with the PMA receiver clock (PMA_RXCLK). The PMA receiver clock is used to convert the serial data to parallel data. The phase shift or inversion on the PMA receiver clock is needed to capture the receiver data.

Stratix and Stratix GX devices contain up to eight fast PLLs. These PLLs provide high-speed outputs for high-speed differential I/O support as well as general- purpose clocking with multiplication and phase shifting. The fast PLL incorporates this 180° phase shift. The Stratix and Stratix GX device's data realignment feature enables you to save more logic elements (LEs). This feature provides a byte-alignment capability, which is embedded inside the SERDES. The data realignment circuitry can correct for bit misalignments by slipping data bits.

For more information about fast PLLs, see the *Stratix Device Family Data Sheet* section of the *Stratix Device Handbook, Volume 1* or the *Stratix GX Device Family Data Sheet* section of the *Stratix GX Device Handbook, Volume 1*.

Figure 8–7. Stratix & Stratix GX Device XSBI Receiver Implementation



With this XSBI transmitter and receiver block implementation, each XSBI core requires two fast PLLs. The potential number of XSBI cores per device corresponds to the number of fast PLLs each Stratix or Stratix GX device contains. Tables 8–2 and 8–3 show the number of LVDS channels, the number of fast PLLs, and the number of XSBI cores that can be supported for each Stratix or Stratix GX device.

Table 8–2. Stratix Device XSBI Core Support

Stratix Device	Number of LVDS Channels (Receive/Transmit) *(1)*	Number of Fast PLLs	Number of XSBI Interfaces (Maximum)
EP1S10	44/44	4	2
EP1S20	66/66	4	2
EP1S25	78/78	4	2
EP1S30	82/82	8	4
EP1S40	90/90	8	4
EP1S60	116/116	8	4
EP1S80	152/156	8	4

Note to Table 8–2:

(1) The LVDS channels can go up to 840 Mbps for flip-chip packages and up to 624 Mbps for wire-bond packages. This number includes both high speed and low speed channels. The high speed LVDS channels can go up to 840 Mbps. The low speed LVDS channels can go up to 462 Mbps. The *High-Speed Differential I/O Support chapter* in the *Stratix Device Handbook, Volume 1,* and the device pin-outs on the web (**www.altera.com**) specify which channels are high and low speed.

Table 8–3. Stratix GX Device XSBI Core Support

Stratix GX Device	Number of LVDS Channels (Receive/Transmit) (1)	Number of Fast PLLs	Number of XSBI Interfaces (Maximum)
EP1SGX10	22/22	2	1
EP1SGX25	39/39	2	2
EP1SGX40	45/45	4	2

Note to Table 8–3:

(1) The LVDS channels can go up to 840 Mbps for flip-chip packages and up to 624 Mbps for wire-bond packages. This number includes both high speed and low speed channels. The high speed LVDS channels can go up to 840 Mbps. The low speed LVDS channels can go up to 462 Mbps. The *High-Speed Differential I/O Support chapter* in the *Stratix Device Handbook, Volume 1,* and the device pin-outs on the web (**www.altera.com**) specify which channels are high and low speed.

AC Timing Specifications

Stratix and Stratix GX devices support a PCS interface. Figures 8–8 and 8–9 and Tables 8–4 and 8–5 illustrate timing characteristics of the PCS transmitter and receiver interfaces.

Figure 8–8 shows the AC timing diagram for the Stratix and Stratix GX PCS transmitter. You can determine PCS channel-to-channel skew by adding the data invalid window before the rising edge (T_{cq_pre}) to the data invalid window after the rising edge (T_{cq_post}).

Figure 8–8. PCS Transmitter Timing Diagram

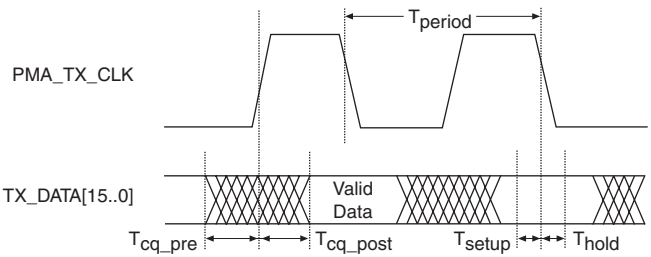


Table 8–4 lists the AC timing specifications for the PCS transmitter.

Table 8–4. PCS Transmitter Timing Specifications

Parameter	Value			Unit
	Min	Typ	Max	
PMA_TX_CLK T_{period} (WAN)		1,608		ps
PMA_TX_CLK T_{period} (LAN)		1,552		ps
Data invalid window before the rising edge (T_{cq_pre})			200	ps
Data invalid window after the rising edge (T_{cq_post})			200	ps
PMA_TX_CLK duty cycle	40		60	%
PCS transmitter channel-to-channel skew			200	ps

Figure 8–9 shows the AC timing diagram for the Stratix and Stratix GX PCS receiver interface. You can determine the PCS sampling window by adding T_{setup} to T_{hold}. Receiver skew margin (RSKM) refers to the amount of skew tolerated on the printed circuit board (PCB).

Figure 8–9. PCS Receiver Timing Diagram

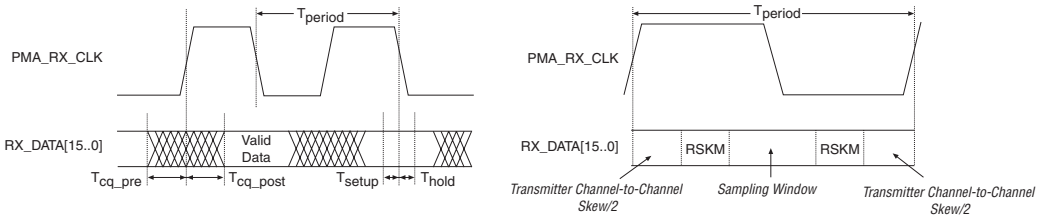


Table 8–5 lists the AC timing specifications for the PCS receiver interface.

Table 8–5. PCS Receiver Timing Specifications (Part 1 of 2)

Parameter	Value			Unit
	Min	Typ	Max	
PMA_RX_CLK T_{period} (WAN)		1,608		ps
PMA_RX_CLK T_{period} (LAN)		1,552		ps
Data invalid window before the rising edge (T_{cq_pre})			200	ps
Data invalid window after the rising edge (T_{cq_post})			200	ps

Table 8–5. PCS Receiver Timing Specifications (Part 2 of 2)

Parameter	Value			Unit
	Min	Typ	Max	
PMA_RX_CLK duty cycle	45		55	%
Data set-up time (T_{setup})	300			ps
Data hold time (T_{hold})	300			ps
PCS sampling window	600			ps
RSKM (WAN)			304	ps
RSKM (LAN)			276	ps

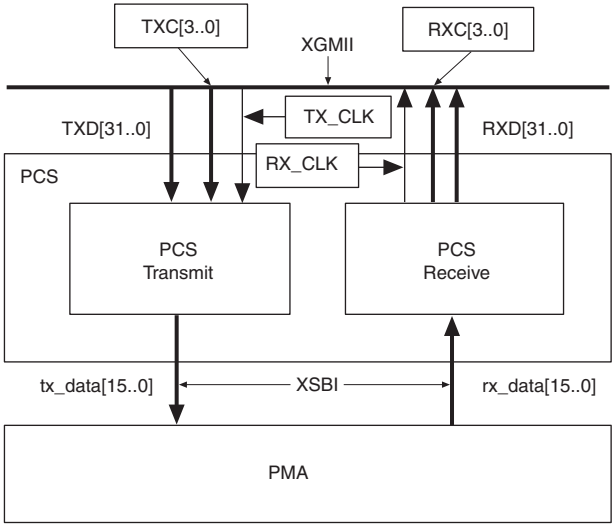
XGMII

The purpose of XGMII is to provide a simple, inexpensive, and easy to implement interconnection between the MAC sublayer and the PHY. Though XGMII is an optional interface, it is used extensively in the 10-Gigabit Ethernet standard as the basis for the specification. The conversion between the parallel data paths of XGMII and the serial MAC data stream is carried out by the reconciliation sublayer. The reconciliation sublayer maps the signal set provided at the XGMII to the physical layer signaling (PLS) service primitives provided at the MAC. XGMII supports a 10-Gbps MAC data rate.

Functional Description

The XGMII is composed of independent transmit and receive paths. Each direction uses 32 data signals, TXD[31..0] and RXD[31..0], 4 control signals, TXC[3..0] and RXC[3..0], and a clock TX_CLK and RX_CLK. Figure 8–10 shows the XGMII functional block diagram.

Figure 8–10. XGMII Functional Block Diagram



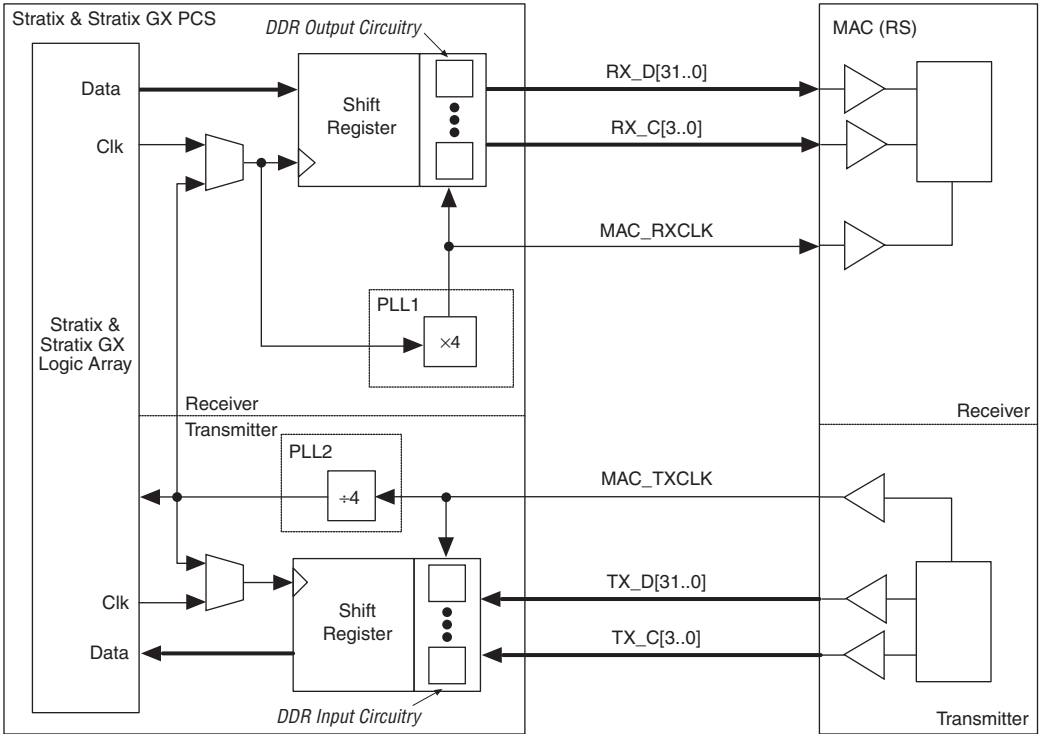
The 32 TXD and four TXC signals as well as the 32 RXD and four RXC signals are organized into four data lanes. The four lanes in each direction share a common clock (TX_CLK for transmit and RX_CLK for receive). The four lanes are used in round-robin sequence to carry an octet stream (8 bits of data per lane). The reconciliation sublayer generates continuous data or control characters on the transmit path and expects continuous data or control characters on the receive path.

Implementation

XGMII uses the 1.5-V HSTL I/O standard. Stratix and Stratix GX devices support the 1.5-V HSTL Class I and Class II I/O standard (EIA/JESD8-6). The standard requires a differential input with an external reference voltage (V_{REF}) of 0.75 V, as well as a termination voltage V_{TT} of 0.75 V, to which termination resistors are connected. The HSTL Class I standard requires a 1.5-V V_{CCIO} voltage, which is supported by Stratix and Stratix GX devices.

Figure 8–11 shows the 32-bit full-duplex 1.5-V HSTL implementation of XGMII.

Figure 8–11. Stratix & Stratix GX XGMII Implementation



For this implementation, the shift register clocks can either be generated from a divided down MAC reconciliation sublayer transmitter clock (MAC_TXCLK), or the asynchronous core clock, or both if using a FIFO buffer.

Figure 8–12 shows one channel of the output half of XGMII. Data that is transmitted from the PCS to the MAC reconciliation sublayer starts at the core of the Stratix or Stratix GX device and travels to the shift register. The shift register takes in the parallel data (even bits sent to the top register and odd bits sent to the bottom register) and serializes the data. After the data is serialized, it travels to the double data rate (DDR) output circuitry, which is clocked with the ×4 clock from the PLL. Out of the DDR output circuitry, the data drives off-chip along with the ×4 clock. This transaction creates the DDR relationship between the clock and the data output. This implementation only shows one channel, but can be duplicated to include all 32 bits of the RX_D signal and all 4 bits of the RX_C signal.

Figure 8–12. Stratix & Stratix GX XGMII Output Implementation (One Channel)

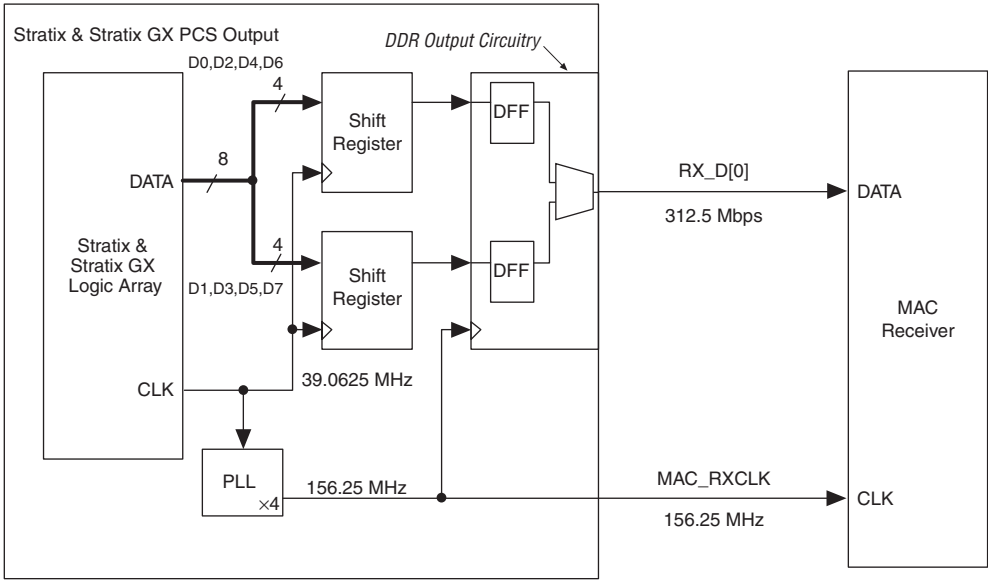
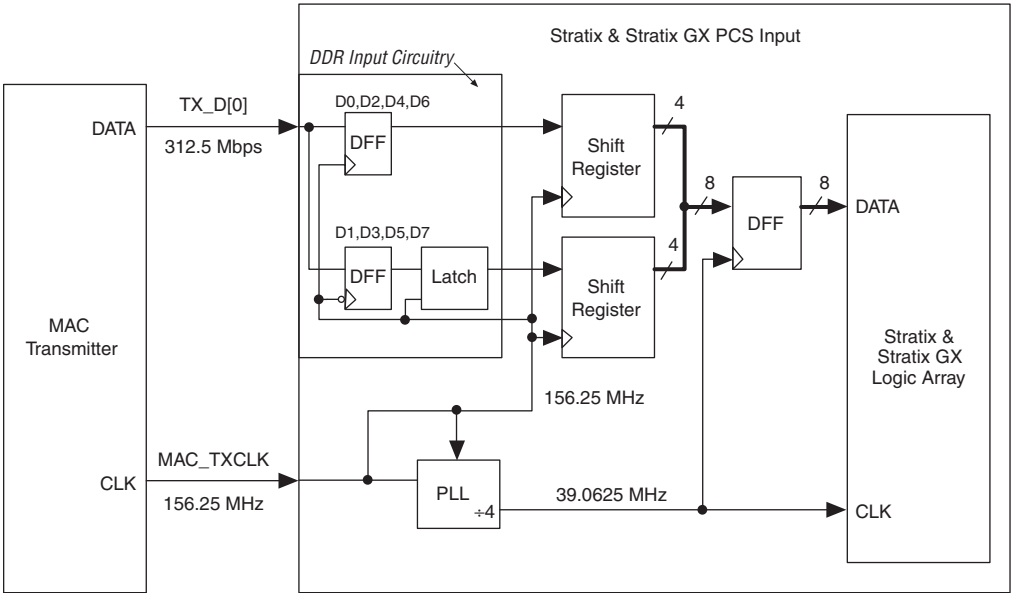


Figure 8–13 shows one channel of the input half of the XGMII interface. From the receiver side, the DDR data is captured from the MAC to the Stratix and Stratix GX PCS DDR input circuitry. The serial data is separated into two individual data streams with the even bits routed to the top register and odd bits routed to the bottom register. The DDR input circuitry produces two output data streams that go into the shift registers. From the shift registers, the data is deserialized using the clock from the MAC, combining into an 8-bit word. This parallel data goes to a register that is clocked by the divide-by-4 clock from the PLL. This data and clock go to the Stratix and Stratix GX core. This implementation shows only one channel, but can be duplicated to include all 32 bits of the `TX_D` signal and all 4 bits of the `TX_C` signal.

Figure 8–13. Stratix & Stratix GX XGMII Input Implementation (One Channel)



Stratix and Stratix GX devices contain up to four enhanced PLLs. These PLLs provide features such as clock switchover, spread-spectrum clocking, programmable bandwidth, phase and delay control, and PLL reconfiguration. Since the maximum clock rate is 156.25 MHz, you can use a fast or enhanced PLL for both the XGMII output and input blocks.

For more information about fast PLLs, see the *Stratix Device Family Data Sheet* section of the *Stratix Device Handbook, Volume 1* or the *Stratix GX Device Family Data Sheet* section of the *Stratix GX Device Handbook, Volume 1*.

With this implementation for the XGMII output and input blocks, the number of XGMII cores per device corresponds to the number of PLLs each Stratix and Stratix GX device contains. Tables 8–6 and 8–7 show the number of 1.5-V HSTL I/O pins, PLLs, and XGMII cores that are supported in each Stratix and Stratix GX device. Each core requires 72 1.5-

V HSTL I/O pins for data and control and 2 clock pins for the transmitter and receiver clocks. Each XGMII core also needs two PLLs (one for each direction).

Table 8–6. Stratix XGMII Core Support

Stratix Device	Number of 1.5-V HSTL Class I I/O Pins	Number of Fast & Enhanced PLLs	Number of XGMII Interfaces
EP1S10	410	6	3
EP1S20	570	6	3
EP1S25	690	6	3
EP1S30	718	10	5
EP1S40	814	12	6
EP1S60	1,014	12	6
EP1S80	1,195	12	6

Table 8–7. Stratix GX XGMII Core Support

Stratix Device	Number of 1.5-V HSTL Class I I/O Pins	Number of Fast & Enhanced PLLs	Number of XGMII Interfaces
EP1SGX10 C, D	226	4	2
EP1SGX25 C	253	4	2
EP1SGX25 D, F	370	4	2
EP1SGX40 D, G	430	8	4

Reduced System Noise

The output buffer of each Stratix and Stratix GX device I/O pin has a programmable drive strength control for certain I/O standards. The 1.5-V HSTL Class I standard supports the minimum setting, which is the lowest drive strength that guarantees I_{OH} and I_{OL} of the standard. Using minimum settings provides signal slew rate control to reduce system noise and signal overshoot.

For more information on I_{OH} and I_{OL} values, see *Operating Conditions* in the *DC & Switching Characteristics* chapter of the *Stratix Device Handbook, Volume 1* or *Operating Conditions* in the *DC & Switching Characteristics* chapter of the *Stratix GX Device Handbook, Volume 1*.

Timing

XGMII signals must meet the timing requirements shown in Figure 8–14. Make all XGMII timing measurements at the driver output (shown in Figure 8–14) and a capacitive load from all sources of 20 pF that are specified relative to the V_{IL}_AC(max) and V_{IH}_AC(min) thresholds.

Figure 8–14. XGMII Timing Diagram

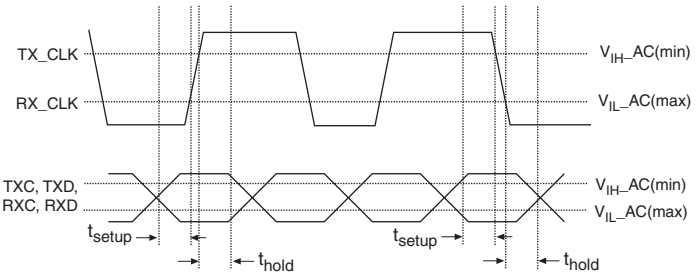


Table 8–8 shows the XGMII timing specifications.

Table 8–8. XGMII Timing Specifications Note (1)

Symbol	Driver	Receiver	Unit
T_{setup}	960	480	ps
T_{hold}	960	480	ps

Note to Table 8–8:

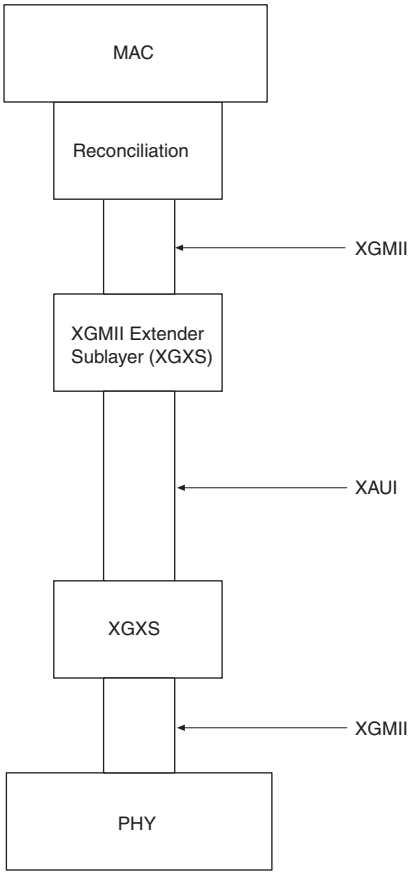
(1) The actual set-up and hold times will be made available after device characterization is complete.

Stratix and Stratix GX devices support DDR data with clock rates of up to 200 MHz, well above the XGMII clock rate of 156.25 MHz. For the HSTL Class I I/O standard, Stratix and Stratix GX device I/O drivers provide a 1.0-V/ns slew rate at the input buffer of the receiving device.

XAUI

XAUI (pronounced Zowie) is located between the XGMII at the reconciliation sublayer and the XGMII at the PHY layer. Figure 8–15 shows the location of XAUI. XAUI is designed to either extend or replace XGMII in chip-to-chip applications of most Ethernet MAC to PHY interconnects.

Figure 8–15. XAUI Location

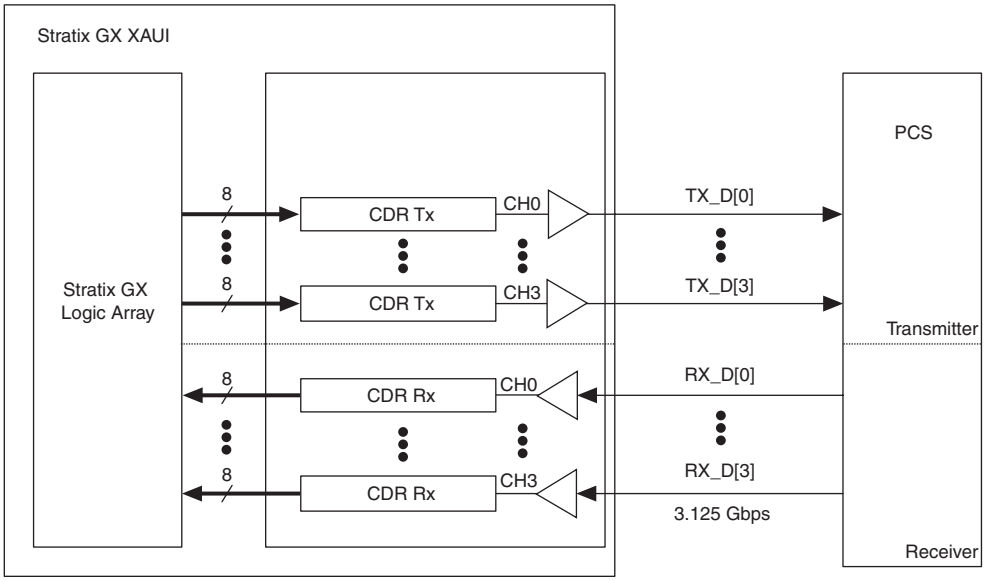


Functional Description

XAUI can replace the 32 bits of parallel data required by XGMII for transmission with just 4 lanes of serial data. XAUI uses clock data recovery (CDR) to eliminate the need for separate clock signals. 8b/10b encoding is employed on the data stream to embed the clock in the data. The 8b/10b protocol to encode an 8-bit word stream to 10-bit codes that results in a DC-balanced serial stream and eases the receiver synchronization. To support 10-Gigabit Ethernet, each lane must run at a speed of at least 2.5 Gbps. Using 8b/10b encoding increases the rate for each lane to 3.125 Gbps, which will be supported in Stratix GX Gbps devices. This circuitry is supported by the embedded 3.125 Gbps transceivers within the Stratix GX architecture. You can find more

information on XAUI support in *Section II, Stratix GX Transceiver User Guide* of the *Stratix GX Device Handbook, Volume 2*. Figure 8–16 shows how XAUI is implemented.

Figure 8–16. Stratix GX XAUI Implementation



I/O Characteristics for XSBI, XGMII & XAUI

The three interfaces of 10-Gigabit Ethernet (XSBI, XGMII, and XAUI) each have different rates and I/O standards. Table 8–9 shows the characteristics for each interface.

Table 8–9. 10-Gigabit Ethernet Interfaces Characteristics

Interface	Width	Clock Rate (MHz)	Data Rate Per Channel	Clocking Scheme	I/O Type
XGMII	32	156.25	312.5 Mbps	DDR source synchronous	1.5-V HSTL
XSBI	16	644.5 or 622.08	644.5 or 622.08 Mbps	SDR source synchronous	LVDS
XAUI	4	None	3.125 Gbps	Clock data recovery (CDR)	1.5-V PCML

Software Implementation

You can use the **Assignment Organizer** in the Altera® Quartus® II software to implement the I/O standards for a particular interface. For example, set the I/O standard to LVDS for XSBI and to HSTL Class I for XGMII. You can use the MegaWizard® Plug-In Manager to create the PLLs and transmitter and receiver SERDES blocks for the XSBI implementation and PLLs and DDR input and output circuitry for the XGMII implementation. For more information on the Assignment Organizer or MegaWizard Plug-In Manager, see the Quartus II Software Help.

AC/DC Specifications

Table 8–10 lists the XSBI DC electrical characteristics, similar to Stratix and Stratix GX devices, that are based on the ANSI/TIA-644 LVDS specification.

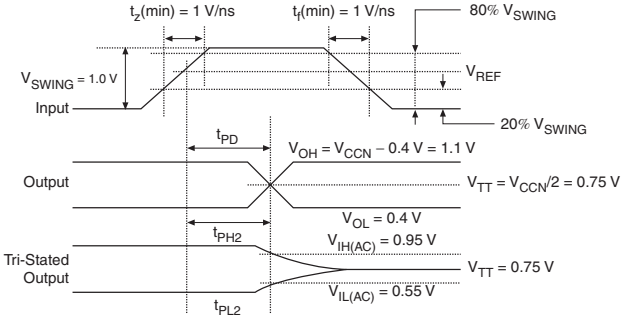
Table 8–10. XSBI DC Specifications

Parameter	Value			Unit
	Min	Typ	Max	
Output differential voltage (V_{OD})	250		400 *(1)*	mV
Output offset voltage (V_{OS})	1,125		1,375	mV
Output Impedance, single ended	40		140	W
Change in V_{OD} between ‘0’ and ‘1’			50	mV
Change in V_{OS} between ‘0’ and ‘1’			50	mV
Input voltage range (V_I)	900		1,600	mV
Differential impedance		100		W
Input differential voltage (V_{ID})	100		600	mV
Receiver differential input impedance	70		130	W
Ground potential difference (between PCS and PMA)			50	mV
Rise and fall times (20% to 80%)	100		400	ps

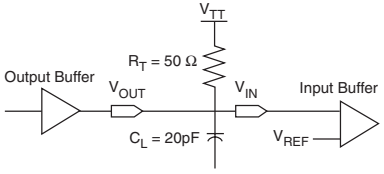
Note to Table 8–10:
(1) Larger V_{OD} is possible for better signal intensity.

I/O characteristics for the 1.5-V HSTL standard for Stratix and Stratix GX devices are shown in Figure 8–17 and comply with XGMII electrical specifications available in 10-Gigabit Ethernet draft IEEE P802.3ae.

Figure 8–17. Electrical Characteristics for Stratix & Stratix GX Devices (1.5-V HSTL Class I)



HSTL AC Load Circuit for Class I



HSTL AC Waveform & I/O Interface

Table 8–11 lists the DC specifications for Stratix and Stratix GX devices (1.5-V HSTL Class I).

Table 8–11. DC Specifications for Stratix & Stratix GX Devices (1.5-V HSTL Class I) Note (1)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{CCIO}	I/O supply voltage		1.4	1.5	1.6	V
V_{REF}	Input reference voltage		0.68	0.75	0.9	V
V_{TT}	Termination voltage		0.7	0.75	0.8	V
V_{IH} (DC)	DC high-level input voltage		V_{REF} + 0.1			V
V_{IL} (DC)	DC low-level input voltage		–0.3		V_{REF} – 0.1	V
V_{IH} (AC)	AC high-level input voltage		V_{REF} + 0.2			V
V_{IL} (AC)	AC low-level input voltage				V_{REF} – 0.2	V
I_I	Input pin leakage current	$0 < V_{IN} < V_{CCIO}$	–10		10	µA
V_{OH}	High-level output voltage	I_{OH} = –8 mA	V_{CCIO} – 0.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA			0.4	V
I_O	Output leakage current (when output is high Z)	$GND \leq V_{OUT} \leq V_{CCIO}$	–10		10	µA

Note to Table 8–11:

(1) Drive strength is programmable according to values shown in the *Stratix Device Family Data Sheet* section of the *Stratix Device Handbook, Volume 1* or the *Stratix GX Device Family Data Sheet* section of the *Stratix GX Device Handbook, Volume 1*.

10-Gigabit Ethernet MAC Core

As an Altera Megafunction Partners Program (AMPP℠) member, MorethanIP provides a 10-Gigabit Ethernet MAC core for Altera customers. MorethanIP's 10-Gigabit Ethernet MAC core implements the RS, the MAC layer, and user-programmable FIFO buffers for clock and data decoupling.

Core Features

MorethanIP's 10-Gigabit Ethernet MAC core provides the following features:

- Includes automatic pause frame generation (per IEEE 802.3×31) with user-programmable pause quanta and pause-frame termination
- Includes a programmable 48-bit MAC address with a promiscuous mode option, and a programmable Ethernet frame length that supports IEEE 802.1Q VLAN-tagged frames or jumbo Ethernet frames

- Supports broadcast traffic and multi-cast address resolution with a 64-entry hash table
- Compliant with the IEEE802.3ae Draft 4.0
- Implements XGMII, allowing it to interface to XAUI through a 10-Gigabit commercial SERDES

Conclusion

10-Gigabit Ethernet takes advantage of the existing Gigabit Ethernet standard. With their rich I/O features, Stratix and Stratix GX devices support the components of 10-Gigabit Ethernet as well as XSBI and XGMII. Stratix GX devices also support XAUI. These interfaces are easily implemented using the core architecture, differential I/O capabilities, and superior PLLs of Stratix and Stratix GX devices.