MV51004-1.0

This chapter provides information about hot-socketing specifications, power-on reset (POR) requirements, and their implementation in MAX® V devices.

MAX V devices offer hot socketing, also known as hot plug-in or hot swap, and power sequencing support. You can insert or remove a MAX V device in a system during system operation without causing undesirable effects to the running system bus. The hot-socketing feature removes some of the difficulty when using MAX V devices on PCBs that contain a mixture of 3.3-, 2.5-, 1.8-, and 1.5-V devices.

The MAX V hot-socketing feature provides the following:

■ Board or device insertion and removal

■ Support for any power-up sequence

■ Non-intrusive I/O buffers to system buses during hot insertion

This chapter contains the following sections:

MAX V Hot-Socketing Specifications

MAX V devices offer the hot-socketing feature without the need for external components or special design requirements. The advantages of hot-socketing support in MAX V devices includes the following:

■ The device can be driven before and during power up or power down without damaging the device.

■ I/O pins remain tri-stated during power up. The device does not drive out before or during power up, thereby affecting other operating buses.

■ Signal pins do not drive the V_{CCIO} or V_{CCINT} power supplies. External input signals to the device I/O pins do not power the device V_{CCIO} or V_{CCINT} power supplies using internal paths. This is true if the V_{CCINT} and V_{CCIO} power supplies are held at GND.

☞ Altera uses GND as a reference for the hot-socketing and I/O buffers circuitry designs. To ensure device reliability and compliance to the hot-socketing specifications, you must connect GND between boards before connecting the V_{CCINT} and V_{CCIO} power supplies.

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Devices Can Be Driven Before Power Up

You can drive signals into the I/O pins and GCLK[3..0] pins of MAX V devices before or during power up or power down without damaging the device. To simplify the system-level design, MAX V devices support any power-up or power-down sequence (V_{CCIO1}, V_{CCIO2}, V_{CCIO3}, V_{CCIO4}, and V_{CCINT}).

I/O Pins Remain Tri-Stated During Power Up

A device that does not support hot socketing may interrupt system operation or cause contention by driving out before or during power up. In a hot-socketing situation, the MAX V device's output buffers are turned off during system power up. MAX V devices do not drive out until the device attains proper operating conditions and is fully configured. For more information about turn-on voltages, refer to "Power-On Reset Circuitry" on page 4–5.

Signal Pins Do Not Drive the V_{CCIO} or V_{CCINT} Power Supplies

MAX V devices do not have a current path from the I/O pins or GCLK[3..0] pins to the V_{CCIO} or V_{CCINT} power supplies before or during power up. A MAX V device may be inserted into (or removed from) a system board that is powered up without damaging or interfering with system-board operation. When hot socketing, MAX V devices may have a minimal effect on the signal integrity of the backplane.

AC and DC Specifications

You can power up or power down the V_{CCIO} and V_{CCINT} power supplies in any sequence. During hot socketing, the I/O pin capacitance is less than 8 pF. MAX V devices meet the following hot-socketing specifications:

- DC specification: | I_{IOPIN} | < 300 µA.
- AC specification: | I_{IOPIN} | < 8 mA for 10 ns or less.

☞ MAX V devices are immune to latch-up when hot socketing. If the TCK JTAG input pin is driven high during hot socketing, the current on that pin might exceed the specifications listed above.

I_{IOPIN} is the current for any user I/O pin on the device. The AC specification applies when the device is being powered up or powered down. This specification takes into account the pin capacitance but not the board trace and external loading capacitance. You must consider additional capacitance for trace, connector, and loading separately. The peak current duration due to power-up transients is 10 ns or less.

The DC specification applies when all V_{CC} supplies to the device are stable in the powered-up or powered-down conditions.

Hot-Socketing Feature Implementation in MAX V Devices

The hot-socketing feature tri-states the output buffer during the power-up event (either the V_{CCINT} or V_{CCIO} power supplies) or power-down event. The hot-socketing circuitry generates an internal HOTSCKT signal when either V_{CCINT} or V_{CCIO} is below the threshold voltage during power up or power down. The HOTSCKT signal cuts off the output buffer to ensure that no DC current leaks through the pin (except for weak pull-up leaking). When V_{CC} ramps up very slowly during power up, V_{CC} may still be relatively low even after the POR signal is released and device configuration is complete.

☞ Ensure that V_{CCINT} is within the recommended operating range even though SRAM download has completed.

Figure 4–1 shows the circuitry for each I/O and clock pin.

**Figure 4–1. Hot-Socketing Circuitry for MAX V Devices**
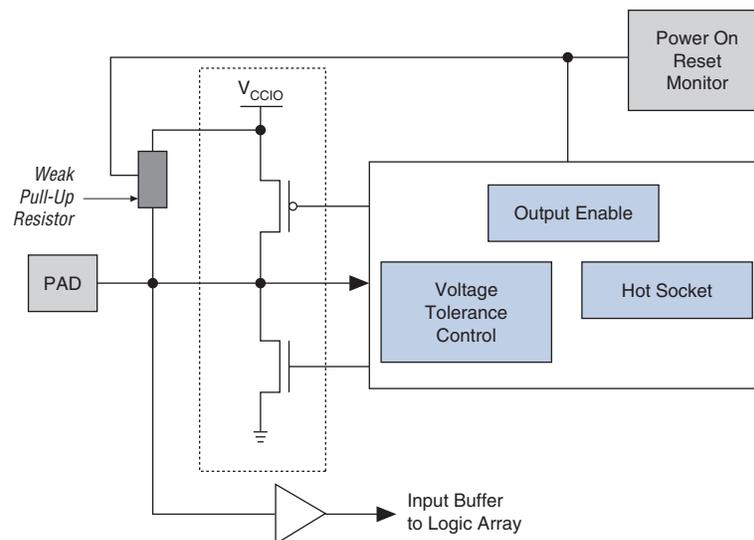
The POR circuit monitors the V_{CCINT} and V_{CCIO} voltage levels and keeps the I/O pins tri-stated until the device has completed its flash memory configuration of the SRAM logic. The weak pull-up resistor (R) from the I/O pin to V_{CCIO} is enabled during download to keep the I/O pins from floating. The 3.3-V tolerance control circuit permits the I/O pins to be driven by 3.3 V before V_{CCIO} and/or V_{CCINT} are powered, and it prevents the I/O pins from driving out when the device is not fully powered or operational. The hot-socketing circuitry prevents the I/O pins from internally powering V_{CCIO} and V_{CCINT} when driven by external signals before the device is powered.

🔖 For more information about the 5.0-V tolerance, refer to the *Using MAX V Devices in Multi-Voltage Systems* chapter.

Figure 4–2 shows a transistor-level cross section of the MAX V device I/O buffers. This design ensures that the output buffers do not drive when V_{CCIO} is powered before V_{CCINT} or if the I/O pad voltage is higher than V_{CCIO}. This also applies for sudden voltage spikes during hot insertion. The V_{PAD} leakage current charges the 3.3-V tolerant circuit capacitance.

Figure 4–2. Transistor-Level I/O Buffers for MAX V Devices
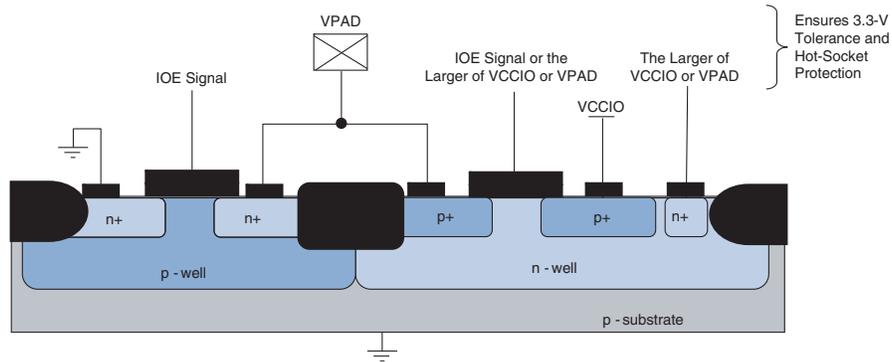
The CMOS output drivers in the I/O pins intrinsically provide electrostatic discharge (ESD) protection. There are two cases to consider for ESD voltage strikes—positive voltage zap and negative voltage zap.

A positive ESD voltage zap occurs when a positive voltage is present on an I/O pin due to an ESD charge event. This can cause the N+ (Drain)/ P-Substrate junction of the N-channel drain to break down and the N+ (Drain)/P-Substrate/N+ (Source) intrinsic bipolar transistor turn on to discharge ESD current from I/O pin to GND. The dashed line in Figure 4–3 shows the ESD current discharge path during a positive ESD zap.

Figure 4–3. ESD Protection During Positive Voltage Zap
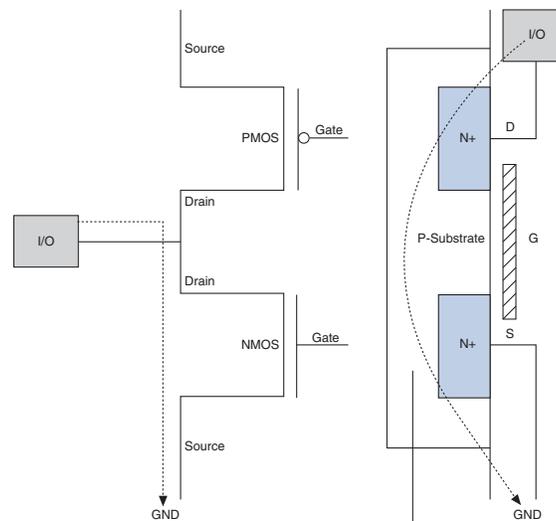
When the I/O pin receives a negative ESD zap at the pin that is less than –0.7 V (0.7 V is the voltage drop across a diode), the intrinsic P-Substrate/N+ drain diode is forward biased. Therefore, the discharge ESD current path is from GND to the I/O pin, as shown in Figure 4–4.

Figure 4–4. ESD Protection During Negative Voltage Zap
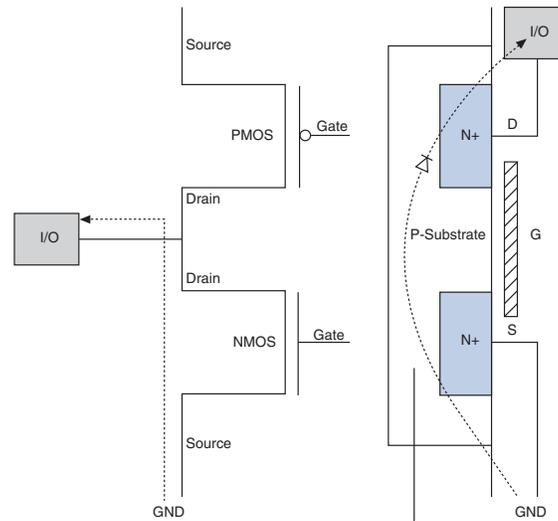
Power-On Reset Circuitry

MAX V devices have POR circuits to monitor the V_{CCINT} and V_{CCIO} voltage levels during power up. The POR circuit monitors these voltages, triggering download from the non-volatile configuration flash memory block to the SRAM logic, maintaining the tri-state of the I/O pins (with weak pull-up resistors enabled) before and during this process. When the MAX V device enters user mode, the POR circuit releases the I/O pins to user functionality. The POR circuit of the MAX V device does not monitor the V_{CCINT} voltage level after the device enters into user mode.

Power-Up Characteristics

When power is applied to a MAX V device, the POR circuit monitors V_{CCINT} and begins SRAM download at 1.55 V for MAX V devices. From this voltage reference, the SRAM download and entry into user mode takes 200 to 450 µs maximum, depending on your device density. This period of time is specified as t_{CONFIG} in the power-up timing section of the *DC and Switching Characteristics for MAX V Devices* chapter.

Entry into user mode is gated by whether all the V_{CCIO} banks are powered with sufficient operating voltage. If V_{CCINT} and V_{CCIO} are powered simultaneously, the device enters user mode within the t_{CONFIG} specifications. If V_{CCIO} is powered more than t_{CONFIG} after V_{CCINT}, the device does not enter user mode until 2 µs after all V_{CCIO} banks are powered.

For MAX V devices, the POR circuitry does not monitor the V_{CCINT} and V_{CCIO} voltage levels after the device enters user mode. If there is a V_{CCINT} voltage sag below 1.4 V during user mode, the functionality of the device is not guaranteed and you must power down V_{CCINT} to 250 mV for a minimum of 10 µs before powering V_{CCINT} and V_{CCIO} up again. After V_{CCINT} rises from 250 mV back to approximately 1.55 V, the SRAM download restarts and the device begins to operate after the t_{CONFIG} time has passed.

Figure 4–5 shows the voltages for POR of MAX V devices during power up into user mode and from user mode to power down or brown out.

☞ All V_{CCINT} and V_{CCIO} power supplies of all banks must be powered on before entering user mode.

Figure 4–5. Power-Up Characteristics for MAX V Devices *(Note 1)*, *(2)*
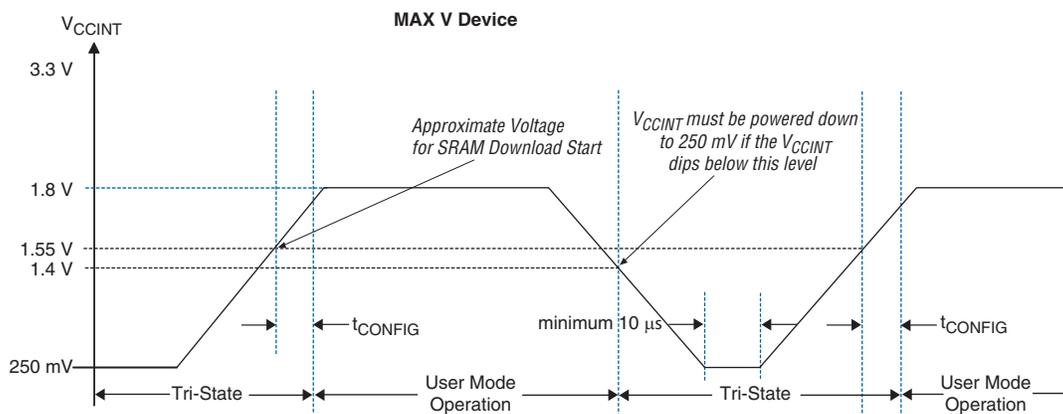
Notes to Figure 4–5:

(1) Time scale is relative.

(2) For this figure, all the V_{CCIO} banks are powered up simultaneously with the V_{CCINT} profile shown. If this is not the case, t_{CONFIG} stretches out until all V_{CCIO} banks are powered.

☞ After SRAM configuration, all registers in the device are cleared and released into user function before the I/O tri-states are released. To release clears after the tri-states are released, use the DEV_CLRn pin option. To hold the tri-states beyond the power-up configuration time, use the DEV_OE pin option.

Document Revision History

Table 4–1 lists the revision history for this chapter.

Table 4–1. Document Revision History

Date	Version	Changes
December 2010	1.0	Initial release.