2. Stratix GX Transceivers

SGX51002-1.1

Transceiver Blocks

Stratix® GX devices incorporate dedicated embedded circuitry on the right side of the device, which contains up to 20 high-speed 3.1875-Gbps serial transceiver channels. Each Stratix GX transceiver block contains four full-duplex channels and supporting logic to transmit and receive high-speed serial data streams. The transceiver block uses the channels to deliver bidirectional point-to-point data transmissions with up to 3.1875 Gbps of data transition per channel.

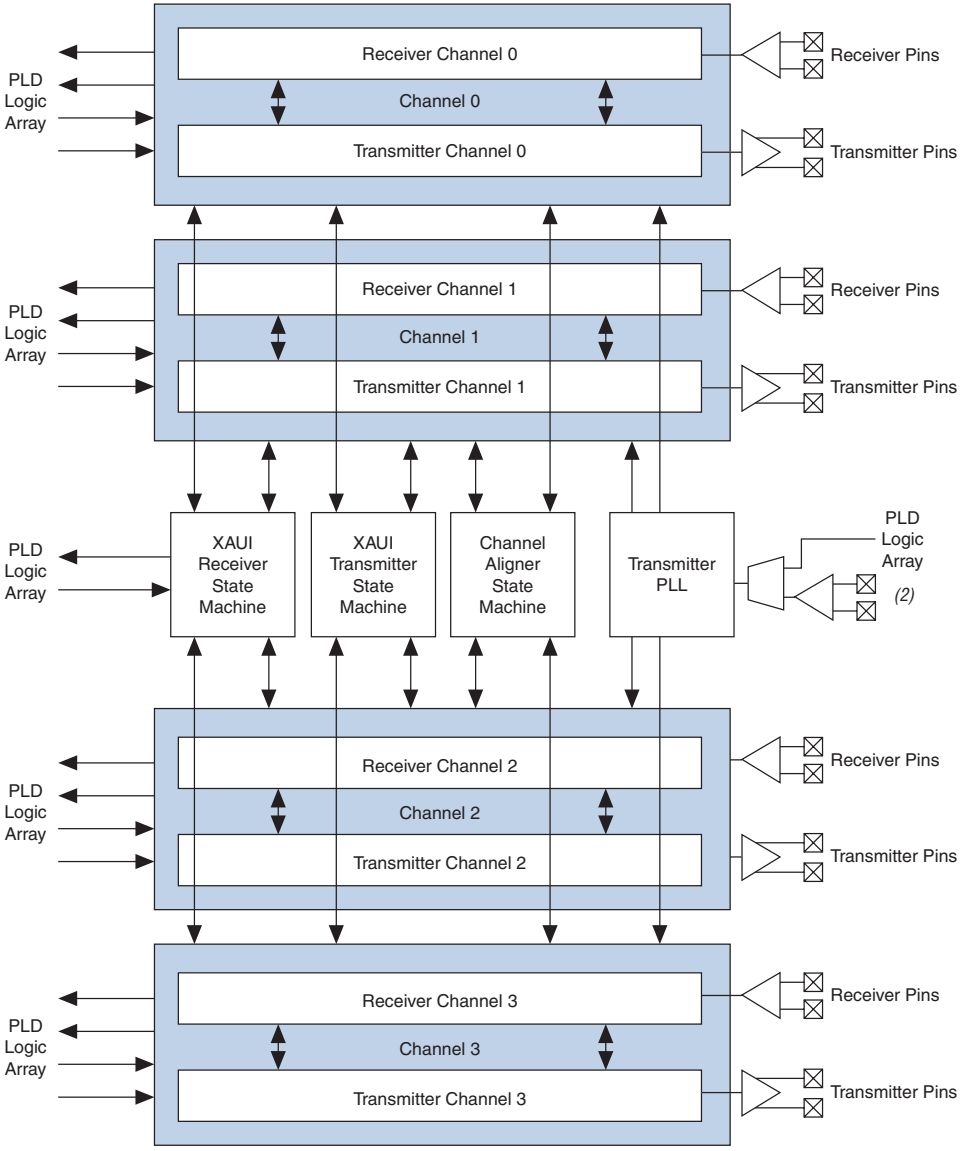
There are up to 20 transceiver channels available on a single Stratix GX device. Table 2–1 shows the number of transceiver channels available on each Stratix GX device.

Table 2–1. Stratix GX Transceiver Channels

Device	Number of Transceiver Channels
EP1SGX10C	4
EP1SGX10D	8
EP1SGX25C	4
EP1SGX25D	8
EP1SGX25F	16
EP1SGX40D	8
EP1SGX40G	20

Figure 2–1 shows the elements of the transceiver block, including the four channels, supporting logic, and I/O buffers. Each transceiver channel consists of a receiver and transmitter. The supporting logic contains a transmitter PLL to generate a high-speed clock used by the four transmitters. The receiver PLL within each transceiver channel generates the receiver reference clocks. The supporting logic also contains state machines to manage rate matching for XAUI and GIGE applications, in addition to channel bonding for XAUI applications.

Figure 2–1. Stratix GX Transceiver Block *Note (1)*



Notes to Figure 2–1:

(1) Each receiver channel has its own PLL and CRU, which are not shown in this diagram. For more information, refer to the section "Receiver Path" on page 2–13.

(2) For possible transmitter PLL clock inputs, refer to the section "Transmitter Path" on page 2–5.

Each Stratix GX transceiver channel consists of a transmitter and receiver. The transmitter contains the following:

- Transmitter PLL
- Transmitter phase compensation FIFO buffer
- Byte serializer
- 8B/10B encoder
- Serializer (parallel to serial converter)
- Transmitter output buffer

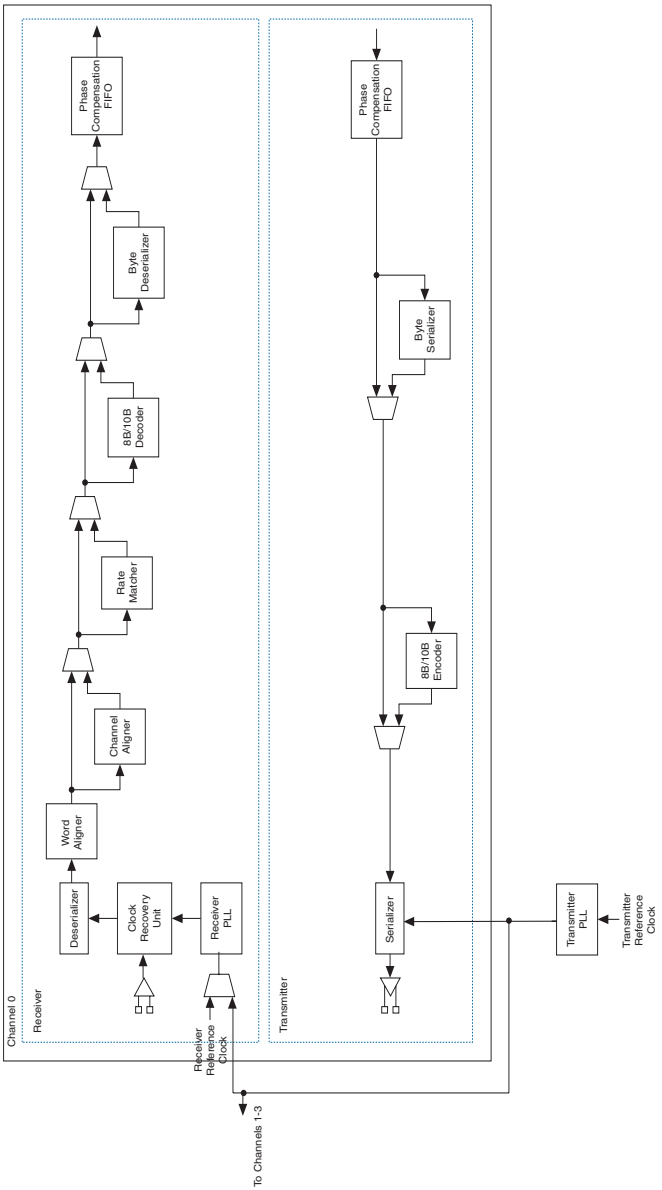
The receiver contains the following:

- Input buffer
- Clock recovery unit (CRU)
- Deserializer
- Pattern detector and word aligner
- Rate matcher and channel aligner
- 8B/10B decoder
- Receiver logic array interface

You can set all the Stratix GX transceiver functions through the Quartus II software. You can set programmable pre-emphasis, programmable equalizer, and programmable V_{OD} dynamically as well. Each Stratix GX transceiver channel is also capable of BIST generation and verification in addition to various loopback modes. Figure 2–2 shows the block diagram for the Stratix GX transceiver channel.

Stratix GX transceivers provide physical coding sublayer (PCS) and physical media attachment (PMA) implementation for protocols such as 10-gigabit XAUI and GIGE. The PCS portion of the transceiver consists of the logic array interface, 8B/10B encoder/decoder, pattern detector, word aligner, rate matcher, channel aligner, and the BIST and pseudo-random binary sequence pattern generator/verifier. The PMA portion of the transceiver consists of the serializer/deserializer, the CRU, and the I/O buffers.

Figure 2–2. Stratix GX Transceiver ChanneL Note (1)



Note to Figure 2–2:
(1) There are four transceiver channels in a transceiver block.

Transmitter Path

This section describes the data path through the Stratix GX transmitter (see Figure 2–2). Data travels through the Stratix GX transmitter via the following modules:

- Transmitter PLL
- Transmitter phase compensation FIFO buffer
- Byte serializer
- 8B/10B encoder
- Serializer (parallel to serial converter)
- Transmitter output buffer

Transmitter PLL

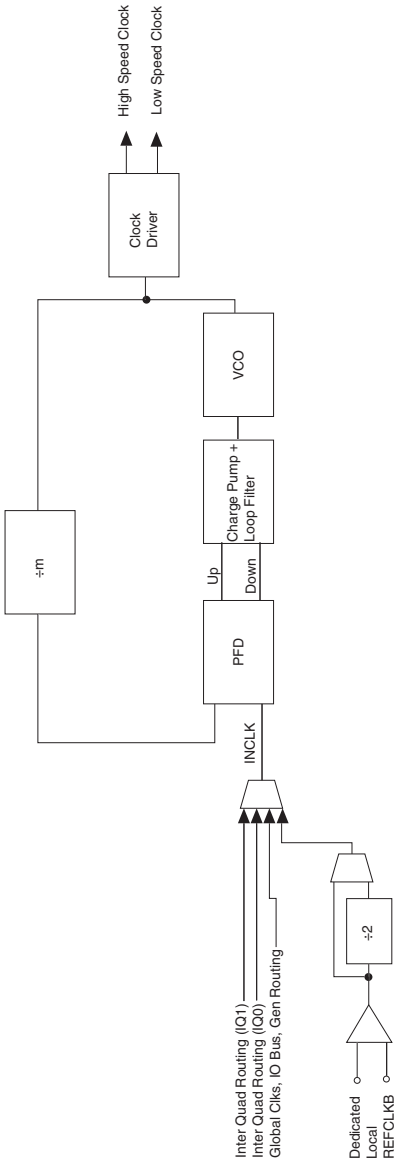
Each transceiver block has one transmitter PLL, which receives the reference clock and generates the following signals:

- High-speed serial clock used by the serializer
- Slow-speed reference clock used by the receiver
- Slow-speed clock used by the logic array (divisible by two for double-width mode)

The INCLK clock is the input into the transmitter PLL. There is one INCLK clock per transceiver block. This clock can be fed by either the REFCLKB pin, PLD routing, or the inter-transceiver routing line. See the section "Stratix GX Clocking" on page 2–30 for more information about the inter-transceiver lines.

The transmitter PLL in each transceiver block clocks the circuits in the transmit path. The transmitter PLL is also used to train the receiver PLL. If no transmit channels are used in the transceiver block, the transmitter PLL can be turned off. Figure 2–3 is a block diagram of the transmitter PLL.

Figure 2–3. Transmitter PLL Block Diagram *Note (1)*



Note to Figure 2–3:
(1) The divider in the PLL divides by 4, 8, 10, 16, or 20.

The transmitter PLL can support up to 3.1875 Mbps. The input clock frequency for –5 and –6 speed grade devices is limited to 650 MHz if you use the REFCLKB pin or to 325 MHz if you use the other clock routing resources. For –7 speed grade devices, the maximum input clock frequency is 312.5 MHz with the REFCLKB pin, and the maximum is 156.25 MHz for all other clock routing resources. An optional PLL_LOCKED port is available to indicate whether the transmitter PLL is locked to the reference clock. The transmitter PLL has a programmable loop bandwidth that can be set to low or high. The loop bandwidth parameter can be statically set in the Quartus II software.

Table 2–2 lists the adjustable parameters in the transmitter PLL.

Table 2–2. Transmitter PLL Specifications

Parameter	Specifications
Input reference frequency range	25 MHz to 650 MHz
Data rate support	500 Mbps to 3.1875 Gbps
Multiplication factor (W)	2, 4, 5, 8, 10, 16, or 20 *(1)*
Bandwidth	Low, high

Note to Table 2–2:
(1) Multiplication factors 2 and 5 can only be achieved with the use of the pre-divider on the REFCLKB pin.

Transmitter Phase Compensation FIFO Buffer

The transmitter phase compensation FIFO buffer resides in the transceiver block at the PLD boundary. This FIFO buffer compensates for the phase differences between the transmitter reference clock (inclk) and the PLD interface clock (tx_coreclk). The phase difference between the two clocks must be less than 360° . The PLD interface clock must also be frequency locked to the transmitter reference clock. The phase compensation FIFO buffer is four words deep and cannot be bypassed.

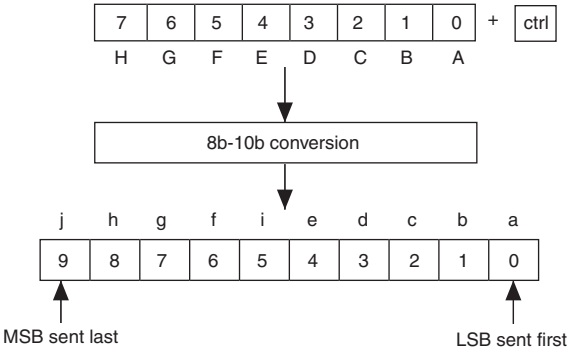
Byte Serializer

The byte serializer takes double-width words (16 or 20 bits) from the PLD interface and converts them to a single width word (8 or 10 bits) for use in the transceiver. The transmit data path after the byte serializer is single width (8 or 10 bits). The byte serializer is bypassed when single width mode (8 or 10 bits) is used at the PLD interface.

8B/10B Encoder

The 8B/10B encoder translates 8-bit wide data + 1 control enable bit into a 10-bit encoded data. The encoded data has a maximum run length of 5. The 8B/10B encoder can be bypassed. Figure 2–4 diagrams the encoding process.

Figure 2–4. Encoding Process



Transmit State Machine

The transmit state machine operates in either XAUI mode or in GIGE mode, depending on the protocol used.

GIGE Mode

In GIGE mode, the transmit state machines convert all idle ordered sets (/K28.5/, /Dx.y/) to either /I1/ or /I2/ ordered sets. /I1/ consists of a negative-ending disparity /K28.5/ (denoted by /K28.5/-) followed by a neutral /D5.6/. /I2/ consists of a positive-ending disparity /K28.5/ (denoted by /K28.5/+) and a negative-ending disparity /D16.2/ (denoted by /D16.2/-). The transmit state machines do not convert any of the ordered sets to match /C1/ or /C2/, which are the configuration ordered sets. (/C1/ and /C2/ are defined by (/K28.5/, /D21.5/) and (/K28.5/, /D2.2/), respectively.) Both the /I1/ and /I2/ ordered sets guarantee a negative-ending disparity after each ordered set. The GIGE transmit state machine can be statically disabled in the Quartus II software, even if using the GIGE protocol mode.

XAUI Mode

The transmit state machine translates the XAUI XGMII code group to the XAUI PCS code group. Table 2–3 shows the code conversion.

Table 2–3. Code Conversion

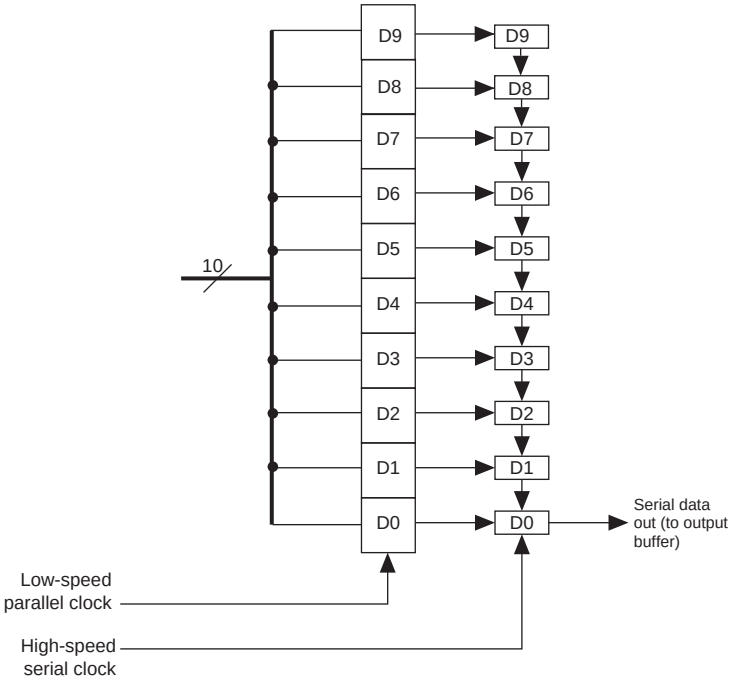
XGMII TXC	XGMII TXD	PCS Code-Group	Description
0	00 through FF	Dxx.y	Normal data
1	07	K28.0 or K28.3 or K28.5	Idle in ||**I**||
1	07	K28.5	Idle in ||**T**||
1	9C	K28.4	Sequence
1	FB	K27.7	Start
1	FD	K29.7	Terminate
1	FE	K30.7	Error
1	See IEEE 802.3 reserved code groups	See IEEE 802.3 reserved code groups	Reserved code groups
1	Other value	K30.7	Invalid XGMII character

The XAUI PCS idle code groups, `/K28.0/` (`/R/`) and `/K28.5/` (`/K/`), are automatically randomized based on a PRBS7 pattern with an x^7+x^6+1 polynomial. The `/K28.3/` (`/A/`) code group is automatically generated between 16 and 31 idle code groups. The idle randomization on the `/A/`, `/K/`, and `/R/` code groups are done automatically by the transmit state machine.

Serializer (Parallel-to-Serial Converter)

The serializer converts the parallel 8-bit or 10-bit data into a serial stream, transmitting the LSB first. The serialized stream is then fed to the transmit buffer. Figure 2–5 is a diagram of the serializer.

Figure 2–5. Serializer

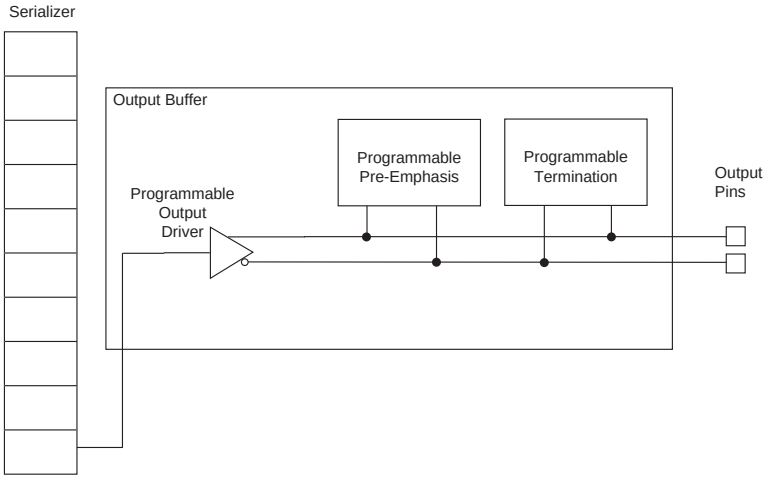


Transmit Buffer

The Stratix GX transceiver buffers support the 1.5-V pseudo current mode logic (PCML) I/O standard at a rate up to 3.1875 Gbps, across up to 40 inches of FR4 trace, and across 2 connectors. Additional I/O standards, LVDS, 3.3-V PCML, LVPECL, can be supported when AC coupled. The common mode of the output driver is 750 mV.

The output buffer, as shown in Figure 2–6, consists of a programmable output driver and a programmable pre-emphasis circuit.

Figure 2–6. Output Buffer



Programmable Output Driver

The programmable output driver can be set to drive out 400 to 1,600 mV. Table 2–4 shows the available settings for each termination value. The V_{OD} can be dynamically or statically set. The output driver requires either internal or external termination at the source.

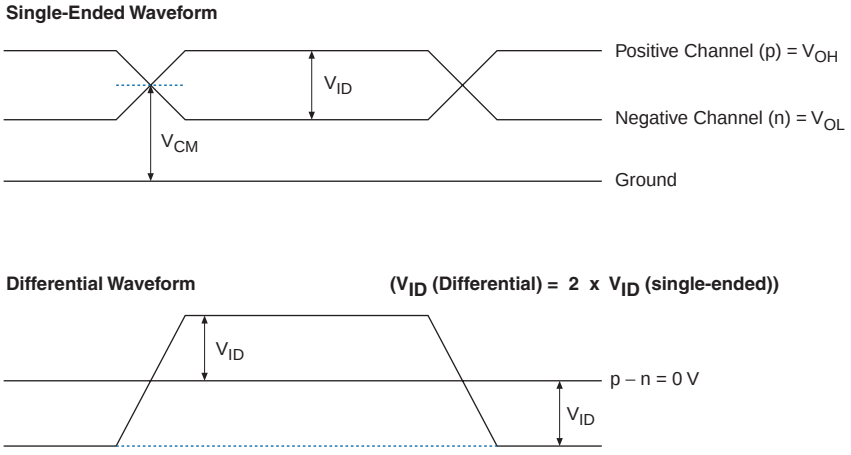
Table 2–4. Programmable V_{OD} (Differential) *Note (1)*

Termination Setting (Ω)	V_{OD} Setting (mV)
100	400, 800, 1000, 1200, 1400, 1600
120	480, 960, 1200, 1440
150	600, 1200, 1500

Note to Table 2–4:

(1) V_{OD} differential is measured as $V_A - V_B$ (see Figure 2–7).

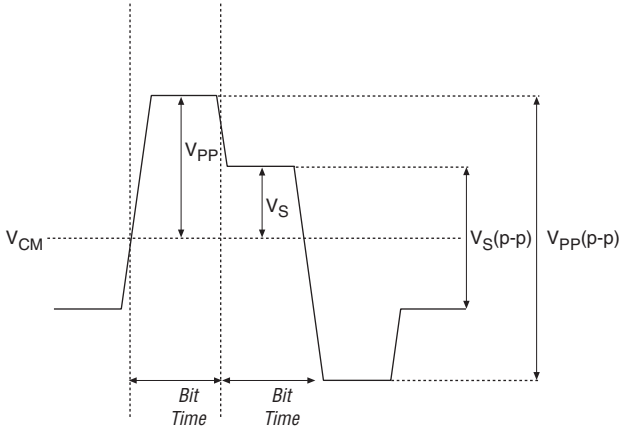
Figure 2–7. V_{OD} Differential



Programmable Pre-Emphasis

The programmable pre-emphasis module controls the output driver to boost the high frequency components, to compensate for losses in the transmission medium, as shown in Figure 2–8. The pre-emphasis can be dynamically or statically set. There are five possible pre-emphasis settings (1 through 5), with 5 being the highest and 0 being no pre-emphasis.

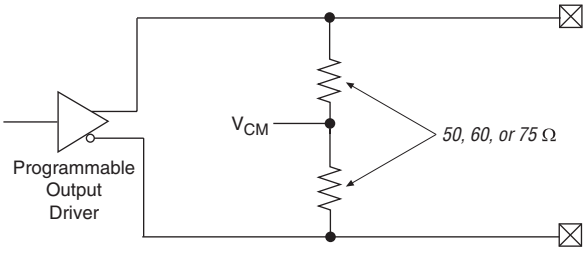
Figure 2–8. Programmable Pre-Emphasis Model



Pre-emphasis percentage is defined as $V_{PP}/V_S - 1$, where V_{PP} is the differential emphasized voltage (peak-to-peak) and V_S is the differential steady-state voltage (peak-to-peak).

Programmable Transmitter Termination
The programmable termination can be statically set in the Quartus II software. The values are 100 Ω, 120 Ω, 150 Ω, and off. Figure 2–9 shows the setup for programmable termination.

Figure 2–9. Programmable Transmitter Termination



Receiver Path

This section describes the data path through the Stratix GX receiver (refer to Figure 2–2 on page 2–4). Data travels through the Stratix GX receiver via the following modules:

- Input buffer
- Clock Recovery Unit (CRU)
- Deserializer
- Pattern detector and word aligner
- Rate matcher and channel aligner
- 8B/10B decoder
- Receiver logic array interface

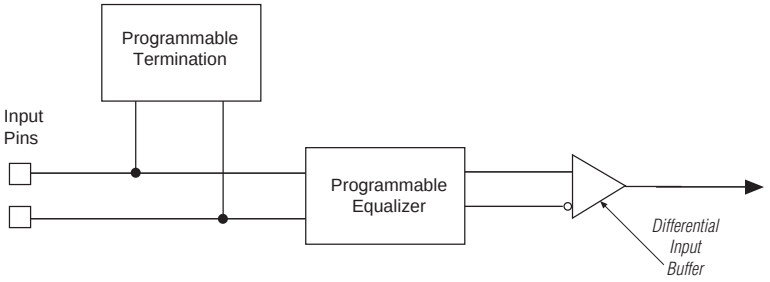
Receiver Input Buffer

The Stratix GX receiver input buffer supports the 1.5-V PCML I/O standard at a rate up to 3.1875 Gbps. Additional I/O standards, LVDS, 3.3-V PCML, and LVPECL can be supported when AC coupled. The common mode of the input buffer is 1.1 V. The receiver can support Stratix GX-to-Stratix GX DC coupling.

Figure 2–10 shows a diagram of the receiver input buffer, which contains:

- Programmable termination
- Programmable equalizer

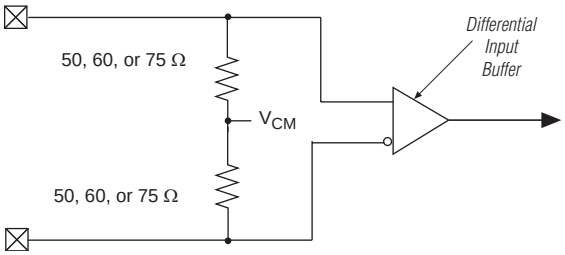
Figure 2–10. Receiver Input Buffer



Programmable Termination

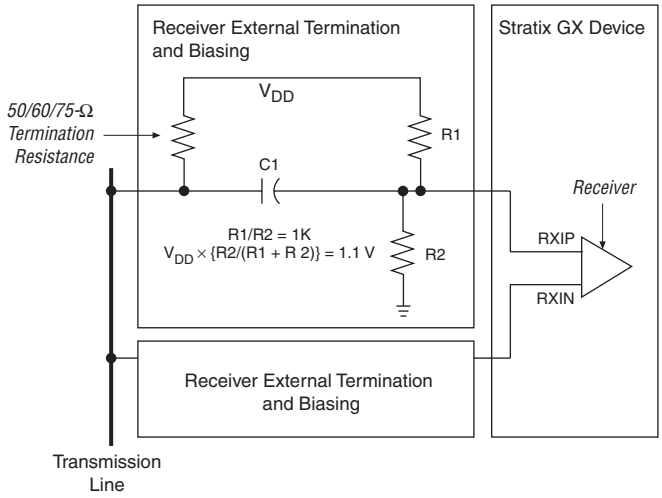
The programmable termination can be statically set in the Quartus II software. Figure 2–11 shows the setup for programmable receiver termination.

Figure 2–11. Programmable Receiver Termination



If you use external termination, then the receiver must be externally terminated and biased to 1.1 V. Figure 2–12 shows an example of an external termination/biasing circuit.

Figure 2–12. External Termination & Biasing Circuit



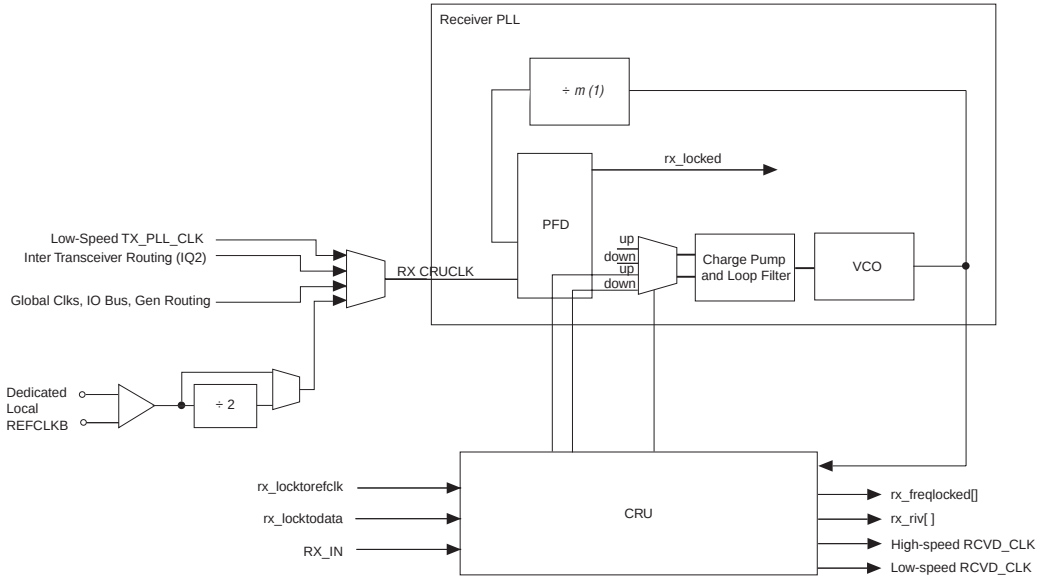
Programmable Equalizer

The programmable equalizer module boosts the high frequency components of the incoming signal to compensate for losses in the transmission medium. There are five possible equalization settings (0, 1, 2, 3, 4) to compensate for 0", 10", 20", 30", and 40" of FR4 trace. These settings should be interpreted loosely. The programmable equalizer can be set dynamically or statically.

Receiver PLL & CRU

Each transceiver block has four receiver PLLs and CRUs, each of which is dedicated to a receive channel. If the receive channel associated with a particular receiver PLL or CRU is not used, then the receiver PLL or CRU is powered down for the channel. Figure 2–13 is a diagram of the receiver PLL and CRU circuits.

Figure 2–13. Receiver PLL & CRU Circuit



Note to Figure 2–13:
(1) m = 8, 10 16, or 20.

The receiver PLLs and CRUs are capable of supporting up to 3.1875 Gbps. The input clock frequency for –5 and –6 speed grade devices is limited to 650 MHz if you use the REFCLKB pin or 325 MHz if you use the other clock routing resources. The maximum input clock frequency for –7 speed grade devices is 312.5 MHz if you use the REFCLKB pin or 156.25 MHz with the other clock routing resources. An optional RX_LOCKED port (active low signal) is available to indicate whether the PLL is locked to the reference clock. The receiver PLL has a programmable loop bandwidth, which can be set to low, medium, or high. The loop bandwidth parameter can be statically set by the Quartus II software.

Table 2–5 lists the adjustable parameters of the receiver PLL and CRU. All the parameters listed are statically programmable in the Quartus II software.

Table 2–5. Receiver PLL & CRU Adjustable Parameters (Part 1 of 2)

Parameter	Specifications
Input reference frequency range	25 MHz to 650 MHz
Data rate support	500 Mbps to 3.1875 Gbps

Table 2–5. Receiver PLL & CRU Adjustable Parameters (Part 2 of 2)	
Multiplication factor (W)	2, 4, 5, 8, 10, 16, or 20 *(1)*
PPM detector	125, 250, 500, 1,000
Bandwidth	Low, medium, high
Run length detector	10-bit or 20-bit mode: 5 to 160 in steps of 5
	8-bit or 16-bit mode: 4 to 128 in steps of 4

Note to Table 2–5:

(1) Multiplication factors 2, 4, and 5 can only be achieved with the use of the pre-divider on the REFCLKB port or if the CRU is trained with the low speed clock from the transmitter PLL.

The CRU has a built-in switchover circuit to select whether the voltage-controlled oscillator of the PLL is trained by the reference clock or the data. The optional port `rx_freqlocked` monitors when the CRU is in locked to data mode.

In the automatic mode, the following conditions must be met for the CRU to switch from locked to reference to locked to data mode:

- The CRU PLL is within the prescribed PPM frequency threshold setting (125 PPM, 250 PPM, 500 PPM, 1,000 PPM) of the CRU reference clock.
- The reference clock and CRU PLL output are phase matched (phases are within .08 UI).

The automatic switchover circuit can be overridden by using the optional ports `rx_lockedtorefclk` and `rx_locktodata`. Table 2–6 shows the possible combinations of these two signals.

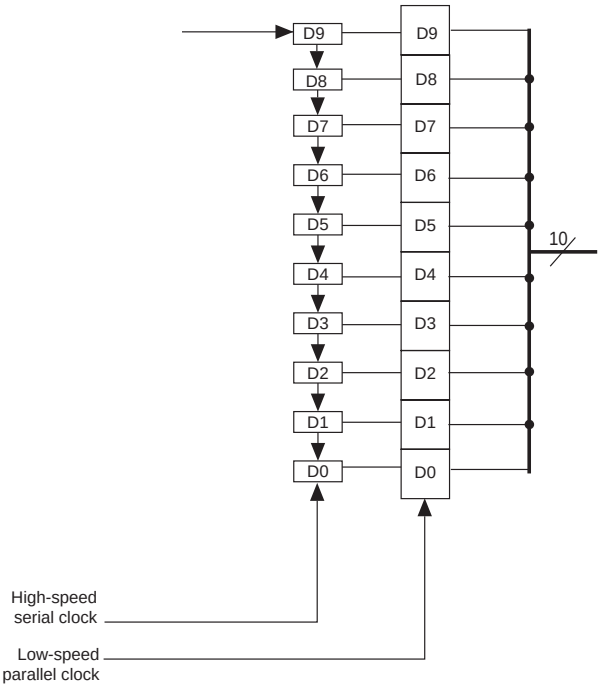
Table 2–6. Possible Combinations of rx_lockedtorefclk & rx_locktodata		
rx_locktodata	**rx_lockedtorefclk**	**VCO (lock to mode)**
0	0	Auto
0	1	Reference CLK
1	x	DATA

If the `rx_lockedtorefclk` and `rx_locktodata` ports are not used, the default is auto mode.

Deserializer (Serial-to-Parallel Converter)

The deserializer converts the serial stream into a parallel 8- or 10-bit data bus. The deserializer receives the least significant bit first. Figure 2–14 is a diagram of the deserializer.

Figure 2–14. Deserializer

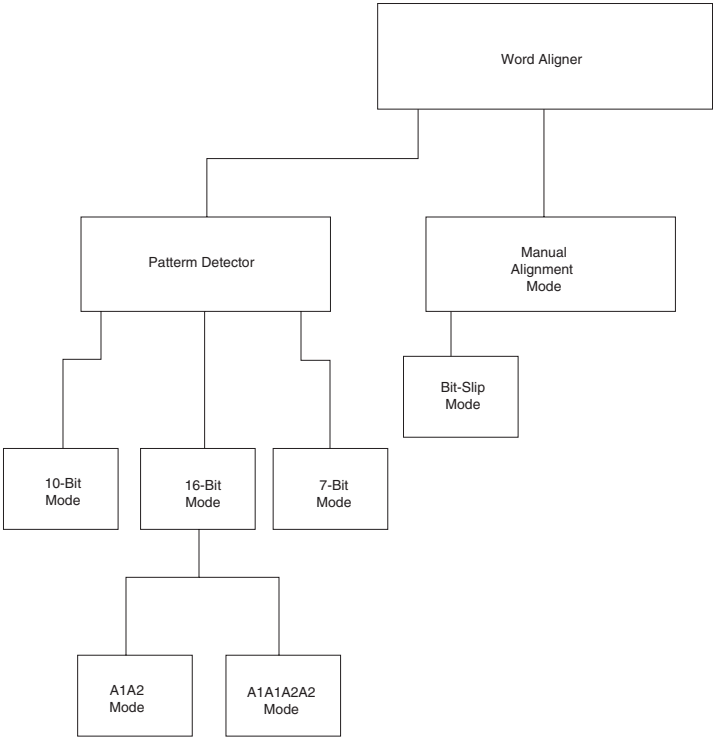


Word Aligner

The word aligner aligns the incoming data based on the specific byte boundaries. The word aligner has three customizable modes of operation: bit-slip mode, 16-bit mode, and 10-bit mode, the last of which is available for the basic and SONET modes. The word aligner also has two non-customizable modes of operation, which are the XAUI and GIGE modes.

Figure 2–15 shows the word aligner in bit-slip mode.

Figure 2–15. Word Aligner in Bit-Slip Mode



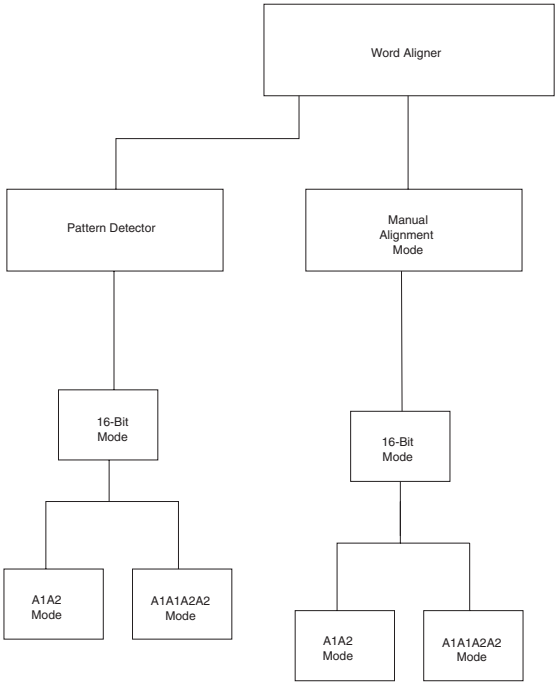
In the bit-slip mode, the byte boundary can be modified by a barrel shifter to slip the byte boundary one bit at a time via a user-controlled bit-slip port. The bit-slip mode supports both 8-bit and 10-bit data paths operating in a single or double-width mode.

The pattern detector is active in the bit-slip mode, and it detects the user-defined pattern that is specified in the MegaWizard® Plug-In Manager.

The bit-slip mode is available only in Custom mode and SONET mode.

Figure 2–16 shows the word aligner in 16-bit mode.

Figure 2–16. Word Aligner in 16-Bit Mode

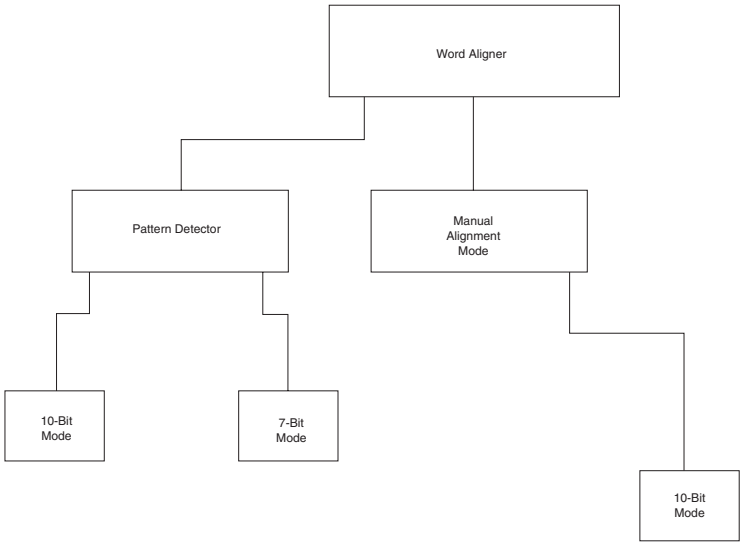


In the 16-bit mode, the word aligner and pattern detector automatically aligns and detects a user-defined 16-bit alignment pattern. This pattern can be in the format of A1A2 or A1A1A2A2 (for the SONET protocol). The re-alignment of the byte boundary can be done via a user-controlled port. The 16-bit mode supports only the 8-bit data path in a single-width or double-width mode.

The 16-bit mode is available only for the Custom mode and SONET mode. The A1A1A2A2 word alignment pattern option is available only for the SONET mode and cannot be used in the Custom mode.

Figure 2–17 shows the word aligner in 10-bit mode.

Figure 2–17. Word Aligner in 10-Bit Mode

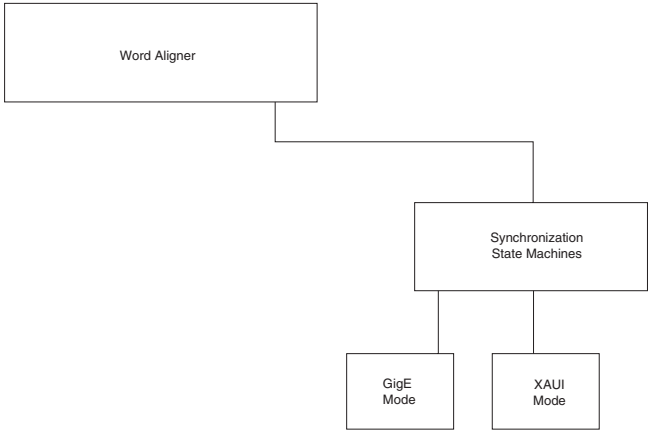


In the 10-bit mode, the word aligner automatically aligns the user's predefined 10-bit alignment pattern. The pattern detector can detect the full 10-bit pattern or only the lower seven bits of the pattern. The word aligner and pattern detector detect both the positive and the negative disparity of the pattern. A user-controlled enable port is available for the word aligner.

The 10-bit mode is available only for the Custom mode.

Figure 2–18 shows the word aligner in XAUI mode.

Figure 2–18. Word Aligner in XAUI Mode



In the XAUI and GIGE modes, the word alignment is controlled by a state machine that adheres to the IEEE 802.3ae standard for XAUI and the IEEE 802.3 standard for GIGE. The alignment pattern is predefined to be a /K28.5/ code group.

The XAUI mode is available only for the XAUI protocol, and the GIGE mode is available only for the GIGE protocol.

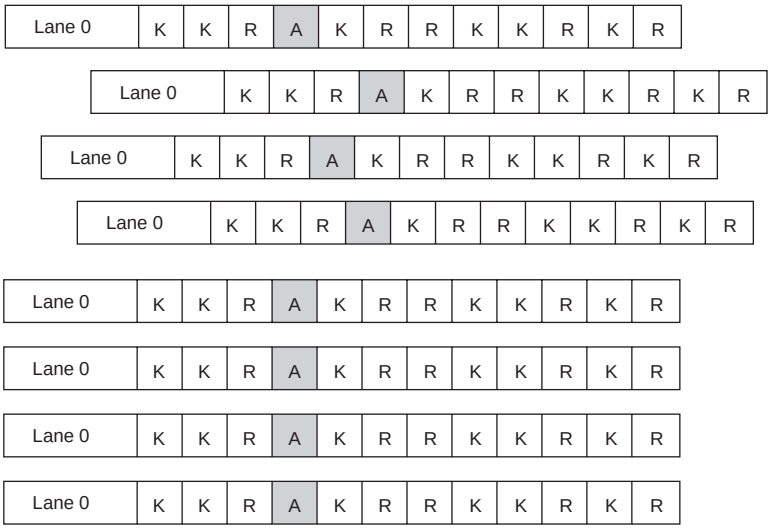
Channel Aligner

The channel aligner is available only in XAUI mode and bonds all four channels within a transceiver. The channel aligner adheres to the IEEE 802.3ae, clause 48 specification for channel bonding.

The channel aligner is a 16-word deep FIFO buffer with a state machine overlooking the channel bonding process. The state machine looks for an /A/ (/K28.3/) in each channel and aligns all the /A/s in the transceiver. When four columns of /A/ (denoted by //A//) are detected, the rx_channelalign port goes high, signifying that all the channels in the transceiver have been bonded. The reception of four consecutive misaligned /A/s restarts the channel alignment sequence and de-asserts rx_channelalign.

Figure 2–19 shows misaligned channels before the channel aligner and the channel alignment after the channel aligner.

Figure 2–19. Before & After the Channel Aligner



Rate Matcher

The rate matcher, which is available only in XAUI and GIGE modes, consists of a 12-word deep FIFO buffer and a FIFO controller. The rate matcher is bypassed when the device is not in XAUI or GIGE mode.

In a multi-crystal environment, the rate matcher compensates for up to a 100-ppm difference between the source and receiver clocks.

GIGE Mode

In the GIGE mode, the rate matcher adheres to the specifications in clause 36 of the IEEE 802.3 documentation, for idle additions or removals. The rate matcher performs clock compensation only on `/I2/` ordered sets, composing a `/K28.5/+` followed by a `/D16.2/-`. The rate matcher does not perform a clock compensation on any other ordered set combinations. An /I2/ is added or deleted automatically based on the number of words in the FIFO buffer. A `9'h19C` is given at the control and data ports when the FIFO is in an overflow or underflow condition.

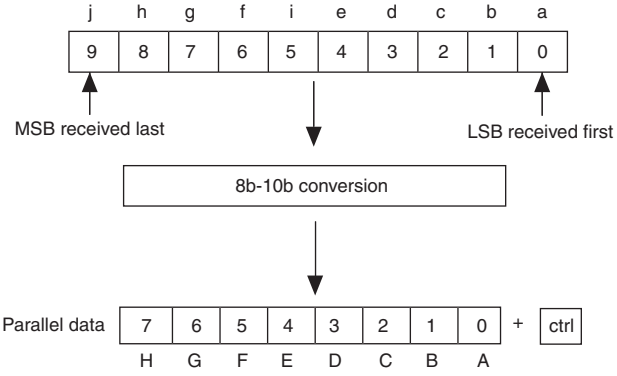
XAUI Mode

In XAUI mode, the rate matcher adheres to clause 48 of the IEEE 802.3ae specification for clock rate compensation. The rate matcher performs clock compensation on columns of /R/ (/K28.0/), denoted by //R//. An //R// is added or deleted automatically based on the number of words in the FIFO buffer.

8B/10B Decoder

The 8B/10B decoder converts the 10-bit encoded code group into 8-bit data and 1 control bit. The 8B/10B decoder can be bypassed. The following is a diagram of the conversion from a 10-bit encoded code group into 8-bit data + 1-bit control.

Figure 2–20. 8B/10B Decoder Conversion



There are two optional error status ports available in the 8B/10B decoder, rx_errdetect and rx_disperr. Table 2–7 shows the values of the ports from a given error. These status signals are aligned with the code group in which the error occurred.

Table 2–7. Error Signal Values

Types of Errors	rx_errdetect	rx_disperr
No errors	1'b0	1'b0
Invalid code groups	1'b1	1'b0
Disparity errors	1'b1	1'b1

Receiver State Machine

The receiver state machine operates in GIGE and XAUI modes. In GIGE mode, the receiver state machine replaces invalid code groups with `9'h1FE`. In XAUI mode, the receiver state machine translates the XAUI PCS code group to the XAUI XGMII code group. Table 2–8 shows the code conversion. The conversion adheres to the IEEE 802.3ae specification.

Table 2–8. Code Conversion

XGMII RXC	XGMII RXD	PCS code-group	Description
0	00 through FF	Dxx.y	Normal Data
1	07	K28.0 or K28.3 or K28.5	Idle in ||**I**||
1	07	K28.5	Idle in ||**T**||
1	9C	K28.4	Sequence
1	FB	K27.7	Start
1	FD	K29.7	Terminate
1	FE	K30.7	Error
1	FE	Invalid code group	Invalid XGMII character
1	See IEEE 802.3 reserved code groups	See IEEE 802.3 reserved code groups	Reserved code groups

Byte Deserializer

The byte deserializer takes a single width word (8 or 10 bits) from the transceiver logic and converts it into double-width words (16 or 20 bits) to the phase compensation FIFO buffer. The byte deserializer is bypassed when single width mode (8 or 10 bits) is used at the PLD interface.

Phase Compensation FIFO Buffer

The receiver phase compensation FIFO buffer resides in the transceiver block at the programmable logic device (PLD) boundary. This buffer compensates for the phase difference between the recovered clock within the transceiver and the recovered clock after it has transferred to the PLD core. The phase compensation FIFO buffer is four words deep and cannot be bypassed.

Loopback Modes

The Stratix GX transceiver has built-in loopback modes to aid in debug and testing. The loopback modes are set in the Stratix GX MegaWizard Plug-In Manager in the Quartus II software. Only one loopback mode can be set at any single instance of the transceiver block. The loopback mode applies to all used channels in a transceiver block.

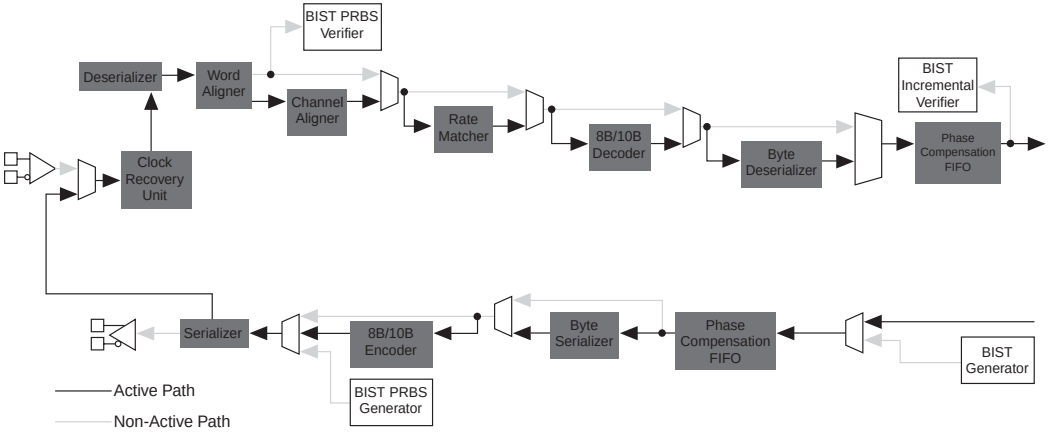
The available loopback modes are:

- Serial loopback
- Parallel loopback
- Reverse serial loopback

Serial Loopback

Serial loopback exercises all the transceiver logic except for the output buffer and input buffer. The loopback function is dynamically switchable through the `rx_slpbk` port on a channel by channel basis. The V_{OD} of the output reduced. If you select 400 mV, the output is tri-stated when the serial loopback option is selected. Figure 2–21 shows the data path in serial loopback mode.

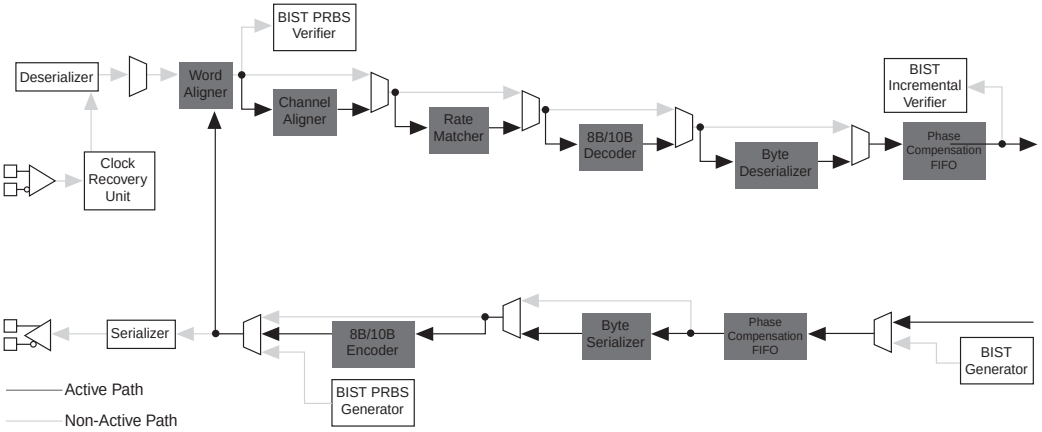
Figure 2–21. Data Path in Serial Loopback Mode



Parallel Loopback

The parallel loopback mode exercises the digital logic portion of the transceiver data path. The analog portions are not use in the loopback path. The received data is not retimed. Figure 2–22 shows the data path in parallel loopback mode. This option is not dynamically switchable. Reception of an external signal is not possible in this mode.

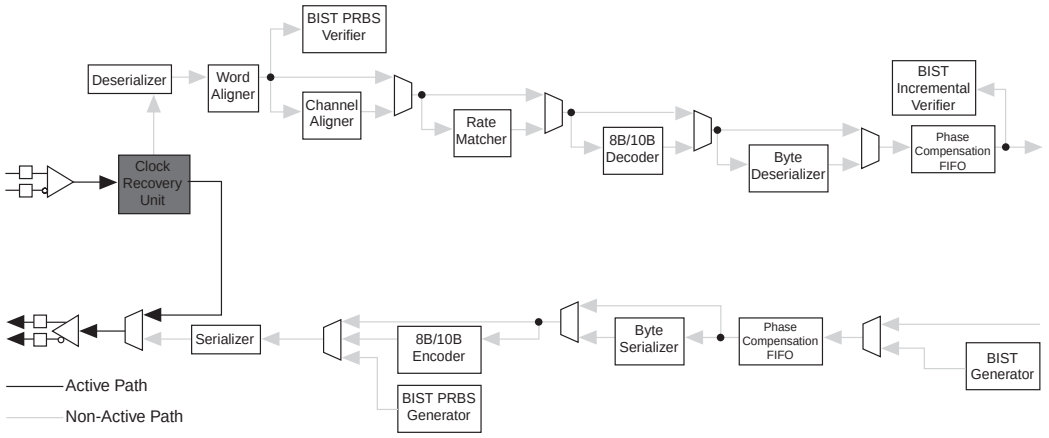
Figure 2–22. Data Path in Parallel Loopback Mode



Reverse Serial Loopback

The reverse serial loopback exercises the analog portion of the transceiver. This loopback mode is dynamically switchable through the `tx_srlpbk` port on a channel by channel basis. Asserting `rxanalogreset` in reverse serial loopback mode powers down the receiver buffer and CRU, preventing data loopback. Figure 2–23 shows the data path in reverse serial loopback mode.

Figure 2–23. Data Path in Reverse Serial Loopback Mode



BIST (Built-In Self Test)

The Stratix GX transceiver has built-in self test modes to aid in debug and testing. The BIST modes are set in the Stratix GX MegaWizard Plug-In Manager in the Quartus II software. Only one BIST mode can be set for any single instance of the transceiver block. The BIST mode applies to all channels used in a transceiver.

The following is a list of the available BIST modes:

- PRBS generator and verifier
- Incremental mode generator and verifier
- High-frequency generator
- Low-frequency generator
- Mixed-frequency generator

Figures 2–24 and 2–25 are diagrams of the BIST PRBS data path and the BIST incremental data path, respectively.

Figure 2–24. BIST PRBS Data Path

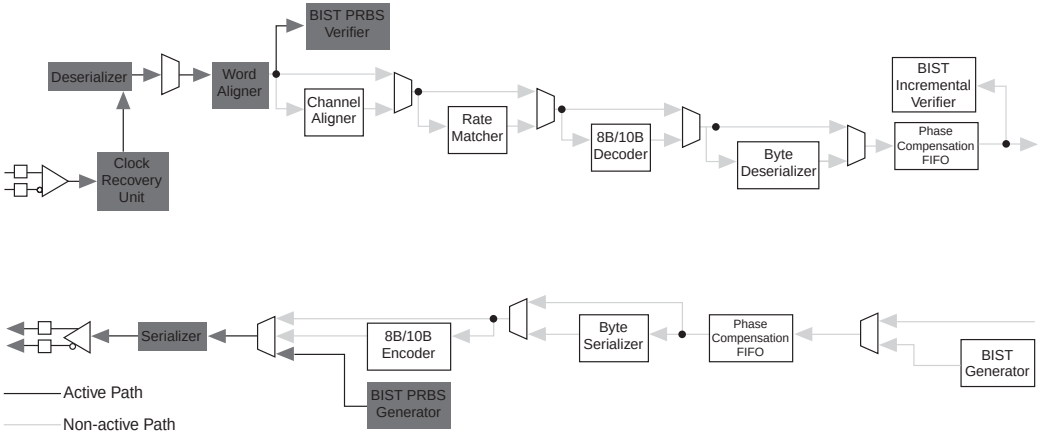


Figure 2–25. BIST Incremental Data Path

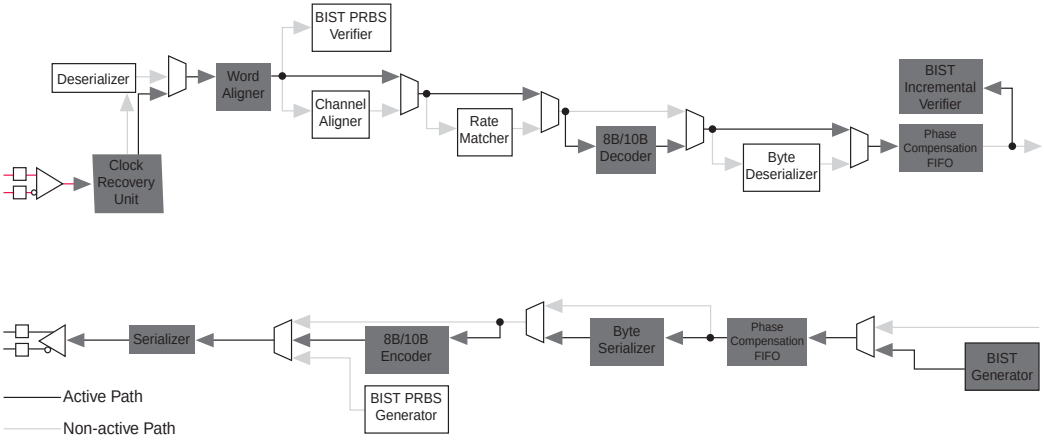


Table 2–9 shows the BIST data output and verifier alignment pattern.

Table 2–9. BIST Data Output & Verifier Alignment Pattern (Part 1 of 2)

BIST Mode	Output	Polynomials	Verifier Word Alignment Pattern
PRBS 8-bit	$2^8 - 1$	$x^8 + x^7 + x^5 + x^3 + 1$	1000000011111111
PRBS 10-bit	$2^{10} - 1$	$x^{10} + x^7 + 1$	1111111111

Table 2–9. BIST Data Output & Verifier Alignment Pattern (Part 2 of 2)

BIST Mode	Output	Polynomials	Verifier Word Alignment Pattern
PRBS 16-bit	$2^8 - 1$	$x^8 + x^7 + x^5 + x^3 + 1$	1000000011111111
PRBS 20-bit	$2^{10} - 1$	$x^{10} + x^7 + 1$	1111111111
Incremental 10-bit	K28.5, K27.7, Data (00-FF incremental), K28.0, K28.1, K28.2, K28.3, K28.4, K28.6, K28.7, K23.7, K30.7, K29.7 *(1)*		0101111100 (K28.5)
Incremental 20-bit	K28.5, K27.7, Data (00-FF incremental), K28.0, K28.1, K28.2, K28.3, K28.4, K28.6, K28.7, K23.7, K30.7, K29.7 *(1)*		0101111100 (K28.5)
High frequency	1010101010		
Low frequency	0011111000		
Mixed frequency	0011111010 or 1100000101		

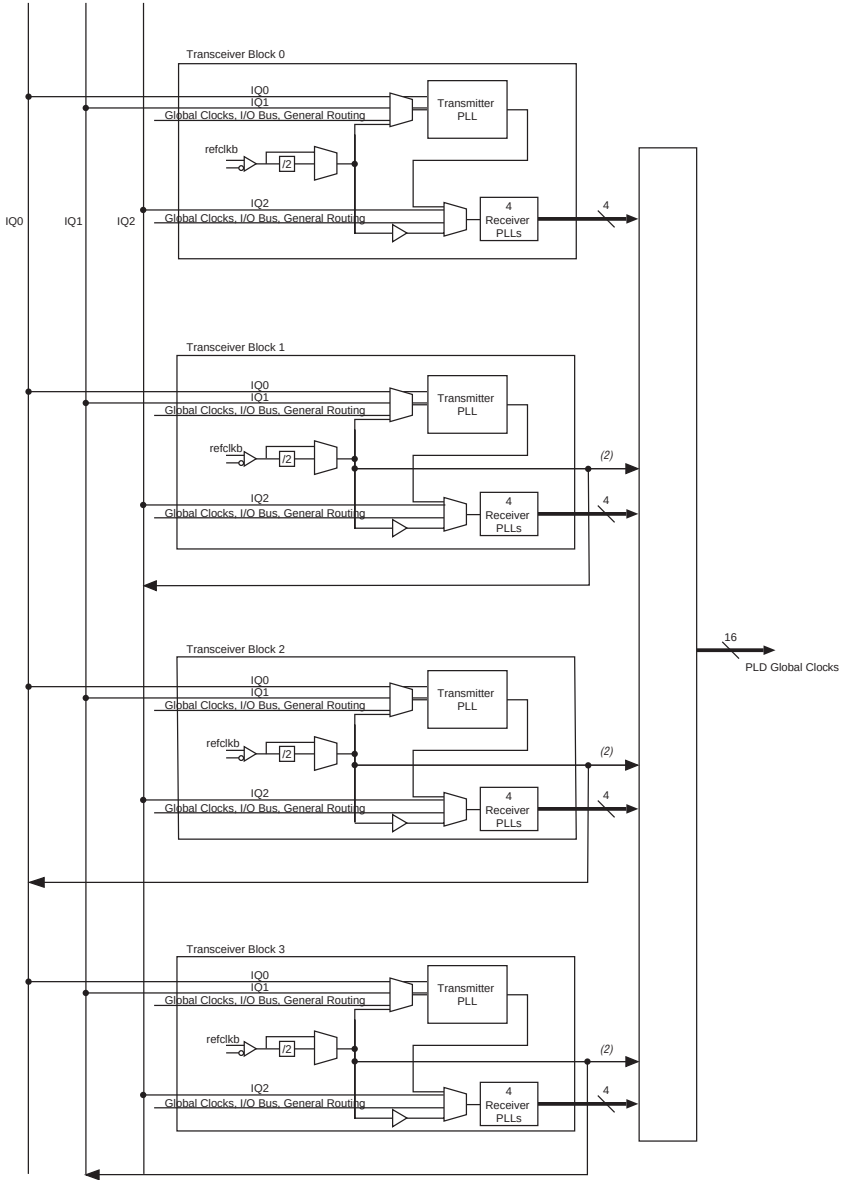
Note to Table 2–9:
(1) This output repeats.

Stratix GX Clocking

The Stratix GX global clock can be driven by certain REFCLKB pins, all transmitter PLL outputs, and all receiver PLL outputs. The REFCLKB pins (except for transceiver block 0 and transceiver block 4) can drive inter-transceiver and global clock lines as well as feed the transmitter and receiver PLLs. The output of the transmitter PLL can only feed global clock lines and the reference clock port of the receiver PLL.

Figures 2–26 and 2–27 are diagrams of the Inter-Transceiver line connections as well as the global clock connections for the EP1SGX25F and EP1SGX40G devices. For devices with fewer transceivers, ignore the information about the unavailable transceiver blocks.

Figure 2–26. EP1SGX25F Device Inter-Transceiver & Global Clock Connections *Note (1)*



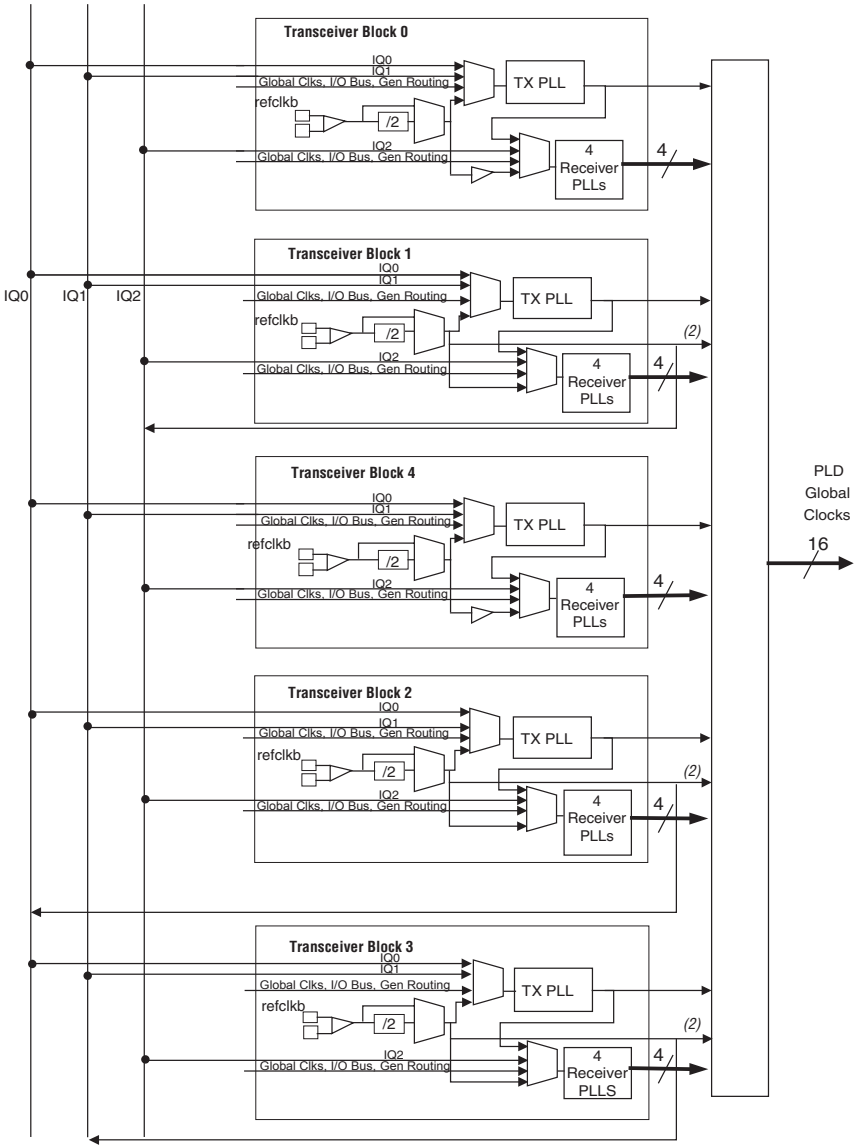
Notes to Figure 2–26:

(1) IQ lines are inter-transceiver block lines.

(2) If the /2 pre-divider is used, the path to drive the PLD logic array, local, or global clocks is not allowed.

(3) There are four receiver PLLs in each transceiver block.

Figure 2–27. EP1SGX40G Device Inter-Transceiver & Global Clock Connections *Note (1)*



Notes to Figure 2–27:

(1) IQ lines are inter-transceiver block lines.

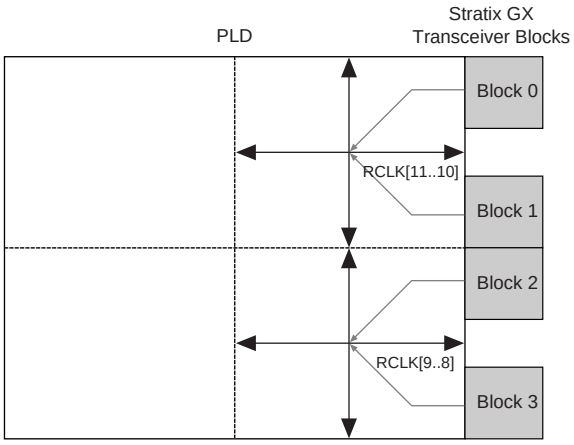
(2) If the /2 pre-divider is used, the path to drive the PLD logic array, local, or global clocks is not allowed.

(3) There are four receiver PLLs in each transceiver block.

The receiver PLL can also drive the fast regional, regional clocks, and local routing adjacent to the associated transceiver block. Figures 2–28 through 2–31 show which fast regional and regional clock resource can be used by the recovered clock.

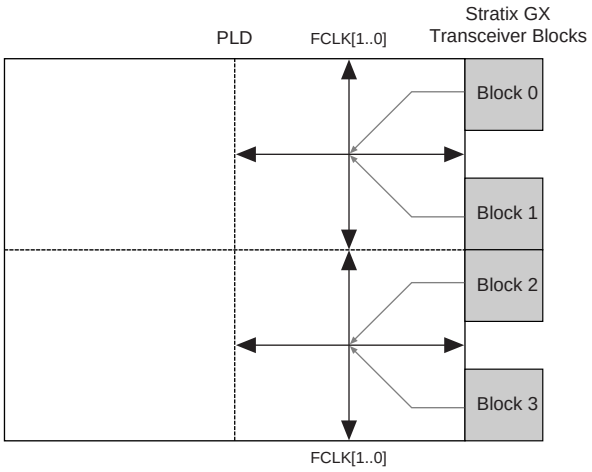
In the EP1SGX25 device, the receiver PLL recovered clocks from transceiver blocks 0 and 1 drive `RCLK[1..0]` while transceiver blocks 2 and 3 drive `RCLK[7..6]`. The regional clocks feed logic in their associated regions.

Figure 2–28. EP1SGX25 Receiver PLL Recovered Clock to Regional Clock Connection



In addition, the receiver PLL's recovered clocks can drive fast regional lines (`FCLK`) as shown Figure 2–29. The fast regional clocks can feed logic in their associated regions.

Figure 2–29. EP1SGX25 Receiver PLL Recovered Clock to Fast Regional Clock Connection



In the EP1SGX40 device, the receiver PLL recovered clocks from transceivers 0 and 1 drive `RCLK[1..0]` while transceivers 2, 3, and 4 drive `RCLK[7..6]`. The regional clocks feed logic in their associated regions.

Figure 2–30. EP1SGX40 Receiver PLL Recovered Clock to Regional Clock Connection

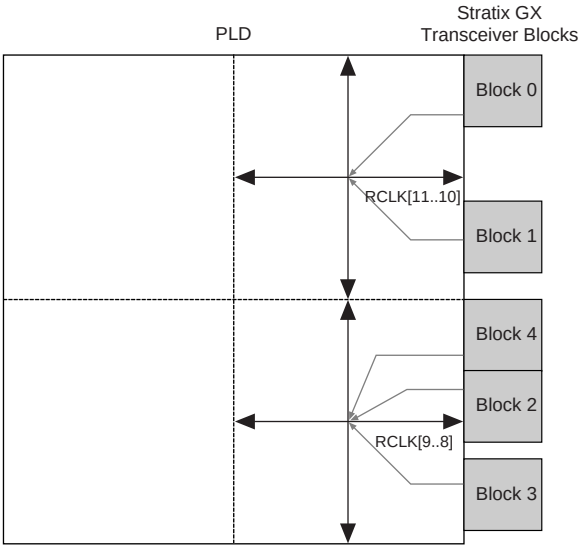


Figure 2–31 shows the possible recovered clock connection to the fast regional clock resource. The fast regional clocks can drive logic in their associated regions.

Figure 2–31. EP1SGX40 Receiver PLL Recovered Clock to Fast Regional Clock Connection

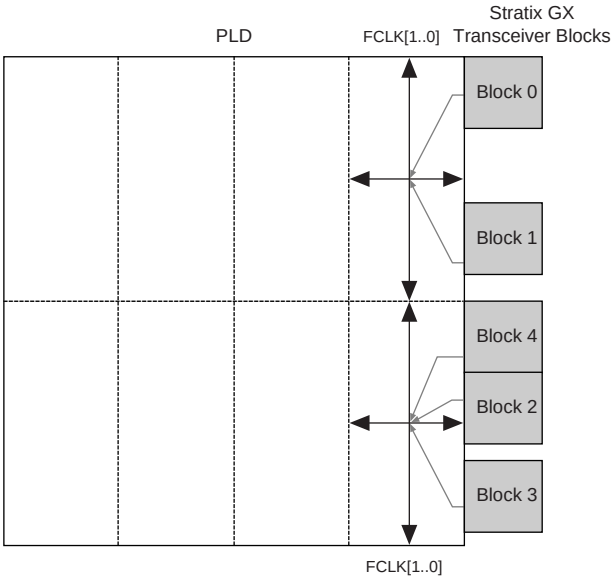


Table 2–10 summarizes the possible clocking connections for the transceivers.

Table 2–10. Possible Clocking Connections for Transceivers (Part 1 of 2)

Source	Destination					
	Transmitter PLL	Receiver PLL	GCLK	RCLK	FCLK	IQ Lines
REFCLKB	✓	✓	✓ *(1)*	✓		✓ *(1)*
Transmitter PLL		✓	✓	✓	✓	
Receiver PLL			✓	✓	✓	
GCLK	✓	✓				
RCLK	✓	✓				
FCLK	✓	✓				

Table 2–10. Possible Clocking Connections for Transceivers (Part 2 of 2)

Source	Destination					
	Transmitter PLL	Receiver PLL	GCLK	RCLK	FCLK	IQ Lines
IQ lines	✓ (2)	✓ (2)				

Notes to Table 2–10:

(1) REFCLKB from transceiver block 0 and transceiver block 4 does not drive the inter-transceiver lines or the GCLK lines.

(2) Inter-transceiver line 0 and inter-transceiver line 1 drive the transmitter PLL, while inter-transceiver line 2 drives the receiver PLLs.

Other Transceiver Features

Other important features of the Stratix GX transceivers are the power down and reset capabilities, the external voltage reference and bias circuitry, and hot swapping.

Individual Power-Down & Reset for the Transmitter & Receiver

Stratix GX transceivers offer a power saving advantage with their ability to shut off functions that are not needed. The device can individually reset the receiver and transmitter blocks and the PLLs. The Stratix GX device can either globally power down and reset the transmitter and receiver channels or do each channel separately. Table 2–11 shows the connectivity between the reset signals and the Stratix GX logical blocks.

Power-down functions are static, in other words., they are implemented upon device configuration and programmed, through the Quartus II software, to static values. Resets can be static as well as dynamic inputs coming from the logic array or pins.

Table 2–11. Reset Signal Map to Stratix GX Blocks

Reset Signal	Transmitter Phase Compensation FIFO Module/ Byte Serializer	Transmitter 8B/10B Encoder	Transmitter Serializer	Transmitter Analog Circuits	Transmitter PLL	Transmitter XAUI State Machine	Transmitter Analog Circuits	BIST Generators	Receiver Deserializer	Receiver Word Aligner	Receiver Deskew FIFO Module	Receiver Rate Matcher	Receiver 8B/10B Decoder	Receiver Phase Comp FIFO Module/ Byte Deserializer	Receiver PLL / CRU	Receiver XAUI State Machine	BIST Verifiers	Receiver Analog Circuits
rxdigitalreset										✓	✓	✓	✓	✓		✓	✓	
rxanalogreset									✓						✓			✓
txdigitalreset	✓	✓				✓		✓										
pll_areset	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
pllenable	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

Voltage Reference Capabilities

Stratix GX transceivers provide voltage reference and bias circuitry. To set-up internal bias for controlling the transmitter output drivers' voltage swing—as well as to provide voltage/current biasing for other analog circuitry—use the internal bandgap voltage reference at 0.7 V. To provide bias for internal pull-up PMOS resistors for I/O termination at the serial interface of receiver and transmitter channels (independent of power supply drift, process changes, or temperature variation) an external resistor, which is connected to the external low voltage power supply, is

accurately tracked by the internal bias circuit. Moreover, the reference voltage and internal resistor bias current is generated and replicated to the analog circuitry in each channel.

Hot-Socketing Capabilities

Each Stratix GX device is capable of hot-socketing. Because Stratix GX devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. Signals can be driven into Stratix GX devices before and during power-up without damaging the device. Once operating conditions are reached and the device is configured, Stratix GX devices operate according to your specifications. This feature provides the Stratix GX transceiver line card behavior, so you can insert it into the system without powering the system down, offering more flexibility.

Applications & Protocols Supported with Stratix GX Devices

Each Stratix GX transceiver block is designed to operate at any serial bit rate from 500 Mbps to 3.1875 Gbps per channel. The wide, data rate range allows Stratix GX transceivers to support a wide variety of standard and future protocols such as 10-Gigabit Ethernet XAUI, InfiniBand, Fibre Channel, and Serial RapidIO. Stratix GX devices are ideal for many high-speed communication applications such as high-speed backplanes, chip-to-chip bridges, and high-speed serial communications standards support.

Stratix GX Example Application Support

Stratix GX devices can be used for many applications, including:

- Backplanes for traffic management and quality of service (QOS)
- Switch fabric applications for complete set for backplane and switch fabric transceivers
- Chip-to-chip applications such as: 10 Gigabit Ethernet XAUI to XGMII bridge, 10 Gigabit Ethernet XGMII to POS-PHY4 bridge, POS-PHY4 to NPSI bridge, or NPSI to backplane bridge

High-Speed Serial Bus Protocols

With wide, serial data rate range, Stratix GX devices can support multiple, high-speed serial bus protocols. Table 2–12 shows some of the protocols that Stratix GX devices can support.

Table 2–12. High-Speed Serial Bus Protocols

Bus Transfer Protocol	Stratix GX (Gbps) (Supports up to 3.1875 Gbps)
SONET backplane	2.488
10 Gigabit Ethernet XAUI	3.125
10 Gigabit fibre channel	3.1875
InfiniBand	2.5
Fibre channel (1G, 2G)	1.0625, 2.125
Serial RapidIO™	1.25, 2.5, 3.125
PCI Express	2.5
SMPTE 292M	1.485