Simulating Altera Devices with IBIS Models

Introduction

High-performance systems that involve complex clock trees or high-data rates tightly constrain design parameters, creating a significant challenge for board designers. Also, because of the short design time and high cost, it is not beneficial to develop a prototype board before the production board is developed. Therefore, the ability to simulate a design before laying out the board has become a critical factor in the success of a project. Designers need device models to perform intensive and accurate board-level simulation.

The input output buffer information specification (IBIS) is a fast and accurate behavioral method of modeling I/O buffers based on the I/V curve data derived from measurement- or SPICE-simulation. The IBIS describes the analog behavior of the digital device's buffers without revealing the device's propriety internal process or architectural information.

Altera IBIS models support multiple voltages, slew rate control, PCI clamp diode, corner cases, different I/O standards and various driver current strength.

This application note provides information regarding the IBIS and characteristics of Altera IBIS models including:

- History of the IBIS
- Advantages of IBIS model simulation
- IBIS file structure
- Required parameters
- Characteristics of Altera IBIS models
- Sample Altera IBIS model
- Sample IBIS simulation results
- Industry support for the IBIS
- IBIS modeling tools

Related Links

- IBIS: www.eigroup.org/ibis/specs.htm
- North Carolina State IBIS cookbook, describes the major steps required to produce IBIS models for digital integrated circuit (IC) input, output, and I/O buffers: www2.ncsu.edu/eos/project/erl_html/ibis/cookbk.html
- Innoveda, a charter member of the IBIS Open Forum Group: www.viewlogic.com/products/datasheets_html/ibis.asp

History of IBIS

The IBIS was developed during the early 1990s by Intel Corporation engineers. The idea was to promote tool-independent I/O models for system-level, signal-integrity analysis.

In May of 1993 a committee of EDA tool vendors, semiconductor vendors, and end-users was formed. Today, the committee is known as the IBIS Open Forum. The IBIS Open Forum proposes updates, organizes summits, and ratifies standards changes. The IBIS standard is supported by almost all signal-integrity simulation engines, including most SPICE-based tools.

There have been two EIA/ANSI standard revisions released along with multiple IBIS revisions. The first release, version 1.0, of the IBIS standard was distributed in April 1993. The most recent revision, version 3.2, was released in 1999; all IBIS revisions are backward compatible.

Version 3.2 provides a multi-driver syntax and definitions of new constructs for bus hold and dynamic clamp devices, as well as the following enhancements:

- Clarification of driver schedule keywords
- Enhanced characterization of receiver thresholds
- Alternate package models
- C_comp refinements
- I ncreased V-T table limit to 100-points
- Clarification of rising & falling timing diagrams
- Timing test loads in [model spec] to support PCI/PCI-X bus protocols
- Accommodating PMOS and NMOS/PMOS Series FET Models

Advantages of IBIS Model Simulation

The advantages of IBIS model simulation over other I/O buffer simulation techniques include the following:

- Intellectual property protection, i.e., by not disclosing the internal circuitry and processes of the device, the semiconductor vendor's proprietary information is protected.
- IBIS model behavior provides faster simulation time than structured models, e.g., SPICE models.

IBIS File Structure

IBIS version 1.1 introduced the baseline architecture suitable for most CMOS and TTL technologies. IBIS version 1.1 includes the following features:

- ASCII file format (**.ibs**) with header information
- Component (pin out) and default package models (e.g., `l_pkg`, `r_pkg`, `c_pkg`)
- Pin-specific model selection (`l_pin`, `r_pin`, `c_pin`)
- Models

- Model type (i.e., input, output, tri-state, I/O, open drain)
- Pull up/down, GND/power clamp I/V tables relative to voltages
- Ramp dV/dt (rising and falling) for defining rising and falling transitions
- `C_comp` parameter for die capacitance
- Typical, minimum, and maximum columns for performance corners
- Defined conditions for temperature and transition loads

IBIS Keywords

At a minimum, a valid IBIS file contains the following data and keywords. Some keywords are required and some are optional. The required keywords are noted with an asterisk (*).

Header Information & End of IBIS File Keywords

The header information and end of the IBIS file are defined by the following keywords:

- `[IBIS Ver]` *
- `[File Name]` *
- `[File Rev]` *
- `[Date]`
- `[Source]`
- `[Notes]`
- `[Disclaimer]`
- `[End]` *

Component & Manufacturer Keywords

One or more components can be defined using the following keywords:

- `[Component]`
- `[Manufacturer]` *

Electrical & Pin-To-Buffer Keywords

The information about the device's electrical characteristics and the pin-to-buffer model mapping (i.e., which pins are connected to which buffer models) is defined using the following keywords:

- `[Package]` * (default `l_pkg`, `r_pkg`, `c_pkg`)
- `[Pin]` *
- `[Diff_pin]` – For differential models only

☞ Because each type of input or output will have its own model, the [Pin] keyword is used to define the correct port model to each pin. Pin number, signal name, model name, l_pin, r_pin, c_pin and reserved words such as GND, POWER, and NC should be used to define the model that is attached to each pin.

Unique Buffer Design Keyword

The data required to model the device's unique input, output, open drain, and I/O buffer design is defined using the following keyword:

■ [Model] *

Voltage & Temperature Keywords

To specify the voltage and temperature range for the process, voltage, and temperature corners, the following keywords are used:

■ [Temperature Range]
■ [Voltage Range] * (If pull up/down, power/GND clamp references are not present)

Five Basic Elements in IBIS Models

The IBIS file format groups corner case descriptions into three columns, i.e., typical, fast, and slow (or typical, minimum, and maximum). The corners are defined with respect to process, temperature, and supply variations.

Buffers are distinguished by their I/V curves and switching characteristics. Buffer I/V curve and switching characteristic information is included in the five basic elements that are required for IBIS modeling. The required keywords are noted with an asterisk (*). The five basic elements are:

■ [Pullup] *
■ [Pulldown] *
■ [GND Clamp] *
■ [Power Clamp] *
■ [Ramp] *, [Rising Waveform], [Falling Waveform]

In most cases, two [Rising Waveform] and [Falling Waveform] tables are necessary for accurate modeling. In one table, the R_fixture of 50 Ω is used with the V_fixture equal to zero. In the other table, the R_fixture of 50 Ω is used with the V_fixture, equal to VCC.

Figure 1 shows the five basic elements in each IBIS model, which are the pull up, pull down, GND clamp, power clamp, and ramp waveforms.

Figure 1. Five Basic Elements in IBIS Models
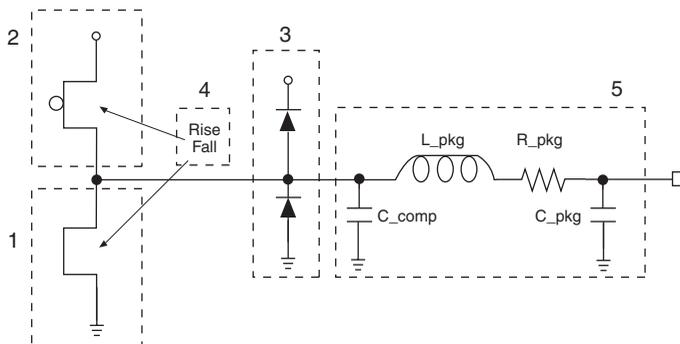
Blocks 1 and 2 show the transistors that are modeled by DC I/V tables under the `[Pullup]` and `[Pulldown]` keywords, which represent the pull up and pull down transistors of a standard TTL, or CMOS I/O buffer output stage.

Block 1 shows the `[Pulldown]` information, including the minimum and maximum currents for the given pull-down voltage. The `[Pulldown]` IBIS table lists voltages from -V_{CC} to 2V_{CC}.

☞   The wide output voltage range (-V_{CC} to 2V_{CC}) provides results when the buffer is subject to undershoot or overshoot.

Block 2 shows the `[Pullup]` information, modeling the characteristics of the buffer when driven high. The voltage range in the pull-up section is -Vcc to Vcc.

Block 3 shows the keywords `[GND_clamp]` and `[Power_clamp]`, which consist of DC I/V tables representing the electrostatic discharge (ESD) or clamping diodes. If the diode is not present in the device, the `[GND_clamp]` and `[Power_clamp]` keywords can be omitted.

The voltage range for `GND_Clamp` is from -V_{CC} to V_{CC}, and for `Power_clamp` the range is from -V_{CC} to GND (using the equation : Vtable= V_{CC}- Voutput).

To ensure that diode characteristics are present even when the output buffer is in high impedance, the clamp diode characteristics are modeled along with the driver information in the pull-up and pull-down section.

☞   The current listed in the IBIS table can be large and is only provided to enable simulators to construct the proper diode curves.

Block 4 shows the [Ramp] keyword, which defines the transition time of the output as it switches from one logic state to another. Rise and fall times are represented separately as non-reduced ratios of transition voltage to transition time: dv/dt.

The minimum column represents the longest and the maximum column represents the shortest rise/fall times.

Block 5 represents the pad and package parasitic seen by the output buffer, which includes the inherent capacitance of the silicon portion of the models (i.e., the die, not the package) as C_comp. The C_comp parameter is the total output capacitance due to the output pad, clamp diodes, and (for I/O structures) input transistors. The L_pkg, R_pkg and C_pkg are the inductance, resistance, and capacitance of the bond wire and pin combination of the package. The table supplies minimum to maximum range for each parameter.

Required Parameters

There are a few required parameters within IBIS models. Some of the required parameters that are supported with Altera IBIS models are described in this section.

Model Types & Corresponding Parameters

There are different model types available in IBIS models, but the most common model types are: input, output, I/O (bi-directional), tri-state, and open_drain. Each model type requires some combination of parameters discussed in this section.

VINH & VINL Parameters

The VINL and VINH parameters are the input voltage threshold low and high, which should be defined for each model type. The values for the VINL and VINH parameters depend on the input or output voltage level, and can be obtained from device's data sheet. For example at 3.3-V LVTTL/LVCMOS, the VINL = 0.8 V and VINH = 2.0 V.

🖙   For input models, only VINL and VINH parameters are required. For other model types (i.e., I/O, output, open_drain, and tri-state), VREF, RREF, and CREF parameters should also be used.

CREF, RREF & VREF Parameters

The CREF and RREF parameters correspond to the test load that the semiconductor vendor uses when specifying the propagation delay or output switching time of the model. VREF corresponds to the test load voltage.

VMEAS Parameter

The VMEAS parameter is the reference voltage level that the semiconductor vendor uses for the model.

C_COMP Parameter

The C_COMP parameter defines the silicon die capacitance without including the capacitance of the package. The C_COMP parameter can only use NA for the minimum and maximum values.

🖙   To run a complete simulation using corner cases, you must enter the type, minimum, and maximum values in the IBIS table. If there are no minimum or maximum values, you should enter NA in the corresponding column(s).

AC Test Load Parameters

There are four parameters (i.e., VMEAS, VREF, RREF, and CREF) within a model that define the timing measurement's AC test load. (The test load parameters must exit for output, tri-state, or I/O model types.) The VREF, RREF, and CREF parameters—which are based on AC test load conditions—allow greater accuracy when using rising and falling waveforms. The waveforms should have two sets of rising and falling waveforms specified with a 50-Ω resistor to V_{CC} or GND. The four test load parameters are defined as:

■   VMEAS = Output voltage measurement point (i.e., typically VDD/2)
■   VREF = Test load pullup or pulldown reference voltage
■   RREF = Test load resistive value
■   CREF = Test load capacitive value

Figure 2 shows the assumed connections for CREF, RREF, and VREF parameters.

Figure 2. AC Test Load Parameters
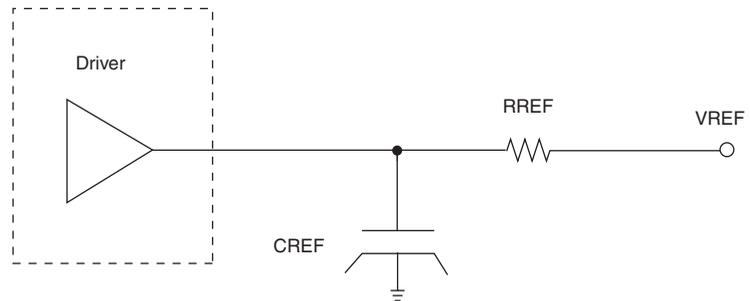
🔈 Input-only models require just power/GND clamp diodes and pin/package parasitic keywords. Along with the keywords, VINL, VINH, and C_COMP, parameters are also required.

Characteristics of Altera IBIS Models

Altera IBIS models are generated from HSPICE models, and are based on either IBIS version 2.1 or 3.2. All of the newer Altera device family models—such as Stratix™, Mercury™, APEX™ II, APEX 20KC, and some APEX 20KE devices—are generated with IBIS version 3.2, and all the other device models are generated with IBIS version 2.1.

This section describes the characteristics of Altera IBIS models.

Multi-Voltage Support

Because Altera devices support multiple voltages (V_{CCIO}), there are separate IBIS models for each supported voltage. To simplify model identification and the corresponding voltage level, the following model names are used:

■ model_name_5 = V_{CCIO} of 5.0 V
■ model_name_3 = V_{CCIO} of 3.3 V
■ model_name_2 = V_{CCIO} of 2.5 V
■ model_name_1 = V_{CCIO} of 1.8 V
■ model_name_15 = V_{CCIO} of 1.5 V

Slow Slew Rate Control

Most Altera devices have the option of turning the slew rate on and off. Files with an *s* or *slew* suffix in the signal/model name, have the slew rate turned on. Likewise, files without an *s* or *slew* suffix, have the slew rate turned off. For example:

- model_name = slew rate off
- model_name_s or model_name_slew = slew rate on

PCI Clamp Diode

Most Altera devices have the option of turning the PCI clamp diode on and off. Files with *p* or *PCI* suffix in the signal/model name have the PCI clamp-diode enabled; likewise, files without a *p* or *PCI* suffix have the PCI clamp-diode disabled. For example:

- model_name = PCI clamp diode off
- model_name_p or model_name_pci = PCI clamp diode on

PCI Diode & Slew Rate Control

Some Altera device models have both PCI clamp diode and slow slew rate control options enabled. Files with an *sp* in the signal/model name have both the PCI clamp diode and slew rate control options enabled; likewise, files without the *sp* have both the PCI clamp diode and slew rate control options disabled. The following file name is the ACEX 1K model with PCI diode and slew rate control enabled:

- acex_3_sp_BI = ACEX1K device model with the PCI diode and slew control rate option on

Corner Case Support

Altera IBIS models support all three corner cases: Typ, Min, and Max. Each corner is defined by its specific voltage, process, and temperature range. The corner case information is available within the Altera IBIS model.

Supported I/O Standards

Altera IBIS models support a variety of I/O standards, including:

- 3.3-V LVTTL/ LVCMOS
- 2.5-V LVTTL
- 1.8-V LVTTL
- 1.5-V LVTTL
- SSTL-2/ SSTL-3
- GTL+
- HSTL
- 3.3-V PCI
- 3.3-V PCML
- LVDS
- LVPECL
- HyperTransport™ (HT)
- AGP
- CTT

Altera IBIS model names specify the supported I/O standard. If the model's name does not specify the supported I/O standard, the model is an LVTTL model by default. For example, the model name ob_20kc_2 specifies the LVTTL models for APEX 20KC devices with a 2.5-V V_{CCIO}, and the model name apex2_sstl2_in specifies the SSTL-2 models for APEX II devices with a 2.5-V V_{CCIO}.

Class I and class II of some SSTL-3, SSTL-2, or HSTL I/O standards, have separate IBIS models. To specify the class of the terminated logic, *cl1* or *cl2* is added to the model's name.

☞   Depending on the I/O standard, single-ended models can run at speeds up to 420 MHz and differential models can run at speeds up to 500 MHz (1.0 Gbps).

Driver Current Strength

For newer Altera devices (e.g., APEX II, Mercury, or Stratix), the drivers have different current strengths at various V_{CCIO} levels. To distinguish between models, each model name specifies the driver's current strength, the V_{CCIO} level, and the I/O standard. For example, the apex2_ttl_18v_4ma_s model name specifies the following:

- APEX II device model
- LVTTL I/O driver
- V_{CCIO} = 1.8 V
- Driver current strength = 4 mA
- Slew rate control option on

LCR Values for Pin & Package

Because LCR values for pin and package keywords should be specified, Altera provides the LCR values for each device family on the Altera web site: www.altera.com/support/software/download/ibis/ibs-ibis_index.html.

Altera's LCR values are for three pin groups: I/O, HSSI, and VCC/GND. Each LCR parameter of the I/O, HSSI, or VCC/GND pin has its own type, minimum, and maximum values.

IBIS Output File Generation with Quartus II Software

The Quartus II software, version 2.0 and later, can automatically generate an IBIS output file to perform board-level signal integrity verification using EDA tools. To use this feature prior to compilation, select **Board-level** in the EDA tools list on the EDA Tool Settings page (Settings dialog box). The Quartus II software applies the appropriate IBIS model to all pins of the device. The software will also select the appropriate LCR values for the selected device.

The Quartus II software uses three files to generate the appropriate IBIS model for a targeted Altera device. There is an IBIS model file for each device family, an LCR file that specifies LCR values for each package in the family, and an IBIS property file that specifies the I/O standard and available settings for the targeted device family. For more information on generating IBIS output files with Quartus II software, refer to the following resources:

- *Generating IBIS Output Files with the Quartus II Software* in Quartus II Help
- The Altera web site: www.altera.com/support/devices/ibis/ibi-quartus.html

New Keywords in IBIS Version 3.2

The Altera IBIS models support some new keywords in IBIS, version 3.2. Two of the new keywords are [Driver Schedule] and [Pullup Reference].

The [Driver Schedule] keyword describes the relative model switching sequence for referenced models to produce a multi-staged driver. The [Driver Schedule] keyword also establishes a hierarchical order between models and should be placed under the [Model] keyword, which acts as the top-level model. The scheduled models are then referenced from the top-level model by the [Driver Schedule] keyword. The [Driver Schedule] keyword is used in some Altera models, such as Mercury LVDS and LVPECL I/O models.

The [Pullup Reference] keyword defines a voltage rail—other than the rail defined by the [Voltage Range] keyword—as the reference voltage for the [Pullup] I/V curve data. The [Pullup Reference] keyword provides the actual voltage level (i.e., not percentage) in the Typical, Minimum, and Maximum formats.

Example of Altera IBIS Model

The following example shows an Altera APEX II IBIS model for an I/O buffer. The example model uses the LVTTL I/O standard, VCCIO tied to 1.5 V, 24 mA driver strength, and the slow slew rate control enabled.

```
[IBIS Ver]   3.2

[File Name] apex2.ibs

[File Rev]   1.2

[Package]

|RCL values are for EP2A15 in 672 FBGA package(I/O pins)

| variable     typ        min        max

R_pkg         420.00m   180.00m    1006.00m

L_pkg         3.44nH    1.86nH     7.57nH

C_pkg         0.90pF    0.44pF     2.08pF



[Pin] signal_name model_name _pin R_pinL_pin  C_pin

1 vttl_15v_24ma_slvttl_15v_24ma_s 420.00m 3.44nH0.90pF

|
*******************************************

|       LVTTL I/O Buffer   (1.5v VCCIO/ 24mA/Slew rate)

|*******************************************

|

[Model]     lvttl_15v_24ma_s

Model_type   I/O

|

Vinl = 0.5600

Vinh = 2.9100
```

```
Vmeas = 0.8000

Cref = 3.50e-11

Rref = 1.00e+08

Vref = 0.00e+00

C_comp      3.0000pF    NA       NA

|

[Temperature Range] 25.0000  85.0000   0.0000

[Voltage Range]    1.5000   1.4000   1.6000

[Pulldown]

| voltage    I(typ)          I(min)        I(max)

-3.600       -4.768e-03   -4.038e-03   -5.343e-03

-2.300       -4.768e-03   -4.038e-03   -5.343e-03

.

.

5.000         1.552e-01     8.943e-02      2.372e-01

6.600         1.552e-01     8.943e-02      2.372e-01

|

[Pullup]

| voltage    I(typ)         I(min)         I(max)

5.100        -6.432e-02   -3.775e-02   -1.024e-01

3.900        -6.432e-02   -3.775e-02   -1.024e-01

.

.

-1.200     5.800e-03      5.120e-03    6.490e-03
```

```
-5.100      5.800e-03      5.120e-03     6.490e-03

|

[Ramp]

dV/dt_r  0.7720/3.5400n0.6621/6.7500n  0.8593/2.1700n

dV/dt_f  0.7955/2.7400n0.6842/5.4800n  0.8780/1.6300n

|

[GND_Clamp]

|Voltage   I(typ)         I(min)         I(max)

-3.600    -7.314e+00    -7.467e+00     -7.255e+00

-3.100    -5.995e+00    -6.164e+00     -5.929e+00

.

.

0.700    -0.000e+00    -0.000e+00     -0.000e+00

1.600     0.000e+00     0.000e+00      0.000e+00

|

[POWER_Clamp]

|Voltage   I(typ)         I(min)         I(max)

 1.600    -0.000e+00    -0.000e+00     -0.000e+00

 0.700    -0.000e+00    -0.000e+00     -0.000e+00

.

.

-4.000     2.393e+01     2.436e+01      2.375e+01

-5.100     3.223e+01     3.333e+01      3.134e+01
```

```
[Rising Waveform]

R_fixture = 50.0000

V_fixture = 0.0000

V_fixture_min = 0.0000

V_fixture_max = 0.0000

|Time          Typ(v)       Min(v)        Max(v)

0.0000n         0.0000      0.0000        0.0000

0.0700n         0.0000      0.0000       -0.0000

.

.

34.4400n        1.2866      1.1007        1.4321

44.9900n        1.2866      1.1034        1.4321

|

[Rising Waveform]

R_fixture = 50.0000

V_fixture = 1.5000

V_fixture_min = 1.4000

V_fixture_max = 1.6000

|Time          Typ(v)       Min(v)        Max(v)

0.0000n         0.1742      0.2591        0.1367

0.2000n         0.1742      0.2591        0.1369

.

.

15.9700n        1.4997      1.3991        1.5999
```

```
44.9900n          1.5000       1.4000        1.6000

|

[Falling Waveform]

R_fixture = 50.0000

V_fixture = 0.0000

V_fixture_min = 0.0000

V_fixture_max = 0.0000

|Time            Typ(v)        Min(v)        Max(v)

0.0000n           1.2866       1.1035        1.4321

0.3600n           1.2866       1.1035        1.4321

.

.

32.2500n          0.1744       0.2643        0.1367

44.9900n          0.1742       0.2596        0.1367


[END]
```

Simulation Results of Altera IBIS Models

This section contains simulation results of Altera IBIS models using various I/O standards.

The example in Figure 3 shows the setup and simulation result of APEX II LVDS models at 450 MHz (i.e., 900 Gbps). The driver models (i.e., LVDS_out_pos for positive signals and LVDS_out_neg for negative signals) are connected to the receiver through a simple transmission line, with 50-Ω impedance and 450 ps of delay. Differential receiver driver models are LVDS_in_pos for positive signals and LVDS_in_neg for negative signals. The signals are terminated at the receiver with a 100-Ω resistor.

Figure 3. LVDS Driver & Receiver with 100 Ω Termination with T-Line
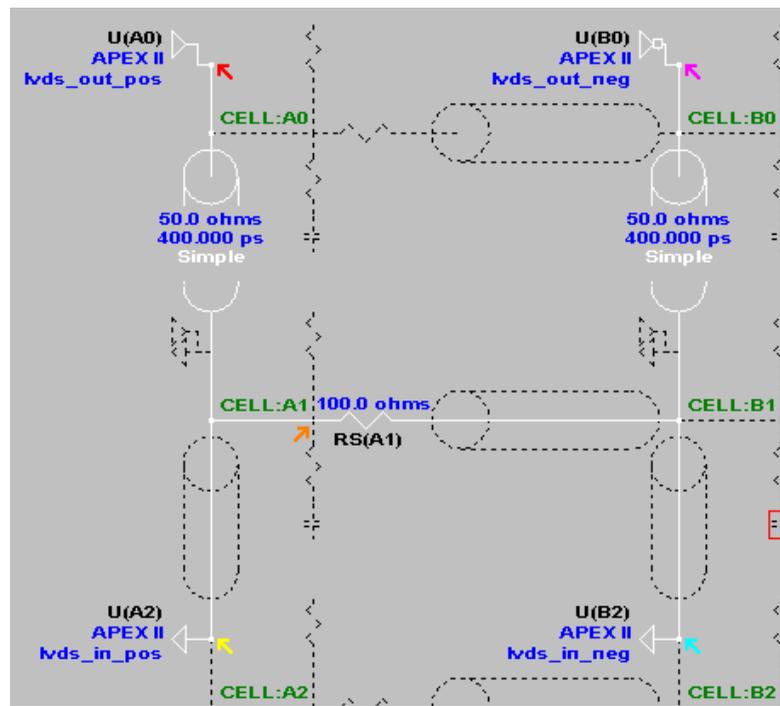
Figure 4 shows the simulation result at the receiver.

Figure 4. LVDS Simulation Result at the Receiver
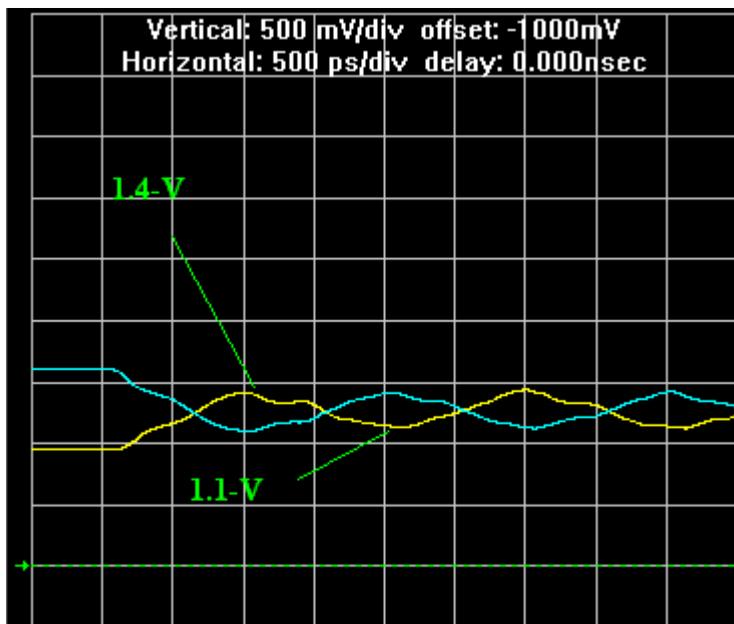
Figures 5 and 6 show the setup and simulation results for an LVTTL model. In the example, an APEX II model with a 24mA driver at 3.3-V V_{CCIO} is used. The driver is connected to the receiver through a 3-inch stackup transmission line and 112.1-Ω impedance. A series termination resistor of 120 Ω is used.

Figure 5. LVTTL Simulation with Driver (lvttl_33v_24ma) & Receiver (lvttl_33v_in)
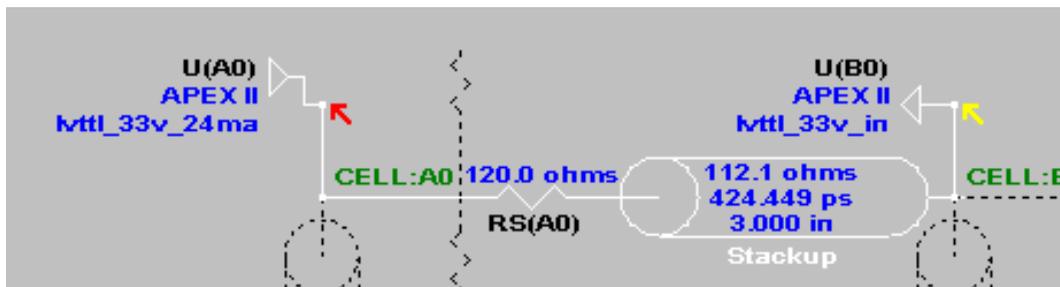
Figure 6. LVTTL Simulation Results with Driver & Receiver
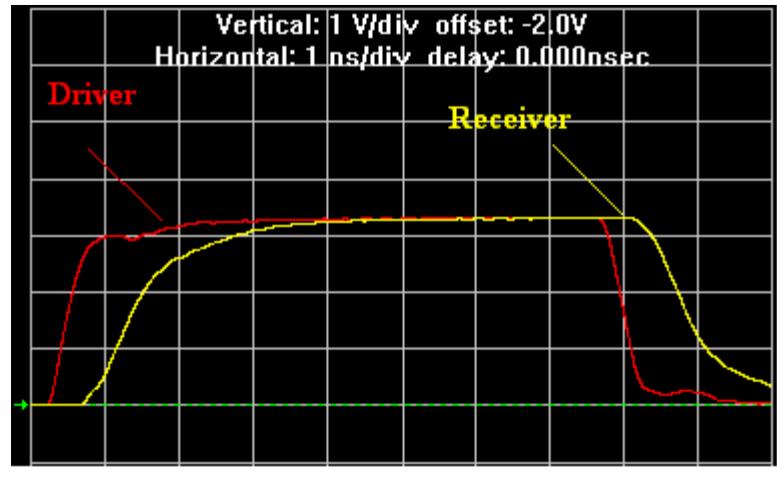
Figures 7 and 8 show the setup and simulation result for a GTL+ model. Because GTL+ output is an open-drain transistor, the output should be tied to V_{TT} via pull-up resistors. In this example, an APEX II model GTL+ driver (gtl_min) is connected to the receiver (gtl_in) through a transmission line of 50-Ω impedance. A series termination resistor of 50 Ω and a pull-up resistor to V_{TT} voltage (V_{TT} = 1.5 V) is used.

Refer to the applicable Altera device data sheet for information on the V_{TT} value.

Figure 7. LVTTL Simulation with Driver (apexii_gtl_min) & Receiver (apexii_gtl_in)
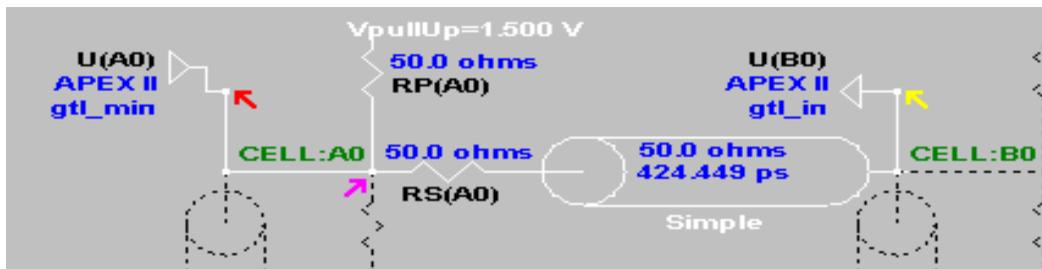
Figure 8. GTL+ Simulation Results with Driver & Receiver
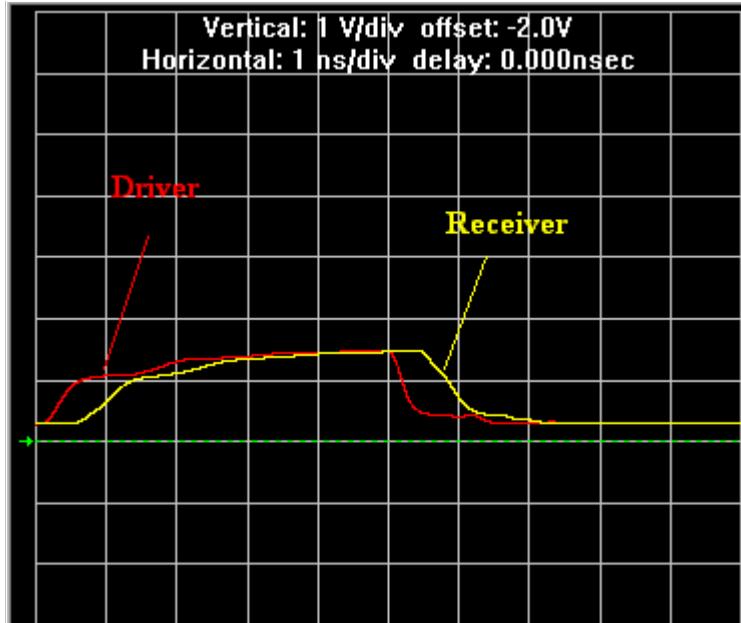
Industry Support for the IBIS

Because IBIS models can resolve many problems early in the design process, industry support of IBIS models is becoming more widespread. In fact, several large semiconductor vendors are requiring IBIS model support as a prerequisite of component purchases. Consequently, semiconductor vendors are providing more IBIS behavioral models with their devices.

Because IBIS models have a standard format, vendors' models are compatible with one another. There are many vendors that support IBIS models such as Altera, AMD, Intel, LSI logic, PCM-Sierra, and others.

For more information on IBIS vendor support, refer to the following web site: www.viewlogic.com/products/datasheets_html/ibis.asp

IBIS Modeling Tools

There are different EDA vendors providing simulation tools for IBIS models, and each tool can play a specific role in the simulation. A few of these vendors include:

- Innoveda, Quad (uses XTK models)
- Innoveda, Hyperlynx
- Mentor Graphic, Interconnectix
- Cadence
- Avanti Corporation

- Microsim
- Veribest

Conclusion

Because of the high demand of IBIS models, Altera began providing IBIS behavioral models of Altera devices in 1998. The Altera IBIS models are generated from SPICE model simulations.

For a complete list of Altera IBIS models and to download the files, please refer to the following Altera web site:
www.altera.com/support/software/download/ibis/ibs-ibis_index.html

101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
http://www.altera.com
Applications Hotline:
(800) 800-EPLD
Literature Services:
lit_req@altera.com

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