9. Hot Socketing and Power-On Reset in Stratix IV Devices

SIV51009-3.2

This chapter describes hot-socketing specifications, power-on reset (POR) requirements, and their implementation in Stratix® IV devices.

Stratix IV devices offer hot socketing, also known as hot plug-in or hot swap, and power sequencing support without the use of external devices. You can insert or remove a Stratix IV device or a board in a system during system operation without causing undesirable effects to the running system bus or board that is inserted into the system.

The hot-socketing feature also removes some of the difficulty when you use Stratix IV devices on PCBs that contain a mixture of 3.0-, 2.5-, 1.8-, 1.5-, and 1.2-V devices.

The Stratix IV hot-socketing feature provides:

- Board or device insertion and removal without external components or board manipulation
- Support for any power-up sequence with the exception that V_{CC} must power up fully before V_{CCAUX} for all Stratix IV production devices
- I/O buffers non-intrusive to system buses during hot insertion

This section also describes POR circuitry in Stratix IV devices. POR circuitry keeps the devices in the reset state until the power supply outputs are within operating range (provided V_{CC} powers up fully before V_{CCAUX}).

This chapter contains the following sections:

Stratix IV Hot-Socketing Specifications

Stratix IV devices are hot-socketing compliant without the need for external components or special design requirements. Hot-socketing support in Stratix IV devices has the following advantages:

Stratix IV Devices can be Driven Before Power Up

You can drive signals into I/O pins, dedicated input pins, and dedicated clock pins of Stratix IV devices before or during power up or power down without damaging the device.

I/O Pins Remain Tri-Stated During Power Up

A device that does not support hot socketing can interrupt system operation or cause contention by driving out before or during power up. In a hot-socketing situation, the Stratix IV device's output buffers are turned off during system power up or power down. Also, the Stratix IV device does not drive out until the device is configured and working within the recommended operating conditions.

Insertion or Removal of a Stratix IV Device from a Powered-Up System

Devices that do not support hot socketing can short power supplies when powered up through the device signal pins. This irregular power up can damage both the driving and driven devices and can disrupt card power up.

You can insert a Stratix IV device into or remove it from a powered-up system board without damaging the system board or interfering with its operation.

You can power up or power down the V_{CCIO}, V_{CC}, V_{CCPGM}, and V_{CCPD} supplies in any sequence (with any time between them) which are monitored by the hot socket circuit. In addition, all other power supplies for the device can be powered up or down in any sequence. Individual power supply ramp-up and ramp-down rates range from 50 µs to 100 ms. During hot socketing, the I/O pin capacitance is less than 15 pF and the clock pin capacitance is less than 20 pF.

To successfully power-up and exit POR on production devices, fully power V_{CC} before V_{CCAUX} begins to ramp.

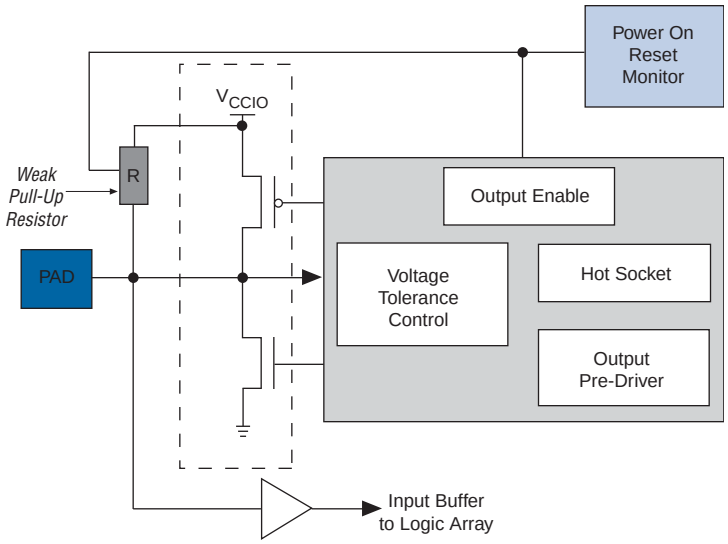
A possible concern regarding hot socketing is the potential for "latch-up." Stratix IV devices are immune to latch-up when hot socketing. Latch-up can occur when electrical subsystems are hot socketed into an active system. During hot socketing, the signal pins can be connected and driven by the active system before the power supply can provide current to the device's power and ground planes. This condition can lead to latch-up and cause a low-impedance path from power to ground within the device. As a result, the device draws a large amount of current, possibly causing electrical damage.

Hot-Socketing Feature Implementation in Stratix IV Devices

The hot-socketing feature turns off the output buffer during power up and power down of the V_{CC}, V_{CCAUX}, V_{CCIO}, V_{CCPGM}, or V_{CCPD} power supplies. The hot-socketing circuitry generates an internal HOTSCKT signal when the V_{CC}, V_{CCAUX}, V_{CCIO}, V_{CCPGM}, or V_{CCPD} power supplies are below the threshold voltage. Hot-socketing circuitry is designed to prevent excess I/O leakage during power up. When the voltage ramps up very slowly, it is still relatively low, even after the POR signal is released and the configuration is completed. The CONF_DONE, nCEO, and nSTATUS pins fail to respond, as the output buffer cannot flip from the state set by the hot-socketing circuit at this low voltage. Therefore, the hot-socketing circuitry has been removed from these configuration pins to make sure that they are able to operate during configuration. Thus, it is expected behavior for these pins to drive out during power-up and power-down sequences.

Figure 9–1 shows the Stratix IV device's I/O pin circuitry.

Figure 9–1. Hot-Socketing Circuitry for Stratix IV Devices



The POR circuit monitors the voltage level of the power supplies (V_{CC}, V_{CCAUX}, V_{CCPT}, V_{CCPGM}, and V_{CCPD}) and keeps the I/O pins tri-stated until the device is in user mode. The weak pull-up resistor (R) in the Stratix IV input/output element (IOE) keeps the I/O pins from floating. The 3.0-V tolerance control circuit permits the I/O pins to be driven by 3.0 V before the V_{CC}, V_{CCAUX}, V_{CCPT}, V_{CCPGM}, or V_{CCPD} supplies are powered. It also prevents the I/O pins from driving out when the device is not in user mode. To successfully power-up and exit POR on production devices, fully power V_{CC} before V_{CCAUX} begins to ramp.

Altera uses GND as a reference for hot-socketing operations and I/O buffer designs. To ensure proper operation, you must connect the GND between boards before connecting the power supplies. This prevents the GND on your board from being pulled up inadvertently by a path to power through other components on your board. A pulled up GND could otherwise cause an out-of-specification I/O voltage or current condition with the Altera device.

Power-On Reset Circuitry

When power is applied to a Stratix IV device, a POR event occurs if the power supply reaches the recommended operating range within the maximum power supply ramp time (t_{RAMP}). If t_{RAMP} is not met, the device I/O pins and programming registers remain tri-stated, during which device configuration could fail. The maximum t_{RAMP} for Stratix IV devices is 100 ms; the minimum t_{RAMP} is 50 µs. When the PORSEL pin is high, the maximum T_{RAMP} for Stratix IV devices is 4 ms.

Stratix IV devices provide a dedicated input pin (PORSEL) to select a POR delay time during power up. When the PORSEL pin is connected to GND, the POR delay time is 100 to 300 ms. When the PORSEL pin is set to high, the POR delay time is 4 to 12 ms.

The POR block consists of a regulator POR, satellite POR, and main POR to check the power supply levels for proper device configuration.

The satellite POR monitors the following:

- V_{CCPD} and V_{CCPGM} power supplies that are used in the I/O buffers and for device programming
- V_{CCAUX} power supply which is the auxiliary supply for the programmable power technology
- V_{CC} and V_{CCPT} power supplies that are used in the device core

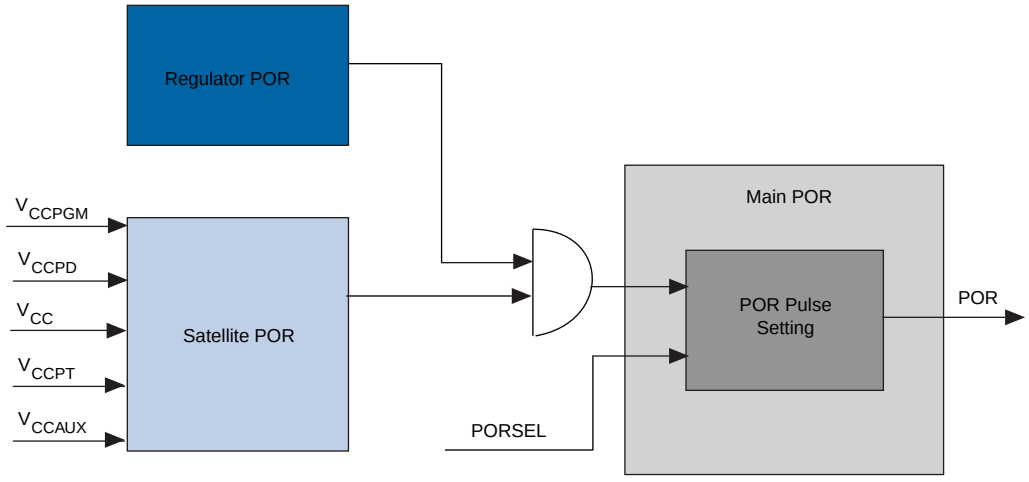
Altera requires powering up V_{CC} before V_{CCAUX}.

The main POR waits for satellite POR and the regulator POR to release the POR signal. Until the release of the POR signal, the device configuration cannot start.

The internal configuration memory supply that is used during device configuration is checked by the regulator POR block and is gated in the main POR block for the final POR trip. Figure 9–2 shows a simplified diagram of the POR block.

All configuration-related dedicated and dual function I/O pins must be powered by V_{CCPGM}.

Figure 9–2. Simplified POR Diagram for Stratix IV Devices



Power-On Reset Specifications

Table 9–1 lists the power supplies that the POR circuit monitors.

Altera requires powering up V_{CC} before V_{CCAUX}.

Table 9–1. Power Supplies Monitored by the POR Circuitry

Power Supply	Description	Setting (V)
V_{CC}	Core and periphery power supply	0.9
V_{CCPT}	Programmable power technology power supply	1.5
V_{CCPD}	I/O pre-driver power supply	2.5, 3.0
V_{CCPGM}	Configuration pins power supply	1.8, 2.5, 3.0
V_{CCAUX}	Auxiliary supply for the programmable power technology	2.5

Table 9–2 lists the power supplies that the POR circuit does not monitor.

Table 9–2. Power Supplies Not Monitored by the POR Circuitry ***(Note 1)***

Power Supply	Description	Setting (V)
V_{CCIO}	I/O power supply	1.2, 1.5, 1.8, 2.5, 3.0
V_{CCA_PLL}	PLL analog global power supply	2.5
V_{CCD_PLL}	PLL digital power supply	0.9
V_{CC_CLKIN}	PLL differential clock input power supply (top and bottom I/O banks only)	2.5
V_{CCBAT}	Battery back-up power supply for design security volatile key storage	1.2-3.3

Note to Table 9–2:

(1) The transceiver supplies are not monitored by POR.

V_{CCIO}, V_{CCA_PLL}, V_{CCD_PLL}, V_{CC_CLKIN}, and V_{CCBAT} are not monitored by POR and have no affect on the device configuration.

The POR specification is designed to ensure that all the circuits in the Stratix IV device are at certain known states during power up.

The POR signal pulse width is programmable using the PORSEL input pin. When the PORSEL pin is connected to GND, the POR delay time is 100 to 300 ms. When the PORSEL pin is set to high, the POR delay time is 4 to 12 ms.

For more information about the POR specification, refer to the *DC and Switching Characteristics in Stratix IV Devices* chapter.

Document Revision History

Table 9–3 lists the revision history for this chapter.

Table 9–3. Document Revision History

Date	Version	Changes
February 2011	3.2	■ Updated Table 9–2. ■ Updated the "Power-On Reset Circuitry", "Power-On Reset Specifications", and "Insertion or Removal of a Stratix IV Device from a Powered-Up System" sections. ■ Applied new template. ■ Minor text edits.
March 2010	3.1	■ Updated the introduction and the "Stratix IV Hot-Socketing Specifications", "Insertion or Removal of a Stratix IV Device from a Powered-Up System", "Hot-Socketing Feature Implementation in Stratix IV Devices", "Power-On Reset Circuitry", and "Power-On Reset Specifications" sections. ■ Updated Table 9–1 and Table 9–2. ■ Updated Figure 9–2. ■ Minor text edits.
November 2009	3.0	■ Updated graphics. ■ Minor text edits.
June 2009	2.2	■ Updated Table 9–2. ■ Added introductory sentences to improve search ability. ■ Removed the Conclusion section. ■ Minor text edits.
March 2009	2.1	■ Changed all "Stratix IV E" to "Stratix IV". ■ Updated "Stratix IV Hot-Socketing Specifications" and "Hot-Socketing Feature Implementation in Stratix IV Devices" sections. ■ Updated Figure 9–2. ■ Removed "Referenced Documents" section.
November 2008	2.0	■ Updated "Hot-Socketing Feature Implementation in Stratix IV Devices" on page 9–2. ■ Updated "Power-On Reset Circuitry" on page 9–4. ■ Updated Table 9–1. ■ Made minor editorial changes.
July 2008	1.1	Revised "Introduction".
May 2008	1.0	Initial release.