Simulating the Turbo Encoder/Decoder Model

with the Visual IP Software

July 2000, ver. 1 User Guide

Introduction

Altera® intellectual property (IP) MegaCore™ functions are developed and pre-tested by Altera, and are optimized for specific Altera device architectures. You can test-drive these functions for free via the OpenCore™ feature by downloading the functions from the Altera web site and installing them on your PC or UNIX workstation. To help in your evaluation, Altera also provides Visual IP simulation models for these functions.

The Visual IP software from Innoveda lets you create simulation models that can be used in third-party VHDL and Verilog HDL simulation tools. Altera distributes the Visual IP software for the end user along with Visual IP models of Altera IP functions.

Altera's Visual IP models are parameterizable, RTL level, functional simulation models. The models let you instantiate Altera IP in your design and simulate it in your choice of simulation tool. This user guide describes how to install and use the Visual IP simulation model for the Altera Turbo Encoder/Decoder MegaCore function.

Before using the Turbo Encoder/Decoder VIP model, you must download and install the Visual IP software, which is available for free from the Altera IP MegaStore site at **http://www.altera.com/IPmegastore**. Follow the instructions in the *Installing the Visual IP Software User Guide*.

Altera recommends that you also obtain the *Turbo Encoder/Decoder MegaCore Function User Guide* from the Altera web site. This user guide describes the technical specifications of the function.

The Turbo Encoder/Decoder Visual IP model contains the following elements:

Table 1. Turbo Encoder/Decoder Visual IP Model Elements

Element	Description
aukte_umts_turbo_encoder.*	The VHDL or Verilog HDL Turbo encoder model file.
turbo_encoder_vectors.*	A set of VHDL or Verilog HDL test vectors for the Turbo encoder .
turbo_encoder_vip_top.*	Top-level VHDL or Verilog HDL file that references the Turbo encoder model file and test vectors.
auktd_umts_turbo_decoder.*	The VHDL or Verilog HDL Turbo decoder model file.
turbo_decoder_vectors.*	A set of VHDL or Verilog HDL test vectors for the Turbo decoder .
turbe_decoder_vip_top.*	Top-level VHDL or Verilog HDL file that references the Turbo decoder model file and test vectors.

Download the Models

If you have not already done so, download Visual IP models from Altera's web site at **http://www.altera.com** by follow the instructions below.

1. Point your web browser to **http://www.altera.com/IPmegastore**.
2. Search in the IP MegaStore for the function/model you wish to obtain.
3. On the search results page, click the name of the function/model you wish to obtain.
4. Click the Free Test Drive icon and follow the on-line instructions to download the function and/or model.

PC Installation

Execute the **turbo_vip_pc.exe** file and follow the on-line instructions to install the model. The following files are installed:

*<installation path>***vip_simulation\turbo**
- **doc**
  - **turbo_vipug.pdf**
- **verilog**
  - **aukte_umts_turbo_encoder.v**
  - **turbo_encoder_vectors.v**
  - **turbo_encoder_vip_top.v**
  - **aukte_umts_turbo_decoder.v**
  - **turbo_decoder_vectors.v**
  - **turbo_decoder_vip_top.v**
- **vhdl**
  - **mti**
    - **aukte_umts_turbo_encoder.vhd**

turbo_encoder_vectors.vhd
turbo_encoder_vip_top.vhd
aukte_umts_turbo_decoder.vhd
turbo_decoder_vectors.vhd
turbo_decoder_vip_top.vhd
leapfrog
aukte_umts_turbo_encoder.vhd
turbo_encoder_vectors.vhd
turbo_encoder_vip_top.vhd
aukte_umts_turbo_decoder.vhd
turbo_decoder_vectors.vhd
turbo_decoder_vip_top.vhd
vss
aukte_umts_turbo_encoder.vhd
turbo_encoder_vectors.vhd
turbo_encoder_vip_top.vhd
aukte_umts_turbo_decoder.vhd
turbo_decoder_vectors.vhd
turbo_decoder_vip_top.vhd
<*installation path*>**\vip_models\turbo***

Before using the Visual IP mode, set the `VIP_MODELS_DIR` environment variable to <*installation path*>**/vip_models**. The installation process sets all other required environment variables in the system registry.

All Altera Visual IP models use the `VIP_MODELS_DIR` environment variable. If you only wish to use one Visual IP model, you can install the model into any directory and set up the variable to point to that directory. However, if you wish to use several models (e.g., both the Turbo Encoder/Decoder and `a8259` models) you should install all Visual IP models into the same directory.

Solaris Installation

The Turbo Encoder/Decoder model is a tape archive file (**.tar**) that has been compressed using the **gzip** utility. To extract the files, move the **turbo_vip_solaris.tar.gz** file to the location in which you would like to install the models and type the following commands at a UNIX prompt:

```
gunzip turbo_vip_solaris.tar.gz ↵
tar xvf turbo_vip_solaris.tar ↵
```

The following directories and files are created:

<installation path>/vip_simulation/turbo/
- setup.csh
- doc/
  - turbo_vipug.pdf
- verilog\
  - aukte_umts_turbo_encoder.v
  - turbo_encoder_vectors.v
  - turbo_encoder_vip_top.v
  - aukte_umts_turbo_decoder.v
  - turbo_decoder_vectors.v
  - turbo_decoder_vip_top.v
- vhdl\
  - mti\
    - aukte_umts_turbo_encoder.vhd
    - turbo_encoder_vectors.vhd
    - turbo_encoder_vip_top.vhd
    - aukte_umts_turbo_decoder.vhd
    - turbo_decoder_vectors.vhd
    - turbo_decoder_vip_top.vhd
  - leapfrog\
    - aukte_umts_turbo_encoder.vhd
    - turbo_encoder_vectors.vhd
    - turbo_encoder_vip_top.vhd
    - aukte_umts_turbo_decoder.vhd
    - turbo_decoder_vectors.vhd
    - turbo_decoder_vip_top.vhd
  - vss\
    - aukte_umts_turbo_encoder.vhd
    - turbo_encoder_vectors.vhd
    - turbo_encoder_vip_top.vhd
    - aukte_umts_turbo_decoder.vhd
    - turbo_decoder_vectors.vhd
    - turbo_decoder_vip_top.vhd

<installation path>/vip_models/turbo/*

Before using the Visual IP models, perform the following steps:

1. Set the `VIP_MODELS_DIR` environment variable to <*installation path*>**/vip_models**.

   ☞ All Altera Visual IP models use the `VIP_MODELS_DIR` environment variable. If you only wish to use one Visual IP model, you can install the model into any directory and set up the variable to point to that directory. However, if you wish to use several models (e.g., both the Turbo and `a8237` models) you should install all Visual IP models into the same directory.

2. Set the `VIP_EU_ROOT` environment variable to the root directory in which you installed the Visual IP software.

3. Source the **setup.csh** file to complete the configuration of the Visual IP environment.

Running Test Vectors

The Turbo Encoder/Decoder Visual IP model includes test vectors for both the encoder and decoder. This section describes how to use the test vectors provided with the simulation model.

Verilog HDL

If you are using Verilog HDL, perform the following steps to simulate the encoder:

1. Set up the PLI interface to the Visual IP software as described in *Installing the Visual IP Software User Guide*.

2. Make sure the `VIP_MODELS_DIR` environment variable is set properly.

3. Change to the <*installation path*>**/vip_simulation/turbo/verilog** directory.

4. Compile the **aukte_umts_turbo_encoder.v** and **turbo_encoder_vectors.v** files. These modules attach to the appropriate Visual IP models using the Verilog-XL PLI interface.

5. Compile the **turbo_encoder_vip_top.v** file.

6. Simulate **turbo_encoder_vip_top**.

To simulate the decoder, perform the steps above using the **aukte_umts_turbo_decoder.v**, **turbo_decoder_vectors.v**, and **turbo_decoder_vip_top.v** files.

VHDL

If you are using VHDL, perform the following steps to simulate the encoder:

1. Set up the C language interface to the Visual IP software as described in *Installing the Visual IP Software User Guide*.
2. Make sure the `VIP_MODELS_DIR` environment variable is set properly.
3. Change to the directory <*installation path*>**/vip_simulation/turbo/vhdl/**<*simulator*>, where <*simulator*> is to the VHDL simulation tool you are using.
4. Compile the **aukte_umts_turbo_encoder.vhd** and **turbo_encoder_vectors.vhd** files into your work library. These components attach to the appropriate Visual IP models using the C language interface of your VHDL simulator.
5. Compile the **turbo_encoder_vip_top.vhd** file into your work library.
6. Simulate **work.turbo_encoder_vip_top(struct)**.

To simulate the decoder, perform the steps above using the **aukte_umts_turbo_decoder.vhd**, **turbo_decoder_vectors.vhd**, and **turbo_decoder_vip_top.vhd** files.

Using the Turbo Encoder/ Decoder Model

This section describes how to use the Turbo Encoder/Decoder simulation model in your designs.

Verilog HDL

If you are using Verilog HDL, perform the following steps:

1. Set up the PLI interface to the Visual IP software as described in *Installing the Visual IP Software User Guide*.
2. Make sure the `VIP_MODELS_DIR` environment variable is set properly.

3. Go to the <*installation path*>**/vip_simulation/turbo/verilog** directory.

4. Compile the Verilog HDL model that corresponds to the function you wish to simulate (i.e., the encoder or decoder). This module attachs to the appropriate Visual IP model using the Verilog-XL PLI interface.

5. Instantiate the model in your Verilog HDL design. When you instantiate the model, you can modify the parameters as needed for your application.

   ☞ The output files generated by the Turbo Encoder/Decoder MegaWizard® Plug-In contain a parameterized instance of the function. You can use the output files with the model file to simulate a function with custom parameters.

VHDL

If you are using VHDL, perform the following steps:

1. Set up the C language interface to the Visual IP software as described in *Installing the Visual IP Software User Guide*.

2. Make sure the `VIP_MODELS_DIR` environment variable is set properly.

3. Go to the<*installation path*>**/vip_simulation/turbo/vhdl/**<*simulator*> directory, where <*simulator*> is the VHDL simulation tool you are using.

4. Compile the VHDL model that corresponds to the function you wish to simulate (i.e., the encoder or decoder). This component attaches to the appropriate Visual IP model using the C language interface of your VHDL simulator.

5. Instantiate the model in your VHDL design. When you instantiate the model, you can modify the generics as needed for your application.

   ☞ The output files generated by the Turbo Encoder/Decoder MegaWizard Plug-In contain a parameterized instance of the function. You can use the output files with the model file to simulate a function with custom parameters.

Known Issues

Visual IP models do not support checkpoint/restart. Therefore, you must reload the simulation model to restart the simulation.

101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
http://www.altera.com
Applications Hotline:
(800) 800-EPLD
Customer Marketing:
(408) 544-7104
Literature Services:
lit_req@altera.com