

Stratix II GX FPGA Family

September 2007, ver. 1.2 Errata Sheet

Introduction

This errata sheet provides updated information on Stratix[®] II GX devices. This document addresses known device issues and includes methods to work around the issues.



For more information on Stratix II GX device errata, refer to the *Stratix II Family Issues* section of the *Stratix II FPGA Family Errata Sheet*. All information in that section pertains to both Stratix II and Stratix II GX devices.

Table 1 shows the specific issues and which Stratix II GX devices each issue affects.

Table 1. Stratix II GX Family Issues (Part 1 of 2)			
Issue	Affected Devices	Fixed Devices	
Stratix II GX Device Handbook (Volume 1: version 3.0 and Volume 2: version 3.2) incorrectly indicates that the 1.2-V HSTL I/O standard is supported on I/O banks 3, 4, and 7 in all speed grade devices. However, the 1.2-V HSTL I/O standard is supported only on I/O banks 4, 7, and 8 and only in the -3 speed grade.	All Stratix II GX devices	Not Applicable	
Quartus [®] II software version 6.0 SP1 and earlier incorrectly supports 1.2V-HSTL on I/O bank 3 in -3 devices. Quartus II software version 6.0 SP1 with Patch 1.18 or version 6.1 and later will correctly support 1.2-V HSTL on bank 8 instead of on bank 3 in -3 devices.			

Table 1. Stratix II GX Family Issues (Part 2 of 2)			
Issue	Affected Devices	Fixed Devices	
In the XAUI operating mode, the Stratix II GX rate matcher might insert a duplicate Start column (S), causing corruption of the data packet.	This issue is for the XAUI operating mode in Stratix II GX devices.		
Altera [®] has implemented a solution for this issue in the Quartus II software version 7.1.			
In Basic double-width mode, the Stratix II GX rate matcher may insert skip characters after the start of packet under certain conditions. This causes corruption of the data packet. See "Basic Double-Width Mode Illegal Skip Characters Insertion" on page 5 for more information.	This issue is for the Basic double-width mode with Rate Matcher in Stratix II GX devices	Not Applicable	
Altera provides two work-arounds: Protocol Work-Around—If the protocol on the upstream transmitter can be modified to send a column of skip characters immediately before the start of packet, the issue will not occur. Quartus II Work-Around—Ensure that the Enable insertion or deletion of consecutive skip characters or ordered sets option (found on the BASIC1 screen of the ALT2GXB MegaWizard) is unchecked.			

Stratix II GX Device Family Issues

The following issues affect all Stratix II GX device densities.

1.2-V HSTL Support Issue

The 1.2-V HSTL support issue relates to both the Stratix II GX technical documentation and the Quartus II software.

Documentation

The Stratix II GX Device Handbook (Volume 1: version 3.0 and Volume 2: version 3.2) incorrectly indicates that the 1.2-V HSTL I/O standard is supported on I/O banks 3, 4, and 7 in all speed grade devices. The 1.2-V HSTL I/O standard is only supported on banks 4, 7, and 8 and only in the -3 speed grade. Volume 1 (version 3.1) and Volume 2 (version 3.3) of the handbook correct this error.

Quartus II Software Version 6.0 SP1

Quartus II software version 6.0 SP1 and earlier incorrectly supports 1.2-V HSTL on I/O banks 3, 4, and 7 in -3 speed grade devices. Quartus II software version 6.0 SP1 with Patch 1.18 or version 6.1 and later will correctly support 1.2-V HSTL on banks 4, 7, and 8 instead of banks 3, 4, and 7 in -3 speed grade devices.

Solution

Case 1: You had planned to implement 1.2-V HSTL on bank 3 of Stratix II GX -3 speed grade devices.

- 1. Install the Quartus II 6.0 SP1 software.
- 2. Install the Quartus II 6.0 Patch 1.18. (http://www.altera.com/support/kdb/rd08092006_527.html)
- 3. Move all 1.2-V HSTL signals to bank 4, 7, or 8 and recompile.

Case 2: 1.2-V HSTL is already implemented on I/O bank 3 of Stratix II GX -3 speed grade devices (board layout is done).

Altera recommends re-spinning the board to move 1.2-V HSTL signals to bank 4, 7, or 8 and recompiling the design with Quartus II software version 6.0 with Patch 1.18 or Quartus II software version 6.1 and later. If a board re-spin is not possible, contact Altera Technical Services for support.

Case 3: You had planned to implement 1.2-V HSTL in Stratix II GX -4 or -5 speed grade devices.

Recompile the design to a -3 speed grade device with Quartus II software version 6.0 with Patch 1.18 or Quartus II version 6.1 and later.

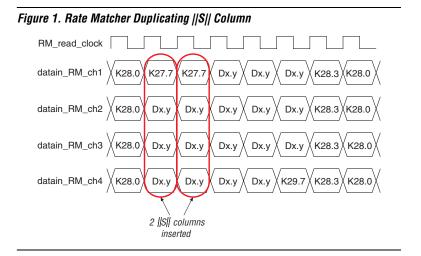
XAUI Mode Duplicate Start Column

In the XAUI operating mode, the Stratix II GX rate matcher might insert a duplicate Start Column (||S||), causing corruption of the data packet.

The rate matcher performs clock rate compensation between the local reference clock and the remote end reference clock by inserting or deleting Skip ordered sets (||R|| [||K28.0||]) from the encoded Idle stream.

When the rate matcher has to insert ||R|| for clock rate compensation, there are instances where the rate matcher inserts a duplicate ||S||. This duplication causes packet corruption. The duplication of ||S|| happens only when the rate matcher block's insertion logic has to insert multiple ||R|| columns before the ||S|| column. This is shown in Figure 1.

This issue is limited to the XAUI operating mode.



Solution

Altera has implemented a solution for this issue in the Quartus II software version 7.1.

If you have implemented a Stratix II GX XAUI design in versions prior to the Quartus II software version 7.1, recompile your design in the Quartus II software version 7.1.

Table 2 provides links to the locations where you can acquire software patches if you must continue using the Quartus II software version 6.1 or 7.0 for your design.

Table 2. Patches for Quartus II			
Soft- ware Version	Operat- ing Sys- tem	Link	
6.1	6.1 Windows ftp.altera.com/outgo-ing/hsio_apps_patches/stratixiigx_patches/pc_quartus_ii_61_siigx_patch_0_64. Linux ftp.altera.com/outgo-ing/hsio_apps_patches/stratixiigx_patches/linux_quartus_ii_61_siigx_patch_0_64.		
	Solaris	ftp.altera.com/outgo-ing/hsio_apps_patches/stratixiigx_patches/solaris_quartus_ii_61_siigx_patch_0_64.tar	
7.0	Windows	ftp.altera.com/outgo-ing/hsio_apps_patches/stratixiigx_patches/pc_quartus_ii_70_siigx_patch_0_06.exe	
	Linux	ftp.altera.com/outgo-ing/hsio_apps_patches/stratixiigx_patches/linux_quartus_ii_70_siigx_patch_0_06.tar	
	Solaris	ftp.altera.com/outgo-ing/hsio_apps_patches/stratixiigx_patches/solaris_quartus_ii_70_siigx_patch_0_06.tar	

Basic Double-Width Mode Illegal Skip Characters Insertion

In Basic double-width mode, the Stratix II GX rate matcher may insert skip characters after the start of packet under certain conditions, as explained below. This causes corruption of the data packet.

Conditions

The rate matcher performs clock rate compensation between the local reference clock and the remote end reference clock by inserting or deleting two bytes of skip characters (both high byte and low byte locations) in the inter packet gap (IPG). This issue is limited only to Basic double-width mode. You can program the skip and control character in the ALT2GXB MegaWizard® Plug-In Manager.

The rate matcher inserts skip characters after the start of packet under the following conditions:

- if the rate matcher has to insert skip characters for clock compensation AND
- the control and the skip characters are received in the lower and upper byte of the data stream, respectively, immediately before the start of packet (SOP)

Figure 2 shows an example of illegal insertion with /K28.0/ and /K28.5/ programmed as skip and control characters, respectively.

Figure 2. Illegal Insertion of /R/ Characters After the Start of Packet (SOP) RM_read_clock Dataout_RMFIFO[15:8] K28.5 K28.5 K28.0 Dx.y K28.0 K28.5 K28.5 K28.5 SOP K28.0 Dataout_RMFIFO[7:0] Illegal skip characters insertion

Solution

Altera provides two work-arounds for this issue. They are:

- Protocol Work-Around
- Quartus II Software Work-Around

Protocol Work-Around

If the protocol on the upstream transmitter can be modified to send a column of skip characters immediately before the start of packet, the issue will not happen (as shown in Figure 3).

K28.0 K28.0 Dx.y Dx.y Serialized data K28.5 K28.0 Dx.y SOP

Figure 3. Parallel Data Sent from Transmitter

Parallel data sent from transmitter

Quartus II Software Work-Around

Quartus II software version 7.2 provides an **Enable insertion or deletion of consecutive skip characters or ordered sets** option in the ALT2GXB MegaWizard (**BASIC1** screen). By default, this option is unchecked to work-around the issue.



When this option is unchecked, the rate matcher does not insert or delete back-to-back skip characters.

If you check this option, you should follow the "Protocol Work-Around" on page 6 to prevent illegal insertion of skip characters.

Tables 3 and 4 provide links to the locations where you can acquire software patches if you must use Quartus II software version 7.1 or Quartus II software version 7.1SP1. Download the appropriate patch and recompile the design. For Quartus II software 7.0 or earlier versions, Altera recommends you move to Quartus II software version 7.2.

Table 3. Patch for Quartus II Software Version 7.1			
Operating System	Links		
Windows	ftp://ftp.altera.com/outgoing/hsio_apps_patches/stratixiigx_patches/pc_quartus_ii_71_siigx_patch_0_26.zip		
Linux	ftp://ftp.altera.com/outgoing/hsio_apps_patches/stratixiigx_patches/linux_quartus_ii_71_siigx_patch_0_26.zip		
Solaris	ftp://ftp.altera.com/outgoing/hsio_apps_patches/stratixiigx_patches/solaris_quartus_ii_71_siigx_patch_0_26.zip		

Table 4. Patch for Quartus II Software Version 7.1SPI			
Operating System	Links		
Windows	ftp://ftp.altera.com/outgoing/hsio_apps_patches/stratixiigx_patches/pc_quartus_ii_71sp1_siigx_patch_1_26.zip		
Linux	ftp://ftp.altera.com/outgoing/hsio_apps_patches/stratixiigx_patches/linux_quartus_ii_71sp1_siigx_patch_1_26.zip		
Solaris	ftp://ftp.altera.com/outgoing/hsio_apps_patches/stratixiigx_patches/solaris_quartus_ii_71sp1_siigx_patch_1_26.zip		

Referenced Document

This errata sheet references the following document:

Stratix II FPGA Family Errata Sheet

Document Revision History

Table 5 shows the revision history for this chapter.

Table 5. Document Revision History			
Date and Document Version	Changes Made	Summary of Changes	
October 2007, v1.2	Added the "Basic Double-Width Mode Illegal Skip Characters Insertion" section.	_	
	Added the "Referenced Document" and "Document Revision History" sections.	_	
July 2007, v1.1	Added the "XAUI Mode Duplicate Start Column" section.	_	
August 2006, v1.0	Initial release.	_	



101 Innovation Drive San Jose, CA 95134 www.altera.com Technical Support: www.altera.com/support Literature Services: literature@altera.com

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