8. High-Speed Differential I/O Interfaces and DPA in Stratix IV Devices

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This chapter describes the significant advantages of the high-speed differential I/O interfaces and the dynamic phase aligner (DPA) over single-ended I/Os and their contribution to the overall system bandwidth achievable with Stratix® IV FPGAs. All references to Stratix IV devices in this chapter apply to Stratix IV E, GT, and GX devices.

The Stratix IV device family consists of the Stratix IV E (Enhanced) devices without high-speed clock data recovery (CDR) based transceivers, Stratix IV GT devices with up to 48 CDR-based transceivers running up to 11.3 Gbps, and Stratix IV GX devices with up to 48 CDR-based transceivers running up to 8.5 Gbps.

The following sections describe the Stratix IV high-speed differential I/O interfaces and DPA:

Overview

All Stratix IV E, GX, and GT devices have built-in serializer/deserializer (SERDES) circuitry that supports high-speed LVDS interfaces at data rates of up to 1.6 Gbps. SERDES circuitry is configurable to support source-synchronous communication protocols such as Utopia, Rapid I/O, XSBI, small form factor interface (SFI), serial peripheral interface (SPI), and asynchronous protocols such as SGMII and Gigabit Ethernet.

The Stratix IV device family has the following dedicated circuitry for high-speed differential I/O support:

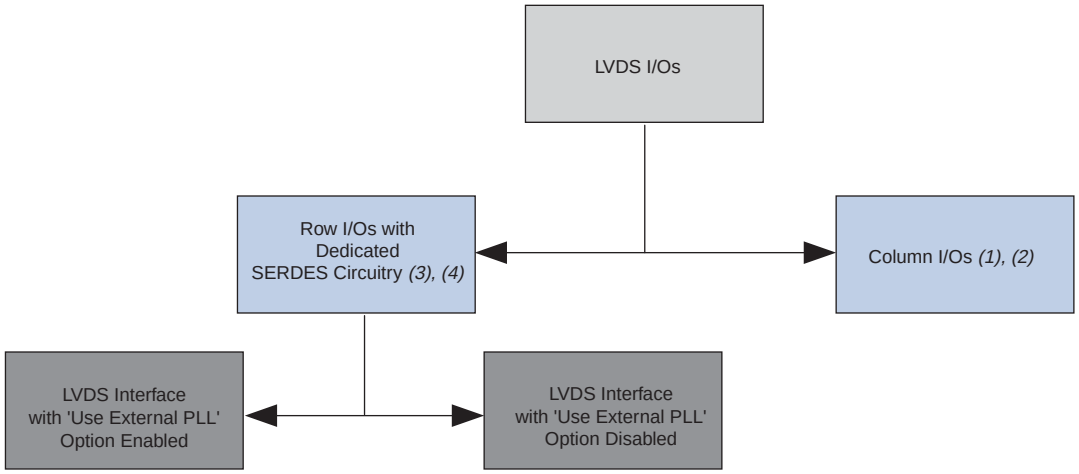
- Differential I/O buffer
- Transmitter serializer
- Receiver deserializer
- Data realignment
- DPA
- Synchronizer (FIFO buffer)
- Phase-locked loops (PLLs) (located on left and right sides of the device)

For high-speed differential interfaces, the Stratix IV device family supports the following differential I/O standards:

- LVDS
- Mini-LVDS
- Reduced swing differential signaling (RSDS)

In the Stratix IV device family, I/Os are divided into row and column I/Os. Figure 8–1 shows I/O bank support for the Stratix IV device family. The row I/Os provide dedicated SERDES circuitry.

Figure 8–1. I/O Bank Support in the Stratix IV Device Family *(1)*, *(2)*, *(3)*, *(4)*



Notes to Figure 8–1:

(1) Column input buffers are true LVDS buffers, but do not support 100-Ω differential on-chip termination.

(2) Column output buffers are single ended and need external termination schemes to support LVDS, mini-LVDS, and RSDS standards. For more information, refer to the *I/O Features in Stratix IV Devices* chapter.

(3) Row input buffers are true LVDS buffers and support 100-Ω differential on-chip termination.

(4) Row output buffers are true LVDS buffers.

The ALTLVDS transmitter and receiver requires various clock and load enable signals from a left or right PLL. The Quartus® II software provides the following two choices when configuring the LVDS SERDES circuitry when using the PLL:

- LVDS interface with the **Use External PLL** option enabled—You control the PLL settings, such as dynamically reconfiguring the PLL to support different data rates, dynamic phase shift, and so on. You must enable the **Use External PLL** option in the ALTLVDS_TX and ALTLVDS_RX megafunctions, using the ALTLVDS MegaWizard™ Plug-in Manager software. You also must instantiate an ALTPLL megafunction to generate the various clocks and load enable signals. For more information, refer to "LVDS Interface with the Use External PLL Option Enabled" on page 8–26.
- LVDS interface with the **Use External PLL** option disabled—The Quartus II software configures the PLL settings automatically. The software is also responsible for generating the various clock and load enable signals based on the input reference clock and data rate selected.

Both choices target the same physical PLL; the only difference is the additional flexibility provided when an LVDS interface has the **Use External PLL** option enabled.

Locations of the I/O Banks

Stratix IV I/Os are divided into 16 to 24 I/O banks. The dedicated circuitry that supports high-speed differential I/Os is located in banks in the right and left side of the device. Figure 8–2 shows a high-level chip overview of the Stratix IV E device.

Figure 8–2. High-Speed Differential I/Os with DPA Locations in Stratix IV E Devices

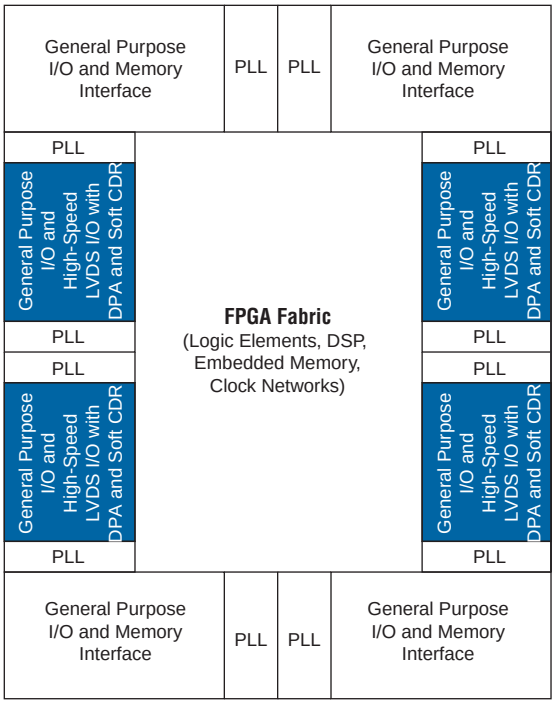
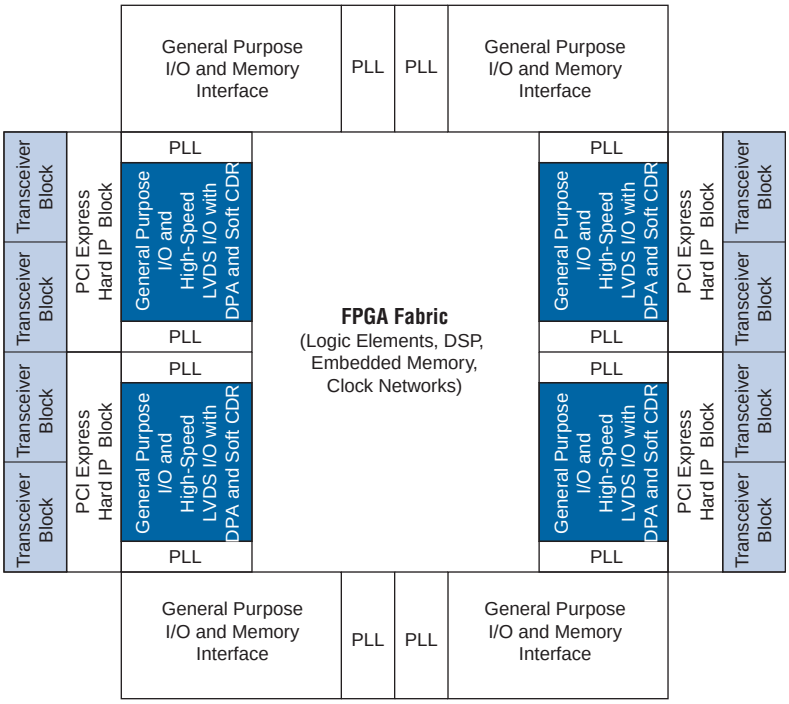


Figure 8–3 shows a high-level chip overview of the Stratix IV GT and GX devices.

Figure 8–3. High-Speed Differential I/Os with DPA Locations in Stratix IV GT and GX Devices



LVDS Channels

The Stratix IV device family supports LVDS on both row and column I/O banks. Row I/Os support true LVDS input with 100-Ω differential input termination (OCT R_D), and true LVDS output buffers. Column I/Os supports true LVDS input buffers without OCT R_D. Alternately, you can configure the row and column LVDS pins as emulated LVDS output buffers that use two single-ended output buffers with an external resistor network to support LVDS, mini-LVDS, and RSDS standards. Stratix IV devices offer single-ended I/O refclk support for the LVDS.

Dedicated SERDES and DPA circuitries are implemented on the row I/O banks to further enhance LVDS interface performance in the device. For column I/O banks, SERDES is implemented in the core logic because there is no dedicated SERDES circuitry on column I/O banks.

☞ Emulated differential output buffers support tri-state capability starting with the Quartus II software version 9.1.

Table 8–1 and Table 8–2 list the maximum number of row and column LVDS I/Os supported in Stratix IV E devices. You can design the LVDS I/Os as true LVDS buffers or emulated LVDS buffers, as long as the combination of the two do not exceed the maximum count.

For example, there are a total of 112 LVDS pairs on row I/Os in the 780-pin EP4SE230 device (refer to Table 8–1). You can design up to a maximum of 56 true LVDS input buffers and 56 true LVDS output buffers, or up to a maximum of 112 emulated LVDS output buffers. For the 780-pin EP4SE230 device (refer to Table 8–2), there are a total of 128 LVDS pairs on column I/Os. You can design up to a maximum of 64 true LVDS input buffers and 64 emulated LVDS output buffers, or up to a maximum of 128 emulated LVDS output buffers.

Table 8–1. LVDS Channels Supported in Stratix IV E Device Row I/O Banks (1), (2), (3)

Device	780-Pin FineLine BGA	1152-Pin FineLine BGA	1517-Pin FineLine BGA	1760- Pin FineLine BGA
EP4SE230	56 Rx or eTx + 56 Tx or eTx	—	—	—
EP4SE360	56 Rx or eTx + 56 Tx or eTx (4)	88 Rx or eTx + 88 Tx or eTx	—	—
EP4SE530	—	88 Rx or eTx + 88 Tx or eTx (5)	112 Rx or eTx + 112 Tx or eTx (6)	112 Rx or eTx + 112 Tx or eTx
EP4SE820	—	88 Rx or eTx + 88 Tx or eTx	112 Rx or eTx + 112 Tx or eTx	132 Rx or eTx + 132 Tx or eTx

Notes to Table 8–1:

(1) Receiver (Rx) = true LVDS input buffers with OCT R_D, Transmitter (Tx) = true LVDS output buffers, eTx = emulated LVDS output buffers (either LVDS_E_1R or LVDS_E_3R).
(2) The LVDS Rx and Tx channels are equally divided between the left and right sides of the device.
(3) The LVDS channel count does not include dedicated clock input pins.
(4) EP4SE360 devices are offered in the H780 package instead of the F780 package.
(5) EP4SE530 devices are offered in the H1152 package instead of the F1152 package.
(6) EP4SE530 devices are offered in the H1517 package instead of the F1517 package.

Table 8–2. LVDS Channels Supported in Stratix IV E Device Column I/O Banks (1), (2), (3)

Device	780-Pin FineLine BGA	1152-Pin FineLine BGA	1517-Pin FineLine BGA	1760-Pin FineLine BGA
EP4SE230	64 Rx or eTx + 64 eTx	—	—	—
EP4SE360	64 Rx or eTx + 64 eTx (4)	96 Rx or eTx + 96 eTx	—	—
EP4SE530	—	96 Rx or eTx + 96 eTx (5)	128 Rx or eTx + 128 eTx (6)	128 Rx or eTx + 128 eTx
EP4SE820	—	96 Rx or eTx + 96 eTx	128 Rx or eTx + 128 eTx	144 Rx or eTx + 144 eTx

Notes to Table 8–2:

(1) Rx = true LVDS input buffers without OCT R_D, eTx = emulated LVDS output buffers (either LVDS_E_1R or LVDS_E_3R).
(2) The LVDS Rx and Tx channels are equally divided between the top and bottom sides of the device.
(3) The LVDS channel count does not include dedicated clock input pins.
(4) EP4SE360 devices are offered in the H780 package instead of the F780 package.
(5) EP4SE530 devices are offered in the H1152 package instead of the F1152 package.
(6) EP4SE530 devices are offered in the H1517 package instead of the F1517 package.

Table 8–3 and Table 8–4 list the maximum number of row and column LVDS I/Os supported in Stratix IV GT devices.

Table 8–3. LVDS Channels Supported in Stratix IV GT Device Row I/O Banks (1), (2)

Device	1517-pin FineLine BGA	1932-pin FineLine BGA
EP4S40G2	46 Rx or eTx + 73 Tx or eTx	—
EP4S40G5	46 Rx or eTx + 73 Tx or eTx	—
EP4S100G2	46 Rx or eTx + 73 Tx or eTx	—
EP4S100G3	—	47 Rx or eTx + 56 Tx or eTx
EP4S100G4	—	47 Rx or eTx + 56 Tx or eTx
EP4S100G5	46 Rx or eTx + 73 Tx or eTx	47 Rx or eTx + 56 Tx or eTx

Notes to Table 8–3:

(1) Rx = true LVDS input buffers with OCT R_D, eTx = emulated LVDS output buffers (either LVDS_E_1R or LVDS_E_3R).

(2) The LVDS Rx and Tx channel count does not include dedicated clock input pins.

Table 8–4. LVDS Channels Supported in Stratix IV GT Device Column I/O Banks (1), (2)

Device	1517-pin FineLine BGA	1932-pin FineLine BGA
EP4S40G2	96 Rx or eTx + 96 eTx	—
EP4S40G5	96 Rx or eTx + 96 eTx	—
EP4S100G2	96 Rx or eTx + 96 eTx	—
EP4S100G3	—	128 Rx or eTx + 128 eTx
EP4S100G4	—	128 Rx or eTx + 128 eTx
EP4S100G5	96 Rx or eTx + 96 eTx	128 Rx or eTx + 128 eTx

Notes to Table 8–4:

(1) Rx = true LVDS input buffers without OCT R_D, eTx = emulated LVDS output buffers (either LVDS_E_1R or LVDS_E_3R).

(2) The LVDS Rx and Tx channel count does not include dedicated clock input pins.

Table 8–5 and Table 8–6 list the maximum number of row and column LVDS I/Os supported in Stratix IV GX devices.

Table 8–5. LVDS Channels Supported in Stratix IV GX Device Row I/O Banks (1), (2), (3) (Part 1 of 2)

Device	780-Pin FineLine BGA	1152-Pin FineLine BGA	1152-Pin FineLine BGA (4)	1517-Pin FineLine BGA	1760-Pin FineLine BGA	1932-Pin FineLine BGA
EP4SGX70	28 Rx or eTx + 28 Tx or eTx	—	56 Rx or eTx + 56 Tx or eTx	—	—	—
EP4SGX110	28 Rx or eTx + 28 Tx or eTx	28 Rx or eTx + 28 Tx or eTx	56 Rx or eTx + 56 Tx or eTx	—	—	—
EP4SGX180	28 Rx or eTx + 28 Tx or eTx	44 Rx or eTx + 44 Tx or eTx	44 Rx or eTx + 44 Tx or eTx	88 Rx or eTx + 88 Tx or eTx	—	—
EP4SGX230	28 Rx or eTx + 28 Tx or eTx	44 Rx or eTx + 44 Tx or eTx	44 Rx or eTx + 44 Tx or eTx	88 Rx or eTx + 88 Tx or eTx	—	—
EP4SGX290	— (5)	44 Rx or eTx + 44 Tx or eTx	44 Rx or eTx + 44 Tx or eTx	88 Rx or eTx + 88 Tx or eTx	88 Rx or eTx + 88 Tx or eTx	98 Rx or eTx + 98 Tx or eTx

Table 8–5. LVDS Channels Supported in Stratix IV GX Device Row I/O Banks (1), (2), (3) (Part 2 of 2)

Device	780-Pin FineLine BGA	1152-Pin FineLine BGA	1152-Pin FineLine BGA (4)	1517-Pin FineLine BGA	1760-Pin FineLine BGA	1932-Pin FineLine BGA
EP4SGX360	— (5)	44 Rx or eTx + 44 Tx or eTx	44 Rx or eTx + 44 Tx or eTx	88 Rx or eTx + 88 Tx or eTx	88 Rx or eTx + 88 Tx or eTx	98 Rx or eTx + 98 Tx or eTx
EP4SGX530	—	—	44 Rx or eTx + 44 Tx or eTx (6)	88 Rx or eTx + 88 Tx or eTx (7)	88 Rx or eTx + 88 Tx or eTx	98 Rx or eTx + 98 Tx or eTx

Notes to Table 8–5:

(1) Rx = true LVDS input buffers with OCT R_D, Tx = true LVDS output buffers, eTx = emulated LVDS output buffers (either LVDS_E_1R or LVDS_E_3R).
(2) The LVDS Rx and Tx channels are equally divided between the left and right sides of the device, except for the devices in the 780-pin Fineline BGA. These devices have the LVDS Rx and Tx located on the left side of the device.
(3) The LVDS channel count does not include dedicated clock input pins.
(4) This package supports PMA-only transceiver channels.
(5) EP4SGX290 and EP4SGX360 devices are offered in the H780 package instead of the F780 package.
(6) EP4SGX530 devices are offered in the H1152 package instead of the F1152 package.
(7) EP4SGX530 devices are offered in the H1517 package instead of the F1517 package.

Table 8–6. LVDS Channels Supported in Stratix IV GX Device Column I/O Banks (1), (2), (3)

Device	780-Pin FineLine BGA	1152-Pin FineLine BGA	1152-Pin FineLine BGA (4)	1517-Pin FineLine BGA	1760-Pin FineLine BGA	1932-Pin FineLine BGA
EP4SGX70	64 Rx or eTx + 64 eTx	—	64 Rx or eTx + 64 eTx	—	—	—
EP4SGX110	64 Rx or eTx + 64 eTx	64 Rx or eTx + 64 eTx	64 Rx or eTx + 64 eTx	—	—	—
EP4SGX180	64 Rx or eTx + 64 eTx	96 Rx or eTx + 96 eTx	96 Rx or eTx + 96 eTx	96 Rx or eTx + 96 eTx	—	—
EP4SGX230	64 Rx or eTx + 64 eTx	96 Rx or eTx + 96 eTx	96 Rx or eTx + 96 eTx	96 Rx or eTx + 96 eTx	—	—
EP4SGX290	72 Rx or eTx + 72 eTx (5)	96 Rx or eTx + 96 eTx	96 Rx or eTx + 96 eTx	96 Rx or eTx + 96 eTx	128 Rx or eTx + 128 eTx	128 Rx or eTx + 128 eTx (8)
EP4SGX360	72 Rx or eTx + 72 eTx (5)	96 Rx or eTx + 96 eTx	96 Rx or eTx + 96 eTx	96 Rx or eTx + 96 eTx	128 Rx or eTx + 128 eTx	128 Rx or eTx + 128 eTx (8)
EP4SGX530	—	—	96 Rx or eTx + 96 eTx (6)	96 Rx or eTx + 96 eTx (7)	128 Rx or eTx + 128 eTx	128 Rx or eTx + 128 eTx

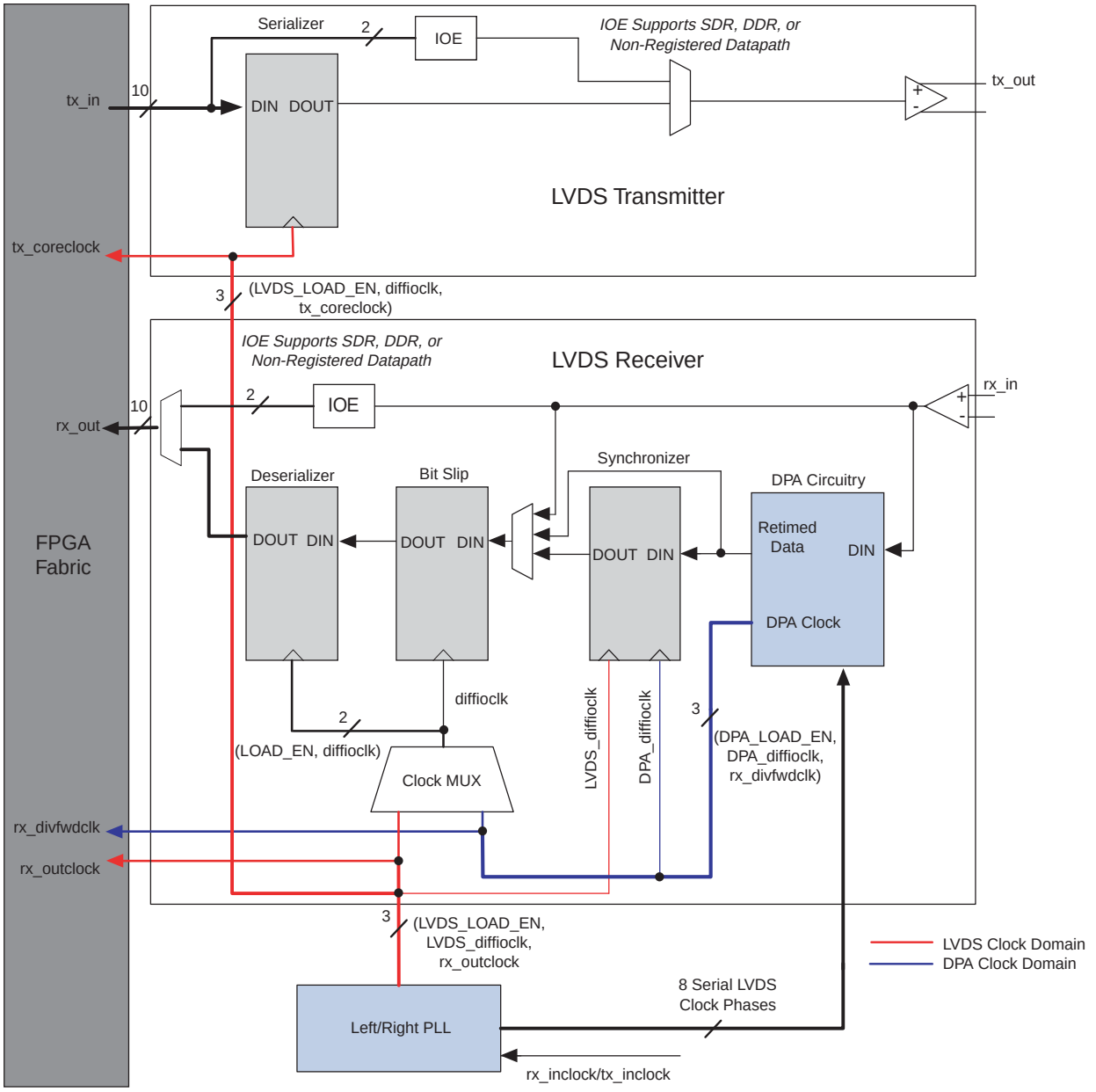
Notes to Table 8–6:

(1) Rx = true LVDS input buffers without OCT R_D, eTx = emulated LVDS output buffers (either LVDS_E_1R or LVDS_E_3R).
(2) The LVDS Rx and Tx channels are equally divided between the left and right sides of the device.
(3) The LVDS channel count does not include dedicated clock input pins.
(4) This package supports PMA-only transceiver channels.
(5) EP4SGX290 and EP4SGX360 devices are offered in the H780 package instead of the F780 package.
(6) EP4SGX530 devices are offered in the H1152 package instead of the F1152 package.
(7) EP4SGX530 devices are offered in the H1517 package instead of the F1517 package.
(8) The Quartus II software version 9.0 does not support EP4SGX290 and EP4SGX360 devices in the 1932-Pin FineLine BGA package. These devices will be supported in a future release of the Quartus II software.

LVDS SERDES

Figure 8–4 shows a transmitter and receiver block diagram for the LVDS SERDES circuitry in the left and right banks. This diagram shows the interface signals of the transmitter and receiver data path. For more information, refer to "Differential Transmitter" on page 8–11 and "Differential Receiver" on page 8–17.

Figure 8–4. LVDS SERDES *(1)*, *(2)*, *(3)*



Notes to Figure 8–4:

(1) This diagram shows a shared PLL between the transmitter and receiver. If the transmitter and receiver are not sharing the same PLL, the two left and right PLLs are required.

(2) In SDR and DDR modes, the data width is 1 and 2 bits, respectively.

(3) The `tx_in` and `rx_out` ports have a maximum data width of 10 bits.

ALTLVDS Port List

Table 8–7 lists the interface signals for an LVDS transmitter and receiver.

Table 8–7. Port List of the LVDS Interface (ALTLVDS) (1), (2) (Part 1 of 3)

Port Name	Input / Output	Description
PLL Signals		
pll_areset	Input	Asynchronous reset to the LVDS transmitter and receiver PLL. The minimum pulse width requirement for this signal is 10 ns.
LVDS Transmitter Interface Signals		
tx_in[ ]	Input	The data bus width per channel is the same as the serialization factor (SF). Input data must be synchronous to the tx_coreclock signal.
tx_inclock	Input	Reference clock input for the transmitter PLL. The ALTLVDS MegaWizard Plug-In Manager software automatically selects the appropriate PLL multiplication factor based on the data rate and reference clock frequency selection. For more information about the allowed frequency range for this reference clock, refer to the "High-Speed I/O Specification" section in the *DC and Switching Characteristics for Stratix IV Devices* chapter.
tx_enable (3)	Input	This port is instantiated only when you select the **Use External PLL** option in the MegaWizard Plug-In Manager software. This input port must be driven by the PLL instantiated though the ALTPLL MegaWizard Plug-In Manager software.
tx_out	Output	LVDS transmitter serial data output port. tx_out is clocked by a serial clock generated by the left and right PLL.
tx_outclock	Output	The frequency of this clock is programmable to be the same as the data rate, half the data rate, or one-fourth the data rate. The phase offset of this clock, with respect to the serial data, is programmable in increments of 45°.
tx_coreclock (3)	Output	FPGA fabric-transmitter interface clock. The parallel transmitter data generated in the FPGA fabric must be clocked with this clock. This port is not available when you select the **Use External PLL** option in the MegaWizard Plug-In Manager software. The FPGA fabric-transmitter interface clock must be driven by the PLL instantiated through the ALTPLL MegaWizard Plug-In Manager software.
tx_locked	Output	When high, this signal indicates that the transmitter PLL is locked to the input reference clock.

Table 8–7. Port List of the LVDS Interface (ALTLVDS) (1), (2) (Part 2 of 3)

Port Name	Input / Output	Description
LVDS Receiver Interface Signals		
rx_in	Input	LVDS receiver serial data input port.
rx_inclock	Input	Reference clock input for the receiver PLL. The ALTLVDS MegaWizard Plug-In Manager software automatically selects the appropriate PLL multiplication factor based on the data rate and reference clock frequency selection. For more information about the allowed frequency range for this reference clock, refer to the "High-Speed I/O Specification" section in the *DC and Switching Characteristics for Stratix IV Devices* chapter.
rx_channel_data_align	Input	Edge-sensitive bit-slip control signal. Each rising edge on this signal causes the data re-alignment circuitry to shift the word boundary by one bit. The minimum pulse width requirement is one parallel clock cycle. There is no maximum pulse width requirement.
rx_dpll_hold	Input	When low, the DPA tracks any dynamic phase variations between the clock and data. When high, the DPA holds the last locked phase and does not track any dynamic phase variations between the clock and data. This port is not available in non-DPA mode.
rx_enable (3)	Input	This port is instantiated only when you select the **Use External PLL** option in the MegaWizard Plug-In Manager software. This input port must be driven by the PLL instantiated though the ALTPLL MegaWizard Plug-In Manager software.
rx_out[ ]	Output	Receiver parallel data output. The data bus width per channel is the same as the deserialization factor (DF). The output data is synchronous to the rx_outclock signal in non-DPA and DPA modes. It is synchronous to the rx_divfwdclk signal in soft-CDR mode.
rx_outclock	Output	Parallel output clock from the receiver PLL. The parallel data output from the receiver is synchronous to this clock in non-DPA and DPA modes. This port is not available when you select the **Use External PLL** option in the MegaWizard Plug-In Manager software. The FPGA fabric-receiver interface clock must be driven by the PLL instantiated through the ALTPLL MegaWizard Plug-In Manager software.
rx_locked	Output	When high, this signal indicates that the receiver PLL is locked to rx_inclock.
rx dpa locked	Output	This signal only indicates an initial DPA lock condition to the optimum phase after power up or reset. This signal is not de-asserted if the DPA selects a new phase out of the eight clock phases to sample the received data. You must not use the rx_dpa_locked signal to determine a DPA loss-of-lock condition.
rx_cda_max	Output	Data re-alignment (bit slip) roll-over signal. When high for one parallel clock cycle, this signal indicates that the user-programmed number of bits for the word boundary to roll-over have been slipped.
rx_divfwdclk	Output	Parallel DPA clock to the FPGA fabric logic array. The parallel receiver output data to the FPGA fabric logic array is synchronous to this clock in soft-CDR mode. This signal is not available in non-DPA and DPA modes.
dpa_pll_recal	Input	Enable PLL calibration dynamically without resetting the DPA circuitry or the PLL.

Table 8–7. Port List of the LVDS Interface (ALTLVDS) (1), (2) (Part 3 of 3)

Port Name	Input / Output	Description
dpa_pll_cal_busy	Output	Busy signal that is asserted high when the PLL calibration occurs.
Reset Signals		
rx_reset	Input	Asynchronous reset to the DPA circuitry and FIFO. The minimum pulse width requirement for this reset is one parallel clock cycle. This signal resets DPA and FIFO blocks.
rx_fifo_reset	Input	Asynchronous reset to the FIFO between the DPA and the data realignment circuits. The synchronizer block must be reset after a DPA loses lock condition and the data checker shows corrupted received data. The minimum pulse width requirement for this reset is one parallel clock cycle. This signal resets the FIFO block.
rx_cda_reset	Input	Asynchronous reset to the data realignment circuitry. The minimum pulse width requirement for this reset is one parallel clock cycle. This signal resets the data realignment block.

Notes to Table 8–7:

(1) Unless stated, signals are valid in all three modes (non-DPA, DPA, and soft-CDR) for a single channel.
(2) All reset and control signals are active high.
(3) For more information, refer to "LVDS Interface with the Use External PLL Option Enabled" on page 8–26.

For more information about the LVDS transmitter and receiver settings using ALTLVDS_TX and ALTLVDS_RX megafunction, refer to the *ALTLVDS Megafunction User Guide*.

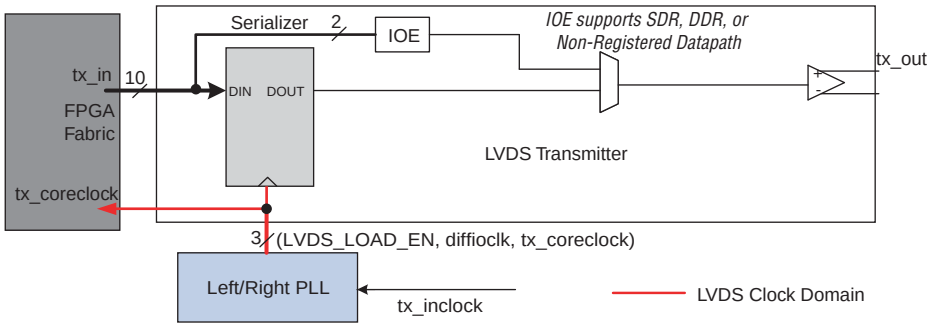
Differential Transmitter

The Stratix IV transmitter has a dedicated circuitry to provide support for LVDS signaling. The dedicated circuitry consists of a differential buffer, a serializer, and left and right PLLs that can be shared between the transmitter and receiver. The differential buffer can drive out LVDS, mini-LVDS, and RSDS signaling levels. The serializer takes up to 10 bits wide parallel data from the FPGA fabric, clocks it into the load registers, and serializes it using shift registers clocked by the left and right PLL before sending the data to the differential buffer. The MSB of the parallel data is transmitted first.

When using emulated LVDS I/O standards at the differential transmitter, the SERDES circuitry must be implemented in logic cells but not hard SERDES.

The load enable (LVDS_LOAD_EN) signal and the diffioclk signal (the clock running at serial data rate) generated from PLL_Lx (left PLL) or PLL_Rx (right PLL) clocks the load and shift registers. You can statically set the serialization factor to ×3, ×4, ×6, ×7, ×8, or ×10 using the Quartus II software. The load enable signal is derived from the serialization factor setting. Figure 8–5 shows a block diagram of the Stratix IV transmitter.

Figure 8–5. Stratix IV Transmitter (1), (2)



Notes to Figure 8–5:

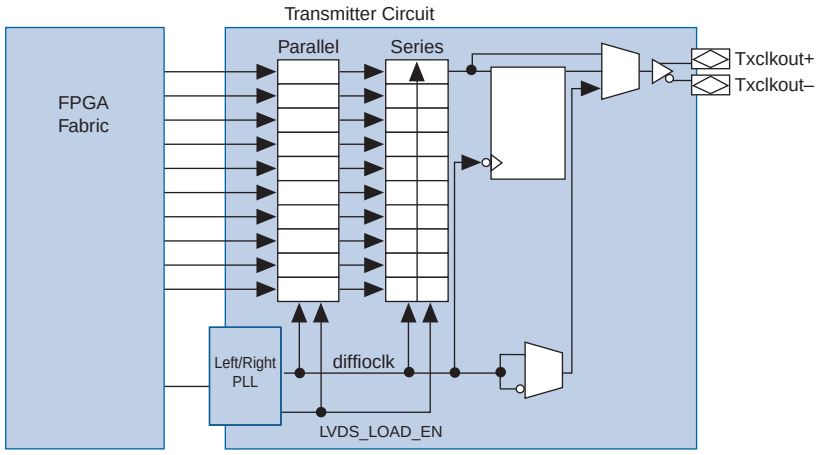
(1) In SDR and DDR modes, the data width is 1 and 2 bits, respectively.

(2) The tx_in port has a maximum data width of 10 bits.

You can configure any Stratix IV transmitter data channel to generate a source-synchronous transmitter clock output. This flexibility allows the placement of the output clock near the data outputs to simplify board layout and reduce clock-to-data skew. Different applications often require specific clock-to-data alignments or specific data-rate-to-clock-rate factors. The transmitter can output a clock signal at the same rate as the data with a maximum frequency of 800 MHz. The output clock can also be divided by a factor of 1, 2, 4, 6, 8, or 10, depending on the serialization factor. You can set the phase of the clock in relation to the data at 0° or 180° (edge or center aligned). The left and right PLLs (PLL_Lx and PLL_Rx) provide additional support for other phase shifts in 45° increments. These settings are made statically in the Quartus II MegaWizard Plug-In Manager software.

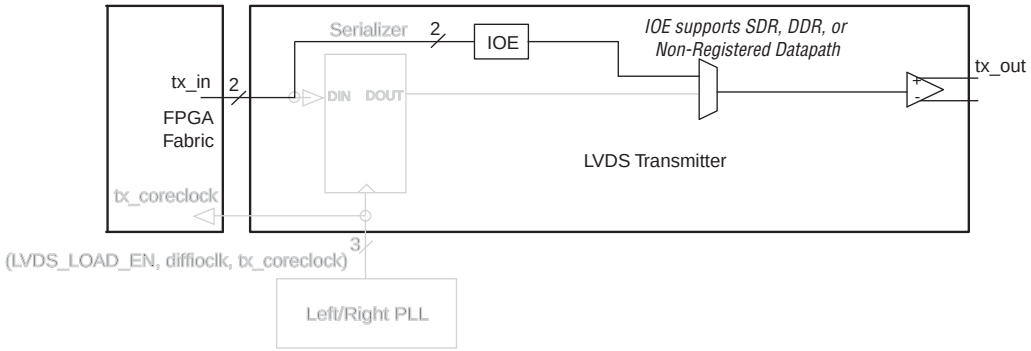
Figure 8–6 shows the Stratix IV transmitter in clock output mode. In clock output mode, you can use an LVDS channel as a clock output channel.

Figure 8–6. Stratix IV Transmitter in Clock Output Mode



You can bypass the Stratix IV serializer to support DDR (×2) and SDR (×1) operations to achieve a serialization factor of 2 and 1, respectively. The I/O element (IOE) contains two data output registers that can each operate in either DDR or SDR mode. Figure 8–7 shows the serializer bypass path.

Figure 8–7. Serializer Bypass in Stratix IV Devices *(1)*, *(2)*, *(3)*



Notes to Figure 8–7:

(1) All disabled blocks and signals are grayed out.

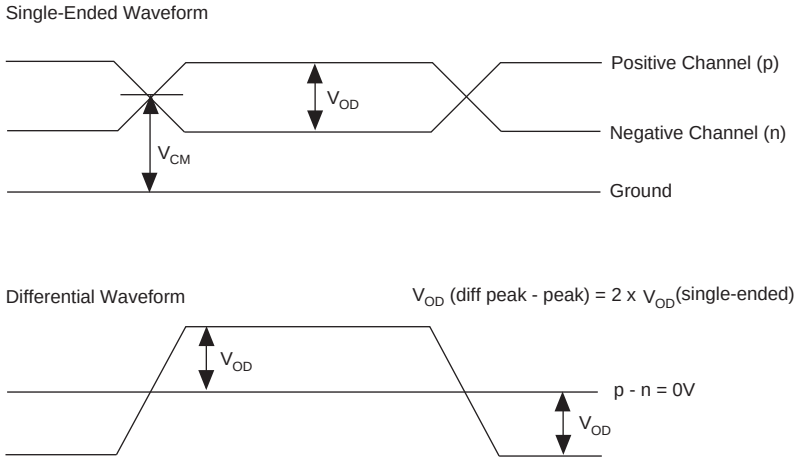
(2) In DDR mode, `tx_inclock` clocks the IOE register. In SDR mode, data is directly passed through the IOE.

(3) In SDR and DDR modes, the data width to the IOE is 1 and 2 bits, respectively.

Programmable V_{OD} and Programmable Pre-Emphasis

Stratix IV LVDS transmitters support programmable pre-emphasis and programmable V_{OD}. Pre-emphasis increases the amplitude of the high-frequency component of the output signal, and thus helps to compensate for the frequency-dependent attenuation along the transmission line. Figure 8–8 shows the differential LVDS output.

Figure 8–8. Differential V_{OD} (1)

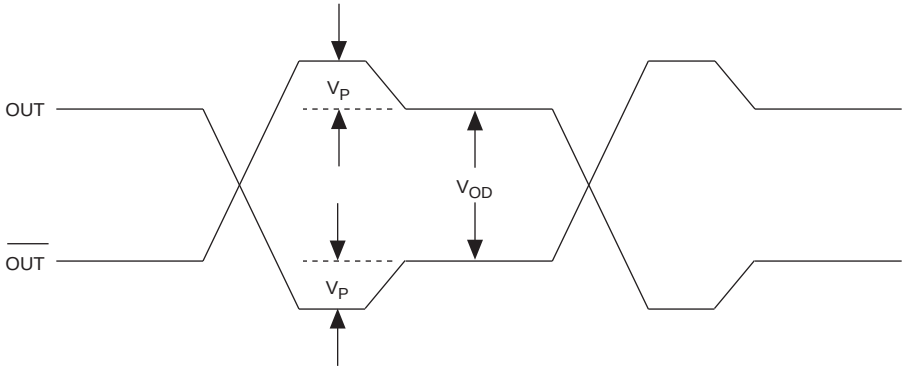


Note to Table 8–8:

(1) The Stratix IV GX device does not provide V_{CM} on the LVDS receiver pin. You must perform external biasing for AC-coupled links.

Figure 8–9 shows the LVDS output with pre-emphasis.

Figure 8–9. Programmable Pre-Emphasis (1)



Note to Figure 8–9:

(1) V_P— voltage boost from pre-emphasis. V_{OD}— Differential output voltage (peak-peak).

Pre-emphasis is an important feature for high-speed transmission. Without pre-emphasis, the output current is limited by the V_{OD} setting and the output impedance of the driver. At high frequency, the slew rate may not be fast enough to reach full V_{OD} before the next edge, producing pattern-dependent jitter.

With pre-emphasis, the output current is boosted momentarily during switching to increase the output slew rate. The overshoot introduced by the extra current happens only during switching and does not ring, unlike the overshoot caused by signal reflection. The amount of pre-emphasis needed depends on the attenuation of the high-frequency component along the transmission line. The Quartus II software allows four settings for programmable pre-emphasis—zero (**0**), low (**1**), medium (**2**), and high (**3**). The default setting is low.

The V_{OD} is also programmable with four settings: low (**0**), medium low (**1**), medium high (**2**), and high (**3**). The default setting is medium low.

Programmable V_{OD}

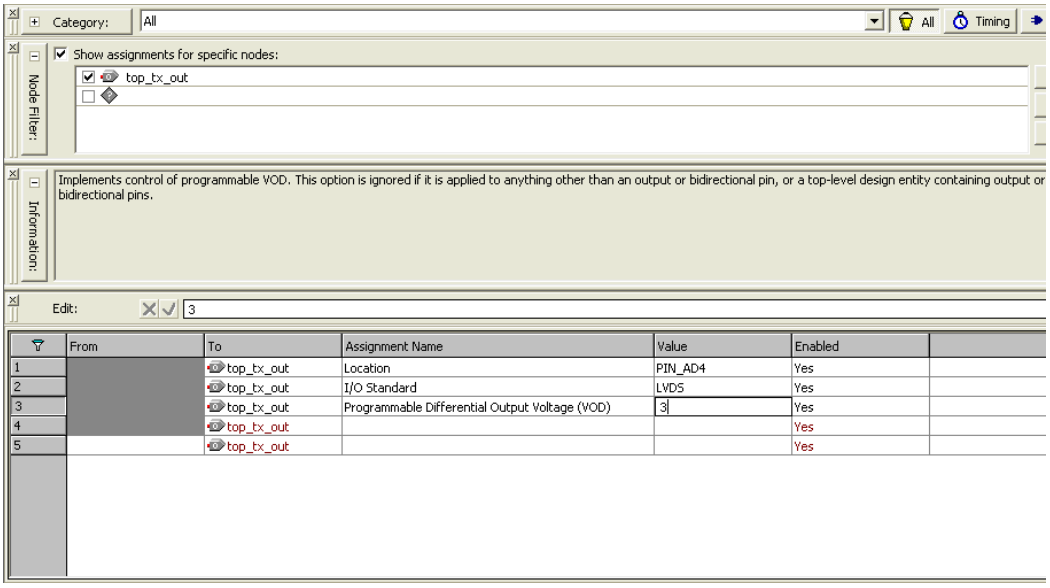
You can statically assign the V_{OD} settings from the Assignment Editor. Table 8–8 lists the assignment name for programmable V_{OD} and its possible values in the Quartus II software Assignment Editor.

Table 8–8. Quartus II Software Assignment Editor

To	tx_out
Assignment name	Programmable Differential Output Voltage (V_{OD})
Allowed values	0, 1, 2, 3

Figure 8–10 shows the assignment of programmable V_{OD} for a transmit data output from the Quartus II software Assignment Editor.

Figure 8–10. Quartus II Software Assignment Editor—Programmable V_{OD}



Programmable Pre-Emphasis

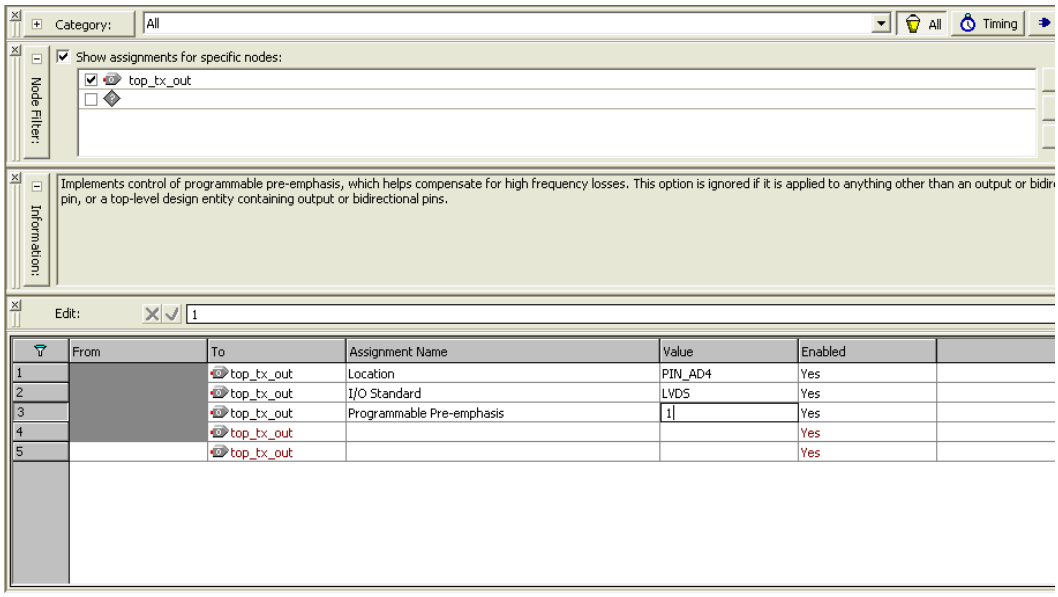
Four different settings are allowed for pre-emphasis from the Assignment Editor for each LVDS output channel. Table 8–9 lists the assignment name and its possible values for programmable pre-emphasis in the Quartus II software Assignment Editor.

Table 8–9. Quartus II Software Assignment Editor

To	tx_out
Assignment name	Programmable Pre-emphasis
Allowed values	0, 1, 2, 3

Figure 8–11 shows the assignment of programmable pre-emphasis for a transmit data output port from the Quartus II software Assignment Editor.

Figure 8–11. Quartus II Software Assignment Editor – Programmable Pre-Emphasis



Differential Receiver

The Stratix IV device family has a dedicated circuitry to receive high-speed differential signals in row I/Os. Figure 8–12 shows the hardware blocks of the Stratix IV receiver. The receiver has a differential buffer and left and right PLLs that can be shared between the transmitter and receiver, a DPA block, a synchronizer, a data realignment block, and a deserializer. The differential buffer can receive LVDS, mini-LVDS, and RSDS signal levels, which are statically set in the Quartus II software Assignment Editor.

The left and right PLL receives the external clock input and generates different phases of the same clock. The DPA block chooses one of the clocks from the left and right PLL and aligns the incoming data on each channel. The synchronizer circuit is a 1 bit wide by 6 bit deep FIFO buffer that compensates for any phase difference between the DPA clock and the data realignment block. If necessary, the user-controlled data realignment circuitry inserts a single bit of latency in the serial bit stream to align to the word boundary. The deserializer includes shift registers and parallel load registers, and sends a maximum of 10 bits to the internal logic.

The Stratix IV device family supports three different receiver modes:

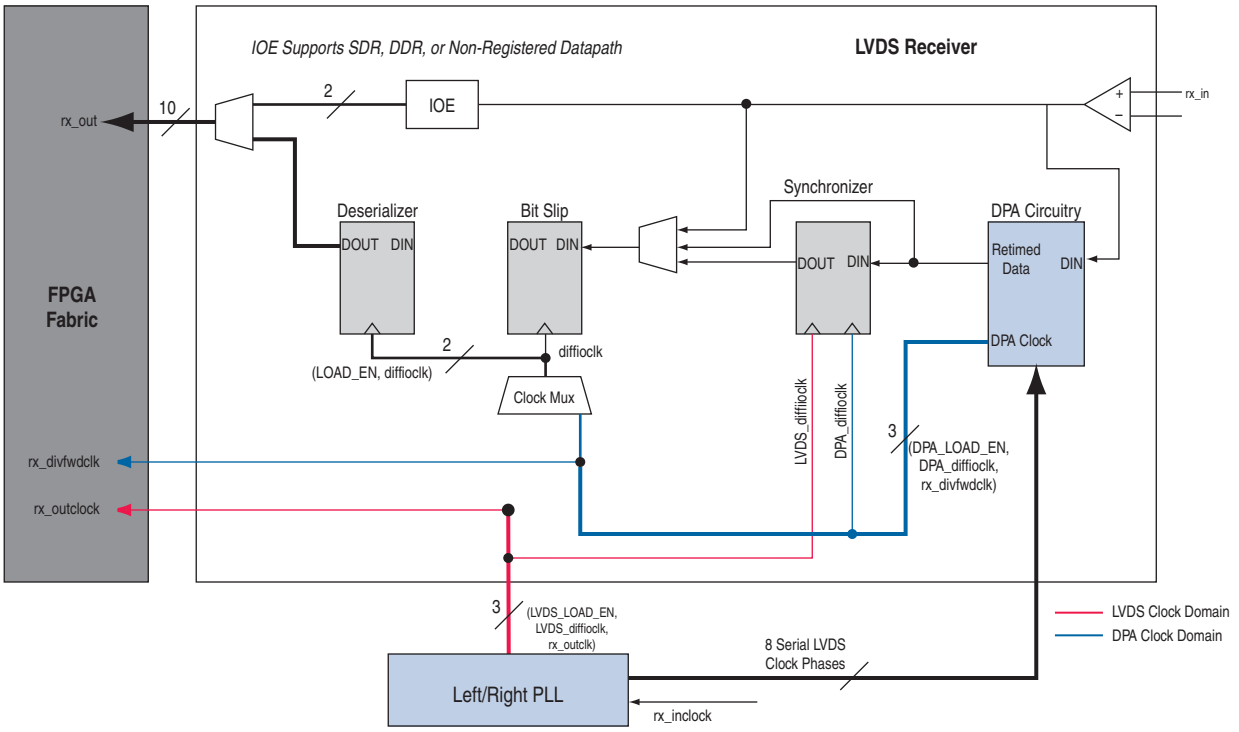
- "Non-DPA Mode" on page 8–22
- "DPA Mode" on page 8–24
- "Soft-CDR Mode" on page 8–25

The physical medium connecting the transmitter and receiver LVDS channels may introduce skew between the serial data and the source-synchronous clock. The instantaneous skew between each LVDS channel and the clock also varies with the jitter on the data and clock signals as seen by the receiver. The three different modes—non-DPA, DPA, and soft-CDR—provide different options to overcome skew between the source synchronous clock (non-DPA, DPA) /reference clock (soft-CDR) and the serial data.

Only non-DPA mode requires manual skew adjustment.

Non-DPA mode allows you to statically select the optimal phase between the source synchronous clock and the received serial data to compensate skew. In DPA mode, the DPA circuitry automatically chooses the best phase to compensate for the skew between the source synchronous clock and the received serial data. Soft-CDR mode provides opportunities for synchronous and asynchronous applications for chip-to-chip and short reach board-to-board applications for SGMII protocols.

Figure 8–12. Receiver Block Diagram *(1)*, *(2)*



Notes to Figure 8–12:

(1) In SDR and DDR modes, the data width from the IOE is 1 and 2 bits, respectively.

(2) The `rx_out` port has a maximum data width of 10 bits.

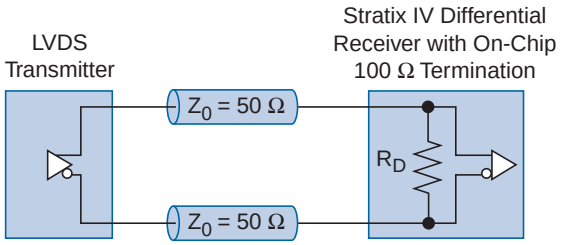
Differential I/O Termination

The Stratix IV device family provides a 100-Ω, on-chip differential termination option on each differential receiver channel for LVDS standards. On-chip termination saves board space by eliminating the need to add external resistors on the board. You can enable on-chip termination in the Quartus II software Assignment Editor.

On-chip differential termination is supported on all row I/O pins and dedicated clock input pins (`CLK[0,2,9,11]`). It is not supported for column I/O pins, dedicated clock input pins (`CLK[1,3,8,10]`), or the corner PLL clock inputs.

Figure 8–13 shows device on-chip termination.

Figure 8–13. On-Chip Differential I/O Termination



Receiver Hardware Blocks

The differential receiver has the following hardware blocks:

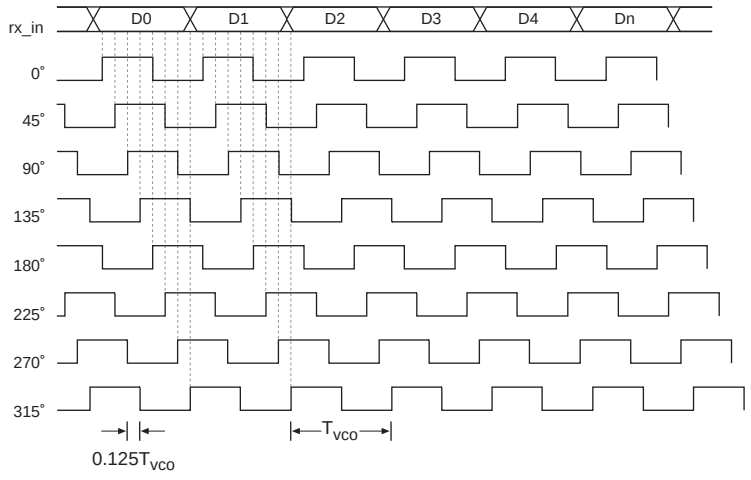
- "DPA Block" on page 8–19
- "Synchronizer" on page 8–20
- "Data Realignment Block (Bit Slip)" on page 8–20
- "Deserializer" on page 8–22

DPA Block

The DPA block takes in high-speed serial data from the differential input buffer and selects one of the eight phases generated by the left and right PLL to sample the data. The DPA chooses a phase closest to the phase of the serial data. The maximum phase offset between the received data and the selected phase is 1/8 UI, which is the maximum quantization error of the DPA. The eight phases of the clock are equally divided, offering a 45° resolution.

Figure 8–14 shows the possible phase relationships between the DPA clocks and the incoming serial data.

Figure 8–14. DPA Clock Phase to Serial Data Timing Relationship *(1)*



Note to Figure 8–14:

(1) T_{VCO} is defined as the PLL serial clock period.

The DPA block continuously monitors the phase of the incoming serial data and selects a new clock phase if needed. You can prevent the DPA from selecting a new clock phase by asserting the optional RX_DPLL_HOLD port, which is available for each channel.

DPA circuitry does not require a fixed training pattern to lock to the optimum phase out of the eight phases. After reset or power up, DPA circuitry requires transitions on the received data to lock to the optimum phase. An optional output port, RX_DPA_LOCKED, is available to indicate an initial DPA lock condition to the optimum phase after power up or reset. This signal is not de-asserted if the DPA selects a new phase out of the eight clock phases to sample the received data. Do not use the rx_dpa_locked signal to determine a DPA loss-of-lock condition. Use data checkers such as a cyclic redundancy check (CRC) or diagonal interleaved parity (DIP-4) to validate the data.

An independent reset port, RX_RESET, is available to reset the DPA circuitry. DPA circuitry must be retrained after reset.

The DPA block is bypassed in non-DPA mode.

Synchronizer

The synchronizer is a 1 bit wide and 6 bit deep FIFO buffer that compensates for the phase difference between DPA_diffioclk, which is the optimal clock selected by the DPA block, and LVDS_diffioclk, which is produced by the left and right PLL. The synchronizer can only compensate for phase differences, not frequency differences between the data and the receiver's input reference clock.

An optional port, RX_FIFO_RESET, is available to the internal logic to reset the synchronizer. The synchronizer is automatically reset when the DPA first locks to the incoming data. Altera recommends using RX_FIFO_RESET to reset the synchronizer when the DPA signals a loss-of-lock condition and the data checker indicates corrupted received data.

The synchronizer circuit is bypassed in non-DPA and soft-CDR mode.

Data Realignment Block (Bit Slip)

Skew in the transmitted data along with skew added by the link causes channel-to-channel skew on the received serial data streams. If the DPA is enabled, the received data is captured with different clock phases on each channel. This may cause the received data to be misaligned from channel to channel. To compensate for this channel-to-channel skew and establish the correct received word boundary at each channel, each receiver channel has a dedicated data realignment circuit that realigns the data by inserting bit latencies into the serial stream.

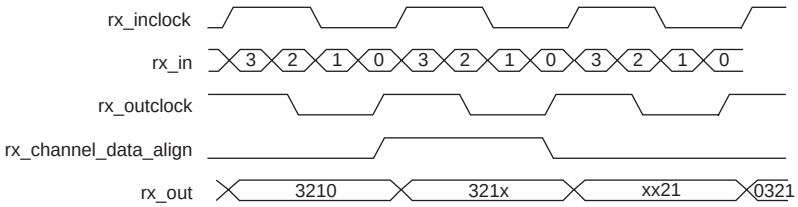
An optional RX_CHANNEL_DATA_ALIGN port controls the bit insertion of each receiver independently controlled from the internal logic. The data slips one bit on the rising edge of RX_CHANNEL_DATA_ALIGN. The requirements for the RX_CHANNEL_DATA_ALIGN signal include:

- The minimum pulse width is one period of the parallel clock in the logic array.
- The minimum low time between pulses is one period of the parallel clock.
- This is an edge-triggered signal.

- Valid data is available two parallel clock cycles after the rising edge of RX_CHANNEL_DATA_ALIGN.

Figure 8–15 shows receiver output (RX_OUT) after one bit slip pulse with the deserialization factor set to **4**.

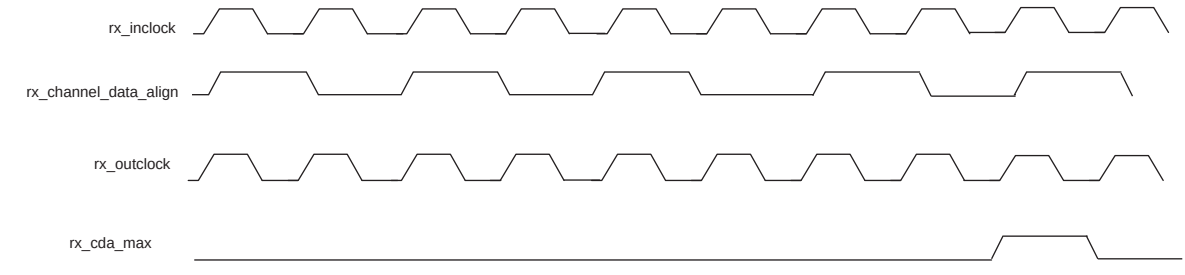
Figure 8–15. Data Realignment Timing



The data realignment circuit can have up to 11 bit-times of insertion before a rollover occurs. The programmable bit rollover point can be from 1 to 11 bit-times, independent of the deserialization factor. The programmable bit rollover point must be set equal to or greater than the deserialization factor, allowing enough depth in the word alignment circuit to slip through a full word. You can set the value of the bit rollover point using the MegaWizard Plug-In Manager software. An optional status port, RX_CDA_MAX, is available to the FPGA fabric from each channel to indicate when the preset rollover point is reached.

Figure 8–16 shows a preset value of four bit-times before rollover occurs. The rx_cda_max signal pulses for one rx_outclock cycle to indicate that rollover has occurred.

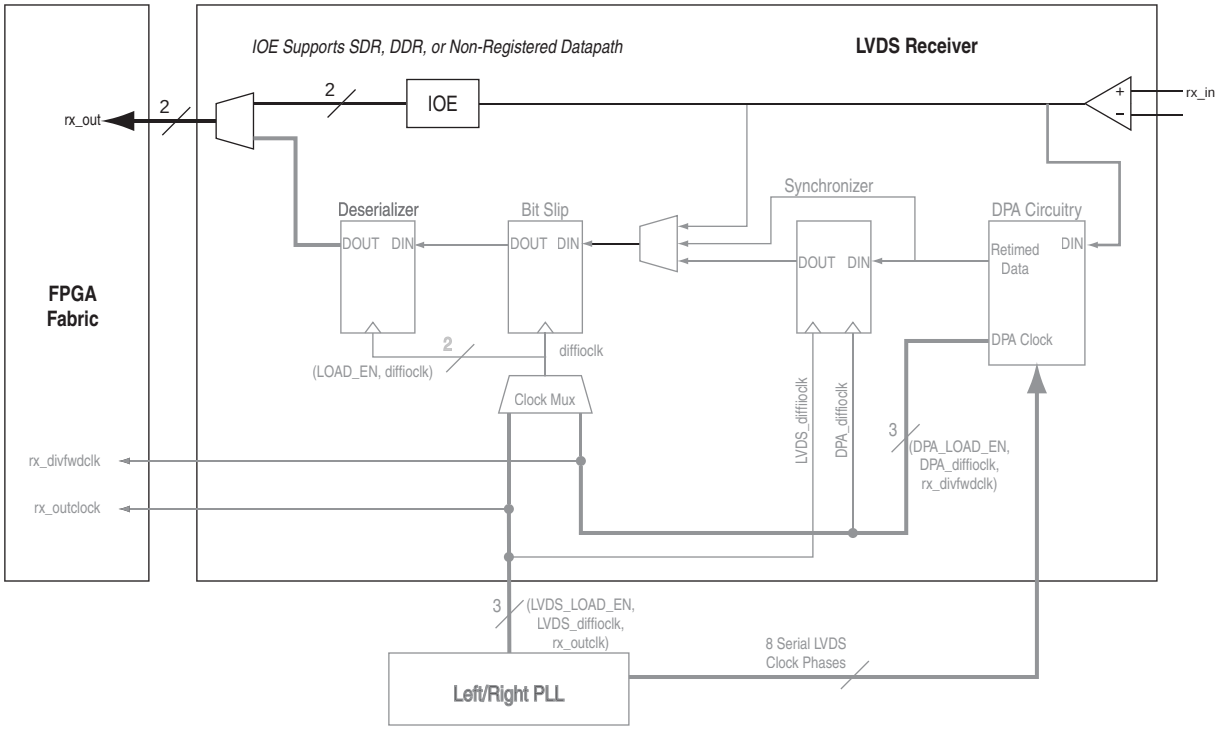
Figure 8–16. Receiver Data Re-alignment Rollover



Deserializer

You can statically set the deserialization factor to 3, 4, 6, 7, 8, or 10 by using the Quartus II software. You can bypass the Stratix IV deserializer in the Quartus II MegaWizard Plug-In Manager software to support DDR (×2) or SDR (×1) operations, as shown Figure 8–17. The DPA and data realignment circuit cannot be used when the deserializer is bypassed. The IOE contains two data input registers that can operate in DDR or SDR mode.

Figure 8–17. Deserializer Bypass in Stratix IV Devices (1), (2), (3)



Notes to Figure 8–17:

(1) All disabled blocks and signals are grayed out.

(2) In DDR mode, `rx_inclock` clocks the IOE register. In SDR mode, data is directly passed through the IOE.

(3) In SDR and DDR modes, the data width from the IOE is 1 and 2 bits, respectively.

Receiver Data Path Modes

The Stratix IV device family supports three receiver datapath modes—non-DPA mode, DPA mode, and soft-CDR mode.

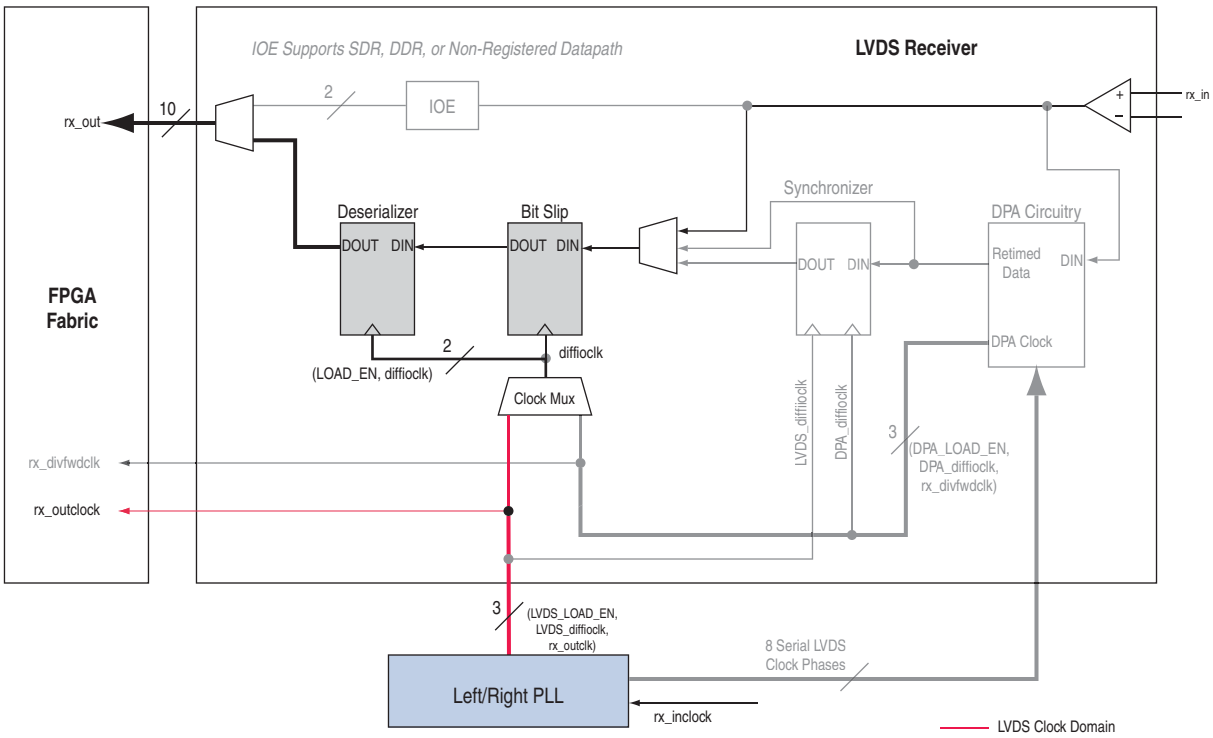
Non-DPA Mode

Figure 8–18 shows the non-DPA datapath block diagram. In non-DPA mode, the DPA and synchronizer blocks are disabled. Input serial data is registered at the rising or falling edge of the serial `LVDS_diffioclk` clock produced by the left and right PLL. You can select the rising/falling edge option using the ALTLDVS MegaWizard Plug-In Manager software. Both data realignment and deserializer blocks are clocked by the `LVDS_diffioclk` clock, which is generated by the left and right PLL.

When using non-DPA receivers, you must drive the PLL from a dedicated and compensated clock input pin. Compensated clock inputs are dedicated clock pins in the same I/O bank as the PLL.

For more information about dedicated and compensated clock inputs, refer to the *Clock Networks and PLLs in Stratix IV Devices* chapter.

Figure 8–18. Receiver Data Path in Non-DPA Mode *(1)*, *(2)*



Notes to Figure 8–18:

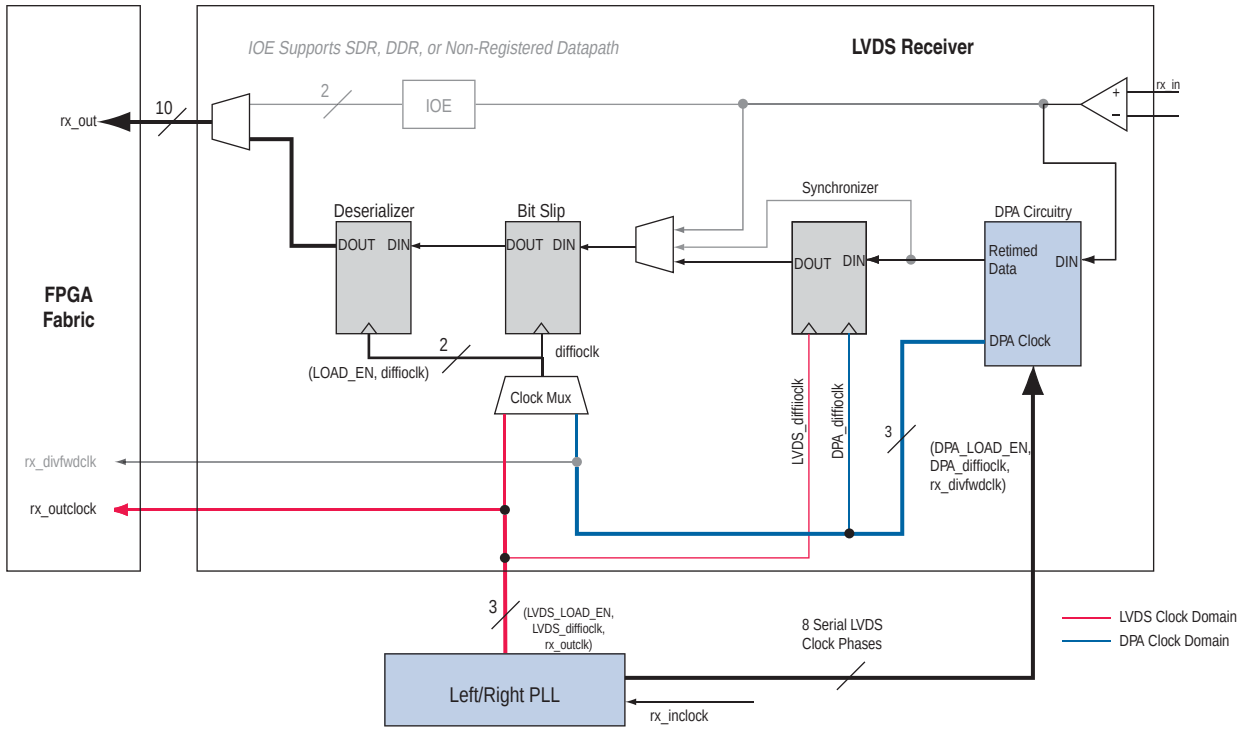
(1) In SDR and DDR modes, the data width from the IOE is 1 and 2 bits, respectively.

(2) The `rx_out` port has a maximum data width of 10 bits.

DPA Mode

Figure 8–19 shows the DPA mode datapath, where all the hardware blocks mentioned in "Receiver Hardware Blocks" on page 8–19 are active. The DPA block chooses the best possible clock (DPA_diffioclk) from the eight fast clocks sent by the left and right PLL. This serial DPA_diffioclk clock is used for writing the serial data into the synchronizer. A serial LVDS_diffioclk clock is used for reading the serial data from the synchronizer. The same LVDS_diffioclk clock is used in data realignment and deserializer blocks.

Figure 8–19. Receiver Datapath in DPA Mode (1), (2), (3)



Notes to Figure 8–19:

(1) All disabled blocks and signals are grayed out.

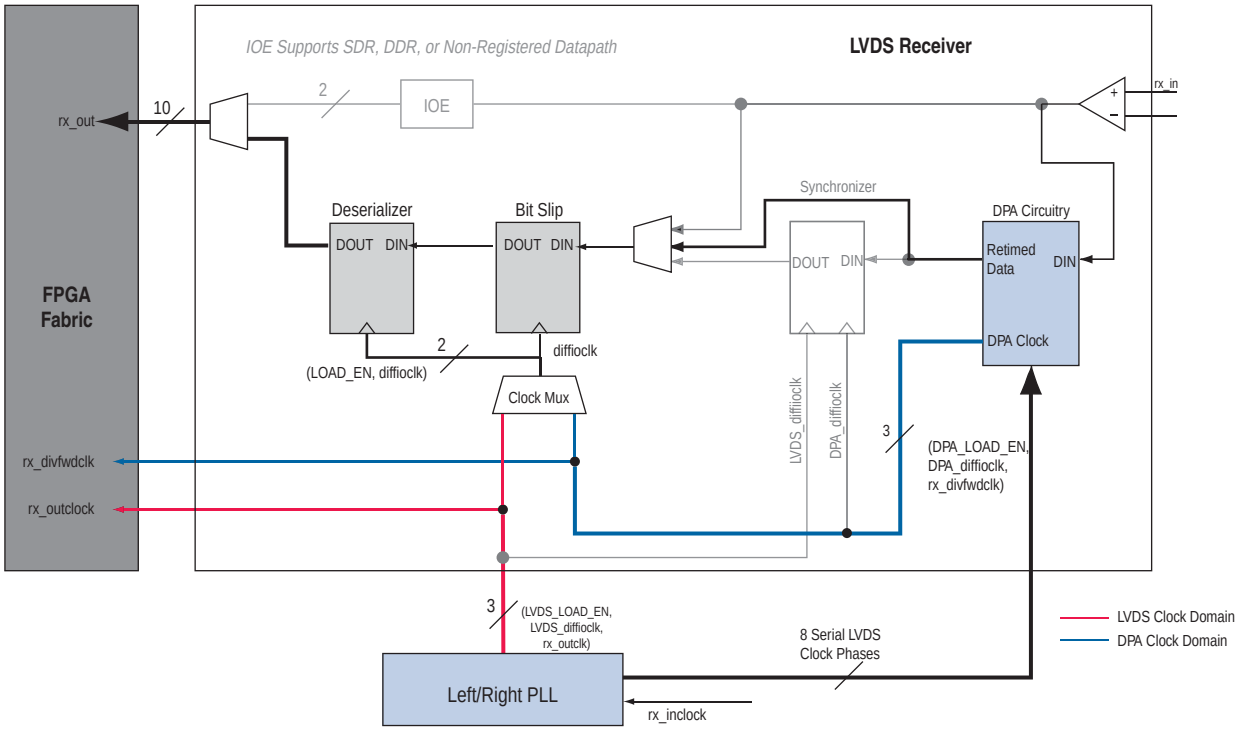
(2) In SDR and DDR modes, the data width from the IOE is 1 and 2 bits, respectively.

(3) The rx_out port has a maximum data width of 10 bits.

Soft-CDR Mode

The Stratix IV LVDS channel offers soft-CDR mode to support the Gigabit Ethernet and SGMII protocols. A receiver PLL uses the local clock source for reference. Figure 8–20 shows the soft-CDR mode datapath.

Figure 8–20. Receiver Datapath in Soft-CDR Mode (1), (2), (3)



Notes to Figure 8–20:

(1) All disabled blocks and signals are grayed out.
(2) In SDR and DDR modes, the data width from the IOE is 1 and 2 bits, respectively.
(3) The `rx_out` port has a maximum data width of 10 bits.

In soft-CDR mode, the synchronizer block is inactive. The DPA circuitry selects an optimal DPA clock phase to sample the data. Use the selected DPA clock for bit-slip operation and deserialization. The DPA block also forwards the selected DPA clock, divided by the deserialization factor called `rx_divfwdclk`, to the FPGA fabric, along with the deserialized data. This clock signal is put on the periphery clock (PCLK) network. When using soft-CDR mode, the `rx_reset` port must not be asserted after the DPA training is asserted because the DPA will continuously choose new phase taps from the PLL to track parts per million (PPM) differences between the reference clock and incoming data.

For more information about periphery clock networks, refer to the *Clock Networks and PLLs in Stratix IV Devices* chapter.

You can use every LVDS channel in soft-CDR mode and can drive the FPGA fabric using the periphery clock network in the Stratix IV device family. The rx_dpa_locked signal is not valid in soft-CDR mode because the DPA continuously changes its phase to track PPM differences between the upstream transmitter and the local receiver input reference clocks. The parallel clock rx_outclock, generated by the left and right PLL, is also forwarded to the FPGA fabric.

LVDS Interface with the Use External PLL Option Enabled

The ALTLVDS MegaWizard Plug-In Manager software provides an option for implementing the LVDS interface with the **Use External PLL** option. With this option enabled you can control the PLL settings, such as dynamically reconfiguring the PLL to support different data rates, dynamic phase shift, and other settings. You also must instantiate an ALTPLL megafunction to generate the various clock and load enable signals.

When you enable the **Use External PLL** option with the ALTLVDS transmitter and receiver, the following signals are required from the ALTPLL megafunction:

- Serial clock input to the SERDES of the ALTLVDS transmitter and receiver
- Load enable to the SERDES of the ALTLVDS transmitter and receiver
- Parallel clock used to clock the transmitter FPGA fabric logic and parallel clock used for the receiver rx_syncclock port and receiver FPGA fabric logic
- Asynchronous PLL reset port of the ALTLVDS receiver

As an example, Table 8–10 describes the serial clock output, load enable output, and parallel clock output generated on ports c0, c1, and c2, respectively, along with the locked signal of the ALTPLL instance. You can choose any of the PLL output clock ports to generate the interface clocks.

With soft SERDES, a different clocking requirement is needed. For more information, refer to the *LVDS SERDES Transmitter/Receiver (ALTLVDS_RX/TX) Megafunction User Guide*.

The high-speed clock generated from the PLL is intended to clock the LVDS SERDES circuitry only. Do not use the high-speed clock to drive other logic because the allowed frequency to drive the core logic is restricted by the PLL F_{OUT} specification. For more information about the F_{OUT} specification, refer to the *DC and Switching Characteristics for Stratix IV Devices* chapter.

Table 8–10 lists the signal interface between the output ports of the ALTPLL megafunction and the input ports of the ALTLVDS transmitter and receiver.

Table 8–10. Signal Interface Between ALTPLL and ALTLVDS_TX and ALTLVDS_RX Megafunctions (Part 1 of 2)

From the ALTPLL Megafunction	To the ALTLVDS Transmitter	To the ALTLVDS Receiver
Serial clock output (c0) (1)	tx_inclock (serial clock input to the transmitter)	rx_inclock (serial clock input)
Load enable output (c1)	tx_enable (load enable to the transmitter)	rx_enable (load enable for the deserializer)

Table 8–10. Signal Interface Between ALTPLL and ALTLVDS_TX and ALTLVDS_RX Megafunctions (Part 2 of 2)

From the ALTPLL Megafunction	To the ALTLVDS Transmitter	To the ALTLVDS Receiver
Parallel clock output (c2)	Parallel clock used inside the transmitter core logic in the FPGA fabric	rx_syncclock (parallel clock input) and parallel clock used inside the receiver core logic in the FPGA fabric
~(locked)	—	pll_areset (asynchronous PLL reset port) (2)

Notes to Table 8–10:

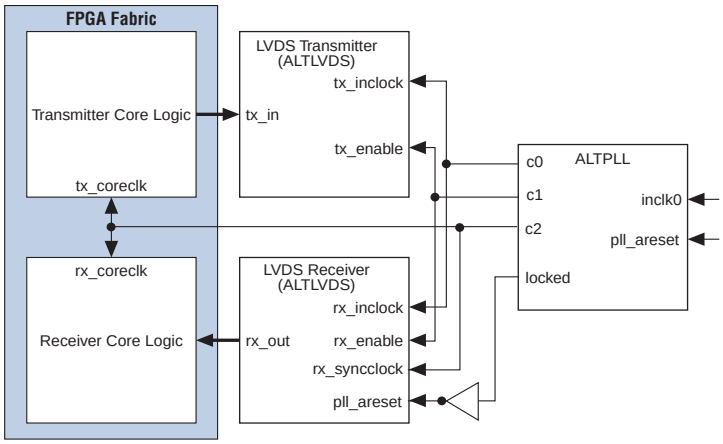
(1) The serial clock output (c0) can only drive tx_inclock on the ALTLVDS transmitter and rx_inclock on the ALTLVDS receiver. This clock cannot drive the core logic.

(2) The pll_areset signal is automatically enabled for the LVDS receiver in external PLL mode. This signal does not exist for LVDS transmitter instantiation when the external PLL option is enabled.

The rx_syncclock port is automatically enabled in an LVDS receiver in external PLL mode. The Quartus II compiler errors out if this port is not connected, as shown in Figure 8–21.

When generating the ALTPLL megafunction, the **Left/Right PLL** option is configured to set up the PLL in LVDS mode. Figure 8–21 shows the connection between the ALTPLL and ALTLVDS_TX and ALTLVDS_RX megafunctions.

Figure 8–21. LVDS Interface with the ALTPLL Megafunction (1)



Note to Figure 8–21:

(1) Instantiation of pll_areset is optional for the ALTPLL instantiation.

Example 8–1 shows how to generate three output clocks using an ALTPLL megafunction.

Example 8–1. Generating Three Output Clocks Using an ALTPLL Megafunction

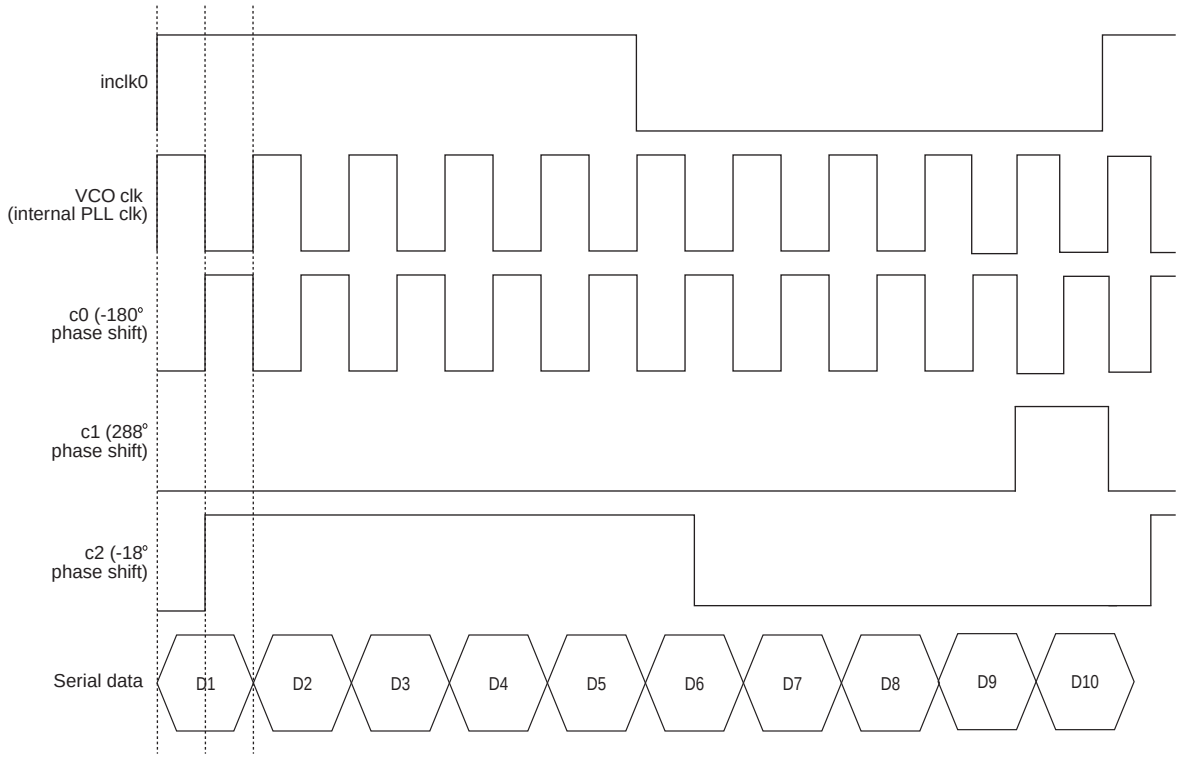
LVDS data rate = 1 Gbps; serialization factor = 10; input reference clock = 100 MHz

The following settings are used when generating the three output clocks using an ALTPLL megafunction. The serial clock must be **1000 MHz** and the parallel clock must be **100 MHz** (serial clock divided by the serialization factor):

- c0
  - Frequency = **1000 MHz** (multiplication factor = 10 and division factor = 1)
  - Phase shift = **–180°** with respect to the voltage-controlled oscillator (VCO) clock
  - Duty cycle = **50%**
- c1
  - Frequency = (1000/10) = **100 MHz** (multiplication factor = 1 and division factor = 1)
  - Phase shift = (10 - 2) × 360/10 = **288°** [(deserialization factor - 2)/deserialization factor] × 360°
  - Duty cycle = (100/10) = **10%** (100 divided by the serialization factor)
- c2
  - Frequency = (1000/10) = **100 MHz** (multiplication factor = 1 and division factor = 1)
  - Phase shift = (–180/10) = **–18°** (c0 phase shift divided by the serialization factor)
  - Duty cycle = **50%**

The Equation 8–1 calculations for phase shift assume that the input clock and serial data are edge aligned. Introducing a phase shift of –180° to sampling clock (c0) ensures that the input data is center-aligned with respect to the c0, as shown in Figure 8–22.

Figure 8–22. Phase Relationship for External PLL Interface Signals



Left and Right PLLs (PLL_Lx and PLL_Rx)

The Stratix IV device family contains up to eight left and right PLLs with up to four PLLs located on the left side and four on the right side of the device. The left PLLs can support high-speed differential I/O banks on the left side; the right PLLs can support high-speed differential I/O banks on the right side of the device. The high-speed differential I/O receiver and transmitter channels use these left and right PLLs to generate the parallel clocks (`rx_outclock` and `tx_outclock`) and high-speed clocks (`diffioclk`).

Figure 8–2 on page 8–3 and Figure 8–3 on page 8–4 show the locations of the left and right PLLs for Stratix IV E, GT, and GX devices. The PLL VCO operates at the clock frequency of the data rate. Clock switchover and dynamic reconfiguration are allowed using the left and right PLL in high-speed differential I/O support mode.

For more information, refer to the *Clock Networks and PLLs in Stratix IV Devices* chapter.

Stratix IV Clocking

The left and right PLLs feed into the differential transmitter and receive channels through the LVDS and DPA clock network. The center left and right PLLs can clock the transmitter and receive channels above and below them. The corner left and right PLLs can drive I/Os in the banks adjacent to them.

Figure 8–23 shows center PLL clocking in the Stratix IV device family. For more information about PLL clocking restrictions, refer to "Differential Pin Placement Guidelines" on page 8–38.

Figure 8–23. LVDS/DPA Clocks in the Stratix IV Device Family with Center PLLs

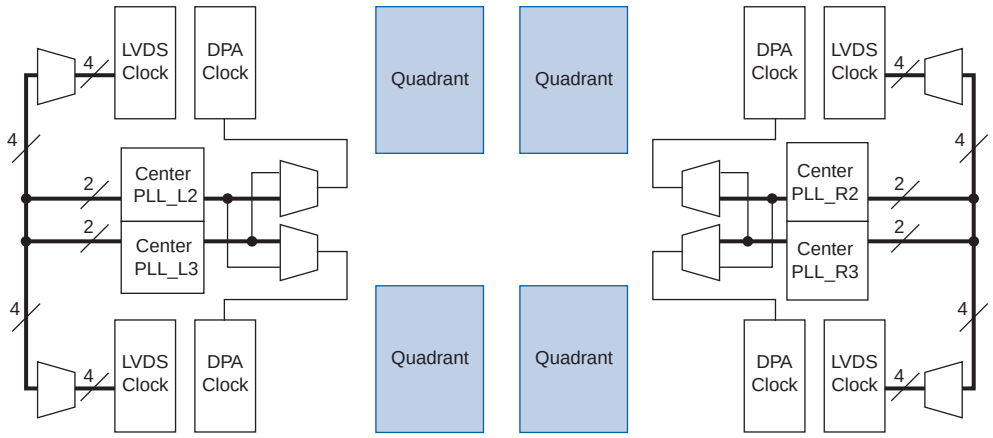
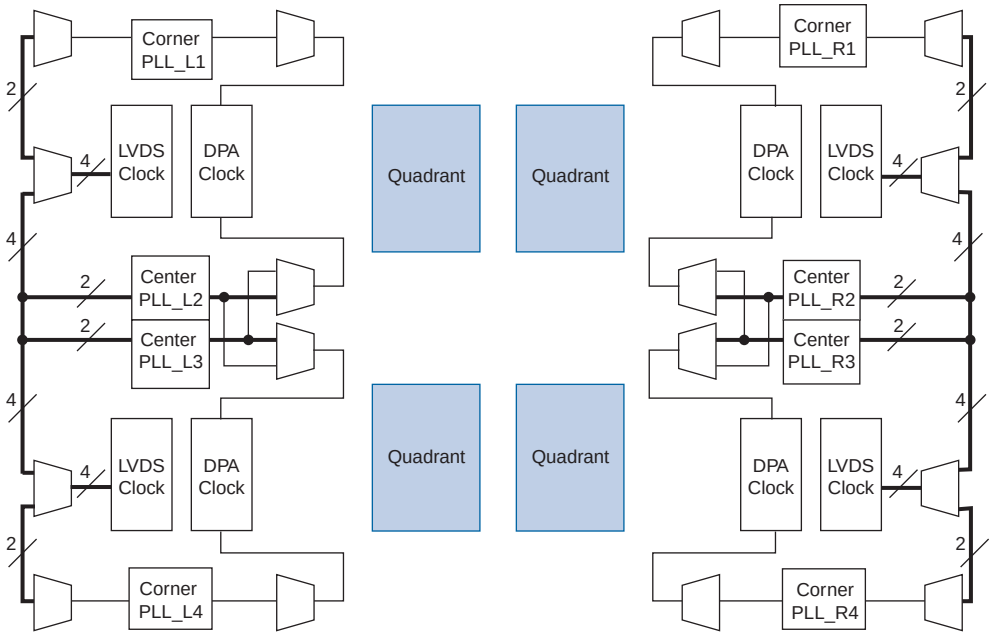


Figure 8–24 shows center and corner PLL clocking in the Stratix IV device family. For more information about PLL clocking restrictions, refer to "Differential Pin Placement Guidelines" on page 8–38.

Figure 8–24. LVDS/DPA Clocks in the Stratix IV Device Family with Center and Corner PLLs



Source-Synchronous Timing Budget

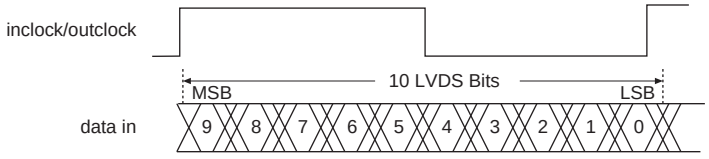
This section describes the timing budget, waveforms, and specifications for source-synchronous signaling in the Stratix IV device family. LVDS I/O standards enable high-speed data transmission. This high data transmission rate results in better overall system performance. To take advantage of fast system performance, it is important to understand how to analyze timing for these high-speed signals. Timing analysis for the differential block is different from traditional synchronous timing analysis techniques.

Instead of focusing on clock-to-output and setup times, source synchronous timing analysis is based on the skew between the data and the clock signals. High-speed differential data transmission requires the use of timing parameters provided by IC vendors and is strongly influenced by board skew, cable skew, and clock jitter. This section defines the source-synchronous differential data orientation timing parameters, the timing budget definitions for the Stratix IV device family, and how to use these timing parameters to determine a design's maximum performance.

Differential Data Orientation

There is a set relationship between an external clock and the incoming data. For operations at 1 Gbps and a serialization factor of 10, the external clock is multiplied by 10. You can set phase-alignment in the PLL to coincide with the sampling window of each data bit. The data is sampled on the falling edge of the multiplied clock. Figure 8–25 shows the data bit orientation of the ×10 mode.

Figure 8–25. Bit Orientation in the Quartus II Software



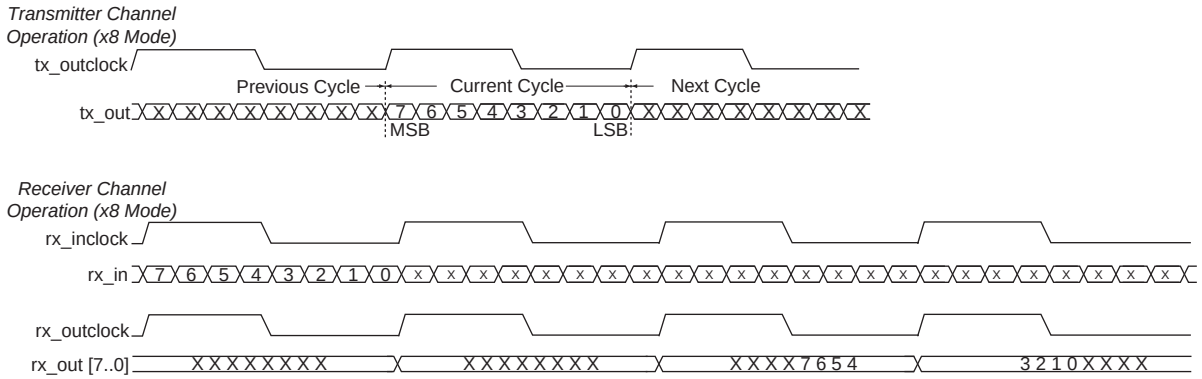
Differential I/O Bit Position

Data synchronization is necessary for successful data transmission at high frequencies. Figure 8–26 shows the data bit orientation for a channel operation. This figure is based on the following:

- Serialization factor equals the clock multiplication factor
- Edge alignment is selected for phase alignment
- Implemented in hard SERDES

For other serialization factors, use the Quartus II software tools to find the bit position within the word. Table 8–11 lists the bit positions after deserialization.

Figure 8–26. Bit-Order and Word Boundary for One Differential Channel *(1)*



Note to Figure 8–26:

(1) These are only functional waveforms and are not intended to convey timing information.

Table 8–11 lists the conventions for differential bit naming for 18 differential channels. The MSB and LSB positions increase with the number of channels used in a system.

Table 8–11. Differential Bit Naming

Receiver Channel Data Number	Internal 8-Bit Parallel Data	
	MSB Position	LSB Position
1	7	0
2	15	8
3	23	16
4	31	24
5	39	32
6	47	40
7	55	48
8	63	56
9	71	64
10	79	72
11	87	80
12	95	88
13	103	96
14	111	104
15	119	112
16	127	120
17	135	128
18	143	136

Transmitter Channel-to-Channel Skew

Transmitter channel-to-channel skew (TCCS) is an important parameter based on the Stratix IV transmitter in a source synchronous differential interface. This parameter is used in receiver skew margin calculation. For more information, refer to "Receiver Skew Margin for Non-DPA Mode" on page 8–33.

TCCS is the difference between the fastest and slowest data output transitions, including the TCO variation and clock skew. For LVDS transmitters, the TimeQuest Timing Analyzer provides a TCCS report, which shows TCCS values for serial output ports.

You can get the TCCS value from the TCCS report (`report_TCCS`) in the Quartus II compilation report under the TimeQuest Timing Analyzer, or from the *DC and Switching Characteristics for Stratix IV Devices* chapter.

Receiver Skew Margin for Non-DPA Mode

Changes in system environment, such as temperature, media (cable, connector, or PCB), and loading effect the receiver's setup and hold times; internal skew affects the sampling ability of the receiver.

Different modes of LVDS receivers use different specifications that can help in deciding the ability to sample the received serial data correctly. In DPA mode, you must use DPA jitter tolerance instead of receiver input skew margin (RSKM).

In non-DPA mode, use TCCS, RSKM, and sampling window (SW) specifications for high-speed source-synchronous differential signals in the receiver data path. The relationship between RSKM, TCCS, and SW is expressed by the RSKM equation shown in Equation 8–1.

Equation 8–1. RSKM

$$RSKM = \frac{TUI - SW - TCCS}{2}$$

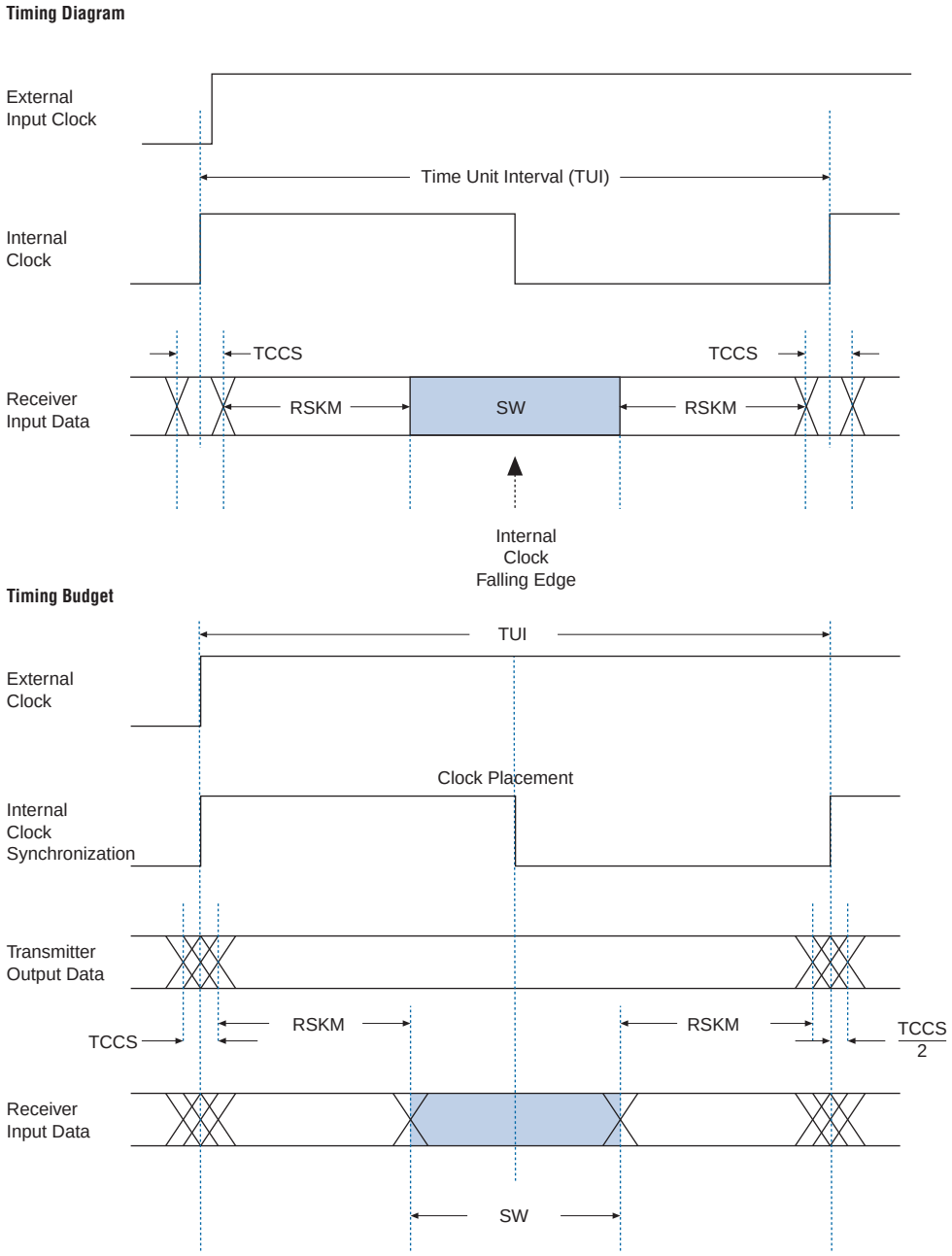
Conventions used for the equation:

- Time unit interval (TUI)—Time period of the serial data.
- RSKM—The timing margin between the receiver's clock input and the data input sampling window.
- SW—The period of time that the input data must be stable to ensure that data is successfully sampled by the LVDS receiver. The SW is a device property and varies with device speed grade.
- TCCS—The timing difference between the fastest and the slowest output edges, including t_{CO} variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement.

Figure 8–27 shows the relationship between the RSKM, TCCS, and the receiver's SW.

You must calculate the RSKM value to decide whether or not data can be sampled properly by the LVDS receiver with the given data rate and device. A positive RSKM value indicates that the LVDS receiver can sample the data properly, whereas a negative RSKM indicates that it cannot.

Figure 8–27. Differential High-Speed Timing Diagram and Timing Budget for Non-DPA Mode



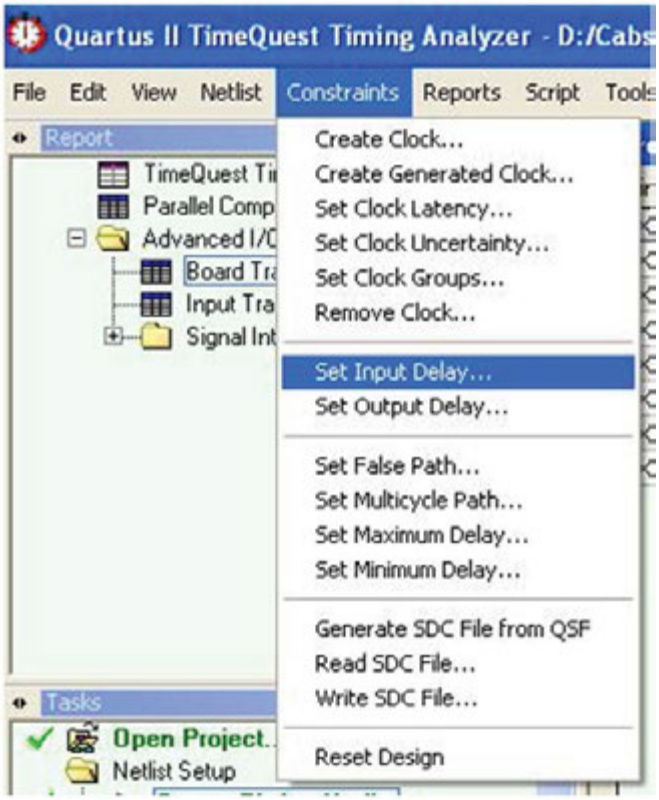
For LVDS receivers, the Quartus II software provides an RSKM report showing the SW, TUI, and RSKM values for non-DPA mode. You can generate the RSKM report by executing the `report_RSKM` command in the TimeQuest Timing Analyzer. You can find the RSKM report in the Quartus II compilation report under the TimeQuest Timing Analyzer section.

In order to obtain the RSKM value, you must assign an appropriate input delay to the LVDS receiver through the TimeQuest Timing Analyzer constraints menu.

For assigning input delay, follow these steps:

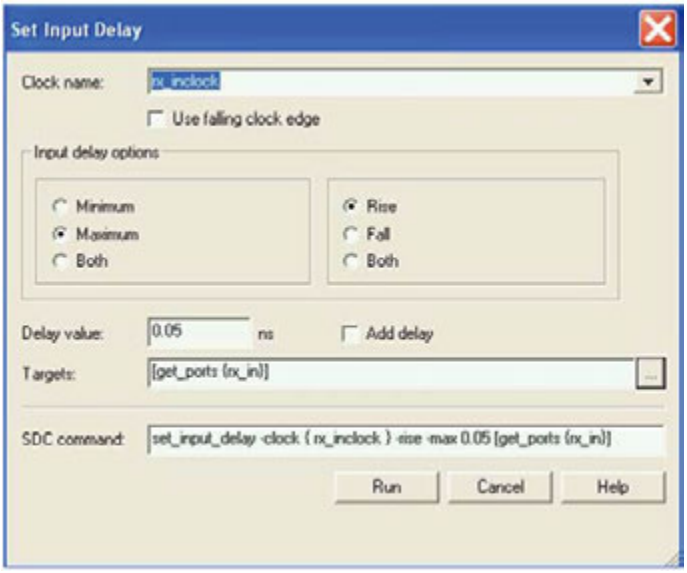
1. The Quartus II TimeQuest Timing Analyzer GUI has many options for setting the constraints and analyzing the design. Figure 8–28 shows various commands on the Constraints menu. For setting input delay, you must select the **Set Input Delay** option.

Figure 8–28. Selection of Constraint Menu in TimeQuest Timing Analyzer



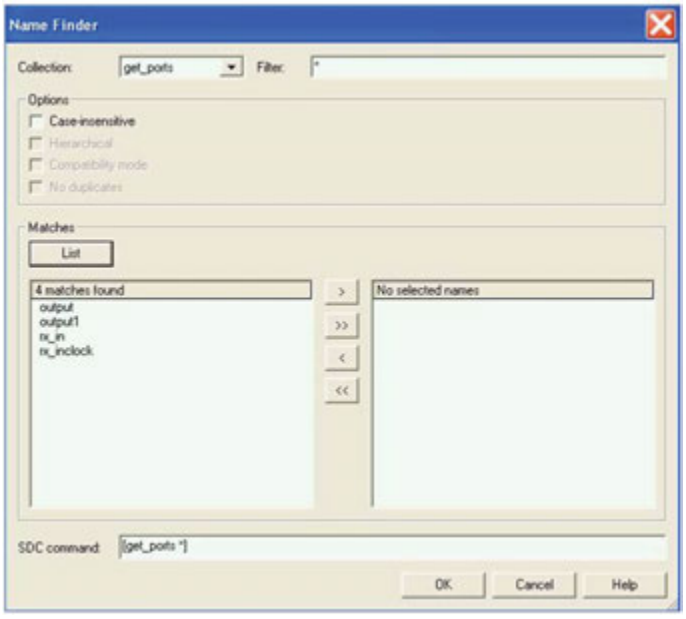
2. Figure 8–29 shows the setting parameters for the **Set Input Delay** option. The clock name must reference the source synchronous clock that feeds the LVDS receiver. Select the desired clock using the pull-down menu.

Figure 8–29. Input Time Delay Assignment Through TimeQuest Timing Analyzer



3. Figure 8–30 shows the **Targets** option. You can view a list of all available ports using the **List** option in the **Name Finder** window.

Figure 8–30. Name Finder Window in Set Input Delay Option



4. Select the LVDS receiver serial input ports (from the list) according to the input delay you set. Click **OK**.
5. In the **Set Input Delay** window, set the appropriate values in the **Input Delay Options** section and **Delay** value.
6. Click **Run** to incorporate these values in the TimeQuest Timing Analyzer.
7. Assign the appropriate delay for all the LVDS receiver input ports following these steps. If you have already assigned **Input Delay** and you need to add more delay to that input port, use the **Add Delay** option in the **Set Input Delay** window.

If no input delay is set in the TimeQuest Timing Analyzer, the receiver channel-to-channel skew (RCCS) defaults to zero. You can also directly set the input delay in a Synopsys Design Constraint file (**.sdc)** using the `set_input_delay` command.

For more information about **.sdc** commands and the TimeQuest Timing Analyzer, refer to the *Quartus II TimeQuest Timing Analyzer* chapter in volume 3 of the *Quartus II Development Software Handbook*.

Example 8–2 shows the RSKM calculation.

Example 8–2. RSKM

Data Rate: 1 Gbps, Board channel-to-channel skew = **200 ps**

For Stratix IV devices:

TCCS = **100 ps** (pending characterization)
SW = **300 ps** (pending characterization)

TUI = **1000 ps**
Total RCCS = TCCS + Board channel-to-channel skew= 100 ps + 200 ps
= **300 ps**

RSKM= **TUI - SW - RCCS**
= **1000 ps - 300 ps - 300 ps**
= **400 ps > 0**

```
Because the RSKM > 0 ps, receiver non-DPA mode must work correctly.
```

You can also calculate RSKM using the steps described in "Guidelines for DPA-Enabled Differential Channels" on page 8–38.

Differential Pin Placement Guidelines

To ensure proper high-speed operation, differential pin placement guidelines have been established. The Quartus II compiler automatically checks that these guidelines are followed and issues an error message if they are not met.

This section is divided into pin placement guidelines with and without DPA usage because DPA usage adds some constraints on the placement of high-speed differential channels.

DPA-enabled differential channels refer to DPA mode or soft-CDR mode; DPA disabled channels refer to non-DPA mode.

Guidelines for DPA-Enabled Differential Channels

The Stratix IV device family has differential receivers and transmitters in I/O banks on the left and right sides of the device. Each receiver has a dedicated DPA circuit to align the phase of the clock to the data phase of its associated channel. When you use DPA-enabled channels in differential banks, you must adhere to the guidelines listed in the following sections.

DPA-Enabled Channels and Single-Ended I/Os

When you enable a DPA channel in a bank, both single-ended I/Os and differential I/O standards are allowed in the bank.

- Single-ended I/Os are allowed in the same I/O bank, as long as the single-ended I/O standard uses the same V_{CCIO} as the DPA-enabled differential I/O bank.
- Single-ended inputs can be in the same logic array block (LAB) row as a differential channel using the SERDES circuitry.
- DDIO can be placed within the same LAB row as a SERDES differential channel but half rate DDIO (single data rate) output pins cannot be placed within the same LAB row as a receiver SERDES differential channel. The input register must be implemented within the FPGA fabric logic.

DPA-Enabled Channel Driving Distance

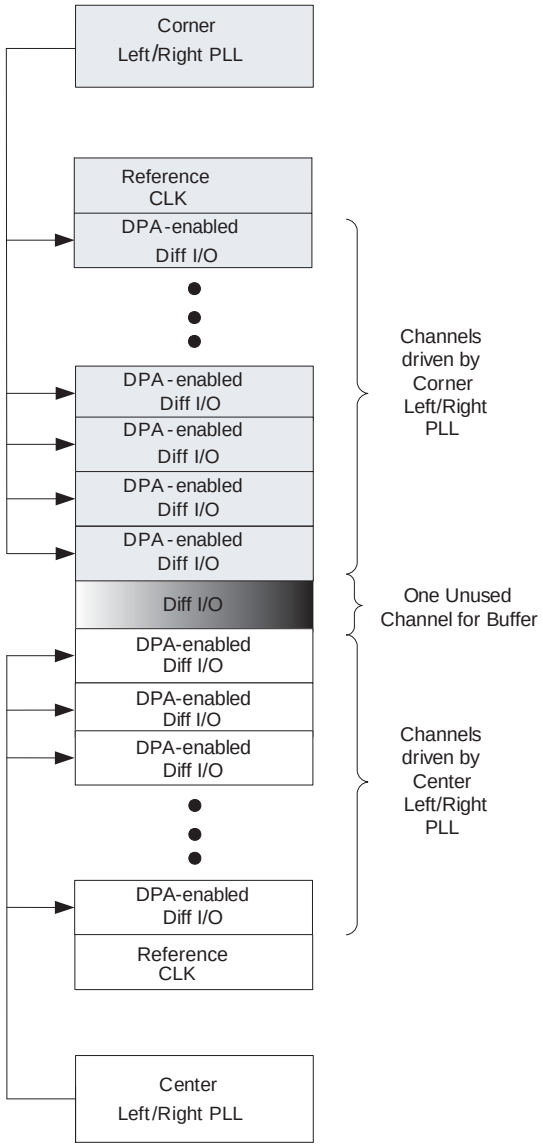
If the number of DPA channels driven by each left and right PLL exceeds 25 LAB rows, Altera recommends implementing data realignment (bit slip) circuitry for all the DPA channels.

Using Corner and Center Left and Right PLLs

If a differential bank is being driven by two left and right PLLs, where the corner left and right PLL is driving one group and the center left and right PLL is driving another group, there must be at least one row of separation between the two groups of DPA-enabled channels (refer to Figure 8–31). The two groups can operate at independent frequencies.

You do not need a separation if a single left and right PLL is driving the DPA-enabled channels as well as DPA-disabled channels.

Figure 8–31. Corner and Center Left and Right PLLs Driving DPA-Enabled Differential I/Os in the Same Bank



Using Both Center Left and Right PLLs

You can use both center left and right PLLs to drive DPA-enabled channels simultaneously, as long as they drive these channels in their adjacent banks only, as shown in Figure 8–32.

If one of the center left and right PLLs drives the top and bottom banks, you cannot use the other center left and right PLL to drive differential channels, as shown in Figure 8–32.

If the top PLL_L2 and PLL_R2 drives DPA-enabled channels in the lower differential bank, the PLL_L3 and PLL_R3 cannot drive DPA-enabled channels in the upper differential banks and vice versa. In other words, the center left and right PLLs cannot drive cross-banks simultaneously, as shown in Figure 8–33.

Figure 8–32. Center Left and Right PLLs Driving DPA-Enabled Differential I/Os

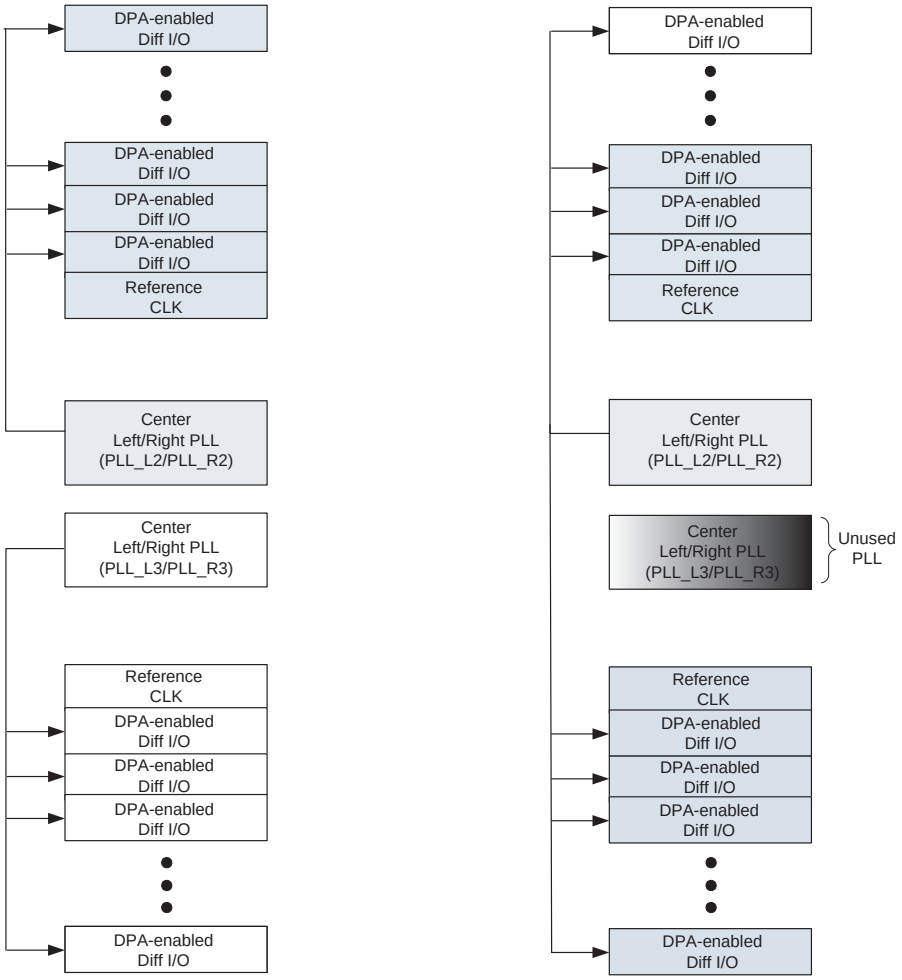
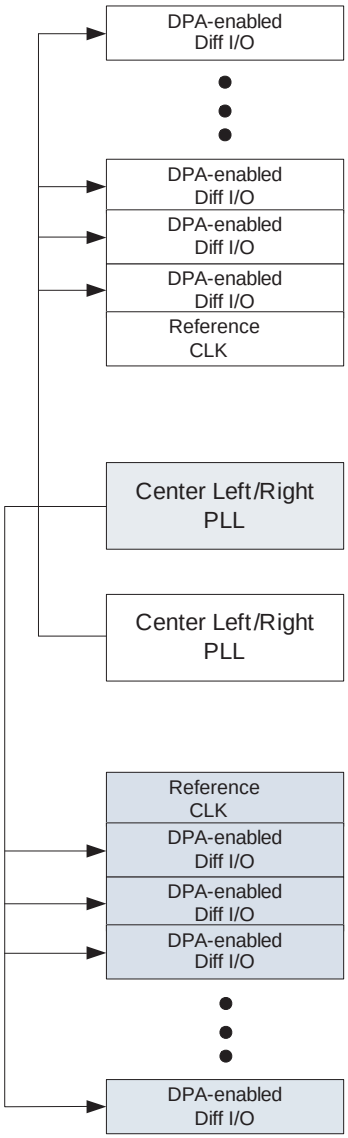


Figure 8–33. Invalid Placement of DPA-Enabled Differential I/Os Driven by Both Center Left and Right PLLs



Guidelines for DPA-Disabled Differential Channels

When you use DPA-disabled channels in the left and right banks of a Stratix IV device, you must adhere to the guidelines in the following sections.

When using non-DPA receivers, you must drive the PLL from a dedicated and compensated clock input pin. Compensated clock inputs are dedicated clock pins in the same I/O bank as the PLL.

For more information about dedicated and compensated clock inputs, refer to the *Clock Networks and PLLs in Stratix IV Devices* chapter.

DPA-Disabled Channels and Single-Ended I/Os

The placement rules for DPA-disabled channels and single-ended I/Os are the same as those for DPA-enabled channels and single-ended I/Os. For more information, refer to "DPA-Enabled Channels and Single-Ended I/Os" on page 8–38.

DPA-Disabled Channel Driving Distance

Each left and right PLL can drive all the DPA-disabled channels in the entire bank.

Using Corner and Center Left and Right PLLs

You can use a corner left and right PLL to drive all transmitter channels and a center left and right PLL to drive all DPA-disabled receiver channels within the same differential bank. In other words, a transmitter channel and a receiver channel in the same LAB row can be driven by two different PLLs, as shown in Figure 8–34.

A corner left and right PLL and a center left and right PLL can drive duplex channels in the same differential bank, as long as the channels driven by each PLL are not interleaved. Separation is not necessary between the group of channels driven by the corner and center left and right PLLs, as shown in Figure 8–34 and Figure 8–35.

Figure 8–34. Corner and Center Left and Right PLLs Driving DPA-Disabled Differential I/Os in the Same Bank

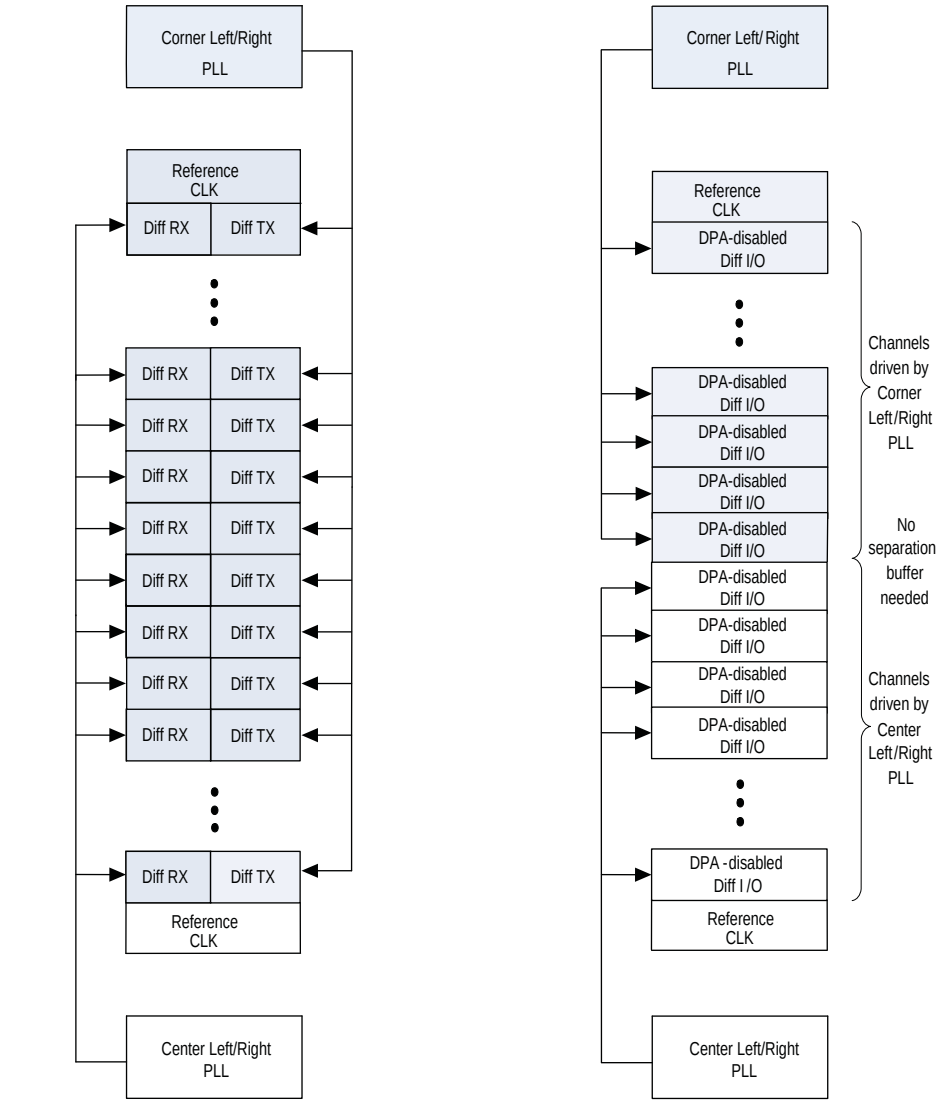
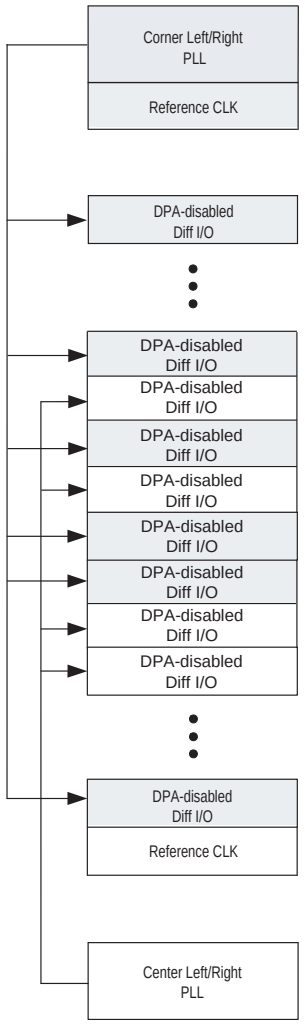


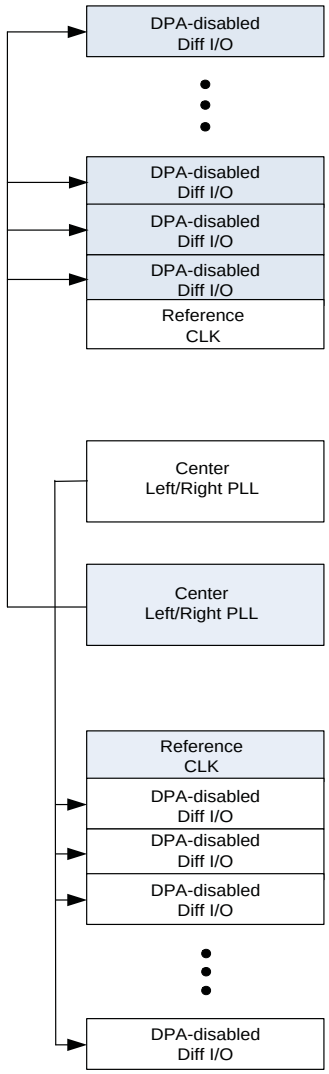
Figure 8–35. Invalid Placement of DPA-Disabled Differential I/Os Due to Interleaving of Channels Driven by the Corner and Center Left and Right PLLs



Using Both Center Left and Right PLLs

You can use both center left and right PLLs simultaneously to drive DPA-disabled channels on upper and lower differential banks. Unlike DPA-enabled channels, the center left and right PLLs can drive cross-banks. For example, the upper-center left and right PLL can drive the lower differential bank at the same time the lower center left and right PLL is driving the upper differential bank, and vice versa, as shown in Figure 8–36.

Figure 8–36. Both Center Left and Right PLLs Driving Cross-Bank DPA-Disabled Channels Simultaneously



Document Revision History

Table 8–12 lists the revision history for this chapter.

Table 8–12. Document Revision History (Part 1 of 2)

Date	Version	Changes
June 2015	3.5	Added note about Stratix IV GX V_{CM} on LVDS receiver pin to Figure 8–8.
September 2012	3.4	■ Updated Figure 8–22 to close FB case #.28708. ■ Updated the "Soft-CDR Mode" section to close FB #41886.
December 2011	3.3	■ Updated the "Overview" and "ALTLVDS Port List" sections. ■ Updated Table 8–10.
February 2011	3.2	■ Updated Table 8–10. ■ Updated the "Differential Transmitter", "Non-DPA Mode", "LVDS Interface with the Use External PLL Option Enabled", "Deserializer", and "Guidelines for DPA-Disabled Differential Channels" sections. ■ Applied new template. ■ Minor text edits.
March 2010	3.1	■ Removed note 7 from Table 8–1 and Table 8–2. ■ Updated Figure 8–5. ■ Updated the "LVDS Channels" section. ■ Updated Table 8–7. ■ Added a note to the "LVDS Interface with the Use External PLL Option Enabled" and "ALTLVDS Port List" sections. ■ Minor text edits.
November 2009	3.0	■ Changed "dedicated LVDS" to "true LVDS". ■ Removed EP4SE110, EP4SE290, and EP4SE680 devices. ■ Added EP4SE820 and Stratix IV GT devices. ■ Updated "LVDS Channels", "Differential Transmitter", "Soft-CDR Mode", and "DPA-Enabled Channels and Single-Ended I/Os" sections. ■ Updated Table 8–1, Table 8–2, Table 8–5, and Table 8–6. ■ Added Table 8–3 and Table 8–4. ■ Updated Example 8–1. ■ Updated Figure 8–22. ■ Minor text edits.
June 2009	2.3	■ Added an introductory paragraph to increase search ability. ■ Minor text edits.
April 2009	2.2	■ Updated "Introduction". ■ Updated Figure 8–3. ■ Removed Table 8-5 and Table 8-6.

Table 8–12. Document Revision History (Part 2 of 2)

Date	Version	Changes
March 2009	2.1	■ Updated “Introduction”, “Stratix IV LVDS Channels”, “Stratix IV Differential Transmitter”, “Differential I/O Termination”, and “Dynamic Phase Alignment (DPA) Block” sections. ■ Updated Table 8–1, Table 8–2, Table 8–3, Table 8–4, and Table 8–7. ■ Added Table 8–5 and Table 8–6. ■ Updated Figure 8–2. ■ Removed “Referenced Documents” section.
November 2008	2.0	■ Updated Figure 8–2, Figure 8–3, Figure 8–21, Figure 8–34. ■ Removed Figure 8–31. ■ Updated Table 8–1, Table 8–10. ■ Updated “Differential Pin Placement Guidelines” section.
May 2008	1.0	Initial release.