Dedicated Pin Information for the MAX® II EPM2210 / EPM2210G Devices Version 1.2

Dedicated Pin	256-Pin FBGA	324-Pin FBGA
IO/GCLK0	H5	J6
IO/GCLK1	J5	K6
IO/GCLK2	J12	K13
IO/GCLK3	H12	J13
IO/DEV_OE	M8	N9
IO/DEV_CLRn	M9	N10
TDI	L6	M7
TMS	N4	P5
TCK	P3	R4
TDO	M5	N6
GNDINT	F7, G6, H7, H9, J8, J10, K11, L10	G8, H7, J8, J10, K9, K11, L12, M11
GNDIO	A1, A16, B2, B15, G7, G8, G9, G10, K7, K8, K9, K10, R2, R15, T1, T16	A1, A18, B2, B17, H8, H9, H10, H11, L8, L9, L10, L11, U2, U17, V1, V18
VCCINT *(1)*	F10, G11, H8, H10, J7, J9, K6, L7	G11, H12, J9, J11, K8, K10, L7, M8
VCCIO1 *(2)*	C1, H6, J6, P1	C1, J7, K7, T1
VCCIO2 *(2)*	A3, A14, F8, F9	A3, A16, G9, G10
VCCIO3 *(2)*	C16, H11, J11, P16	C18, J12, K12, T18
VCCIO4 *(2)*	L8, L9, T3, T14	M9, M10, V3, V16
No Connect (N.C.)	-	-
Total User I/O Pins	204	272

Notes:

1. For EPM2210 devices, all VCCINT pins must be connected to either 3.3V or 2.5V (but not a combination of both). For EPM2210G devices, all VCCINT pins must be connected to 1.8V.
2. Each set of VCCIO pins (VCCIO1, VCCIO2, etc.) can be connected to 3.3V, 2.5V, 1.8V, or 1.5V.

I/O Pin Information for the MAX® II
EPM2210 / EPM2210G Devices
Version 1.2

Bank Number	Pad Number Orientation	Pin/Pad Function	Optional Function(s)	256-Pin FBGA	324-Pin FBGA
B1	0	VCCIO1			
B1	1	GNDIO			
B1	2	IO			C2
B1	3	IO		D3	C3
B1	4	IO		C2	D2
	5	VCCINT			
B1	6	IO			D1
B1	7	IO			D3
B1	8	IO		C3	E2
B1	9	IO		E3	D4
B1	10	IO		D2	E1
B1	11	IO		E4	E3
B1	12	IO		D1	F3
B1	13	IO		E5	E4
B1	14	IO		E2	F2
B1	15	VCCIO1			
B1	16	GNDIO			
B1	17	IO			E5
B1	18	IO			F1
B1	19	IO			F4
B1	20	IO			G3
B1	21	IO			F5
B1	22	IO			G2
B1	23	IO		F3	F6
B1	24	IO		E1	G1
B1	25	IO		F4	G4
B1	26	IO		F2	H3
B1	27	IO		F5	G5
B1	28	IO		F1	H2
B1	29	IO		F6	G6
B1	30	IO		G2	H1
B1	31	IO		G3	G7
B1	32	IO		G1	J3
B1	33	VCCIO1			
B1	34	GNDIO			
B1	35	IO		G4	H4
B1	36	IO		H2	J2
B1	37	IO		G5	H5
B1	38	IO		H1	J1
B1	39	IO		H3	H6
B1	40	IO		J1	K1
	41	GNDINT			
B1	42	IO	GCLK0	H5	J6
	43	VCCINT			
B1	44	IO	GCLK1	J5	K6
B1	45	IO		H4	J4

B1	46	IO		J2	K2
B1	47	IO		J4	J5
B1	48	IO		K1	K3
B1	49	IO			K5
B1	50	IO			L1
B1	51	VCCIO1			
B1	52	GNDIO			
B1	53	IO		J3	K4
B1	54	IO		K2	L2
B1	55	IO		K5	L6
B1	56	IO		L1	L3
B1	57	IO		K4	L5
B1	58	IO			M1
B1	59	IO			L4
B1	60	IO		L2	M2
B1	61	IO		K3	M6
B1	62	IO		M1	M3
B1	63	IO		L5	M5
B1	64	IO		M2	N1
B1	65	IO		L4	M4
B1	66	IO			N2
B1	67	IO		L3	N5
B1	68	IO			N3
B1	69	VCCIO1			
B1	70	GNDIO			
B1	71	IO			N4
B1	72	IO		N1	P1
B1	73	IO		M4	P4
B1	74	IO		N2	P2
B1	75	IO		M3	P3
B1	76	IO			R1
	77	GNDINT			
B1	78	IO		N3	R2
B1	79	IO			R3
B1	80	TMS		N4	P5
B1	81	TDI		L6	M7
B1	82	TCK		P3	R4
B1	83	TDO		M5	N6
B1	84	IO		P2	T2
B1	85	IO			T3
B1	86	VCCIO1			
B1	87	GNDIO			
B1	88	N.C. *(1)*			
B4	89	VCCIO4			
B4	90	GNDIO			
B4	91	IO			U1
	92	VCCINT			
B4	93	IO		R1	V2
B4	94	IO		P4	R5
B4	95	IO		T2	U3
B4	96	IO		P5	P6

B4	97	IO		R3	T4
B4	98	IO		N5	R6
B4	99	IO			U4
B4	100	IO			T6
B4	101	IO			V4
B4	102	IO			N7
B4	103	IO			T5
B4	104	IO			P7
B4	105	GNDIO			
B4	106	VCCIO4			
B4	107	IO		R4	U5
B4	108	IO		P6	R7
B4	109	IO		T4	V5
B4	110	IO		N6	T7
B4	111	IO		R5	U6
B4	112	IO		M6	N8
B4	113	IO		T5	V6
B4	114	IO		P7	P8
B4	115	IO		R6	U7
B4	116	IO		N7	R8
B4	117	IO		T6	V7
B4	118	IO		M7	T8
B4	119	IO		R7	U8
B4	120	VCCIO4			
B4	121	GNDIO			
B4	122	IO		P8	P9
B4	123	IO		T7	V8
B4	124	IO		N8	R9
B4	125	IO		R8	U9
B4	126	IO		N9	T9
B4	127	IO		T8	V9
	128	GNDINT			
B4	129	IO		T9	U10
	130	VCCINT			
B4	131	IO		R9	V10
B4	132	IO		P9	P10
B4	133	IO		T10	U11
B4	134	IO	DEV_OE	M8	N9
B4	135	IO	DEV_CLRn	M9	N10
B4	136	IO		M10	R10
B4	137	IO		R10	V11
B4	138	VCCIO4			
B4	139	GNDIO			
B4	140	IO		N10	T10
B4	141	IO		T11	U12
B4	142	IO		P10	N11
B4	143	IO		R11	V12
B4	144	IO		M11	P11
B4	145	IO		T12	U13
B4	146	IO		N11	R11
B4	147	IO		R12	V13

B4	148	IO		P11	T11
B4	149	IO		T13	T14
B4	150	IO		M12	N12
B4	151	IO		R13	U14
B4	152	VCCIO4			
B4	153	GNDIO			
B4	154	IO		N12	P12
B4	155	IO		R14	V14
B4	156	IO		P12	R12
B4	157	IO		T15	T15
B4	158	IO			T12
B4	159	IO			U15
B4	160	IO			P13
B4	161	IO			V15
B4	162	IO			R13
B4	163	IO			U16
B4	164	IO			T13
B4	165	IO			V17
	166	GNDINT			
B4	167	IO		R16	U18
B4	168	IO		P13	R14
B4	169	VCCIO4			
B4	170	GNDIO			
B3	171	VCCIO3			
B3	172	GNDIO			
B3	173	IO			T17
B3	174	IO			R15
B3	175	IO		P14	T16
	176	VCCINT			
B3	177	IO			R16
B3	178	IO			P15
B3	179	IO		P15	R17
B3	180	IO		N13	P14
B3	181	IO			R18
B3	182	IO			N15
B3	183	IO			P16
B3	184	IO			N14
B3	185	IO		N14	P17
B3	186	IO		M14	N13
B3	187	IO		N15	P18
B3	188	IO		M13	M15
B3	189	IO		N16	N16
B3	190	VCCIO3			
B3	191	GNDIO			
B3	192	IO			M14
B3	193	IO			N17
B3	194	IO		L14	M13
B3	195	IO		M15	N18
B3	196	IO		L13	M12
B3	197	IO		M16	M16
B3	198	IO		L12	L16

B3	199	IO		L15	M17
B3	200	IO		L11	L15
B3	201	IO		L16	M18
B3	202	IO		K14	L14
B3	203	IO		K15	L17
B3	204	IO		K13	L13
B3	205	IO		K16	L18
B3	206	VCCIO3			
B3	207	GNDIO			
B3	208	IO		K12	K16
B3	209	IO		J15	K17
B3	210	IO		J14	K15
B3	211	IO		J16	K18
B3	212	IO		J13	K14
B3	213	IO	GCLK2	J12	K13
	214	VCCINT			
B3	215	IO	GCLK3	H12	J13
	216	GNDINT			
B3	217	IO		H16	J18
B3	218	IO		H13	J14
B3	219	IO		H15	J17
B3	220	IO		H14	J15
B3	221	IO		G16	H18
B3	222	IO		G12	J16
B3	223	GNDIO			
B3	224	VCCIO3			
B3	225	IO		G15	H17
B3	226	IO		G13	H13
B3	227	IO		F16	G18
B3	228	IO		G14	H14
B3	229	IO		F15	G17
B3	230	IO		F11	H15
B3	231	IO		E16	G16
B3	232	IO		F12	H16
B3	233	IO		E15	F18
B3	234	IO		F13	G12
B3	235	IO		D16	F17
B3	236	IO		F14	G13
B3	237	GNDIO			
B3	238	VCCIO3			
B3	239	IO		D15	F16
B3	240	IO		E12	G14
B3	241	IO			E18
B3	242	IO			G15
B3	243	IO		D14	E17
B3	244	IO			F13
B3	245	IO			D18
B3	246	IO		E13	F14
B3	247	IO			E16
B3	248	IO			F15
B3	249	IO		C15	D17

B3	250	IO			E14
B3	251	IO			D16
	252	GNDINT			
B3	253	IO		C14	C16
B3	254	IO		E14	E15
B3	255	IO			C17
B3	256	IO		D13	D15
B3	257	N.C. *(1)*			
B3	258	VCCIO3			
B3	259	GNDIO			
B2	260	VCCIO2			
B2	261	GNDIO			
	262	VCCINT			
B2	263	IO		B16	B18
B2	264	IO		C13	D14
B2	265	IO		A15	A17
B2	266	IO		C12	E13
B2	267	IO			B16
B2	268	IO			D13
B2	269	IO			C15
B2	270	IO			F12
B2	271	IO			B15
B2	272	IO			E12
B2	273	IO			A15
B2	274	IO			D12
B2	275	GNDIO			
B2	276	VCCIO2			
B2	277	IO		B14	C14
B2	278	IO		D12	C12
B2	279	IO		B13	B14
B2	280	IO		C11	F11
B2	281	IO		A13	A14
B2	282	IO		D11	E11
B2	283	IO		B12	C13
B2	284	IO		E11	D11
B2	285	IO		A12	B13
B2	286	IO		C10	C11
B2	287	IO		B11	A13
B2	288	IO		D10	F10
B2	289	GNDIO			
B2	290	VCCIO2			
B2	291	IO		A11	B12
B2	292	IO		E10	E10
B2	293	IO		B10	A12
B2	294	IO		C9	D10
B2	295	IO		A10	B11
B2	296	IO		D9	C10
B2	297	IO		B9	A11
B2	298	IO		E9	C9
B2	299	IO		A9	B10
	300	VCCINT			

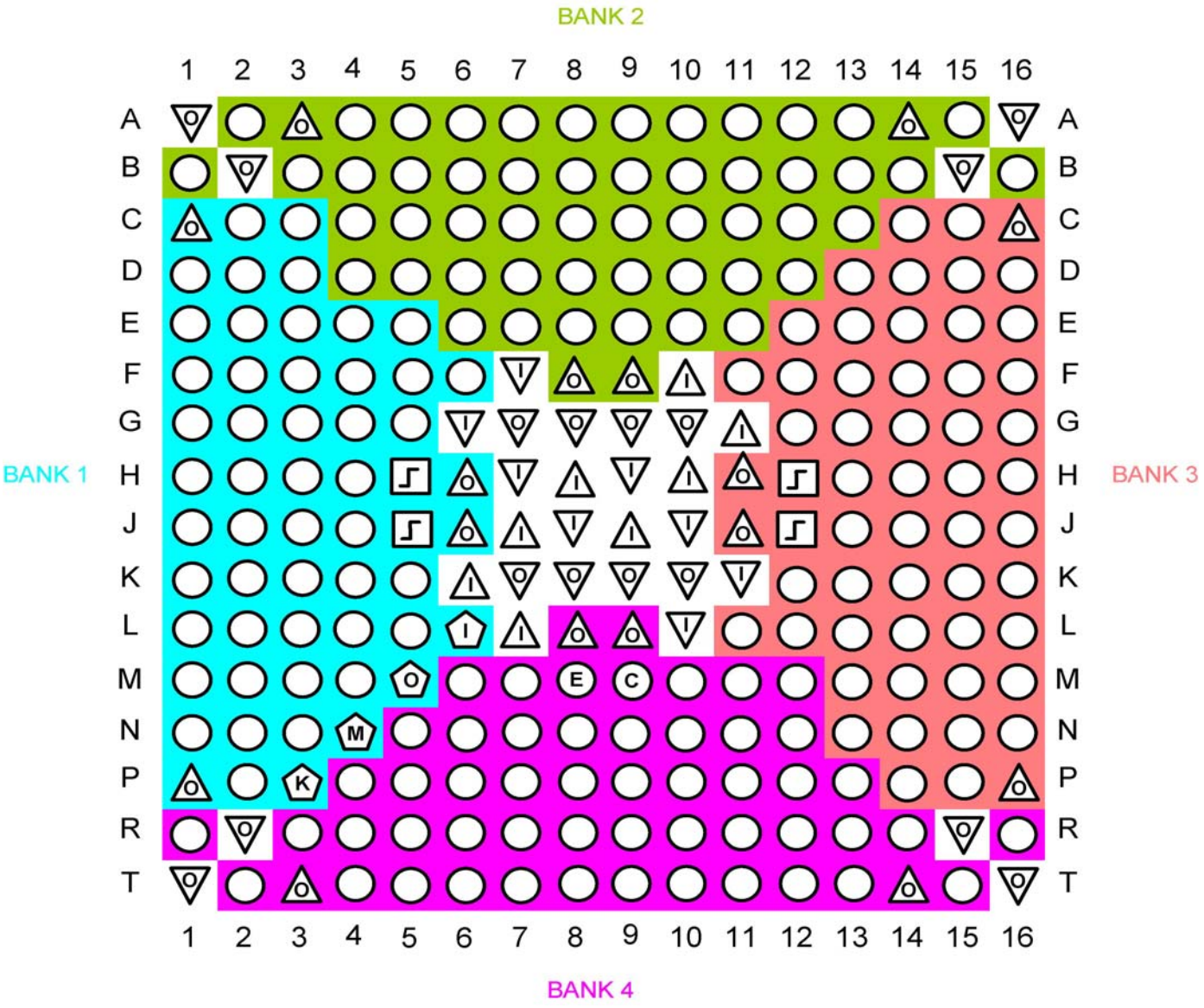
B2	301	IO		A8	A10
	302	GNDINT			
B2	303	IO		B8	A9
B2	304	IO		E8	D9
B2	305	IO		A7	B9
B2	306	IO		D8	E9
B2	307	IO		B7	A8
B2	308	IO		C8	F9
B2	309	GNDIO			
B2	310	VCCIO2			
B2	311	IO		A6	B8
B2	312	IO		E7	C8
B2	313	IO		B6	A7
B2	314	IO		D7	D8
B2	315	IO		A5	B7
B2	316	IO		C7	E8
B2	317	IO		B5	A6
B2	318	IO		E6	F8
B2	319	IO		A4	B6
B2	320	IO		D6	C7
B2	321	IO		B4	A5
B2	322	IO		C6	D7
B2	323	IO		C4	B5
B2	324	IO		C5	E7
B2	325	GNDIO			
B2	326	VCCIO2			
B2	327	IO		B3	C5
B2	328	IO		D5	F7
B2	329	IO			A4
B2	330	IO			C6
B2	331	IO			B4
B2	332	IO			D6
B2	333	IO			C4
B2	334	IO			E6
B2	335	IO		A2	B3
	336	GNDINT			
B2	337	IO		B1	A2
B2	338	IO		D4	D5
B2	339	IO			B1
B2	340	VCCIO2			
B2	341	GNDIO			

Notes: 1. No Connect

Pin Description Information for the MAX® II and MAX® IIG Devices
Version 1.2

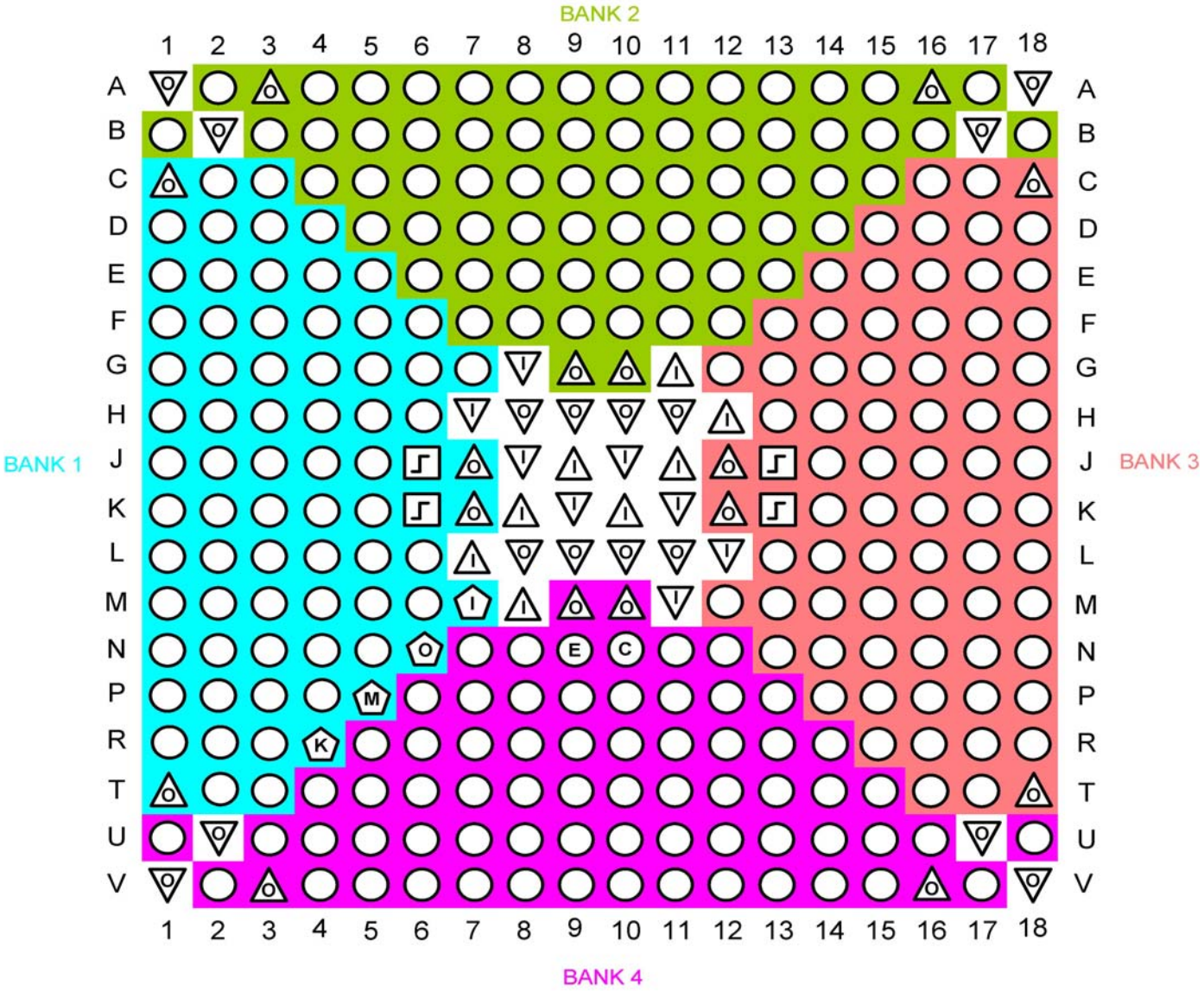
Pin Name	Pin Type	Pin Description
		Supply and Reference pins
VCCIO[1..4]	Power	I/O supply voltage pins for banks 1 through 4 respectively. EPM2210 and EPM1270 use VCCIO[1..4] while EPM240 and EPM570 use VCCIO[1..2]. Each VCCIO bank supports a different voltage level with the VCCIO pins providing power for the input and output buffers within that particular I/O bank. Each VCCIO bank can be powered with either 3.3 V, 2.5 V, 1.8 V or 1.5 V.
GNDIO	Ground	Ground pins for all the I/O banks.
VCCINT	Power	Voltage supply pins for the device.
GNDINT	Ground	Ground pins for the internal supply.
		Programming and JTAG pins
DEV_CLRn	I/O	Dual-purpose pin that can override all clears on all device registers. All registers are cleared when the pin is driven low and all registers behave as defined in the design when this pin is driven high. If not used for its dual-purpose function this pin is a regular I/O.
DEV_OE	I/O	Dual-purpose pin that can override all tri-states on the device. All output pins are tristated when the pin is driven low and all output pins behave as defined in the design when this pin is driven high. If not used for its dual-purpose function this pin is a regular I/O.
TCK	Input	Dedicated JTAG input pin.
TDI	Input	Dedicated JTAG input pin.
TMS	Input	Dedicated JTAG input pin.
TDO	Output	Dedicated JTAG output pin.
		Clock Pins
GCLK [0..3]	I/O	Dual-purpose clock pins that connect to the global clock network. If not used for its dual-purpose function this pin is a regular I/O.

Figure 1. MAX II EPM2210 / EPM2210G F256 Device Top View Package Diagram and Bank Information



USER I/O PINS	DEDICATED PINS	POWER / GROUND PINS
USER IOs	GCLK	VCCINT
DUAL PURPOSE PINS	TDI	VCCIO
DEV_OE	TCK	GNDINT
DEV_CLRn	TMS	GNDIO
NO CONNECT	TDO	

Figure 2. MAX II EPM2210 / EPM2210G F324 Device Top View Package Diagram and Bank Information



Pin Information for the MAX® II EPM2210 and EPM2210G Devices
Revision History
Version 1.2

The table below shows the revision history

Date/Version	Changes Made
January 2005, v1.2	Added MAX IIG Device Naming to Titles, Notes, and Figures
July 2004, v1.1	Added Package Diagram and Bank Information Figures for Each Package
May 2004, v1.0	Initial Release