Dedicated Pin Information for the MAX® II EPM1270 / EPM1270G Devices Version 1.5

Dedicated Pin	144-Pin TQFP	256-Pin FBGA	256-Pin MBGA
IO/GCLK0	18	H5	K1
IO/GCLK1	20	J5	L1
IO/GCLK2	89	J12	M20
IO/GCLK3	91	H12	L20
IO/DEV_OE	60	M8	W12
IO/DEV_CLRn	61	M9	Y13
TDI	34	L6	U2
TMS	33	N4	T3
TCK	35	P3	W2
TDO	36	M5	V2
GNDINT	17, 54, 92, 128	H7, H9, J8, J10	J4, U12, M17, D12
GNDIO	10, 26, 47, 65, 83, 99, 115, 135	A1, A16, B2, B15, G7, G8, G9, G10, K7, K8, K9, K10, R2, R15, T1, T16	H3, J3, M4, N3, U9, V8, V9, V13, H18, J17, N18, C8, D9, C12, C13, M18
VCCINT *(1)*	19, 56, 90, 126	H8, H10, J7, J9	K4, U11, L17, D11
VCCIO1 *(2)*	9, 25	C1, H6, J6, P1	K3, L3, L4, M3
VCCIO2 *(2)*	116, 136	A3, A14, F8, F9	C9, C10, D10, C11
VCCIO3 *(2)*	82, 100	C16, H11, J11, P16	J18, K17, K18, L18
VCCIO4 *(2)*	46, 64	L8, L9, T3, T14	U10, V10, V11, V12
No Connect (N.C.)	-	-	-
Total User I/O Pins	116	212	212

Notes:

1. For EPM1270 devices, all VCCINT pins must be connected to either 3.3 V or 2.5 V, but not a combination of both. For EPM1270G devices, all VCCINT pins must be connected to 1.8 V.
2. Each set of VCCIO pins (VCCIO1, VCCIO2, etc.) can be connected to 3.3 V, 2.5 V, 1.8 V, or 1.5 V.

Bank Number	Pad Number Orientation	Pin/Pad Function	Optional Function(s)	144-Pin TQFP	256-Pin FBGA	256-Pin MBGA
B1	0	VCCIO1				
B1	1	GNDIO				
B1	2	IO			D3	E3
B1	3	IO			C2	C2
B1	4	IO		1	E3	H2
B1	5	IO		2	C3	D3
B1	6	IO			E4	C3
B1	7	IO		3	D2	D2
B1	8	IO			E5	C4
B1	9	IO		4	D1	C1
B1	10	IO			F3	F3
B1	11	IO		5	E2	B1
B1	12	VCCIO1				
B1	13	GNDIO				
B1	14	IO		6	F4	D4
B1	15	IO			E1	D1
B1	16	IO			F5	H4
B1	17	IO			F2	F2
B1	18	IO		7	F6	G4
B1	19	IO		8	F1	E1
B1	20	IO			G3	J2
B1	21	IO			G2	G2
B1	22	IO			G4	E4
B1	23	IO			G1	E2
B1	24	VCCIO1				
B1	25	GNDIO				
B1	26	IO		11	G5	G3
B1	27	IO		12	H2	G1
B1	28	IO		13	G6	F4
B1	29	IO		14	H1	H1
B1	30	IO		15	H3	F1
B1	31	IO		16	J1	J1
	32	GNDINT				
B1	33	IO	GCLK0	18	H5	K1
	34	VCCINT				
B1	35	IO	GCLK1	20	J5	L1
B1	36	IO		21	H4	K2
B1	37	IO		22	J2	M1
B1	38	IO		23	J4	L2
B1	39	IO		24	K1	N1
B1	40	VCCIO1				
B1	41	GNDIO				
B1	42	IO			J3	M2
B1	43	IO		27	K2	P1
B1	44	IO			K6	N4
B1	45	IO			L1	R1
B1	46	IO		28	K5	P4
B1	47	IO		29	L2	P2
B1	48	IO			K4	R4
B1	49	IO			M1	T1
B1	50	IO			K3	N2
B1	51	IO		30	M2	U1
B1	52	IO			L5	P3
B1	53	IO			M3	R2
B1	54	VCCIO1				
B1	55	GNDIO				
B1	56	IO		31	L4	R3

Bank Number	Pad Number Orientation	Pin/Pad Function	Optional Function(s)	144-Pin TQFP	256-Pin FBGA	256-Pin MBGA
B1	57	IO			N1	V1
B1	58	IO			L3	T4
B1	59	IO		32	N2	W1
B1	60	IO			M4	V3
B1	61	IO			N3	T2
B1	62	TMS		33	N4	T3
B1	63	TDI		34	L6	U2
B1	64	TCK		35	P3	W2
B1	65	TDO		36	M5	V2
B1	66	IO			P2	U3
B1	67	VCCIO1				
B1	68	GNDIO				
B1	69	N.C. *(1)*				
B4	70	VCCIO4				
B4	71	GNDIO				
B4	72	IO			P4	V4
B4	73	IO		37	R1	W3
B4	74	IO		38	P5	V5
B4	75	IO			T2	Y1
B4	76	IO			N5	W5
B4	77	IO		39	R3	W4
B4	78	IO			P6	U4
B4	79	GNDIO				
B4	80	VCCIO4				
B4	81	IO		40	R4	Y2
B4	82	IO		41	N6	U5
B4	83	IO			T4	W6
B4	84	IO			M6	U6
B4	85	IO			R5	Y3
B4	86	IO		42	P7	V6
B4	87	IO		43	T5	Y4
B4	88	IO		44	N7	V7
B4	89	IO			R6	W7
B4	90	IO			M7	U7
B4	91	IO			T6	Y5
B4	92	IO			L7	U8
B4	93	IO		45	R7	Y6
B4	94	VCCIO4				
B4	95	GNDIO				
B4	96	IO		48	P8	W8
B4	97	IO		49	T7	Y7
B4	98	IO		50	N8	W9
B4	99	IO		51	R8	Y8
B4	100	IO		52	N9	W10
B4	101	IO		53	T8	Y9
	102	GNDINT				
B4	103	IO		55	T9	Y10
	104	VCCINT				
B4	105	IO		57	R9	Y11
B4	106	IO		58	P9	W11
B4	107	IO		59	T10	Y12
B4	108	IO	DEV_OE	60	M8	W12
B4	109	IO	DEV_CLRn	61	M9	Y13
B4	110	IO		62	L10	U16
B4	111	IO		63	R10	Y14
B4	112	VCCIO4				
B4	113	GNDIO				

Bank Number	Pad Number Orientation	Pin/Pad Function	Optional Function(s)	144-Pin TQFP	256-Pin FBGA	256-Pin MBGA
B4	114	IO			M10	U13
B4	115	IO			T11	Y15
B4	116	IO		66	N10	V15
B4	117	IO		67	R11	Y16
B4	118	IO			P10	W14
B4	119	IO			T12	W15
B4	120	IO		68	M11	U14
B4	121	IO			R12	W16
B4	122	IO			N11	V14
B4	123	IO		69	T13	Y17
B4	124	IO			P11	W13
B4	125	IO			R13	Y18
B4	126	VCCIO4				
B4	127	GNDIO				
B4	128	IO		70	M12	U15
B4	129	IO			R14	Y19
B4	130	IO			N12	V16
B4	131	IO		71	T15	W17
B4	132	IO			P12	V17
B4	133	IO			R16	W18
B4	134	IO		72	P13	V18
B4	135	VCCIO4				
B4	136	GNDIO				
B3	137	VCCIO3				
B3	138	GNDIO				
B3	139	IO			P14	W19
B3	140	IO			N13	U18
B3	141	IO			P15	V19
B3	142	IO		73	M14	T18
B3	143	IO		74	N14	U19
B3	144	IO		75	M13	R18
B3	145	IO			N15	Y20
B3	146	IO		76	L14	W20
B3	147	IO			N16	T19
B3	148	VCCIO3				
B3	149	GNDIO				
B3	150	IO			L13	U17
B3	151	IO		77	M15	V20
B3	152	IO			L12	P17
B3	153	IO			M16	R19
B3	154	IO			L11	T17
B3	155	IO		78	L15	U20
B3	156	IO		79	K14	N19
B3	157	IO		80	L16	T20
B3	158	IO			K13	R17
B3	159	IO			K15	P19
B3	160	IO		81	K12	P18
B3	161	IO			K16	R20
B3	162	VCCIO3				
B3	163	GNDIO				
B3	164	IO		84	K11	N17
B3	165	IO		85	J15	P20
B3	166	IO		86	J14	M19
B3	167	IO		87	J16	N20
B3	168	IO		88	J13	L19
B3	169	IO	GCLK2	89	J12	M20
	170	VCCINT				

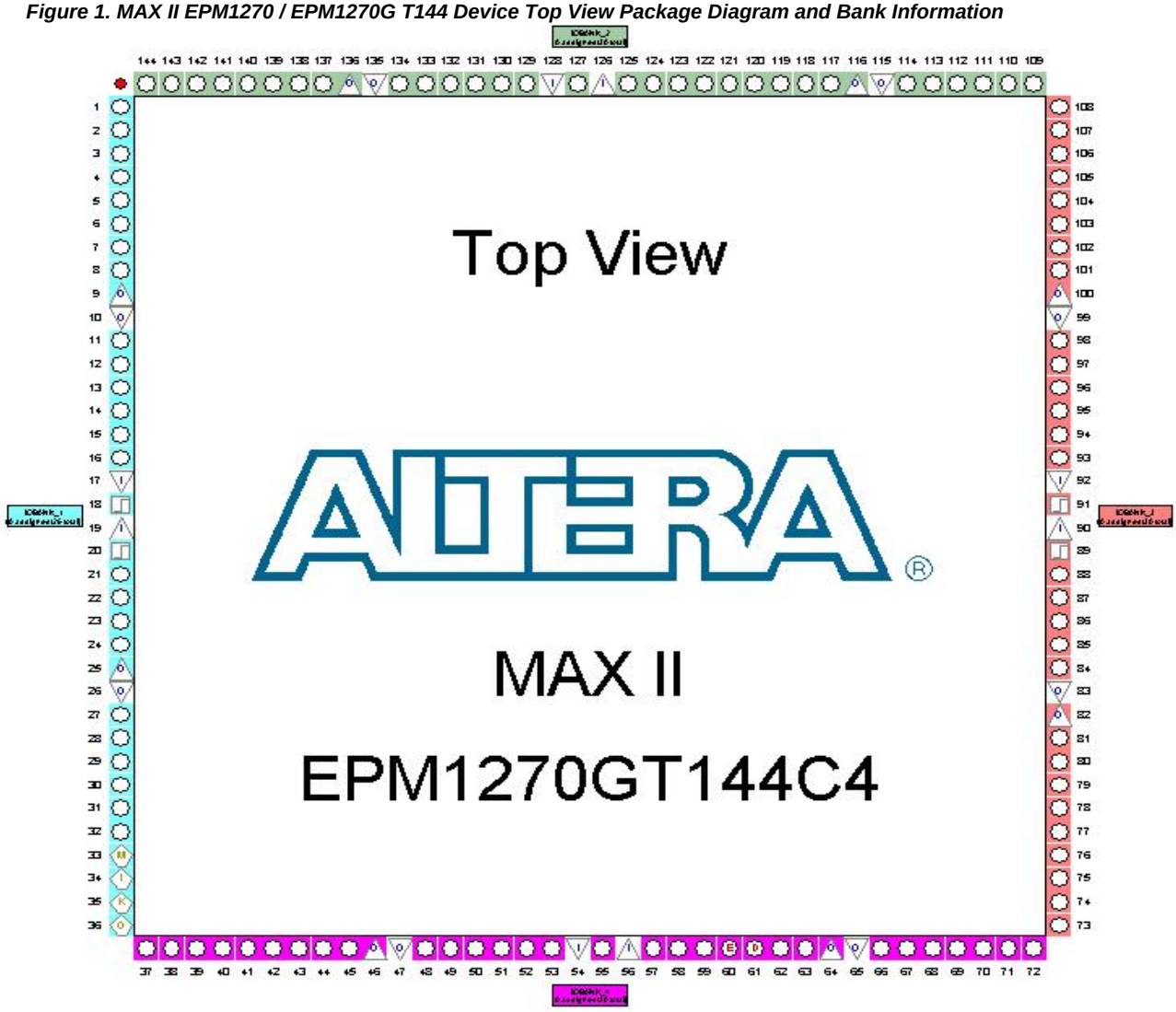
Bank Number	Pad Number Orientation	Pin/Pad Function	Optional Function(s)	144-Pin TQFP	256-Pin FBGA	256-Pin MBGA
B3	171	IO	GCLK3	91	H12	L20
	172	GNDINT				
B3	173	IO		93	H16	K20
B3	174	IO		94	H13	K19
B3	175	IO		95	H15	J20
B3	176	IO		96	H14	J19
B3	177	IO		97	G16	H20
B3	178	IO		98	G12	G18
B3	179	GNDIO				
B3	180	VCCIO3				
B3	181	IO		101	G15	G20
B3	182	IO			G11	H17
B3	183	IO			F16	G19
B3	184	IO			G13	F17
B3	185	IO		102	F15	F20
B3	186	IO		103	G14	E17
B3	187	IO			E16	E20
B3	188	IO			F11	G17
B3	189	IO			E15	F19
B3	190	IO		104	F12	D17
B3	191	IO		105	D16	D20
B3	192	IO			F13	C18
B3	193	GNDIO				
B3	194	VCCIO3				
B3	195	IO		106	D15	C20
B3	196	IO			F14	H19
B3	197	IO		107	D14	B20
B3	198	IO			E12	F18
B3	199	IO		108	C15	E19
B3	200	IO			E13	E18
B3	201	IO			C14	D19
B3	202	IO			E14	D18
B3	203	IO			D13	C19
B3	204	N.C. *(1)*				
B3	205	VCCIO3				
B3	206	GNDIO				
B2	207	VCCIO2				
B2	208	GNDIO				
B2	209	IO			C13	C16
B2	210	IO		109	B16	A20
B2	211	IO		110	C12	B16
B2	212	IO		111	A15	B17
B2	213	IO			D12	C15
B2	214	GNDIO				
B2	215	VCCIO2				
B2	216	IO			B14	A19
B2	217	IO			C11	B18
B2	218	IO			B13	A18
B2	219	IO		112	D11	B19
B2	220	IO			A13	A17
B2	221	IO			E11	D15
B2	222	IO		113	B12	B15
B2	223	IO			C10	C17
B2	224	IO			A12	B14
B2	225	IO		114	D10	C14
B2	226	IO			B11	A16
B2	227	IO			E10	D16

Bank Number	Pad Number Orientation	Pin/Pad Function	Optional Function(s)	144-Pin TQFP	256-Pin FBGA	256-Pin MBGA
B2	228	GNDIO				
B2	229	VCCIO2				
B2	230	IO		117	A11	B13
B2	231	IO		118	F10	D13
B2	232	IO		119	B10	A15
B2	233	IO		120	C9	B12
B2	234	IO		121	A10	A14
B2	235	IO		122	D9	D14
B2	236	IO		123	B9	A13
B2	237	IO		124	E9	B11
B2	238	IO		125	A9	A12
	239	VCCINT				
B2	240	IO		127	A8	A11
	241	GNDINT				
B2	242	IO		129	B8	A10
B2	243	IO		130	E8	B10
B2	244	IO		131	A7	A9
B2	245	IO		132	D8	D8
B2	246	IO		133	B7	A8
B2	247	IO		134	C8	B9
B2	248	GNDIO				
B2	249	VCCIO2				
B2	250	IO			A6	A7
B2	251	IO			F7	D7
B2	252	IO			B6	B7
B2	253	IO		137	E7	C6
B2	254	IO		138	A5	A6
B2	255	IO		139	D7	C7
B2	256	IO			B5	A5
B2	257	IO			C7	B8
B2	258	IO		140	A4	A4
B2	259	IO		141	E6	D6
B2	260	IO			B4	B6
B2	261	IO			D6	D5
B2	262	IO		142	C4	A3
B2	263	IO			C6	B2
B2	264	GNDIO				
B2	265	VCCIO2				
B2	266	IO			B3	A2
B2	267	IO			C5	B3
B2	268	IO		143	A2	B5
B2	269	IO			D5	C5
B2	270	IO			B1	A1
B2	271	IO		144	D4	B4
B2	272	VCCIO2				
B2	273	GNDIO				

Note:
1. No Connect

Pin Name	Pin Type	Pin Description
		Supply and Reference pins
VCCIO[1..4]	Power	I/O supply voltage pins for banks 1 through 4. Each VCCIO bank supports a different voltage level with the VCCIO pins providing power for the input and output buffers within that particular I/O bank. Each VCCIO bank can be powered with either 3.3 V, 2.5 V, 1.8 V, or 1.5 V.
GNDIO	Ground	Ground pins for all the I/O banks.
VCCINT	Power	Voltage supply pins for the device.
GNDINT	Ground	Ground pins for the internal supply.
NC	No Connect	Do not drive signals into these pins.
		Programming and JTAG pins
DEV_CLRn	I/O	Dual-purpose pin that can override all clears on all device registers. All registers are cleared when the pin is driven low and all registers behave as defined in the design when this pin is driven high. If not used for its dual-purpose function, this pin is a regular I/O.
DEV_OE	I/O	Dual-purpose pin that can override all tri-states on the device. All output pins are tri-stated when the pin is driven low and all output pins behave as defined in the design when this pin is driven high. If not used for its dual-purpose function, this pin is a regular I/O.
TCK	Input	Dedicated JTAG input pin.
TDI	Input	Dedicated JTAG input pin.
TMS	Input	Dedicated JTAG input pin.
TDO	Output	Dedicated JTAG output pin.
		Clock Pins
GCLK [0..3]	I/O	Dual-purpose clock pins that connect to the global clock network. If not used for its dual-purpose function, this pin is a regular I/O.

Figure 1. MAX II EPM1270 / EPM1270G T144 Device Top View Package Diagram and Bank Information



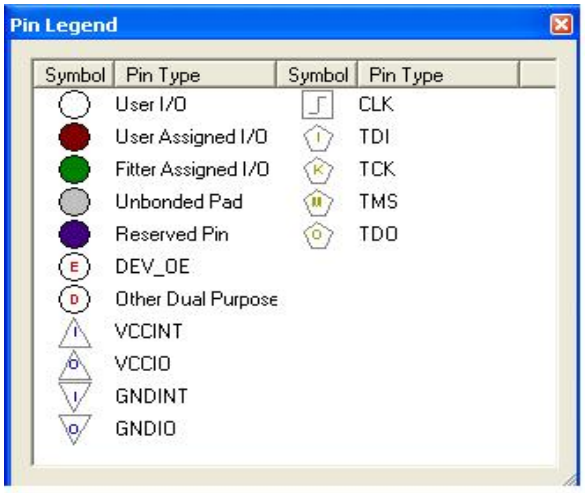
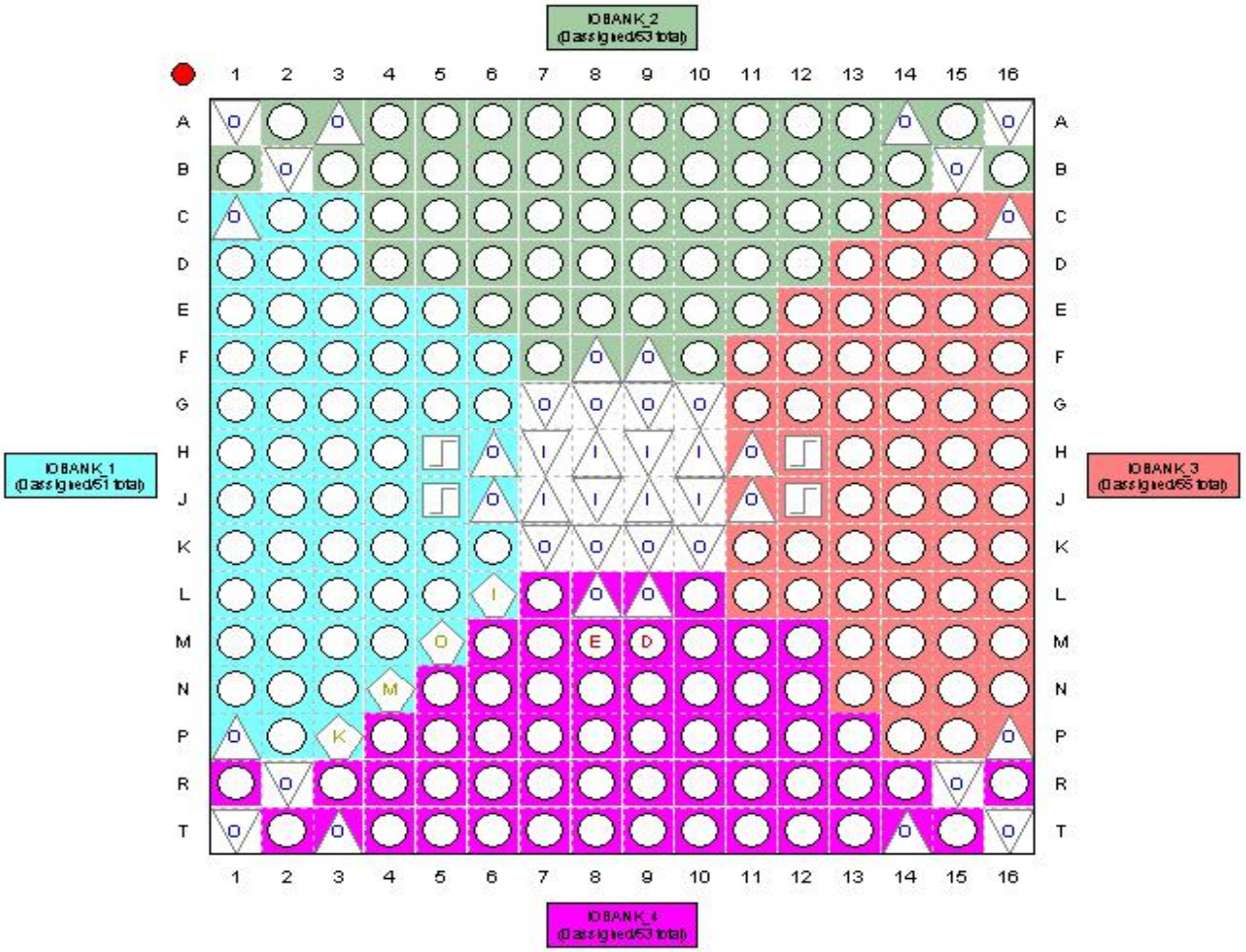


Figure 2. MAX II EPM1270 / EPM1270G F256 Device Top View Package Diagram and Bank Information



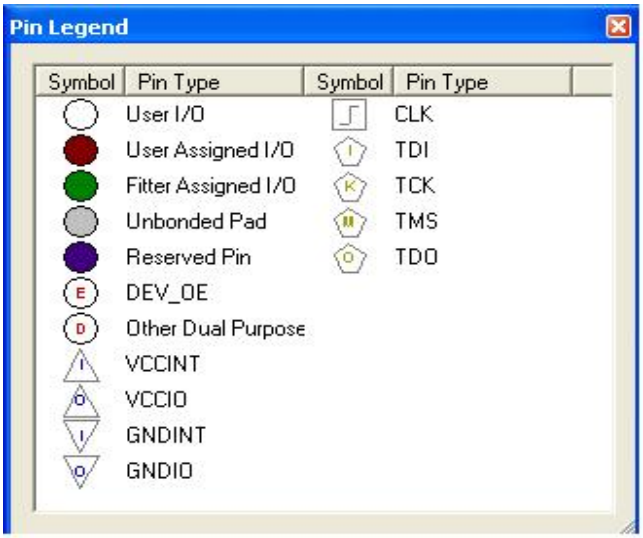
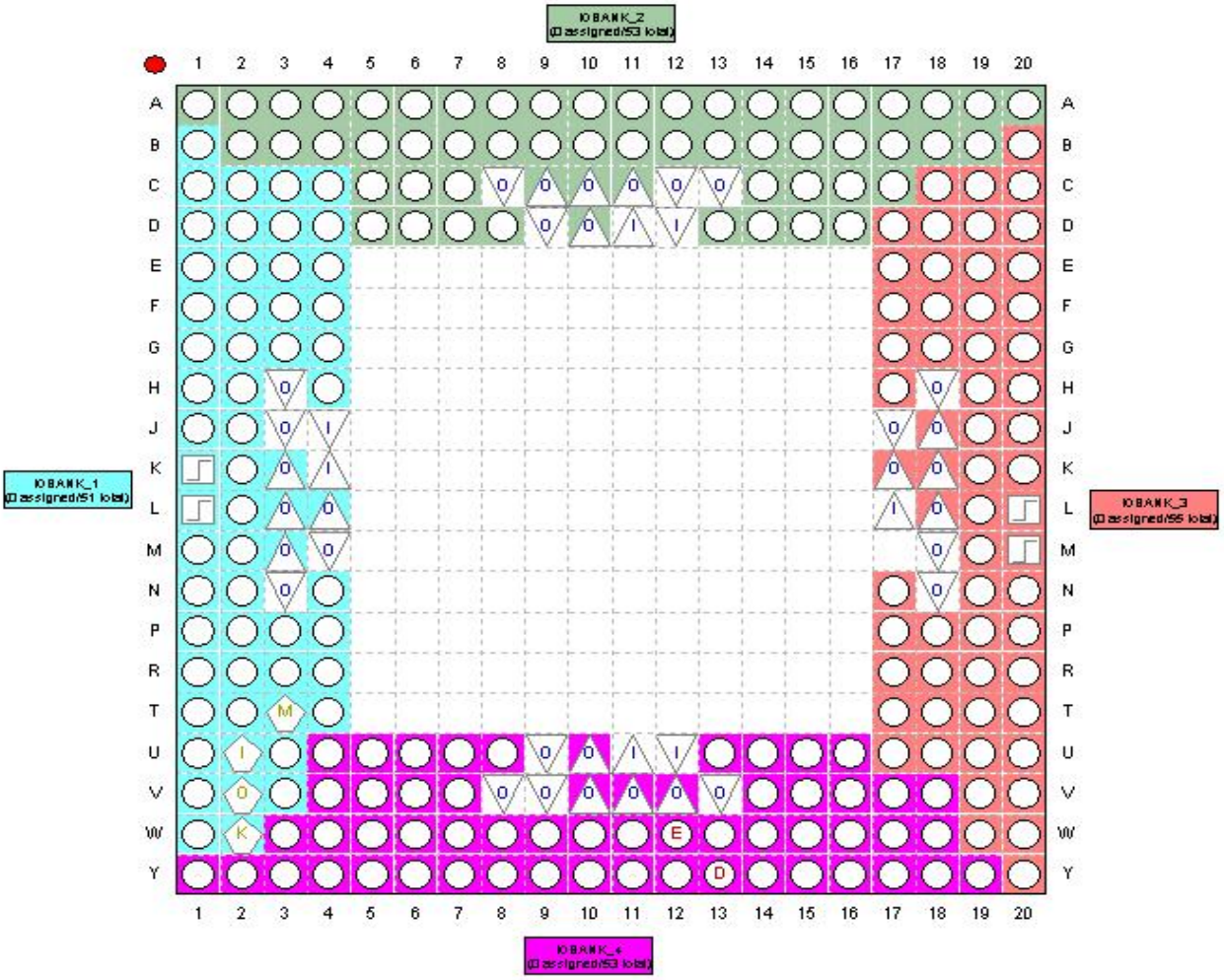
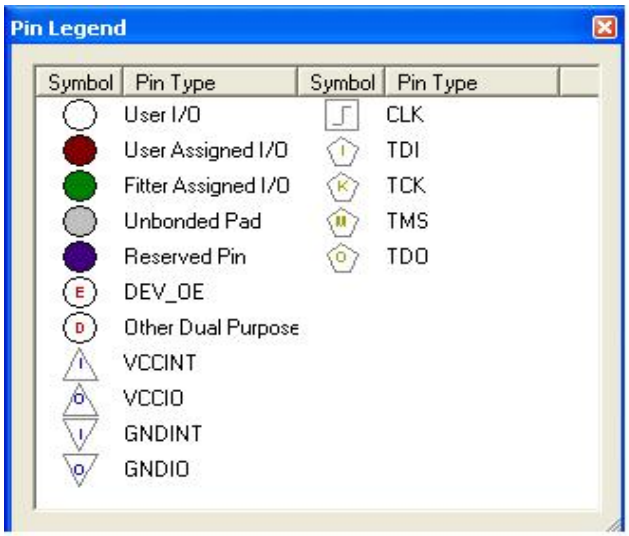


Figure 3. MAX II EPM1270 / EPM1270G M256 Device Top View Package Diagram and Bank Information





Date	Version	Changes Made
Sep-07	1.5	Added support for M256 package in the EPM1270G device
May-07	1.4	Changed the VCCIO2 and VCCIO4 pins for EPM1270 (256-Pin MBGA package) to match Quartus II pin-out
Apr-06	1.3	Added M256 package
Jan-05	1.2	Added MAX IIG device naming to titles, notes, and figures
Jul-04	1.1	Added package diagram and bank information figures for each package
May-04	1.0	Initial release