

Cyclone-V I/O Buffer Encrypted Hspice Model User Guide

For use only with Hspice version 2008.03 or later

Early Access Uncorrelated Model



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1. Introduction

This document is an Hspice model user guide for all regular output buffers available in the Cyclone-V device. The Cyclone-V I/O is re-configurable in nature and provides for a combination of various features built into the device. The information in this document enables the user to configure the Hspice models to his/her requirement.

This document will discuss the naming convention for the Hspice models, file layout and organization, procedure for setting various output standards, and a list of all Hspice models for various I/O standards in the Cyclone-V device.

Please also note that these models are “early access” models. They have not been correlated to actual performance on the silicon. The user assumes the risk that actual I/O behavior of Cyclone-V device may differ materially from the models' prediction.

What is included in this kit?

This kit contains the following materials:

1. Encrypted transistor and logic cell library models
2. Encrypted output buffer circuit models for single ended and differential I/Os
3. Single Ended and Differential sample spice decks

2. File Directory Structure

Figure 1 shows the directory structure of the Cyclone-V Hspice model kit.

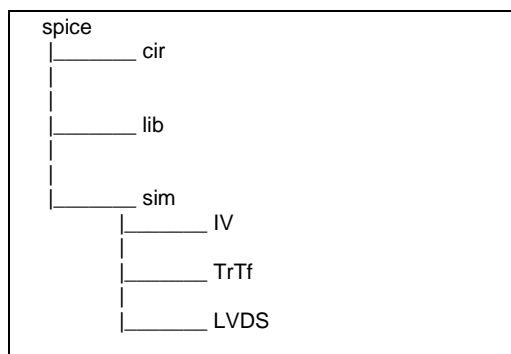


Figure 1. - Directory structure of Cyclone-V Hspice Modeling Kit

The content of each directory is as follows:

sim: This directory contains the top-level spice files for all I/O standard simulations. The files that reside here can be modified to simulate any available I/O standard, drive strength, process corner, supply voltage, and/or temperature. File names marked in bold are available at present.

IV – IV curve simulations of the single-ended buffers

1. **IO_TT_N.spi** – IV simulations for TT using NMOS pulldown.
2. **IO_TT_P.spi** – IV simulations for TT using PMOS pullup.

TrTf – Transient rise and fall simulations of the single-ended output buffers

1. **IO_HSTL.spi** – HSTL simulations using the output buffer
2. **IO_HSUL.spi** – HSUL simulations using the output buffer
3. **IO_SSTL.spi** – SSTL simulations using the output buffer
4. **IO_TTL.spi** – TTL & CMOS simulations using the output buffer
5. **IO_OCTRS_TT.spi** – Non-calibrated OCT Rs output buffer simulations
6. **IO_OCTRS_calibrated_TT.spi** – calibrated OCT Rs output buffer simulations under TT corner
7. **IO_OCTRS_calibrated_SS.spi** – calibrated OCT Rs output buffer simulations under SS corner
8. **IO_OCTRS_calibrated_FF.spi** – calibrated OCT Rs output buffer simulations under FF corner
9. **IO_OCTRT_calibrated_TT.spi** – calibrated OCT Rt output buffer simulations under TT corner
10. **IO_OCTRT_calibrated_SS.spi** – calibrated OCT Rt output buffer simulations under SS corner
11. **IO_OCTRT_calibrated_FF.spi** – calibrated OCT Rt output buffer simulations under FF corner

LVDS – Transient and DC simulations of the differential output buffer

1. **LVDS_TT.spi** – DC measurements of the differential output buffer
2. **LVDS_AC_TT.spi** – Transient simulation of the differential output buffer
3. **LVDS_LINK_TT.spi** – Transient simulation of the differential output buffer or SLVS to the differential input buffer. Simulation can be used for both off-chip and on-chip differential input termination.

cir: This directory contains the encrypted spice netlists for the I/O structures. All netlist file content is encrypted, with the exception of the .subckt definition. Separate circuit files exist for each I/O buffer component, for improved simulation runtime, as only the required circuits are instantiated for simulation. File names marked in bold are currently available.

Single Ended and Differential I/O Models

1. **IO_buffer.inc** – Encrypted model of the input and output buffers.
2. **IO_buffer_OCTRS.inc** – Encrypted model of the input and output buffers used for OCT-Rs output buffer simulations.
3. **IO_buffer_OCTRT.inc** – Encrypted model of the input and output buffers used for OCT-Rt output buffer simulations.
4. **LVDS_OUTPUT.inc** – Encrypted model of the LVDS output buffer. Must be used in conjunction with the IO_buffer_LOAD.inc load circuit for proper loading.

Single Ended and Differential I/O Loads

1. **IO_buffer_LOAD.inc** – Encrypted and simplified CV_IO model for loading LVDS simulations.
2. **LVDS_OUTPUT_LOAD.inc** – Encrypted and simplified LVDS output buffer model for loading SE IO simulations.
3. **LVDS_INPUT_LOAD.inc** – Encrypted and simplified LVDS input buffer model for loading SE IO simulations and for LVDS input buffer simulations.
4. **LVDS_OCT_LOAD.inc** – Encrypted and simplified LVDS OCT model for loading SE IO simulations and for LVDS input buffer simulations with external differential input termination.
5. **LVDS_OCT_RD.inc** – Encrypted model of the LVDS OCT Rd with active termination for on-chip terminated LVDS input buffer simulations.

lib: This directory contains libraries of transistor models and various settings of Cyclone-V I/O features.

Single Ended I/O features:

1. Programmable Drive Strength
2. Slew Rate Control
3. Output Delay Control

Differential I/O features:

1. Programmable Pre-emphasis
2. Programmable VOD

All files in this **lib** directory are listed below.

1. CV_TT.inc – Encrypted process model for typical corner
2. CV_FF.inc – Encrypted process model for fast corner

3. CV_SS.inc – Encrypted process model for slow corner
4. package.lib – Unencrypted package models for IO.
5. drive_select_IO.lib – Unencrypted drive strength ram settings for SE IO.
6. output_delay_control.lib – Unencrypted delay control ram settings for SE IO.
7. slew_rate_control.lib – Unencrypted ram settings for SE IO slew rate control.
8. lvds_preemphasis_select.lib – Unencrypted pre-emphasis settings for LVDS Output.
9. lvds_vod_select.lib – Unencrypted VOD settings for LVDS Output.
10. sample_brd.sp – Unencrypted sample w-element board trace model.
11. IO_load.lib – Unencrypted termination and loading library.
12. IO_OCTRS_calibrated.lib – Calibrated OCT Rs ram settings for SE IO
13. IO_OCTRT_calibrated.lib – Calibrated OCT Rt ram settings for SE IO

Single Ended I/O Spice Models

Figure 2 shows the general setup for all single ended spice decks provided in this kit. In general, setup contains the transmitter buffer, package parasitic, driver (series or parallel) terminations, simple topology of a transmission line interconnect, receiver parallel terminations and the receiver buffer. The package parasitic can be changed according to user's requirement for the specific device and package. Depending on the I/O standard, either series or parallel, or both terminations are used at the transmitter end. The followings are the description of major sections in the single ended I/O spice deck:

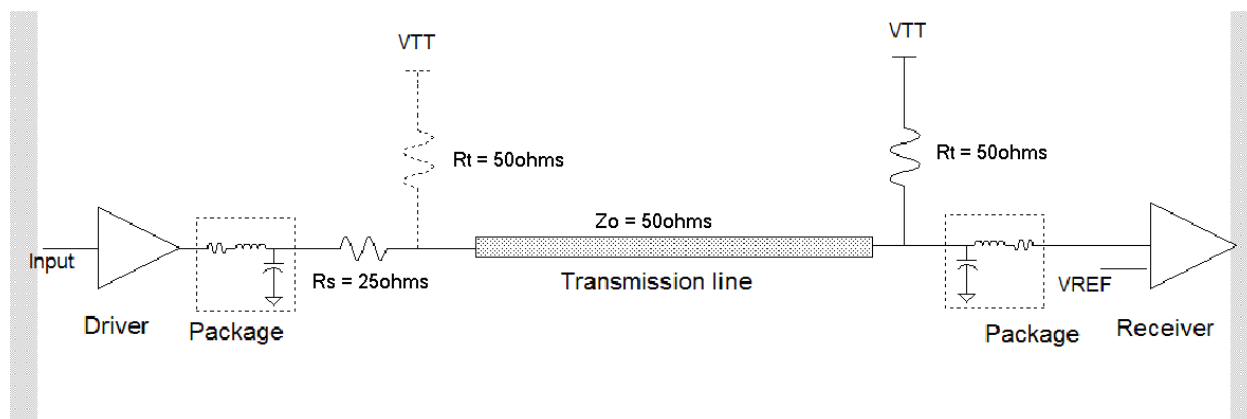


Figure 2. - Single Ended spice model sample setup.

Hspice Optimization/Initialization Header:

The section 'Options and Initial Conditions' defines some of the Avanti Hspice tool specific simulation control options. The user may need to adjust the value of these option parameters depending on the complexity of the topology of the spice circuit. These options improve the DC and transient convergence and ultimately speedup the simulation time. Some of these options are explained below:

```
.options badchr      * warns if a nonprintable character in input
.options co=132      * Set number of columns of output
.options ingold=2     * Define output format as exponential
.options nomod       * Suppress model parameter output
.options dv=1.0      * Limits iteration-to-iteration voltage change for
                    * circuit node in both DCTAN analysis(default=100)
.options probe       * Suppress post-analysis output to variables in
                    * .probe, .print, .plot, & .graph statements
.options captab=0     * 1 = Report node caps at each operating point
.options csdf=2       * Set output display for Viewtrace element template
.options accurate     * 1 = Sets timestep to give better TRAN accuracy
.options post        * 2 = Output format is ASCII
```

The sections 'Process/Voltage/Temperature Setting' set the PVT for the TYPICAL, FAST and SLOW corner case analysis. It also defines file paths of the encrypted transistor model libraries. The voltage parameter 'vc' is defined in this section and it is a unique voltage level that is used throughout this kit to define all 'logic 1' control signals.

The section 'Power Supplies' defines the global supply voltage VCC and global ground VSS. It also defines the VTT voltage, which is used as the pull-up termination voltage for the parallel terminations.

Buffer netlist instantiation:

In this section, the single ended Cyclone-V output buffer models, located in the "cir" subdirectory, is instantiated. The instantiation differs depending on the type of buffer.

Single-ended IO:

```
XIO_buffer din oeb ropdrain pin rambh rndly<1> rndly<0> rpdly<1> rpdly<0>
+ rpcdn<9> rpcdn<8> rpcdn<7> rpcdn<6> rpcdn<5> rpcdn<4> rpcdn<3> rpcdn<2>
rpcdn<1> rpcdn<0>
+ rpcdp<9> rpcdp<8> rpcdp<7> rpcdp<6> rpcdp<5> rpcdp<4> rpcdp<3> rpcdp<2>
rpcdp<1> rpcdp<0>
+ rslewn rslewp vccn vccpd vcpad vcc io_buffer
```

Calibrated and non-calibrated OCT Rs IO:

```
XIO_buffer din oeb ropdrain pin rambh rndly<1> rndly<0> rpdly<1> rpdly<0>
+rpcdn<9> rpcdn<8> rpcdn<7> rpcdn<6> rpcdn<5> rpcdn<4> rpcdn<3> rpcdn<2>
rpcdn<1> rpcdn<0>
+rpcdp<9> rpcdp<8> rpcdp<7> rpcdp<6> rpcdp<5> rpcdp<4> rpcdp<3> rpcdp<2>
rpcdp<1> rpcdp<0>
+ vccn vccpd vcpad vcc IO_buffer_OCTRS
```

Calibrated OCT Rt IO:

```
XIO_buffer din oeb ropdrain pin rambh rndly<1> rndly<0> rpdly<1> rpdly<0>
+ rpcdn<9> rpcdn<8> rpcdn<7> rpcdn<6> rpcdn<5> rpcdn<4> rpcdn<3> rpcdn<2>
rpcdn<1> rpcdn<0>
+ rpcdp<9> rpcdp<8> rpcdp<7> rpcdp<6> rpcdp<5> rpcdp<4> rpcdp<3> rpcdp<2>
rpcdp<1> rpcdp<0>
+ vccn vccpd vcpad vcc IO_buffer_OCTRt
```

In these sub-circuits, the spice node 'DIN' is the data input signal to the output buffer. Any input stimulus is applied to this node. Similarly, the node 'PIN' is the output node. All of these nodes are defined in detail in Table 2 to Table 5 of the 'Control Signals' section of this document.

Also in this section, some files in the "lib" directory are called. These files define all control signal voltage levels to select output buffer drive strength based on the type of I/O standard, slew rate, and output delay. Another file within the "lib" directory defines the termination resistor and load capacitor values based on the termination scheme. A complete listing of available I/O standards can be found in the 'Appendix' section of this document.

IO Buffer Loading:

To accurately model the device capacitance on-chip, the IO buffer must be used in conjunction with the LVDS buffer load components. Every single ended IO pin is shared with either an

LVDS input pin or an LVDS output pin. Depending on the LVDS pin, whether it is an input or an output pin, a different loading scheme to the single-ended IO pin is required.

For the LVDS output pin, the LVDS Output Buffer Load should be attached. As for the LVDS input pin, the LVDS Input Buffer Load and the LVDS OCT Load should be attached. Detailed examples illustrating these loading setups are provided in the following pages. The load components are highlighted in Table 1.

Pin Type	Load Components Required
DIFFIO_TX	LVDS_OUTPUT_LOAD
DIFFIO_RX	LVDS_INPUT_LOAD LVDS_OCT_LOAD

Table 1: IO Buffer Loading Table

The generic instantiation of the LVDS loading blocks is as follows:

LVDS Output Buffer Load:

```
XLVDS_OUTPUT_LOAD pin vss vccn vcpad vcpad vcc LVDS_OUTPUT_LOAD
```

LVDS Input Buffer Load:

```
XLVDS_INPUT_LOAD pin vss vccpd vcc LVDS_INPUT_LOAD
```

LVDS OCT Load:

```
XLVDS_OCT_LOAD pin vss vccpd vcpad vcpad vcc LVDS_OCT_LOAD
```

IO Buffer Loading Example – IO Buffer pin shared with LVDS Input pin:

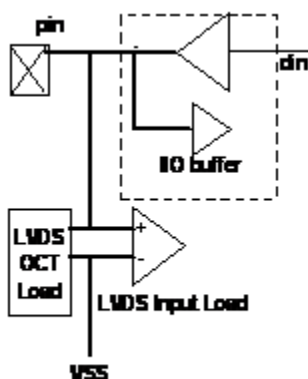


Figure 3. - Proper loading of IO buffer with LVDS input pin

The IO buffer, along with the LVDS OCT Load and LVDS Input Load should be instantiated as shown on Figure 3 above. The spice netlist for this instantiation is shown below.

```
XIO_buffer din oeb ropdrain pin rambh rndly<1> rndly<0> rpdly<1> rpdly<0>
+ rpcdn<9> rpcdn<8> rpcdn<7> rpcdn<6> rpcdn<5> rpcdn<4> rpcdn<3> rpcdn<2>
rpcdn<1> rpcdn<0>
```



```

+ rpcdp<9> rpcdp<8> rpcdp<7> rpcdp<6> rpcdp<5> rpcdp<4> rpcdp<3> rpcdp<2>
rpcdp<1> rpcdp<0>
+ vccn vccpd vcpad vcc IO_buffer_OCTRS

```

```

XLVDS_INPUT_LOAD pin vss vccpd vcc LVDS_INPUT_LOAD
XLVDS_OCT_LOAD pin vss vccpd vcpad vcpad vcc LVDS_OCT_LOAD

```

IO Buffer Loading Example – IO Buffer pin shared with LVDS Output pin:

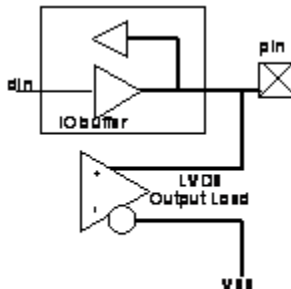


Figure 4. - Proper loading of IO buffer with LVDS output pin

The IO buffer, along with the LVDS Output Buffer Load should be instantiated as shown on Figure 4 above. The spice netlist for the circuit depicted above, is shown on the following page.

```

XIO_buffer din oeb ropdrain pin ramh rndly<1> rndly<0> rpdly<1> rpdly<0>
+ rpcdn<9> rpcdn<8> rpcdn<7> rpcdn<6> rpcdn<5> rpcdn<4> rpcdn<3> rpcdn<2>
rpcdn<1> rpcdn<0>
+ rpcdp<9> rpcdp<8> rpcdp<7> rpcdp<6> rpcdp<5> rpcdp<4> rpcdp<3> rpcdp<2>
rpcdp<1> rpcdp<0>
+ vccn vccpd vcpad vcc IO_buffer_OCTRS

```

```

XLVDS_OUTPUT_LOAD pin vss vccn vcpad vcpad vcc LVDS_OUTPUT_LOAD

```

Package Model:

The package model sub-circuit is instantiated in this section. The package sub-circuit is a lumped RLC model. The package parasitic values for various packages/devices of Cyclone-V can be obtained from Altera Applications when available.

Transmission Line Interconnect:

This section defines the topology of the target board. This may include transmission lines, interconnect, vias, connectors and cable spice sub-circuits. The end user must modify this section to represent the actual board design, or target board environment. The link provided is for reference only.

3. Differential I/O Spice Models

Figure 5 shows the general setup for the differential model spice deck. It contains the differential output buffer, package model, transmission line, termination and the differential receiver load. The package model can be changed according to the application's requirement for a specific device and package.

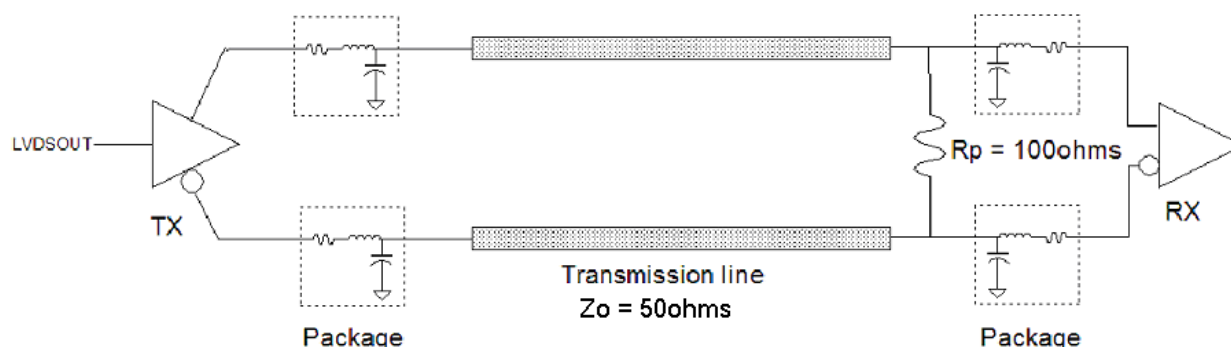


Figure 5. - Differential Spice Model Setup – Off-chip Differential Input Termination

Hspice Optimization/Initialization Header:

The section 'Options and Initial Conditions' defines some of the Avanti Hspice tool specific simulation control options. The user may need to adjust the value of these option parameters depending on the complexity of the topology of the spice circuit. These options improve the DC and transient convergence and ultimately speedup the simulation time. Some of these options are explained below:

```
.options badchr      * warns if a nonprintable character in input
.options co=132      * Set number of columns of output
.options scale=1e-6  * Linear scaling factor for L & W dimensions (um)
.options ingold=2     * Define output format as exponential
.options nomod        * Suppress model parameter output
.options dv=1.0       * Limits iteration-to-iteration voltage change for
                      * circuit node in both DCTRAN analysis(default=100)
.options probe        * Suppress post-analysis output to variables in
                      * .probe, .print, .plot, & .graph statements
.options captab=0     * 1 = Report node caps at each operating point
.options csdf=2       * Set output display for Viewtrace element template
.options accurate     * 1 = Sets timestep to give better TRAN accuracy
.options post         * 2 = Output format is ASCII
```

The section 'Process/Voltage/Temperature Setting' sets the PVT for the TYPICAL, FAST and SLOW corner case analysis. It also defines file paths of the encrypted transistor model libraries.

The voltage parameter 'vc' is defined in this section and it is a unique voltage level that is used throughout this kit to define all 'logic 1' control signals.

The section 'Power Supplies' defines the global supply voltage VCC and global ground VSS. It also defines the VTT voltage which is used as the pull-up termination voltage for the parallel terminations.

LVDS Output Buffer:

In this section, the differential Cyclone-V LVDS output buffer is instantiated by the following subcircuit:

```
XLVDS_OUT din0 out outb vccn vcpad0 vcpad1 vcc
+ kick0 vod2 vod1 vod0 rlvdsOE lvds_out
```

In this sub-circuit, the spice node 'DIN0' is the input to the differential output buffer model. Any input stimulus is applied to this node. Similarly, the nodes 'OUT' and 'OUTB' are the output nodes of the differential buffer. All these nodes are defined in detail in Table 6 of the 'Control Signals' section of this document.

LVDS Output Buffer Loading:

To appropriately model the LVDS output buffer operation, a load circuit has been created. The IO_buffer_LOAD.inc file duplicates the loading presented to each of LVDS output pins by the single-ended IO buffer. In the instantiation, the single-ended IO buffer output pins must match those of the LVDS output for proper LVDS output buffer simulation.

Note: VCPAD port of each IO Buffer Load model is connected to one of VCPAD input ports (VCPAD0, VCPAD1) of the LVDS Output buffer model in this instantiation. This is required for high voltage tolerance.

The generic instantiation of the single-ended IO buffer loading to LVDS output pins is as follows:

```
XIO_LOAD out vccn vccpd vcpad0 vcc IO_buffer_LOAD
XIO_LOADB outb vccn vccpd vcpad1 vcc IO_buffer_LOAD
```

LVDS Output Buffer Loading Example:

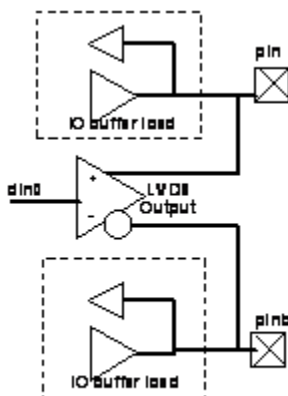


Figure 6. - Proper loading of LVDS output buffer

The LVDS output buffer, along with the IO buffer loads should be instantiated as shown above. The spice netlist for this circuit is shown below:

```
XLVDS_OUT din0 out outb vccn vccpd0 vccpd1 vcc
+ kick0 vod2 vod1 vod0 rlvds0e lvds_out

XIO_LOAD out vccn vccpd vccpd0 vcc IO_buffer_LOAD

XIO_LOADB outb vccn vccpd vccpd1 vcc IO_buffer_LOAD
```

LVDS Input Buffer:

In this section, the differential Cyclone-V LVDS Input buffer is instantiated by the following subcircuit:

```
XLVDS_INPUT_LOAD PIN PINB VCCPD VCC LVDS_INPUT_LOAD
```

In this sub-circuit, the spice nodes 'PIN' and 'PINB' are the inputs to the differential input buffer model. All these nodes are defined in detailed in Table 16 of the 'Control Signals' section of this document.

LVDS Input Buffer Loading:

To appropriately model the LVDS input buffer operation, a load circuit has been created. The `IO_buffer_LOAD.inc` file duplicates the loading presented to each of LVDS input pins by the single-ended IO buffer. In addition, the LVDS OCT Rd (differential input termination) block must be included. There are two available LVDS OCT Rd loading blocks, one for on-chip termination (`LVDS_OCT_RD`) and another for off-chip termination (`LVDS_OCT_LOAD`). These two blocks are functionally the same. However, LVDS OCT Rd is enabled in the on-chip termination case. It is disabled in the off-chip termination case so that external 100 Ω differential input termination resistor must be instantiated between two LVDS input pins. In the instantiation, the single-ended

IO buffer output pins and the LVDS OCT Rd termination pins must match those of the LVDS input buffer for proper simulation.

The generic instantiation of loading blocks to LVDS input pins is as follows:

OCT Rd Disabled (Off-chip termination)

```
XIO_LOAD_RX  PIN  VCCN VCCPD VCPAD2 VCC IO_buffer_LOAD
XIO_LOADB_RX PINB VCCN VCCPD VCPAD3 VCC IO_buffer_LOAD
XLVDS_OCT_LOAD PIN PINB VCCPD VCPAD2 VCPAD3 VCC LVDS_OCT_LOAD
```

OCT Rd Enabled (On-chip termination)

```
XIO_LOAD_RX  PIN  VCCN VCCPD VCPAD2 VCC IO_buffer_LOAD
XIO_LOADB_RX PINB VCCN VCCPD VCPAD3 VCC IO_buffer_LOAD
XLVDS_OCT_RD PIN PINB VCCPD VCPAD2 VCPAD3 VCC LVDS_OCT_RD
```

LVDS Input Buffer Loading Example:

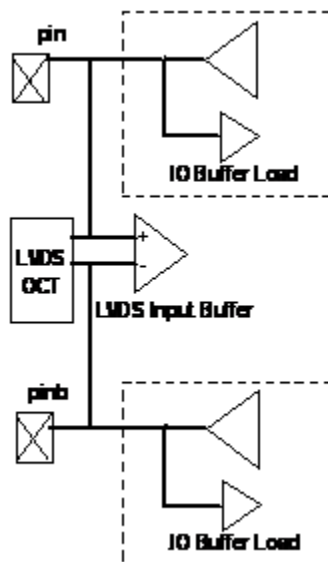


Figure 7. - Proper loading of LVDS input buffer

The LVDS input buffer, along with the IO buffer loads and OCT Rd should be instantiated as shown above. The spice netlist for this circuit, with or without active LVDS OCT Rd termination, is shown below.

OCT Rd Disabled (Off-chip termination)

```
XLVDS_INPUT_LOAD PIN PINB VCCPD VCC LVDS_INPUT_LOAD
XIO_LOAD_RX  PIN  VCCN VCCPD VCPAD2 VCC IO_buffer_LOAD
```

```
XIO_LOADB_RX PINB VCCN VCCPD VCPAD3 VCC IO_buffer_LOAD
XLVDS_OCT_LOAD PIN PINB VCCPD VCPAD2 VCPAD3 VCC LVDS_OCT_LOAD
```

OCT Rd Enabled (On-chip termination)

```
XLVDS_INPUT_LOAD PIN PINB VCCPD VCC LVDS_INPUT_LOAD
XIO_LOAD_RX PIN VCCN VCCPD VCPAD2 VCC IO_buffer_LOAD
XIO_LOADB_RX PINB VCCN VCCPD VCPAD3 VCC IO_buffer_LOAD
XLVDS_OCT_RD PIN PINB VCCPD VCPAD2 VCPAD3 VCC LVDS_OCT_RD
```

Package Model:

The package model sub-circuit is instantiated in this section. The package sub-circuit is a lumped RLC model. The package parasitic values for various packages/devices of Cyclone-V can be obtained from Altera Applications when available.

4. Control Signals

This section defines control signals used by the Cyclone-V single ended and differential output buffer models. Table 2 to 5 show the control signals used by the single ended output buffer model. Similarly, Table 6 describes the controls used by the differential output buffer model. Table 7 to 11 show the load model for both single ended or differential buffers.

Section 6 'Setting I/O Standards' describes how to use these parameters to set up the buffer for a specific I/O standard. Section 7 'Controlling Output Delay of SE Output Buffer' shows how to independently control the output rising and falling edge delay of the single-ended output buffer. Section 8 'Setting Output Slew Rate of SE Output Buffer' explains how to use slew rate feature of the Cyclone-V single-ended output buffer. Section 9 describes programmable pre-emphasis and VOD features of the differential output buffers.

Model Port Names	Description
DIN	Data input to the single ended output buffer from the core.
OEB	Output Enable. Set to 0 to enable, vc to disable.
ROPDRAIN	Open Drain. Set to vc to enable, 0 to disable.
PIN	Output of the output buffer.
RAMBH	Bus Hold Enable. Set to vc to enable, 0 to disable.
RPCDP<9:0>	Controls the PMOS output transistors. Set by drive_select_IO.lib.
RPCDN<9:0>	Controls the NMOS output transistors. Set by drive_select_IO.lib.
RPULLUP	Weak Pull-Up Enable. Set to vc to enable and to 0 to disable.
RPDLY<1:0> RNDLY<1:0>	Controls output rise and fall edge delay of the output buffer. Set by output_delay_control.lib.
RSLEWP	Controls output slew rate of rise edge. Set by slew_rate_control.lib.
RSLEWN	Controls output slew rate of fall edge. Set by slew_rate_control.lib.
VCCN	I/O buffer supply voltage.
VCCPD	Fixed 3.0v supply voltage for 3V I/O standards. Fixed 2.5v supply voltage for 2.5V or below I/O standards.
VCCPADXG	Supply voltage output port used for high voltage tolerance.
VCC	Global supply voltage.
VSS	Global supply ground.

Table 2: Control Signals for Single Ended Output Buffer Model - IO_buffer.inc

Model Port Names	Description
DIN	Data input to the single ended output buffer from the core.
OEB	Output Enable. Set to 0 to enable, vc to disable.
ROPDRAIN	Open Drain. Set to vc to enable, 0 to disable.
PIN	Output of the output buffer.
RAMBH	Bus Hold Enable. Set to vc to enable, 0 to disable.
RPCDP<9:0>	Controls the PMOS output transistors. Set by drive_select_IO.lib.
RPCDN<9:0>	Controls the NMOS output transistors. Set by drive_select_IO.lib.
RPDLY<1:0> RNDLY<1:0>	Controls output rise and fall edge delay of the output buffer. Set by output_delay_control.lib.
VCCN	I/O buffer supply voltage.
VCCPD	Fixed 3.0v supply voltage for 3V I/O standards. Fixed 2.5v supply voltage for 2.5V or below I/O standards.
VCCPADXG	Supply voltage output port used for high voltage tolerance.
VCC	Global supply voltage.
VSS	Global supply ground.

Table 3: Control Signals for OCT Rs Single Ended IO Buffer Model - IO_buffer_OCTRS.inc

Model Port Names	Description
DIN	Data input to the single ended output buffer from the core.
OEB	Output Enable. Set to 0 to enable, vc to disable.
ROPDRAIN	Open Drain. Set to vc to enable, 0 to disable.
PIN	Output of the output buffer.
RAMBH	Bus Hold Enable. Set to vc to enable, 0 to disable.
RPCDP<9:0>	Controls the PMOS output transistors. Set by IO_OCTRS_calibrated.lib.
RPCDN<9:0>	Controls the NMOS output transistors. Set by IO_OCTRS_calibrated.lib.
RPDLY<1:0> RNDLY<1:0>	Controls output rise and fall edge delay of the output buffer. Set by output_delay_control.lib.
VCCN	I/O buffer supply voltage.
VCCPD	Fixed 3.0v supply voltage for 3.0V I/O standards. Fixed 2.5v supply voltage for 2.5V or below I/O standards.
VCCPADXG	Supply voltage output port used for high voltage tolerance.
VCC	Global supply voltage.
VSS	Global supply ground.

Table 4: Control Signals for Calibrated OCT-Rs IO Buffer Model – IO_buffer_OCTRS.inc

Model Port	Description
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Names	
DIN	Data input to the single ended output buffer from the core.
OEB	Output Enable. Set to 0 to enable, vc to disable.
ROPDRAIN	Open Drain. Set to vc to enable, 0 to disable.
PIN	Output of the output buffer.
RAMBH	Bus Hold Enable. Set to vc to enable, 0 to disable.
RPCDP<9:0>	Controls the PMOS output transistors. Set by IO_OCTRT_calibrated.lib.
RPCDN<9:0>	Controls the NMOS output transistors. Set by IO_OCTRT_calibrated.lib.
RPDLY<1:0> RNDLY<1:0>	Controls output rise and fall edge delay of the output buffer. Set by output_delay_control.lib.
VCCN	I/O buffer supply voltage.
VCCPD	Fixed 3.0v supply voltage for 3.0V I/O standards. Fixed 2.5v supply voltage for 2.5V or below I/O standards.
VCCPADXG	Supply voltage output port used for high voltage tolerance.
VCC	Global supply voltage.
VSS	Global supply ground.

Table 5: Control Signals for Calibrated OCT-Rt IO Buffer Model – IO_buffer_OCTRT.inc

Model Port Names	Description
DIN0	Data input to the differential output buffer from the core.
OUT/OUTB	Output pins of differential output buffer.
RLVDSOE	To enable/disable differential output buffer. Set to vc to enable, 0 to disable.
KICK<0>	Controls pre-emphasis strength. Set by lvds_preemphasis_select.lib.
VOD<2:0>	Controls VOD strength. Set by lvds_vod_select.lib.
VCCN	Fixed 2.5v supply voltage for LVDS I/O standard.
VCPAD0 VCPAD1	Supply input ports to be connected to IO_buffer_LOAD VCPAD output port for high voltage tolerance.
VCC	Global supply voltage.
VSS	Global supply ground.

Table 6: Control Signals for Differential Output Buffer Model – LVDS_OUTPUT.inc

Model Port Names	Description
PIN	Output pin for loading.
VCCPD	Fixed 3.0v supply voltage for 3V I/O standards. Fixed 2.5v supply voltage for 2.5V or below I/O standards.
VCCPADXG	Supply voltage output port used for high voltage tolerance. Connects to the VCPAD0/VCPAD1 ports of the LVDS load models.
VCCN	I/O buffer supply voltage.
VCC	Global supply voltage.
VSS	Global supply ground.

Table 7: Control Signals for Single Ended Output Buffer Load Model – IO_buffer_LOAD.inc

Model Port Names	Description
OUT/OUTB	Output pins for loading.
VCCN	I/O buffer supply voltage.
VCPAD0 VCPAD1	Supply input pins to be connected to the IO_buffer VCPAD output ports for high voltage tolerance.
VCC	Global supply voltage.
VSS	Global supply ground.

Table 8: Control Signals for LVDS Output Buffer Load Model – LVDS_OUTPUT_LOAD.inc

Model Port Names	Description
IN/INA	Input pins for loading.
VCCPD	Fixed 3.0v supply voltage for 3V I/O standards. Fixed 2.5v supply voltage for 2.5V or below I/O standards.
VCC	Global supply voltage.
VSS	Global supply ground.

Table 9: Control Signals for LVDS Input Buffer Load Model – LVDS_INPUT_LOAD.inc

Model Port Names	Description
LVDSIN/LVDSINA	Input pins for loading.
VCCPD	Fixed 3.0v supply voltage for 3V I/O standards. Fixed 2.5v supply voltage for 2.5V or below I/O standards.
VCPAD0 VCPAD1	Supply voltage input pins to be connected to the VCPAD output port of the IO_buffer for high voltage tolerance.
VCC	Global supply voltage.
VSS	Global supply ground.

Table 10: Control Signals for LVDS OCT Load Model – LVDS_OCT_LOAD.inc

Model Port Names	Description
LVDSIN/LVDSINA	Input pins for loading.
VCCPD	Fixed 3.0v supply voltage for 3V I/O standards. Fixed 2.5v supply voltage for 2.5V or below I/O standards.
VCPAD0 VCPAD1	Supply voltage input pins to be connected to the VCPAD output port of the IO_buffer for high voltage tolerance.
VCC	Global supply voltage.
VSS	Global supply ground.

Table 11: Control Signals for LVDS OCT Rd Model – LVDS_OCT_RD.inc

5. Setting I/O Standards

Output standards that are supported in Cyclone-V output buffer models:

Standard	Supply
3.3V LVTTL/LVCMOS	3.3v
3.0V LVTTL/LVCMOS	3.0v
LVCMOS	2.5v
LVCMOS	1.8v
LVCMOS	1.5v
LVCMOS	1.2v
SSTL2 Class I	2.5v
SSTL2 Class II	2.5v
SSTL18 Class I	1.8v
SSTL18 Class II	1.8v
SSTL15 Class I	1.5v
SSTL15 Class II	1.5v
SSTL15	1.5v
SSTL135	1.35v
SSTL125	1.25v
SSTL12	1.2v
1.8V HSTL Class I	1.8v
1.8V HSTL Class II	1.8v
1.5V HSTL Class I	1.5v
1.5V HSTL Class II	1.5v
1.2V HSTL Class I	1.2v
1.2V HSTL Class II	1.2v
HSUL12	1.2v
LVDS	2.5v

Table 12: I/O Standards supported in the Cyclone-V Hspice models

Setting Single Ended Standards

To enable a single ended output standard, the following steps need to be taken:

- 1) Set OEB to 0 to enable the single-ended output buffer: `VOEB OEB 0 0`
- 2) Select the required output standard by using the `drive_select_IO.lib` library.
For example, to select 3.0v LVTTL 8mA output for the IO, use the following line:
`.lib '../lib/drive_select_IO.lib' 3p0ttl_8ma`
- 3) Set the VCCN and VCCPD buffer power supplies to the appropriate voltage for the selected output standard. Set VCCPD to 3.0v for 3.0V I/O standards, 2.5v for 2.5V I/O standards.

Example:	3.0v LVTTL 8mA standard:	SSTL18 Class II 8mA standard:
	<code>.param vcn = 3.0</code>	<code>.param vcn = 1.8</code>
	<code>.param vpd = 3.0</code>	<code>.param vpd = 2.5</code>

Setting Differential Standards

To enable the differential output buffer, user needs to set RLVDSON to vc to enable the differential output buffer: `VRLVDSON RLVDSON 0 vc`

6. Enabling Calibrated OCT-Rs

Cyclone-V devices incorporate calibration circuitry to adjust the output buffer to maintain calibrated OCT-Rs resistances within specifications across process, voltage, and temperature variations. This model is intended to provide typical and worst case conditions to guarantee system designs across worst-case corners. To facilitate typical and worst case system simulations, three corner settings have been provided for each operating voltage level and Rs value. The “typical” operating condition specifies the TT process model, 25°C, and nominal voltage conditions. The “fast” worst case operating condition specifies the FF process model, 0°C, and high voltage conditions (+5% V_{CCN} and V_{CCPD} , +50mV V_{CC}). The “slow” worst-case operating condition specifies the SS process model, 85°C, and low voltage conditions (-5% V_{CCN} and V_{CCPD} , -50mV V_{CC}). The simulation conditions are illustrated in Table 20:

Simulation Corner	Process	Voltage			Temperature
		Vcc	Vccn	Vccpd	
Typical	TT	Nom.	Nom.	Nom.	25°C
Fast	FF	+ 50mV	+ 5%	+ 5%	0°C
Slow	SS	- 50mV	- 5%	- 5%	85°C

Table 13: Corner Simulation Conditions and Settings

Simulation Setting Example – IO OCT-Rs 50ohm 3.0v – “Slow” condition:

To enable simulation of the calibrated OCT-Rs IO buffer, make the following adjustments to the spice simulation deck. Use the three decks provided (IO_OCTRS_calibrated_TT.spi, IO_OCTRS_calibrated_SS.spi, IO_OCTRS_calibrated_FF.spi) as a starting point.

1. Adjust the process corner:

```
* Process settings
*.inc '../lib/CV_TT.inc'      * Typical Typical
*.inc '../lib/CV_SS.inc'     * Slow Slow
*.inc '../lib/CV_FF.inc'     * Fast Fast
```

2. Adjust the temperature setting:

```
* Temperature
*.temp 25c
*.temp 0
*.temp 85
```

3. Adjust the voltage levels:

```
* Supply Voltages
.param vc='1.1-0.05'
.param vcn='3.0*0.95'
*.param vcn='1.8*0.95'
.param vpd='3.0*0.95'
*.param vpd='2.5*0.95'
```

4. Select the proper OCT-Rs calibration setting:

```
.lib '../lib/IO_OCTRS_calibrated.inc' 50_3p0_SS
```

Simulating other conditions and settings:

Note that these models solely provide the “typical” and worst-case simulation corners “fast” and “slow.” **Simulations outside of these specific operating conditions are not supported by this model.** Use of this calibration model outside of its specified operating conditions will not accurately reflect silicon behavior, and results may exceed OCT-Rs variance specifications.

7. Enabling Calibrated OCT-Rt

Cyclone V devices incorporate calibration circuitry to adjust the output buffer to maintain calibrated OCT-Rt resistances within specifications across process, voltage, and temperature variations. This model is intended to provide typical and worst case conditions to guarantee system designs across worst-case corners. To facilitate typical and worst case system simulations, three corner settings have been provided for each operating voltage level. The “typical” operating condition specifies the TT process model, 25°C, and nominal voltage conditions. The “fast” worst case operating condition specifies the FF process model, 0°C, and high voltage conditions (+5% V_{CCN} and V_{CCPD} , +50mV V_{CC}). The “slow” worst-case operating condition specifies the SS process model, 85°C, and low voltage conditions (-5% V_{CCN} and V_{CCPD} , -50mV V_{CC}). The simulation conditions are illustrated in Table 14:

Simulation Corner	Process	Voltage			Temperature
		Vcc	Vccn	Vccpd	
Typical	TT	Nom.	Nom.	Nom.	25°C
Fast	FF	+ 50mV	+ 5%	+ 5%	0°C
Slow	SS	- 50mV	- 5%	- 5%	85°C

Table 14: Corner Simulation Conditions and Settings

Simulation Setting Example – IO OCT-Rt 50ohm 1.5V – “Slow” condition:

To enable simulation of the calibrated OCT-Rt IO buffer, make the following adjustments to the spice simulation deck. Use the six decks provided (IO_OCTRT_calibrated_TT.spi, IO_OCTRT_calibrated_SS.spi, IO_OCTRT_calibrated_FF.spi) as a starting point.

5. Adjust the process corner:

```
* Process settings
*.inc '../..../lib/CV_TT.inc'      * Typical Typical
*.inc '../..../lib/CV_SS.inc'      * Slow Slow
*.inc '../..../lib/CV_FF.inc'      * Fast Fast
```

6. Adjust the temperature setting:

```
* Temperature
*.temp 25c
*.temp 0
*.temp 85
```

7. Adjust the voltage levels:

```
* Supply Voltages
.param vc='1.1-0.05'
.param vcn='1.5*0.95'
*.param vcn='1.8*0.95'
*.param vcn='1.5*0.95'
*.param vcn='1.2*0.95'
.param vpd='2.5*0.95'
```

8. Select the proper OCT-Rt calibration setting:

```
.lib '../..../lib/IO_OCTRT_calibrated.inc' 50_1p5_SS
```

Simulating other conditions and settings:

To setup the spice deck for other simulation corners or OCT-Rt settings, simply follow these same steps outlined above (1-4).

Note that these models solely provide the “typical” and worst-case simulation corners “fast” and “slow” for commercial temperature ranges. **Simulations outside of these specific operating conditions are not supported by this model.** Use of this calibration model outside of its specified operating conditions will not accurately reflect silicon behavior, and results may exceed OCT-Rt variance specifications.

8. Controlling Output Delay of SE Output Buffer

Cyclone-V SE output buffer has a new feature called programmable output delay control. It allows the user to independently delay output signal's rising and falling edges of the output buffer. Therefore, user can adjust output buffer duty cycle, compensate or deliberately introduce channel to channel skew, and improve high speed memory interface timing margin. The supported output delay settings are shown on Table 15 below.

Delay Settings	
No Delay	
Falling	50ps
	100ps
	150ps
Rising	50ps
	100ps
	150ps
Both Falling and Rising	50ps
	100ps
	150ps

Table 15: Output Delay Control settings supported by the Cyclone-V SE Output Buffer

Setting Output Delay Control

User can select the preferred output delay setting by using `output_delay_control.lib` library. The default setting is 'No Delay'.

Example #1: No Delay

```
.lib ../../lib/output_delay_control.lib' no_delay
```

Example #2: Both Falling and Rising 50ps

```
.lib ../../lib/output_delay_control.lib' both_50ps
```


9. Setting Output Slew Rate of SE Output Buffer

Another new feature of Cyclone-V SE output buffer is programmable slew rate. The slew rate of the rising and falling edges can be controlled independently of each other. Fast slew rate is used to achieve maximum I/O performance. Slower slew rate settings, on the other hand, are used to reduce system noise and signal overshoot.

The default setting for slew rate depends on the I/O standard being used. When default setting is chosen, both the rising and falling edges use the same default slew rate setting assigned for the particular I/O standard being used. Table 16 shows slew rate settings supported by the Cyclone-V SE output buffer.

Slew Rate	Default Setting
Fast	SSTL, HSTL, TTL, CMOS, HSUL, OCT_Rs
Slow	-

Table 16: Output Slew Rate Control settings supported by the Cyclone-V SE Output Buffer

Setting Output Slew Rate Control

User can select the preferred slew rate setting by using `slew_rate_control.lib` library.

Example #1: Fast Slew Rate for both rise and fall edge

```
.lib `../../lib/slew_rate_control.lib' fast
```

Example #2: Slow Slew Rate on both rise and fall edge

```
.lib `../../lib/slew_rate_control.lib' slow
```

Example #3: Default setting for any SSTL I/O standard

```
.lib `../../lib/slew_rate_control.lib' sstl_def
```

10. Pre-Emphasis and VOD of LVDS Output Buffer

Cyclone-V LVDS output buffers include programmable pre-emphasis circuit to compensate frequency dependent attenuation of the transmission line. It increases the amplitude of high frequency component of the output signal. Figure 8 shows the effect of pre-emphasis as well as VOD. Pull-up and pull-down of either Pre-emphasis or VOD feature must be set to the same setting by the user.

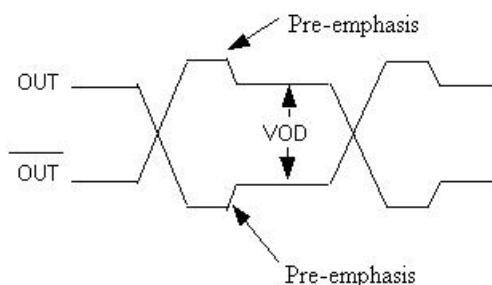


Figure 8. LVDS Output with Pre-emphasis

Available VOD Settings
Vod_def
Low
High

Available Pre-emphasis Settings
Zero
Preemp_def

Table 17: VOD and Pre-emphasis settings available in the Cyclone-V LVDS Output Buffer

Setting Pre-emphasis

User can select the preferred pre-emphasis setting by using `lvds_preemphasis_select.lib` library.

Example #1: Default pre-emphasis

```
.lib ../../lib/lvds_preemphasis_select.lib' preemp_def
```

Example #2: Zero pre-emphasis

```
.lib ../../lib/lvds_preemphasis_select.lib' Zero
```

Setting VOD

User can select the preferred VOD setting by using `lvds_vod_select.lib` library.

Example #1: High VOD on pull-up and on pull-down

```
.lib ../../lib/lvds_vod_select.lib' high
```

Example #2: Low VOD on pull-up and on pull-down

```
.lib ../../lib/ lvds_vod_select.lib' low
```

11. Scale Factor

For Cyclone V, Altera is using scale factor = 1, but some other vendors might not use a scale factor=1. To be able to use the Hspice models of various vendors, with mix technology, **Hier_scale** needs to be used.

Following steps should be taken:

- 1) If you want to do the mixed technology simulations, you will have to override the .OPTION SCALE of the two vendors
- 2) Enable option HIER_SCALE
- 3) Make sure that neither vendor is using the parameter "S" in their subcircuits.
- 4) At the top-level, add "S=1e-6" AT THE END of the instance call for the vendor instance which requires SCALE=1e-6. (example Altera)

Below is an example of how to implement Hier_scale in the spice deck:

```
* top-level netlist
.inc vendor1.inc    $ Uses SCALE=1e-6
.inc altera.inc     $ Uses SCALE=1
.option SCALE=1 HIER_SCALE
x1 in wire_in vendor1_outbuf S=1e-6
x2 wire_out out altera_inbuf S=1
w1 wire_in 0 wire_out 0 RLGCmodel=...
...
```

12. Simulation Example – SSTL I/O Standard using IO

This section provides a tutorial example spice deck, describing in detail how to successfully simulate board designs that contain Cyclone-V devices. It is recommended that the user follow this example to get started. This example can be easily modified to replace the current board trace with any user specified board design.

Topology of the spice deck IO_SSTL.spi:

1. **Process settings:** This section defines the process corner for worst, best, and typical cases. For typical PVT, the CV_TT.inc model is used.

```
* Process settings
.inc '../lib/CV_TT.inc'      * Typical Typical
*.inc '../lib/CV_SS.inc'    * Slow Slow
*.inc '../lib/CV_FF.inc'    * Fast Fast
```

2. **Options and initial conditions:** This section contains various Hspice options required to improve the overall simulation quality such as DC and transient convergence. The user may need to adjust these parameters and/or their values each time the topology of the spice deck is changed.

```
* Simulation options
.options brief=0
.options badchr co=132 acct ingold=2 nomod dv=1.0
+      dcstep=1 absv=1e-3 absi=1e-8 probe captab csdf=2 accurate=1
.param ccoflag=1
.param rgflag=0
```

3. **Temperature Setting:** This section defines the temperature for worst, best, and typical cases. For typical PVT, temp=25c.

```
* Temperature
.temp 25c
*.temp 0
*.temp 85
```

4. **Supply voltage setting:** This section defines the operating voltage of the device, for both core and IO voltages.

```
* Supply Voltages
.param vc=1.1
*.param vcn=3.0
.param vcn=2.5
*.param vcn=1.8
*.param vcn=1.5
.param vpd=2.5
```

5. **Power supplies:** This sections sets the supply voltages used by the IO buffer.

```
vcc      vcc      0      vc
vccn     vccn     0      vcn
```

```

vcccpd      vccpd      0      vpd
vvss        vss        0      0

```

6. **Constant definition:** Here the ram bits and control voltages of the output buffer are set. The majority are parameters that are defined by the drive_select, output_delay_control, and slew_rate_control libraries.

7. **Netlist:** This section includes the encrypted buffer netlist.

```
.include '../..../cir/IO_buffer.inc'
```

8. **Circuit instantiation:** This section instantiates the output buffers and defines the nodes connected to the output buffer

```

XIO_buffer din oeb ropdrain pin rambh rndly<1> rndly<0> rpdly<1> rpdly<0>
+ rpcdn<9> rpcdn<8> rpcdn<7> rpcdn<6> rpcdn<5> rpcdn<4> rpcdn<3> rpcdn<2>
rpcdn<1> rpcdn<0>
+ rpcdp<9> rpcdp<8> rpcdp<7> rpcdp<6> rpcdp<5> rpcdp<4> rpcdp<3> rpcdp<2>
rpcdp<1> rpcdp<0>
+ rslewn rslewp vccn vccpd vcpad vcc io_buffer

```

9. **Package model:** This section includes and instantiates the lumped RLC package model used on this output trace.

```
.lib '../..../lib/package.lib' io
XPKG pin ball IO_PKG
```

10. **Board trace, discontinuities, and termination:** This section creates the sample trace model. This example uses a sample board, one 25 ohm series resistor, two 50 ohm parallel termination resistors, and a capacitive load at the destination. All termination devices are set by the IO_load.lib library.

```

* Transmission line
.inc '../..../lib/sample_brd.sp'
Xtline source vss dest vss sample_brd

* Termination resistors
rrs ball source rseries
rrt1 source vtt rt1
rrt2 dest vtt rt2

* Destination loading
cload dest 0 loadcap

```

11. **Transient simulation and spice output:** This section executes the transient simulation for 17ns, outputs the waveforms seen at the nodes listed, and measures the rise and fall time of the waveform at the destination node.

```

* Transient Simulation
.tran 0.001ns 17ns

* Waveform Output Data
.print tran v(din) v(pin) v(ball) v(source) v(dest)

```

```

* Measure Output Data
.meas vmax MAX v(dest) from = 6ns to = 10ns
.meas vmin MIN v(dest) from = 0.1ns to = 4ns
.meas tran rise_time trig v(dest) val='0.2*(vmax-vmin)+vmin' rise=1 targ
v(dest) val='0.8*(vmax-vmin)+vmin' rise=1
.meas tran fall_time trig v(dest) val='0.8*(vmax-vmin)+vmin' fall=1 targ
v(dest) val='0.2*(vmax-vmin)+vmin' fall=1

```

- 12. Drive strength settings:** This final section selects the IO standard to be simulated, selects the termination scheme to be used, and allows for re-simulation with other IO standards and settings.

```

* sst12i_8ma
.lib '../..../lib/drive_select_IO.inc' sst12i_8ma
.lib '../..../lib/IO_load.lib' sst12_class1

.alter sst18ii_16ma
.lib '../..../lib/drive_select_IO.inc' sst18ii_16ma
.lib '../..../lib/IO_load.lib' ssst18_class2
.param vcn=1.8

```

13. APPENDIX

Valid drive strengths for drive_select_IO.lib

IO – Valid Drive Strengths		Library Call
3.3V LVTTTL	4mA	3p3ttl_4ma
3.3V LVTTTL	8mA	3p3ttl_8ma
3.3V LVTTTL	16mA	3p3ttl_16ma
3.0V LVTTTL	4mA	3p0ttl_4ma
3.0V LVTTTL	8mA	3p0ttl_8ma
3.0V LVTTTL	12mA	3p0ttl_12ma
3.0V LVTTTL	16mA	3p0ttl_16ma
3.3V LVCMOS	2mA	3p3cmos_2ma
3.0V LVCMOS	4mA	3p0cmos_4ma
3.0V LVCMOS	8mA	3p0cmos_8ma
3.0V LVCMOS	12mA	3p0cmos_12ma
3.0V LVCMOS	16mA	3p0cmos_16ma
2.5V CMOS	4mA	2p5cmos_4ma
2.5V CMOS	8mA	2p5cmos_8ma
2.5V CMOS	12mA	2p5cmos_12ma
2.5V CMOS	16mA	2p5cmos_16ma
1.8V CMOS	2mA	1p8cmos_2ma
1.8V CMOS	4mA	1p8cmos_4ma
1.8V CMOS	6mA	1p8cmos_6ma
1.8V CMOS	8mA	1p8cmos_8ma
1.8V CMOS	10mA	1p8cmos_10ma
1.8V CMOS	12mA	1p8cmos_12ma
1.5V CMOS	2mA	1p5cmos_2ma
1.5V CMOS	4mA	1p5cmos_4ma
1.5V CMOS	6mA	1p5cmos_6ma
1.5V CMOS	8mA	1p5cmos_8ma
1.5V CMOS	10mA	1p5cmos_10ma
1.5V CMOS	12mA	1p5cmos_12ma
1.2V CMOS	2mA	1p2cmos_2ma
1.2V CMOS	4mA	1p2cmos_4ma
1.2V CMOS	6mA	1p2cmos_6ma
1.2V CMOS	8mA	1p2cmos_8ma
SSTL2 class I	8mA	sstl2i_8ma
SSTL2 class I	10mA	sstl2i_10ma
SSTL2 class I	12mA	sstl2i_12ma
SSTL2 class II	16mA	sstl2ii_16ma
SSTL18 class I	4mA	sstl18i_4ma
SSTL18 class I	6mA	sstl18i_6ma
SSTL18 class I	8mA	sstl18i_8ma
SSTL18 class I	10mA	sstl18i_10ma
SSTL18 class I	12mA	sstl18i_12ma
SSTL18 class II	16mA	sstl18ii_16ma
SSTL15 class I	4mA	sstl15i_4ma
SSTL15 class I	6mA	sstl15i_6ma
SSTL15 class I	8mA	sstl15i_8ma
SSTL15 class I	10mA	sstl15i_10ma
SSTL15 class I	12mA	sstl15i_12ma

IO – Valid Drive Strengths		Library Call
SSTL15 class II	16mA	sstl15ii_16ma
SSTL15	34ohm	sstl15_34ohm
SSTL15	40ohm	sstl15_40ohm
SSTL135	34ohm	sstl135_34ohm
SSTL135	40ohm	sstl135_40ohm
SSTL125	34ohm	sstl125_34ohm
SSTL125	40ohm	sstl125_40ohm
SSTL12	40ohm	sstl12_40ohm
SSTL12	60ohm	sstl12_60ohm
SSTL12	240ohm	sstl12_240ohm
HSTL18 class I	4mA	hstl18i_4ma
HSTL18 class I	6mA	hstl18i_6ma
HSTL18 class I	8mA	hstl18i_8ma
HSTL18 class I	10mA	hstl18i_10ma
HSTL18 class I	12mA	hstl18i_12ma
HSTL18 class II	16mA	hstl18ii_16ma
HSTL15 class I	4mA	hstl15i_4ma
HSTL15 class I	6mA	hstl15i_6ma
HSTL15 class I	8mA	hstl15i_8ma
HSTL15 class I	10mA	hstl15i_10ma
HSTL15 class I	12mA	hstl15i_12ma
HSTL15 class II	16mA	hstl15ii_16ma
HSTL12 class I	4mA	hstl12i_4ma
HSTL12 class I	6mA	hstl12i_6ma
HSTL12 class I	8mA	hstl12i_8ma
HSTL12 class I	10mA	hstl12i_10ma
HSTL12 class I	12mA	hstl12i_12ma
HSTL12 class II	16mA	hstl12ii_16ma
HSUL12	34ohm	hsul12_34ohm
HSUL12	40ohm	hsul12_40ohm
HSUL12	48ohm	hsul12_48ohm
HSUL12	60ohm	hsul12_60ohm
HSUL12	80ohm	hsul12_80ohm
3.0V 50ohm OCT-Rs		30v_50ohm
3.0V 25ohm OCT-Rs		30v_25ohm
2.5V 50ohm OCT-Rs		25v_50ohm
2.5V 25ohm OCT-Rs		25v_25ohm
1.8V 50ohm OCT-Rs		18v_50ohm
1.8V 25ohm OCT-Rs		18v_25ohm
1.5V 50ohm OCT-Rs		15v_50ohm
1.5V 25ohm OCT-Rs		15v_25ohm
1.2V 50ohm OCT-Rs		12v_50ohm
1.2V 25ohm OCT-Rs		12v_25ohm

Table 18: Library calls for valid SE IO drive strengths within drive_select_IO.lib

Valid OCT-Rs settings for IO_OCTRS_calibrated.lib

OCT-Rs	I/O Voltage	Tolerance	Typical	Slow	Fast
50 ohms	1.2V	+/-15%	50_1p2_TT	50_1p2_SS	50_1p2_FF
50 ohms	1.5V	+/-15%	50_1p5_TT	50_1p5_SS	50_1p5_FF
50 ohms	1.8V	+/-15%	50_1p8_TT	50_1p8_SS	50_1p8_FF
50 ohms	2.5V	+/-15%	50_2p5_TT	50_2p5_SS	50_2p5_FF
50 ohms	3.0V	+/-15%	50_3p0_TT	50_3p0_SS	50_3p0_FF

Table 19: Provided Corner 50ohm OCT-Rs Settings in IO_OCTRS_calibrated.lib

OCT-Rs	I/O Voltage	Tolerance	Typical	Slow	Fast
25 ohms	1.2V	+/-15%	25_1p2_TT	25_1p2_SS	25_1p2_FF
25 ohms	1.5V	+/-15%	25_1p5_TT	25_1p5_SS	25_1p5_FF
25 ohms	1.8V	+/-15%	25_1p8_TT	25_1p8_SS	25_1p8_FF
25 ohms	2.5V	+/-15%	25_2p5_TT	25_2p5_SS	25_2p5_FF
25 ohms	3.0V	+/-15%	25_3p0_TT	25_3p0_SS	25_3p0_FF

Table 20: Provided Corner 25ohm OCT-Rs Settings in IO_OCTRS_calibrated.lib**Valid OCT-Rt settings for IO_OCTRT_calibrated.lib**

OCT-Rt	I/O Voltage	Tolerance	Typical	Slow	Fast
50 ohms	1.2V	-10% to +40%	50_1p2_TT	50_1p2_SS	50_1p2_FF
50 ohms	1.5V	-10% to +40%	50_1p5_TT	50_1p5_SS	50_1p5_FF
50 ohms	1.8V	-10% to +40%	50_1p8_TT	50_1p8_SS	50_1p8_FF
50 ohms	2.5V	-10% to +40%	50_2p5_TT	50_2p5_SS	50_2p5_FF
50 ohms	3.0V	-10% to +40%	50_3p0_TT	50_3p0_SS	50_3p0_FF

Table 21: Provided Corner 50ohm OCT-Rt Settings in IO_OCTRT_calibrated.lib

OCT-Rt	I/O Voltage	Tolerance	Typical	Slow	Fast
25 ohms	1.2V	-10% to +40%	25_1p2_TT	25_1p2_SS	25_1p2_FF
25 ohms	1.5V	-10% to +40%	25_1p5_TT	25_1p5_SS	25_1p5_FF
25 ohms	1.8V	-10% to +40%	25_1p8_TT	25_1p8_SS	25_1p8_FF

25 ohms	2.5V	-10% to +40%	25_2p5_TT	25_2p5_SS	25_2p5_FF
25 ohms	3.0V	-10% to +40%	25_3p0_TT	25_3p0_SS	25_3p0_FF

Table 22: Provided Corner 25ohm OCT-Rt Settings in IO_OCTRT_calibrated.lib

Valid output delays for output_delay_control.lib

Delay Settings		Library Call
No Delay		def_delay no_delay
Falling	50ps	fall_50ps
	100ps	fall_100ps
	150ps	fall_150ps
Rising	50ps	rise_50ps
	100ps	rise_100ps
	150ps	rise_150ps
Both Falling and Rising	50ps	both_50ps
	100ps	both_100ps
	150ps	both_150ps

Table 23: Library calls for valid SE IO output delays within output_delay_control.lib

Valid slew rates for slew_rate_control.lib

Pull-Up Slew Rate	Pull-Down Slew Rate	Fast	Slow
	Fast	Fast ttl_def cmos_def sstl_def hstl_def hsul_rs oct_rs	
	Slow		Slow

Table 24: Library calls for valid IO slew rates within slew_rate_control.lib

Valid LVDS pre-emphasis settings for lvds_preemphasis_select.lib

Pre-emphasis Settings	Library Call
Zero	zero

Default	preemp_def
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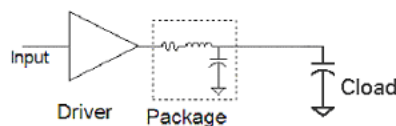
Table 25: Library calls for valid LVDS pre-emphasis settings within lvds_preemphasis_select.lib**Valid LVDS VOD settings for lvds_vod_select.lib**

VOD Settings	Library Call
Low	low
Medium	vod_def
High	high

Table 26: Library calls for valid LVDS VOD settings within lvds_vod_select.lib**Valid sample termination schemes and loadings within IO_load.lib**

- Termination schemes are for single-ended signaling standards only

Termination Scheme	Library Call
LVTTL/LVCMOS	ttl
SSTL2 Class-I	sstl2_class1
SSTL2 Class-II	sstl2_class2
SSTL18 Class-I	sstl18_class1
SSTL18 Class-II	sstl18_class2
SSTL15 Class-I	sstl15_class1
SSTL15 Class-II	sstl15_class2
HSTL18 Class-I	hstl18_class1
HSTL18 Class-II	hstl18_class2
HSTL15 Class-I	hstl15_class1
HSTL15 Class-II	hstl15_class2
HSTL12 Class-I	hstl12_class1
HSTL12 Class-II	hstl12_class2
HSUL12	Hsul12
50ohm OCT-Rs	oct_rs_50ohm
25ohm OCT-Rs	oct_rs_25ohm
50ohm OCT-Rt	oct_rt_50ohm
25ohm OCT-Rt	oct_rt_25ohm

Table 27: Library calls for sample termination schemes in IO_load.lib*Figure 9. - LVTTL/LVCMOS Termination*

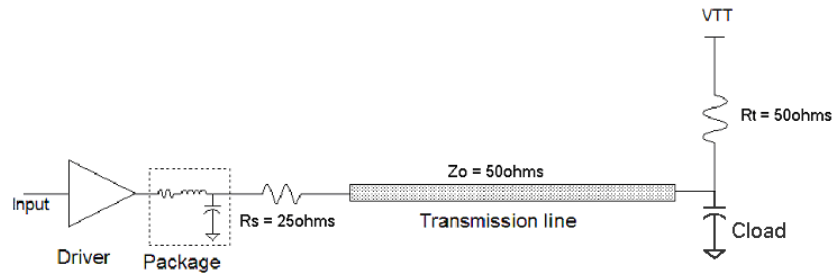


Figure 10. - SSTL Class I Termination

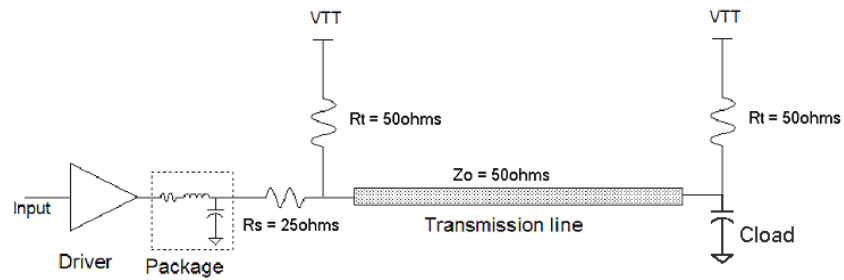


Figure 11. - SSTL Class II Termination

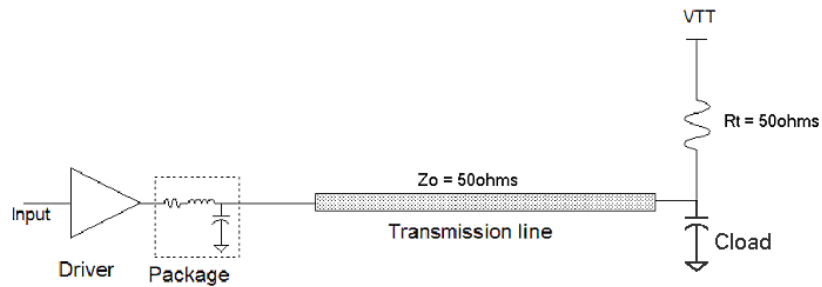


Figure 12. - HSTL Class I Termination

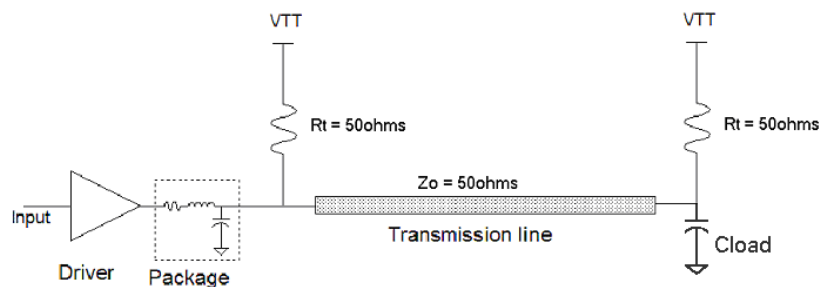


Figure 13. - HSTL Class II Termination

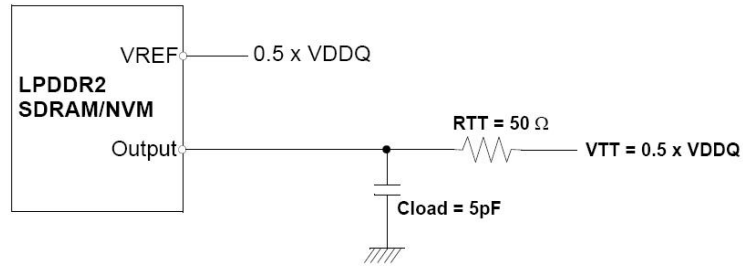


Figure 14. - HSULI Termination

Version	Date	Details of Release
0.1	January 2012	Preliminary Cyclone-V I/O Buffer Encrypted Hspice Early Access Uncorrelated Model release (version 0.1)
0.2	March 2012	RPCDN<8> and RPCDN<9> added into IO_HSTL.spi (version 0.2)
0.3	March 2012	IO_PCI.spi I/O standard is added (version 0.3)



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