Pin Information For The Stratix™ EP1S40 Device, ver 3.6

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
		VCCA_PLL7				L23	D31	J31			
		GND									
		GNDA_PLL7				M23	D32	K31			
		VCCG_PLL7				J23	D30	L30			
		GNDG_PLL7				K23	E30	L31			
B2	VREF0B2	FPLL7CLKp				E31	L29	J38			
B2	VREF0B2	FPLL7CLKn				D31	L28	J39			
B2	VREF0B2	IO						N30			
B2	VREF0B2	IO						N31			
B2	VREF0B2	IO	DIFFIO_RX44p				E29	G39			LOW
B2	VREF0B2	IO	DIFFIO_RX44n				F28	G38			LOW
B2	VREF0B2	IO	DIFFIO_TX44p		D25	K24	G25	M30			HIGH
B2	VREF0B2	IO	DIFFIO_TX44n		D26	J24	G26	M31			HIGH
B2	VREF0B2	IO	DIFFIO_RX43p				E32	H39			LOW
B2	VREF0B2	IO	DIFFIO_RX43n				E31	H38			LOW
B2	VREF0B2	IO	DIFFIO_TX43p		E25	K25	G28	J32			HIGH
B2	VREF0B2	IO	DIFFIO_TX43n		E26	J25	G27	J33			HIGH
B2	VREF0B2	IO	DIFFIO_RX42p		C27	F28	F29	K36			HIGH
B2	VREF0B2	IO	DIFFIO_RX42n		C28	G28	F30	K37			HIGH
B2	VREF0B2	IO	DIFFIO_TX42p		F24	H24	H28	K32			HIGH
B2	VREF0B2	IO	DIFFIO_TX42n		F23	G24	H27	K33			HIGH
B2	VREF0B2	VREF0B2			E24	L22	F27	M29			
B2	VREF0B2	IO	DIFFIO_RX41p			J28	F31	J36			HIGH
B2	VREF0B2	IO	DIFFIO_RX41n			H28	F32	J37			HIGH
B2	VREF0B2	IO	DIFFIO_TX41p		G23	H25	J27	L33			HIGH
B2	VREF0B2	IO	DIFFIO_TX41n		G24	G25	J28	L32			HIGH
B2	VREF0B2	IO	DIFFIO_RX40p			D29	G29	L37			HIGH
B2	VREF0B2	IO	DIFFIO_RX40n			E29	G30	L36			HIGH
B2	VREF0B2	IO	DIFFIO_TX40p		H24	K26	H25	M32			HIGH
B2	VREF0B2	IO	DIFFIO_TX40n		H23	L26	H26	M33			HIGH
B2	VREF0B2	IO	DIFFIO_RX39p			F29	H30	K38			HIGH

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B2	VREF0B2	IO	DIFFIO_RX39n			G29	H29	K39			HIGH
B2	VREF0B2	IO	DIFFIO_TX39p		H22	J26	J25	N32			HIGH
B2	VREF0B2	IO	DIFFIO_TX39n		H21	H26	J26	N33			HIGH
B2	VREF0B2	IO	DIFFIO_RX38p		D27	H29	G31	M36			HIGH
B2	VREF0B2	IO	DIFFIO_RX38n		D28	J29	G32	M37			HIGH
B2	VREF0B2	IO	DIFFIO_TX38p		J24	G26	K28	K34			HIGH
B2	VREF0B2	IO	DIFFIO_TX38n		J23	F26	K27	K35			HIGH
B2	VREF1B2	IO	DIFFIO_RX37p		E27	D30	H31	L38			HIGH
B2	VREF1B2	IO	DIFFIO_RX37n		E28	E30	H32	L39			HIGH
B2	VREF1B2	IO	DIFFIO_TX37p		K23	F27	K26	L35			HIGH
B2	VREF1B2	IO	DIFFIO_TX37n		K24	G27	K25	L34			HIGH
B2	VREF1B2	IO	DIFFIO_RX36p		F25	F30	J29	M38			HIGH
B2	VREF1B2	IO	DIFFIO_RX36n		F26	G30	J30	M39			HIGH
B2	VREF1B2	IO	DIFFIO_TX36p		J21	H27	L27	M34			HIGH
B2	VREF1B2	IO	DIFFIO_TX36n		J22	J27	L26	M35			HIGH
B2	VREF1B2	IO	DIFFIO_RX35p		F27	H30	K30	N36			HIGH
B2	VREF1B2	IO	DIFFIO_RX35n		F28	J30	K29	N37			HIGH
B2	VREF1B2	IO	DIFFIO_TX35p		K21	K27	M26	N34			HIGH
B2	VREF1B2	IO	DIFFIO_TX35n		K22	L27	M27	N35			HIGH
B2	VREF1B2	IO	DIFFIO_RX34p		G26	F31	J32	N38			HIGH
B2	VREF1B2	IO	DIFFIO_RX34n		G25	G31	J31	P38			HIGH
B2	VREF1B2	IO	DIFFIO_TX34p		L22	L24	M24	P32			HIGH
B2	VREF1B2	IO	DIFFIO_TX34n		L21	M24	M25	P33			HIGH
B2	VREF1B2	VREF1B2			K20	M22	L25	N29			
B2	VREF1B2	IO	DIFFIO_RX33p		G27	H31	K31	P39			HIGH
B2	VREF1B2	IO	DIFFIO_RX33n		G28	J31	L32	R38			HIGH
B2	VREF1B2	IO	DIFFIO_TX33p		L23	L25	N24	P34			HIGH
B2	VREF1B2	IO	DIFFIO_TX33n		L24	M25	N23	P35			HIGH
B2	VREF1B2	IO	DIFFIO_RX32p/RUP2		H26	K28	M28	P36			HIGH
B2	VREF1B2	IO	DIFFIO_RX32n/RDN2		H25	K29	M29	P37			HIGH

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B2	VREF1B2	IO	DIFFIO_TX32p		L20	P24	N27	R33			HIGH
B2	VREF1B2	IO	DIFFIO_TX32n		L19	N24	N28	R32			HIGH
B2	VREF1B2	IO	DIFFIO_RX31p		H27	M28	L30	R36			HIGH
B2	VREF1B2	IO	DIFFIO_RX31n		H28	L28	L31	R37			HIGH
B2	VREF1B2	IO	DIFFIO_TX31p		M22	N25	P23	R34			HIGH
B2	VREF1B2	IO	DIFFIO_TX31n		M21	P25	P24	R35			HIGH
B2	VREF1B2	IO	DIFFIO_RX30p		J25	M29	M31	T36			HIGH
B2	VREF1B2	IO	DIFFIO_RX30n		J26	L29	M30	T37			HIGH
B2	VREF1B2	IO	DIFFIO_TX30p		M24	M26	N25	T33			HIGH
B2	VREF1B2	IO	DIFFIO_TX30n		M23	N26	N26	T32			HIGH
B2	VREF2B2	IO	DIFFIO_RX29p		J27	P28	N29	T39			HIGH
B2	VREF2B2	IO	DIFFIO_RX29n		J28	N28	N30	T38			HIGH
B2	VREF2B2	IO	DIFFIO_TX29p		M20	M27	P28	T30			HIGH
B2	VREF2B2	IO	DIFFIO_TX29n		M19	N27	P27	T31			HIGH
B2	VREF2B2	IO	DIFFIO_RX28p		K26	N29	N31	U36			HIGH
B2	VREF2B2	IO	DIFFIO_RX28n		K25	P29	N32	U37			HIGH
B2	VREF2B2	IO	DIFFIO_TX28p		N26	P27	R28	T34			HIGH
B2	VREF2B2	IO	DIFFIO_TX28n		N25	R27	R27	T35			HIGH
B2	VREF2B2	IO	DIFFIO_RX27p		K27	L30	P29	U38			HIGH
B2	VREF2B2	IO	DIFFIO_RX27n		K28	K30	P30	U39			HIGH
B2	VREF2B2	IO	DIFFIO_TX27p		N24	R26	P25	U35			HIGH
B2	VREF2B2	IO	DIFFIO_TX27n		N23	P26	P26	U34			HIGH
B2	VREF2B2	IO	DIFFIO_RX26p		L25	N30	P31	V36			HIGH
B2	VREF2B2	IO	DIFFIO_RX26n		L26	M30	P32	V37			HIGH
B2	VREF2B2	IO	DIFFIO_TX26p		N22	N23	R23	U33			HIGH
B2	VREF2B2	IO	DIFFIO_TX26n		N21	P23	R24	U32			HIGH
B2	VREF2B2	VREF2B2			P19	N22	R21	P29			
B2	VREF2B2	IO	DIFFIO_RX25p		L27	L31	R32	V38			HIGH
B2	VREF2B2	IO	DIFFIO_RX25n		L28	K31	R31	V39			HIGH
B2	VREF2B2	IO	DIFFIO_TX25p		N20	T25	R25	V35			HIGH

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B2	VREF2B2	IO	DIFFIO_TX25n		N19	R25	R26	V34			HIGH
B2	VREF2B2	IO	DIFFIO_RX24p		M25	R30	R30	W39			HIGH
B2	VREF2B2	IO	DIFFIO_RX24n		M26	P30	R29	W38			HIGH
B2	VREF2B2	IO	DIFFIO_TX24p				M23	V32			LOW
B2	VREF2B2	IO	DIFFIO_TX24n				M22	V31			LOW
B2	VREF2B2	IO	DIFFIO_RX23p		M27	P31	T32	W37			HIGH
B2	VREF2B2	IO	DIFFIO_RX23n		N28	R31	T31	W36			HIGH
B2	VREF2B2	IO	DIFFIO_TX23p				N22	W31			LOW
B2	VREF2B2	IO	DIFFIO_TX23n				P22	W32			LOW
B2	VREF2B2	CLK0n			N27	R28	T30	Y39			
B2	VREF2B2	CLK0p			P27	R29	T29	Y38			
B2	VREF2B2	IO	CLK1n		P26	T30	T28	Y34			
B2	VREF2B2	CLK1p			P25	T31	T27	Y35			
		VCCA_PLL1			P23	R24	T25	AA32			
		GND									
		GNDA_PLL1			P24	T24	T26	Y31			
		VCCG_PLL1			P21	R22	R22	Y28			
		GNDG_PLL1			P22	R23	T22	Y29			
		VCCA_PLL2			R23	U24	U25	AA30			
		GND									
		GNDA_PLL2			R24	V24	U26	AA31			
		VCCG_PLL2			R21	U23	U24	AA28			
		GNDG_PLL2			R22	V23	T24	AA29			
B1	VREF0B1	CLK2p			R27	T29	U31	Y37			
B1	VREF0B1	CLK2n			T27	T28	U32	Y36			
B1	VREF0B1	CLK3p			R25	U29	U29	AA35			
B1	VREF0B1	IO	CLK3n		R26	U28	U30	AA34			
B1	VREF0B1	IO	DIFFIO_RX22p		T28	U31	U28	AA39			HIGH
B1	VREF0B1	IO	DIFFIO_RX22n		U27	V31	U27	AA38			HIGH
B1	VREF0B1	IO	DIFFIO_TX22p				U22	Y33			LOW

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B1	VREF0B1	IO	DIFFIO_TX22n				V22	AA33			LOW
B1	VREF0B1	IO	DIFFIO_RX21p		U26	AB31	V32	AA37			HIGH
B1	VREF0B1	IO	DIFFIO_RX21n		U25	AA31	V31	AA36			HIGH
B1	VREF0B1	IO	DIFFIO_TX21p				W21	AB33			LOW
B1	VREF0B1	IO	DIFFIO_TX21n				W22	AB32			LOW
B1	VREF0B1	IO	DIFFIO_RX20p		V27	V30	V30	AB38			HIGH
B1	VREF0B1	IO	DIFFIO_RX20n		V28	U30	V29	AB39			HIGH
B1	VREF0B1	IO	DIFFIO_TX20p				Y21	AB31			LOW
B1	VREF0B1	IO	DIFFIO_TX20n				Y22	AB30			LOW
B1	VREF0B1	VREF0B1			R19	V22	V21	AE29			
B1	VREF0B1	IO	DIFFIO_RX19p		V26	W30	W32	AB37			HIGH
B1	VREF0B1	IO	DIFFIO_RX19n		V25	Y30	W31	AB36			HIGH
B1	VREF0B1	IO	DIFFIO_TX19p		T21	V25	V26	AB34			HIGH
B1	VREF0B1	IO	DIFFIO_TX19n		T22	U25	V25	AB35			HIGH
B1	VREF0B1	IO	DIFFIO_RX18p		W28	AA30	W30	AC39			HIGH
B1	VREF0B1	IO	DIFFIO_RX18n		W27	AB30	W29	AC38			HIGH
B1	VREF0B1	IO	DIFFIO_TX18p		T19	U26	V28	AC32			HIGH
B1	VREF0B1	IO	DIFFIO_TX18n		T20	T26	V27	AC33			HIGH
B1	VREF0B1	IO	DIFFIO_RX17p		W26	V29	Y32	AC37			HIGH
B1	VREF0B1	IO	DIFFIO_RX17n		W25	W29	Y31	AC36			HIGH
B1	VREF0B1	IO	DIFFIO_TX17p		T23	T27	W25	AC34			HIGH
B1	VREF0B1	IO	DIFFIO_TX17n		T24	U27	W26	AC35			HIGH
B1	VREF0B1	IO	DIFFIO_RX16p		Y28	Y29	Y30	AD39			HIGH
B1	VREF0B1	IO	DIFFIO_RX16n		Y27	AA29	Y29	AD38			HIGH
B1	VREF0B1	IO	DIFFIO_TX16p		T26	V26	W27	AD34			HIGH
B1	VREF0B1	IO	DIFFIO_TX16n		T25	W26	W28	AD35			HIGH
B1	VREF1B1	IO	DIFFIO_RX15p		Y26	V28	AA31	AD37			HIGH
B1	VREF1B1	IO	DIFFIO_RX15n		Y25	W28	AA30	AD36			HIGH
B1	VREF1B1	IO	DIFFIO_TX15p		U19	W24	V24	AD33			HIGH
B1	VREF1B1	IO	DIFFIO_TX15n		U20	Y24	V23	AD32			HIGH

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B1	VREF1B1	IO	DIFFIO_RX14p		AA28	Y28	AB31	AE37			HIGH
B1	VREF1B1	IO	DIFFIO_RX14n		AA27	AA28	AB30	AE36			HIGH
B1	VREF1B1	IO	DIFFIO_TX14p		U24	W25	Y26	AD31			HIGH
B1	VREF1B1	IO	DIFFIO_TX14n		U23	Y25	Y25	AD30			HIGH
B1	VREF1B1	IO	DIFFIO_RX13p/RUP1		AA25	AB29	AA28	AF37			HIGH
B1	VREF1B1	IO	DIFFIO_RX13n/RDN1		AA26	AB28	AA29	AF36			HIGH
B1	VREF1B1	IO	DIFFIO_TX13p		U21	Y26	Y28	AE35			HIGH
B1	VREF1B1	IO	DIFFIO_TX13n		U22	AA26	Y27	AE34			HIGH
B1	VREF1B1	IO	DIFFIO_RX12p		AB28	AC31	AB32	AE38			HIGH
B1	VREF1B1	IO	DIFFIO_RX12n		AB27	AD31	AC31	AF39			HIGH
B1	VREF1B1	IO	DIFFIO_TX12p		V19	W23	W23	AE33			HIGH
B1	VREF1B1	IO	DIFFIO_TX12n		V20	Y23	W24	AE32			HIGH
B1	VREF1B1	VREF1B1			W20	W22	AA23	AF29			
B1	VREF1B1	IO	DIFFIO_RX11p		AB26	AE31	AD32	AF38			HIGH
B1	VREF1B1	IO	DIFFIO_RX11n		AB25	AF31	AD31	AG38			HIGH
B1	VREF1B1	IO	DIFFIO_TX11p		V24	V27	Y23	AF35			HIGH
B1	VREF1B1	IO	DIFFIO_TX11n		V23	W27	Y24	AF34			HIGH
B1	VREF1B1	IO	DIFFIO_RX10p		AC28	AC30	AC29	AG37			HIGH
B1	VREF1B1	IO	DIFFIO_RX10n		AC27	AD30	AC30	AG36			HIGH
B1	VREF1B1	IO	DIFFIO_TX10p		V22	Y27	AA25	AF33			HIGH
B1	VREF1B1	IO	DIFFIO_TX10n		V21	AA27	AA24	AF32			HIGH
B1	VREF1B1	IO	DIFFIO_RX9p		AD28	AF30	AD30	AH39			HIGH
B1	VREF1B1	IO	DIFFIO_RX9n		AD27	AE30	AD29	AH38			HIGH
B1	VREF1B1	IO	DIFFIO_TX9p		W23	AB27	AA27	AG35			HIGH
B1	VREF1B1	IO	DIFFIO_TX9n		W24	AC27	AA26	AG34			HIGH
B1	VREF1B1	IO	DIFFIO_RX8p		AE28	AG30	AE32	AH37			HIGH
B1	VREF1B1	IO	DIFFIO_RX8n		AE27	AH30	AE31	AH36			HIGH
B1	VREF1B1	IO	DIFFIO_TX8p		W21	AE27	AB27	AG33			HIGH
B1	VREF1B1	IO	DIFFIO_TX8n		W22	AD27	AB26	AG32			HIGH
B1	VREF1B1	IO	DIFFIO_RX7p			AC29	AE30	AJ39			HIGH

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B1	VREF1B1	IO	DIFFIO_RX7n			AD29	AE29	AJ38			HIGH
B1	VREF2B1	IO	DIFFIO_TX7p		Y21	AG27	AC25	AH34			HIGH
B1	VREF2B1	IO	DIFFIO_TX7n		Y22	AF27	AC26	AH35			HIGH
B1	VREF2B1	IO	DIFFIO_RX6p			AE29	AF32	AJ37			HIGH
B1	VREF2B1	IO	DIFFIO_RX6n			AF29	AF31	AJ36			HIGH
B1	VREF2B1	IO	DIFFIO_TX6p		Y24	AB26	AC27	AK35			HIGH
B1	VREF2B1	IO	DIFFIO_TX6n		Y23	AC26	AC28	AK34			HIGH
B1	VREF2B1	IO	DIFFIO_RX5p			AH29	AF30	AK38			HIGH
B1	VREF2B1	IO	DIFFIO_RX5n			AG29	AF29	AK39			HIGH
B1	VREF2B1	IO	DIFFIO_TX5p		AA23	AD26	AD28	AH33			HIGH
B1	VREF2B1	IO	DIFFIO_TX5n		AA24	AE26	AD27	AH32			HIGH
B1	VREF2B1	IO	DIFFIO_RX4p			AC28	AG31	AK37			HIGH
B1	VREF2B1	IO	DIFFIO_RX4n			AD28	AG32	AK36			HIGH
B1	VREF2B1	IO	DIFFIO_TX4p			AA25	AD26	AJ35			HIGH
B1	VREF2B1	IO	DIFFIO_TX4n		U18	AB25	AD25	AJ34			HIGH
B1	VREF2B1	VREF2B1			AE26	Y22	AB25	AG29			
B1	VREF2B1	IO	DIFFIO_RX3p		AF28	AE28	AG30	AL37			HIGH
B1	VREF2B1	IO	DIFFIO_RX3n		AF27	AF28	AG29	AL36			HIGH
B1	VREF2B1	IO	DIFFIO_TX3p		AB23	AD25	AE28	AJ33			HIGH
B1	VREF2B1	IO	DIFFIO_TX3n		AB24	AC25	AE27	AJ32			HIGH
B1	VREF2B1	IO	DIFFIO_RX2p				AG25	AM39			LOW
B1	VREF2B1	IO	DIFFIO_RX2n				AG26	AM38			LOW
B1	VREF2B1	IO	DIFFIO_TX2p		AA21	AA24	AE25	AK32			HIGH
B1	VREF2B1	IO	DIFFIO_TX2n		AA22	AB24	AE26	AK33			HIGH
B1	VREF2B1	IO	DIFFIO_RX1p				AH32	AN39			LOW
B1	VREF2B1	IO	DIFFIO_RX1n				AH31	AN38			LOW
B1	VREF2B1	IO	DIFFIO_TX1p		AC25	AD24	AF27	AL33			HIGH
B1	VREF2B1	IO	DIFFIO_TX1n		AC26	AC24	AF28	AL32			HIGH
B1	VREF2B1	IO	DIFFIO_RX0p				AH29	AP38			LOW
B1	VREF2B1	IO	DIFFIO_RX0n				AG28	AP39			LOW

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B1	VREF2B1	IO	DIFFIO_TX0p		AD25	AE25	AF26	AH31			HIGH
B1	VREF2B1	IO	DIFFIO_TX0n		AD26	AF25	AF25	AH30			HIGH
B1	VREF2B1	FPLL8CLKn				AG31	AB29	AL38			
B1	VREF2B1	FPLL8CLKp				AH31	AB28	AL39			
B1	VREF2B1	IO					AA22	AG30			
B1	VREF2B1	IO					AB23	AG31			
		VCCA_PLL8				AB23	AJ31	AJ30			
		GND									
		GNDA_PLL8				AA23	AJ32	AJ31			
		VCCG_PLL8				AD23	AJ30	AL31			
		GNDG_PLL8				AC23	AH30	AK31			
B8	VREF0B8	IO			AC24	AG28	AD24	AR35			
B8	VREF0B8	IO	DQ9B7		AG26	AK29	AH28	AV34	DQ3B15	DQ1B31	
B8	VREF0B8	IO			AC23	AJ30	AE24	AU36			
B8	VREF0B8	IO	DQ9B6		AH26	AJ29	AK30	AU34	DQ3B14	DQ1B30	
B8	VREF0B8	IO					AF24	AP33			
B8	VREF0B8	IO	DQ9B5		AG25	AJ28	AJ28	AU33	DQ3B13	DQ1B29	
B8	VREF0B8	IO						AN33			
B8	VREF0B8	IO	DQ9B4		AH25	AL28	AJ29	AW33	DQ3B12	DQ1B28	
B8	VREF0B8	IO			AB22	AH28	AC24	AR34			
B8	VREF0B8	IO	DQ9B3		AF25	AH27	AK29	AW34	DQ3B11	DQ1B27	
B8	VREF0B8	IO					AG24	AU35			
B8	VREF0B8	IO	DQS9B		AF24	AK28	AK28	AV33			
B8	VREF0B8	VREF0B8			AD22	AB22	AH27	AJ29			
B8	VREF0B8	IO				AF26	AB24	AT35			
B8	VREF0B8	IO	DQ9B2		AG24	AL27	AL30	AV32	DQ3B10	DQ1B26	
B8	VREF0B8	IO			AE25	AE24	AC23	AV36			
B8	VREF0B8	IO	DQ9B1		AE24	AJ27	AL29	AU32	DQ3B9	DQ1B25	
B8	VREF0B8	IO					AG23	AR33			
B8	VREF0B8	IO	DQ9B0		AH24	AK27	AM29	AW32	DQ3B8	DQ1B24	

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B8	VREF0B8	IO			AD24			AN32			
B8	VREF0B8	IO				AC22	AD23	AT34			
B8	VREF0B8	IO	DQ8B7		AG23	AH26	AH26	AU31	DQ3B7	DQ1B23	
B8	VREF0B8	IO					AB22	AN31			
B8	VREF0B8	IO	DQ8B6		AD23	AG26	AJ27	AV31	DQ3B6	DQ1B22	
B8	VREF0B8	IO				AD22	AF23	AV35			
B8	VREF0B8	IO	DQ8B5		AF23	AK26	AL28	AW31	DQ3B5	DQ1B21	
B8	VREF0B8	IO			AB21		AC22	AP32			
B8	VREF0B8	IO	DQ8B4		AH23	AL26	AK27	AW30	DQ3B4	DQ1B20	
B8	VREF0B8	IO						AW36			
B8	VREF0B8	IO	DQ8B3		AE22	AH25	AJ26	AU30	DQ3B3	DQ1B19	
B8	VREF0B8	IO				AC21	AE23	AT33			
B8	VREF1B8	IO	DQS8B		AE23	AJ26	AL27	AV30	DQS3B		
B8	VREF1B8	IO	DQ8B0		AG22	AL25	AK26	AW29	DQ3B0	DQ1B16	
B8	VREF1B8	IO	DQ8B2		AF22	AK25	AM27	AU29	DQ3B2	DQ1B18	
B8	VREF1B8	IO			AB20	AE22	AE22	AT32			
B8	VREF1B8	IO	DQ8B1		AH22	AJ25	AM28	AV29	DQ3B1	DQ1B17	
B8	VREF1B8	IO					AF22	AT31			
B8	VREF1B8	IO				AA21	AD22	AR32			
B8	VREF1B8	IO						AN30			
B8	VREF1B8	IO			Y20	AD21	AA21	AW35			
B8	VREF1B8	IO	DQ7B7		AD21	AG24	AH24	AR28	DQ2B15	DQ1B15	
B8	VREF1B8	IO					AG22	AN29			
B8	VREF1B8	IO	DQ7B6		AE21	AH23	AJ24	AT28	DQ2B14	DQ1B14	
B8	VREF1B8	VREF1B8			AD20	AB21	AH25	AJ28			
B8	VREF1B8	IO						AP31			
B8	VREF1B8	IO	DQ7B5		AG21	AK24	AJ25	AU28	DQ2B13	DQ1B13	
B8	VREF1B8	IO			AC22	AC20	AB21	AP30			
B8	VREF1B8	IO	DQ7B4		AF21	AH24	AK25	AV28	DQ2B12	DQ1B12	
B8	VREF1B8	IO					AG21	AT30			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B8	VREF1B8	IO	DQ7B3		AE20	AJ23	AL25	AR27	DQ2B11	DQ1B11	
B8	VREF1B8	IO				AA19	AC21	AR31			
B8	VREF1B8	IO	DQS7B		AG20	AJ24	AL26	AT27		DQS1B	
B8	VREF1B8	IO						AP29			
B8	VREF1B8	IO	DQ7B2		AF20	AL24	AK24	AW28	DQ2B10	DQ1B10	
B8	VREF1B8	IO					AD21	AR29			
B8	VREF1B8	IO	DQ7B1		AH21	AK23	AM25	AU27	DQ2B9	DQ1B9	
B8	VREF1B8	IO						AR30			
B8	VREF1B8	IO	DQ7B0		AH20	AL23	AM26	AV27	DQ2B8	DQ1B8	
B8	VREF1B8	IO						AN28			
B8	VREF1B8	IO			AC20	AD20	AG20	AM27			
B8	VREF1B8	IO	FCLK3		AC21	AF23	AE21	AT29			
B8	VREF1B8	IO	FCLK2		AC19	AF22	AF21	AN26			
B8	VREF2B8	IO	DQ6B7		AE19	AG22	AJ23	AR26	DQ2B7	DQ1B7	
B8	VREF2B8	IO	DQ6B6		AD19	AH22	AL24	AT26	DQ2B6	DQ1B6	
B8	VREF2B8	IO	DQ6B5		AF19	AK22	AH22	AU26	DQ2B5	DQ1B5	
B8	VREF2B8	IO				AE20	AB20	AP28			
B8	VREF2B8	IO	DQ6B4		AG19	AG21	AM24	AV26	DQ2B4	DQ1B4	
B8	VREF2B8	IO		PGM2	AB19	AF24	AA20	AL25			
B8	VREF2B8	IO	DQ6B3		AH19	AH21	AK23	AW26	DQ2B3	DQ1B3	
B8	VREF2B8	IO					AD20	AN27			
B8	VREF2B8	IO	DQS6B		AF18	AJ22	AJ22	AU25	DQS2B		
B8	VREF2B8	IO					AE20	AM26			
B8	VREF2B8	IO	DQ6B2		AD18	AL22	AL23	AT25	DQ2B2	DQ1B2	
B8	VREF2B8	IO		CRC_ERROR	AA20	AE21	AF20	AN25			
B8	VREF2B8	VREF2B8			AH18	AB20	AH23	AJ27			
B8	VREF2B8	IO	RDN8		Y19	AE23	AC20	AH24			
B8	VREF2B8	IO	RUP8		W19	AG25	AH19	AF23			
B8	VREF2B8	IO	DQ6B0		AG18	AK21	AL22	AV25	DQ2B0	DQ1B0	
B8	VREF2B8	IO						AP27			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B8	VREF2B8	IO	DQ6B1		AE18	AJ21	AK22	AR25	DQ2B1	DQ1B1	
B8	VREF2B8	IO	DQ5B7		AF17	AG20	AM22	AT24			
B8	VREF2B8	IO						AP26			
B8	VREF2B8	IO	DQ5B6		AG17	AH20	AJ21	AU24			
B8	VREF2B8	IO					AB19	AM25			
B8	VREF2B8	IO	DQ5B5		AE17	AK20	AK21	AV24			
B8	VREF2B8	IO				AC19	AK18	AP25			
B8	VREF2B8	IO	DQ5B4		AD17	AL20	AL21	AW24			
B8	VREF2B8	IO		RDYnBSY	AA19	AG23	AA19	AH23			
B8	VREF2B8	IO	DQ5B3		AG16	AG19	AH20	AW23			
B8	VREF2B8	IO			AB18	AD19	AD19	AM24			
B8	VREF2B8	IO	DQS5B		AH16	AJ20	AJ20	AU23			
B8	VREF2B8	IO				AE19	AJ18	AN24			
B8	VREF2B8	IO	DQ5B2		AD16	AH19	AK20	AR23			
B8	VREF3B8	IO		nCS	Y18	AF20	AC19	AL23			
B8	VREF3B8	IO	DQ5B1		AF16	AJ19	AL20	AV23			
B8	VREF3B8	IO						AP24			
B8	VREF3B8	IO	DQ5B0		AE16	AK19	AM20	AT23			
B8	VREF3B8	IO			W18	AE18	AH18	AR24			
B8	VREF3B8	IO			V18			AM23			
B8	VREF3B8	IO						AN23			
B8	VREF3B8	IO						AN22			
B8	VREF3B8	IO						AP23			
B8	VREF3B8	IO		CS	AA18	AF21	AG19	AJ23			
B8	VREF3B8	IO						AR22			
B8	VREF3B8	IO						AP22			
B8	VREF3B8	VREF3B8				AB19	AH21	AJ26			
B8	VREF3B8	IO	CLK5n		Y17	AH18	AJ19	AU22			
B8	VREF3B8	CLK5p			AA17	AJ18	AK19	AT22			
B8	VREF3B8	IO	CLK4n		AB17	AK18	AL19	AW22			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B8	VREF3B8	CLK4p			AC17	AL18	AM19	AV22			
B8	VREF3B8	PLL_ENA		PLL_ENA	AC18	AF19	AF19	AM22			
B8	VREF3B8	MSEL0		MSEL0	AC16	AF18	AG18	AP21			
B8	VREF3B8	MSEL1		MSEL1	W17	AG18	AE18	AG21			
B8	VREF3B8	MSEL2		MSEL2	AB15	AG17	AE19	AM21			
B12	VREF3B8	IO	PLL6_OUT3n		Y16	AL17	AM18	AV20			
B12	VREF3B8	IO	PLL6_OUT3p		W16	AK17	AL18	AW20			
B12	VREF3B8	IO	PLL6_OUT2n		AG15	AJ17	AK17	AW21			
B12	VREF3B8	IO	PLL6_OUT2p		AF15	AH17	AJ17	AV21			
B11	VREF3B8	IO	PLL6_FBn		AA15	AJ15	AM17	AU20			
B11	VREF3B8	IO	PLL6_FBp		AA14	AH15	AL17	AT20			
B11	VREF3B8	IO	PLL6_OUT1n		W15	AL15	AK16	AU21			
B11	VREF3B8	IO	PLL6_OUT1p		W14	AK15	AJ16	AT21			
B11	VREF3B8	IO	PLL6_OUT0n		AE15	AL16	AM16	AU19			
B11	VREF3B8	IO	PLL6_OUT0p		AD15	AK16	AL16	AT19			
B12		VCC_PLL6_OUTB			AB16	AC18	AB17	AH21			
B11		VCC_PLL6_OUTA			AC14	AD17	AE17	AJ21			
		VCCA_PLL6			AG14	AB17	AG17	AK21			
		GND									
		GNDA_PLL6			AF14	AC17	AH17	AL20			
		VCCG_PLL6			AA13	AD15	AD16	AJ20			
		GNDG_PLL6			AB14	AD16	AB16	AH20			
		VCCA_PLL12				AC14	AG16	AK19			
		GND									
		GNDA_PLL12				AD14	AH16	AL19			
		VCCG_PLL12				AC15	AF16	AJ19			
		GNDG_PLL12				AB15	AE16	AH19			
B7	VREF0B7	CLK7p			W13	AJ14	AM15	AW18			
B7	VREF0B7	IO	CLK7n		Y13	AH14	AL15	AV18			
B7	VREF0B7	CLK6p			AD14	AL14	AK15	AW19			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B7	VREF0B7	IO	CLK6n/PLL12_OUT		AE14	AK14	AJ15	AV19			
B7	VREF0B7	nCE		nCE	AB13	AF17	AF18	AN20			
B7	VREF0B7	nCEO		nCEO	AC13	AF16	AH15	AP20			
B7	VREF0B7	IO						AP19			
B7	VREF0B7	IO						AR19			
B7	VREF0B7	IO		PGM0	W12	AE17	AD18	AG20			
B7	VREF0B7	nIO_PULLUP		nIO_PULLUP	Y12	AE16	AF15	AR20			
B7	VREF0B7	VCCSEL		VCCSEL	AA12	AE15	AJ14	AM19			
B7	VREF0B7	PORSEL		PORSEL	AC12	AG16	AG15	AN19			
B7	VREF0B7	VREF0B7			AD11	AB14	AH12	AJ15			
B7	VREF0B7	IO		INIT_DONE	W11	AF15	AE15	AL18			
B7	VREF0B7	IO					AC18	AN18			
B7	VREF0B7	IO	DQ4B7		AD13	AK13	AL13	AU17			
B7	VREF0B7	IO			V11	AA16	AD15	AP18			
B7	VREF0B7	IO	DQ4B6		AE13	AG13	AM13	AR17			
B7	VREF0B7	IO		nRS	AC11	AE14	AB18	AL17			
B7	VREF0B7	IO	DQ4B5		AF13	AH13	AH13	AT17			
B7	VREF0B7	IO			Y11	AA15	AC15	AR18			
B7	VREF0B7	IO	DQ4B4		AD12	AJ13	AJ13	AV17			
B7	VREF0B7	IO				AH16	AD14	AT18			
B7	VREF0B7	IO	DQ4B3		AG13	AK12	AK13	AV16			
B7	VREF0B7	IO		RUnLU	W10	AJ16	AF14	AK17			
B7	VREF1B7	IO	DQS4B		AH13	AJ12	AJ12	AU16			
B7	VREF1B7	IO					AA18	AP16			
B7	VREF1B7	IO	DQ4B2		AE12	AL12	AK12	AW17			
B7	VREF1B7	IO			AB12	AE13	AE14	AU18			
B7	VREF1B7	IO	DQ4B1		AF12	AG12	AL12	AT16			
B7	VREF1B7	IO		PGM1	AA11	AG15	AG14	AF16			
B7	VREF1B7	IO	DQ4B0		AG12	AH12	AM11	AW16			
B7	VREF1B7	IO	DQ3B6		AH11	AJ11	AK11	AR15	DQ1B14	DQ0B30	

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B7	VREF1B7	IO					AK14	AR16			
B7	VREF1B7	IO	DQ3B7		AG11	AL10	AL10	AT15	DQ1B15	DQ0B31	
B7	VREF1B7	IO	RDN7		AC10	AG14	AC14	AP17			
B7	VREF1B7	IO	RUP7		AB11	AF13	AF13	AN16			
B7	VREF1B7	IO				AC13	AB15	AP13			
B7	VREF1B7	IO	DQ3B5		AE11	AK11	AL11	AV15	DQ1B13	DQ0B29	
B7	VREF1B7	IO	DEV_CLRn		AC9	AF14	AH14	AN17			
B7	VREF1B7	IO	DQ3B4		AF11	AG11	AK10	AV14	DQ1B12	DQ0B28	
B7	VREF1B7	IO				AD13	AL14	AP15			
B7	VREF1B7	IO	DQ3B3		AE10	AH11	AM9	AW14	DQ1B11	DQ0B27	
B7	VREF1B7	VREF1B7				AB13	AH10	AJ14			
B7	VREF1B7	IO			Y10	AA13	AA15	AR11			
B7	VREF1B7	IO	DQS3B		AG10	AJ10	AJ11	AU15	DQS1B		
B7	VREF1B7	IO			AA10	AE12	AD13	AN13			
B7	VREF1B7	IO	DQ3B2		AH10	AG10	AL9	AR14	DQ1B10	DQ0B26	
B7	VREF1B7	IO					AG13	AP14			
B7	VREF1B7	IO	DQ3B1		AF10	AH10	AJ10	AT14	DQ1B9	DQ0B25	
B7	VREF1B7	IO					AA14	AN12			
B7	VREF1B7	IO	DQ3B0		AD10	AK10	AH11	AU14	DQ1B8	DQ0B24	
B7	VREF1B7	IO			Y9	AD12	AB14	AP12			
B7	VREF1B7	IO						AT10			
B7	VREF1B7	IO	FCLK5		AC8	AF12	AM14	AN14			
B7	VREF1B7	IO	FCLK4		AB10	AF11	AF12	AT11			
B7	VREF2B7	IO	DQ2B7		AG9	AL8	AL8	AT13	DQ1B7	DQ0B23	
B7	VREF2B7	IO	DQ2B6		AF9	AK9	AJ9	AU13	DQ1B6	DQ0B22	
B7	VREF2B7	IO	DQ2B5		AE9	AL9	AK9	AV13	DQ1B5	DQ0B21	
B7	VREF2B7	IO				AC12	AC13	AN11			
B7	VREF2B7	IO	DQ2B4		AH8	AH8	AM8	AV12	DQ1B4	DQ0B20	
B7	VREF2B7	IO				AE11	AE13	AP11			
B7	VREF2B7	IO	DQ2B3		AH9	AK8	AH9	AR13	DQ1B3	DQ0B19	

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B7	VREF2B7	IO				AA11	AB13	AW5			
B7	VREF2B7	IO	DQS2B		AE8	AJ8	AK8	AU12		DQS0B	
B7	VREF2B7	IO				AG9	AD12	AP10			
B7	VREF2B7	IO	DQ2B2		AD8	AG8	AM7	AR12	DQ1B2	DQ0B18	
B7	VREF2B7	IO			AA9	AD11	AE12	AT9			
B7	VREF2B7	IO	DQ2B1		AF8	AH9	AJ8	AT12	DQ1B1	DQ0B17	
B7	VREF2B7	IO					AC12	AP9			
B7	VREF2B7	IO	DQ2B0		AG8	AJ9	AL7	AW12	DQ1B0	DQ0B16	
B7	VREF2B7	IO						AT8			
B7	VREF2B7	IO			AB9	AF10	AG12	AR10			
B7	VREF2B7	IO				AE10	AG11	AR9			
B7	VREF2B7	VREF2B7			AD9	AB12	AH8	AJ13			
B7	VREF2B7	IO					AA13	AT7			
B7	VREF2B7	IO	DQ1B6		AG7	AL7	AM6	AW11	DQ0B14	DQ0B14	
B7	VREF2B7	IO			AB8	AC11	AD11	AN10			
B7	VREF2B7	IO	DQ1B5		AH7	AH6	AJ7	AU10	DQ0B13	DQ0B13	
B7	VREF2B7	IO	DQ1B7		AF6	AK7	AL6	AV11	DQ0B15	DQ0B15	
B7	VREF2B7	IO	DQ1B4		AF7	AK6	AM5	AW10	DQ0B12	DQ0B12	
B7	VREF2B7	IO				AD10	AB12	AR7			
B7	VREF2B7	IO	DQ1B3		AD6	AL6	AK7	AU11	DQ0B11	DQ0B11	
B7	VREF2B7	IO					AE11	AW4			
B7	VREF2B7	IO	DQS1B		AE7	AJ6	AH7	AV10	DQS0B		
B7	VREF2B7	IO			AD5	AF9	AF11	AR8			
B7	VREF2B7	IO	DQ1B2		AH6	AH7	AL5	AW9	DQ0B10	DQ0B10	
B7	VREF3B7	IO				AC10	AC11	AU5			
B7	VREF3B7	IO	DQ1B1		AG6	AJ7	AK6	AV9	DQ0B9	DQ0B9	
B7	VREF3B7	IO					AF10	AP8			
B7	VREF3B7	IO	DQ1B0		AE6	AG6	AJ6	AU9	DQ0B8	DQ0B8	
B7	VREF3B7	IO			AC7			AV5			
B7	VREF3B7	IO				AE9	AG10	AN9			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B7	VREF3B7	IO	DQ0B7		AF5	AL4	AL3	AV8	DQ0B7	DQ0B7	
B7	VREF3B7	IO			AE4		AA12	AT5			
B7	VREF3B7	IO	DQ0B6		AH5	AL5	AL4	AW8	DQ0B6	DQ0B6	
B7	VREF3B7	IO			AB7	AE8	AD10	AN8			
B7	VREF3B7	IO	DQ0B5		AF4	AJ4	AM4	AW6	DQ0B5	DQ0B5	
B7	VREF3B7	IO				AF8	AE10	AT6			
B7	VREF3B7	VREF3B7			AD7	AB11	AH6	AJ12			
B7	VREF3B7	IO	DQ0B4		AG4	AK3	AJ4	AU8	DQ0B4	DQ0B4	
B7	VREF3B7	IO				AG4	AB11	AN7			
B7	VREF3B7	IO	DQ0B3		AG5	AK5	AJ5	AW7	DQ0B3	DQ0B3	
B7	VREF3B7	IO				AF6	AE9	AR6			
B7	VREF3B7	IO	DQS0B		AH3	AK4	AK5	AV7			
B7	VREF3B7	IO			AC6	AG7	AG9	AV4			
B7	VREF3B7	IO	DQ0B2		AG3	AH5	AH5	AU7	DQ0B2	DQ0B2	
B7	VREF3B7	IO					AC9	AR5			
B7	VREF3B7	IO	DQ0B1		AE5	AJ5	AK3	AV6	DQ0B1	DQ0B1	
B7	VREF3B7	IO			AC5	AJ2	AD9	AU4			
B7	VREF3B7	IO	DQ0B0		AH4	AJ3	AK4	AU6	DQ0B0	DQ0B0	
B7	VREF3B7	IO				AH4	AF9	AP7			
		GNDG_PLL9				AC9	AH3	AK9			
		VCCG_PLL9				AD9	AJ3	AL9			
		GNDA_PLL9				AA9	AJ1	AJ9			
		GND									
		VCCA_PLL9				AB9	AJ2	AJ10			
B6	VREF0B6	IO					AB9	AG10			
B6	VREF0B6	IO					AC10	AG9			
B6	VREF0B6	FPLL9CLKp				AH1	AB5	AL1			
B6	VREF0B6	FPLL9CLKn				AG1	AB4	AL2			
B6	VREF0B6	IO	DIFFIO_TX89n		AC3	AC8	AF8	AH10			HIGH
B6	VREF0B6	IO	DIFFIO_TX89p		AC4	AD8	AF7	AH9			HIGH

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B6	VREF0B6	IO	DIFFIO_RX89n				AG5	AP1			LOW
B6	VREF0B6	IO	DIFFIO_RX89p				AH4	AP2			LOW
B6	VREF0B6	IO	DIFFIO_TX88n		AD3	AF7	AF5	AL8			HIGH
B6	VREF0B6	IO	DIFFIO_TX88p		AD4	AE7	AF6	AL7			HIGH
B6	VREF0B6	IO	DIFFIO_RX88n				AH2	AN2			LOW
B6	VREF0B6	IO	DIFFIO_RX88p				AH1	AN1			LOW
B6	VREF0B6	IO	DIFFIO_TX87n		AA7	AB8	AE7	AK7			HIGH
B6	VREF0B6	IO	DIFFIO_TX87p		AA8	AA8	AE8	AK8			HIGH
B6	VREF0B6	IO	DIFFIO_RX87n				AG7	AM2			LOW
B6	VREF0B6	IO	DIFFIO_RX87p				AG8	AM1			LOW
B6	VREF0B6	IO	DIFFIO_TX86n		AB5	AC7	AD6	AJ7			HIGH
B6	VREF0B6	IO	DIFFIO_TX86p		AB6	AD7	AD5	AJ8			HIGH
B6	VREF0B6	IO	DIFFIO_RX86n		AF2	AF4	AG4	AL4			HIGH
B6	VREF0B6	IO	DIFFIO_RX86p		AF1	AE4	AG3	AL3			HIGH
B6	VREF0B6	VREF0B6			AE3	AA10	AG6	AH11			
B6	VREF0B6	IO	DIFFIO_TX85n		U12	AB7	AE6	AH8			HIGH
B6	VREF0B6	IO	DIFFIO_TX85p			AA7	AE5	AH7			HIGH
B6	VREF0B6	IO	DIFFIO_RX85n			AD4	AG1	AK4			HIGH
B6	VREF0B6	IO	DIFFIO_RX85p			AC4	AG2	AK3			HIGH
B6	VREF0B6	IO	DIFFIO_TX84n		AA5	AE6	AD8	AG8			HIGH
B6	VREF0B6	IO	DIFFIO_TX84p		AA6	AD6	AD7	AG7			HIGH
B6	VREF0B6	IO	DIFFIO_RX84n			AG3	AF4	AK1			HIGH
B6	VREF0B6	IO	DIFFIO_RX84p			AH3	AF3	AK2			HIGH
B6	VREF0B6	IO	DIFFIO_TX83n		Y6	AC6	AC5	AK6			HIGH
B6	VREF0B6	IO	DIFFIO_TX83p		Y5	AB6	AC6	AK5			HIGH
B6	VREF0B6	IO	DIFFIO_RX83n			AF3	AF2	AJ4			HIGH
B6	VREF0B6	IO	DIFFIO_RX83p			AE3	AF1	AJ3			HIGH
B6	VREF0B6	IO	DIFFIO_TX82n		Y7	AF5	AC7	AJ5			HIGH
B6	VREF0B6	IO	DIFFIO_TX82p		Y8	AG5	AC8	AJ6			HIGH
B6	VREF1B6	IO	DIFFIO_RX82n			AD3	AE4	AJ2			HIGH

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B6	VREF1B6	IO	DIFFIO_RX82p			AC3	AE3	AJ1			HIGH
B6	VREF1B6	IO	DIFFIO_TX81n		W7	AD5	AB7	AH5			HIGH
B6	VREF1B6	IO	DIFFIO_TX81p		W8	AE5	AB6	AH6			HIGH
B6	VREF1B6	IO	DIFFIO_RX81n		AE2	AH2	AE2	AH4			HIGH
B6	VREF1B6	IO	DIFFIO_RX81p		AE1	AG2	AE1	AH3			HIGH
B6	VREF1B6	IO	DIFFIO_TX80n		W5	AC5	AA6	AG6			HIGH
B6	VREF1B6	IO	DIFFIO_TX80p		W6	AB5	AA7	AG5			HIGH
B6	VREF1B6	IO	DIFFIO_RX80n		AD2	AE2	AC3	AH1			HIGH
B6	VREF1B6	IO	DIFFIO_RX80p		AD1	AF2	AC4	AH2			HIGH
B6	VREF1B6	IO	DIFFIO_TX79n		V8	AA6	AA9	AF8			HIGH
B6	VREF1B6	IO	DIFFIO_TX79p		V7	Y6	AA8	AF7			HIGH
B6	VREF1B6	IO	DIFFIO_RX79n		AC2	AD2	AD3	AG4			HIGH
B6	VREF1B6	IO	DIFFIO_RX79p		AC1	AC2	AD4	AG3			HIGH
B6	VREF1B6	IO	DIFFIO_TX78n		V6	Y9	Y5	AF6			HIGH
B6	VREF1B6	IO	DIFFIO_TX78p		V5	W9	Y6	AF5			HIGH
B6	VREF1B6	IO	DIFFIO_RX78n		AB4	AF1	AD2	AG2			HIGH
B6	VREF1B6	IO	DIFFIO_RX78p		AB3	AE1	AD1	AF2			HIGH
B6	VREF1B6	VREF1B6			W9	Y10	AB8	AG11			
B6	VREF1B6	IO	DIFFIO_TX77n		V9	Y8	Y7	AE8			HIGH
B6	VREF1B6	IO	DIFFIO_TX77p		V10	W8	Y8	AE7			HIGH
B6	VREF1B6	IO	DIFFIO_RX77n		AB2	AD1	AC2	AF1			HIGH
B6	VREF1B6	IO	DIFFIO_RX77p		AB1	AC1	AB1	AE2			HIGH
B6	VREF1B6	IO	DIFFIO_TX76n		U7	AA5	W5	AE6			HIGH
B6	VREF1B6	IO	DIFFIO_TX76p		U8	Y5	W6	AE5			HIGH
B6	VREF1B6	IO	DIFFIO_RX76n/RDN6		AA3	AB4	AA4	AF4			HIGH
B6	VREF1B6	IO	DIFFIO_RX76p/RUP6		AA4	AB3	AA5	AF3			HIGH
B6	VREF1B6	IO	DIFFIO_TX75n		U6	Y7	Y10	AD10			HIGH
B6	VREF1B6	IO	DIFFIO_TX75p		U5	W7	Y9	AD9			HIGH
B6	VREF1B6	IO	DIFFIO_RX75n		AA2	Y4	AB3	AE4			HIGH
B6	VREF1B6	IO	DIFFIO_RX75p		AA1	AA4	AB2	AE3			HIGH

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B6	VREF1B6	IO	DIFFIO_TX74n		U9	U7	W10	AD8			HIGH
B6	VREF1B6	IO	DIFFIO_TX74p		U10	V7	W9	AD7			HIGH
B6	VREF1B6	IO	DIFFIO_RX74n		Y4	W4	AA3	AD4			HIGH
B6	VREF1B6	IO	DIFFIO_RX74p		Y3	V4	AA2	AD3			HIGH
B6	VREF2B6	IO	DIFFIO_TX73n		T6	W6	V9	AD5			HIGH
B6	VREF2B6	IO	DIFFIO_TX73p		T5	V6	V10	AD6			HIGH
B6	VREF2B6	IO	DIFFIO_RX73n		Y2	AA3	Y4	AD2			HIGH
B6	VREF2B6	IO	DIFFIO_RX73p		Y1	Y3	Y3	AD1			HIGH
B6	VREF2B6	IO	DIFFIO_TX72n		T10	U6	V5	AC5			HIGH
B6	VREF2B6	IO	DIFFIO_TX72p		T9	T6	V6	AC6			HIGH
B6	VREF2B6	IO	DIFFIO_RX72n		W4	W3	Y2	AC4			HIGH
B6	VREF2B6	IO	DIFFIO_RX72p		W3	V3	Y1	AC3			HIGH
B6	VREF2B6	IO	DIFFIO_TX71n		T7	W5	V8	AC7			HIGH
B6	VREF2B6	IO	DIFFIO_TX71p		T8	V5	V7	AC8			HIGH
B6	VREF2B6	IO	DIFFIO_RX71n		W2	AB2	W4	AC2			HIGH
B6	VREF2B6	IO	DIFFIO_RX71p		W1	AA2	W3	AC1			HIGH
B6	VREF2B6	IO	DIFFIO_TX70n		T4	T5	W8	AB5			HIGH
B6	VREF2B6	IO	DIFFIO_TX70p		T3	U5	W7	AB6			HIGH
B6	VREF2B6	IO	DIFFIO_RX70n		V4	Y2	W2	AB4			HIGH
B6	VREF2B6	IO	DIFFIO_RX70p		V3	W2	W1	AB3			HIGH
B6	VREF2B6	VREF2B6			R10	W10	AA10	AF11			
B6	VREF2B6	IO	DIFFIO_TX69n				AB10	AB8			LOW
B6	VREF2B6	IO	DIFFIO_TX69p				AA11	AB9			LOW
B6	VREF2B6	IO	DIFFIO_RX69n		V1	AA1	V4	AB1			HIGH
B6	VREF2B6	IO	DIFFIO_RX69p		V2	AB1	V3	AB2			HIGH
B6	VREF2B6	IO	DIFFIO_TX68n				Y11	AA11			LOW
B6	VREF2B6	IO	DIFFIO_TX68p				Y12	AA10			LOW
B6	VREF2B6	IO	DIFFIO_RX68n		U4	V2	V2	AA4			HIGH
B6	VREF2B6	IO	DIFFIO_RX68p		U3	U2	V1	AA3			HIGH
B6	VREF2B6	IO	DIFFIO_TX67n				W11	AA9			LOW

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B6	VREF2B6	IO	DIFFIO_TX67p				W12	AA8			LOW
B6	VREF2B6	IO	DIFFIO_RX67n		U2	V1	U5	AA2			HIGH
B6	VREF2B6	IO	DIFFIO_RX67p		T1	U1	U6	AA1			HIGH
B6	VREF2B6	IO	CLK8n		R3	U4	U3	Y5			
B6	VREF2B6	CLK8p			R4	U3	U4	Y6			
B6	VREF2B6	CLK9n			T2	T3	U1	Y2			
B6	VREF2B6	CLK9p			R2	T4	U2	Y1			
		GNDG_PLL3			R7	V9	U11	Y11			
		VCCG_PLL3			R8	U9	V11	Y12			
		GNDA_PLL3			R5	V8	U7	Y9			
		GND									
		VCCA_PLL3			R6	U8	U8	W8			
		GNDG_PLL4			P7	R9	U9	W11			
		VCCG_PLL4			P8	R10	T9	W12			
		GNDA_PLL4			P5	R8	T7	W9			
		GND									
		VCCA_PLL4			P6	T8	T8	W10			
B5	VREF0B5	CLK10p			P4	T1	T6	Y3			
B5	VREF0B5	IO	CLK10n		P3	T2	T5	Y4			
B5	VREF0B5	CLK11p			P2	R3	T4	W5			
B5	VREF0B5	CLK11n			N2	R4	T3	W6			
B5	VREF0B5	IO	DIFFIO_TX66n				T11	Y7			LOW
B5	VREF0B5	IO	DIFFIO_TX66p				R11	W7			LOW
B5	VREF0B5	IO	DIFFIO_RX66n		M2	R1	T2	W1			HIGH
B5	VREF0B5	IO	DIFFIO_RX66p		N1	P1	T1	W2			HIGH
B5	VREF0B5	IO	DIFFIO_TX65n				P11	V7			LOW
B5	VREF0B5	IO	DIFFIO_TX65p				N11	V8			LOW
B5	VREF0B5	IO	DIFFIO_RX65n		M3	P2	R1	W4			HIGH
B5	VREF0B5	IO	DIFFIO_RX65p		M4	R2	R2	W3			HIGH
B5	VREF0B5	IO	DIFFIO_TX64n		N10	R7	R7	V6			HIGH

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B5	VREF0B5	IO	DIFFIO_TX64p		N9	T7	R8	V5			HIGH
B5	VREF0B5	IO	DIFFIO_RX64n		L1	K1	R3	V1			HIGH
B5	VREF0B5	IO	DIFFIO_RX64p		L2	L1	R4	V2			HIGH
B5	VREF0B5	VREF0B5			P10	P10	R12	R11			
B5	VREF0B5	IO	DIFFIO_TX63n		N5	P8	P7	U8			HIGH
B5	VREF0B5	IO	DIFFIO_TX63p		N6	N8	P8	U7			HIGH
B5	VREF0B5	IO	DIFFIO_RX63n		L3	N2	P1	V3			HIGH
B5	VREF0B5	IO	DIFFIO_RX63p		L4	M2	P2	V4			HIGH
B5	VREF0B5	IO	DIFFIO_TX62n		N7	R6	R5	U6			HIGH
B5	VREF0B5	IO	DIFFIO_TX62p		N8	P6	R6	U5			HIGH
B5	VREF0B5	IO	DIFFIO_RX62n		K1	L2	P3	U1			HIGH
B5	VREF0B5	IO	DIFFIO_RX62p		K2	K2	P4	U2			HIGH
B5	VREF0B5	IO	DIFFIO_TX61n		N4	P9	R10	T5			HIGH
B5	VREF0B5	IO	DIFFIO_TX61p		N3	N9	R9	T6			HIGH
B5	VREF0B5	IO	DIFFIO_RX61n		K4	P3	N1	U3			HIGH
B5	VREF0B5	IO	DIFFIO_RX61p		K3	N3	N2	U4			HIGH
B5	VREF0B5	IO	DIFFIO_TX60n		M10	P7	P6	T7			HIGH
B5	VREF0B5	IO	DIFFIO_TX60p		M9	N7	P5	T8			HIGH
B5	VREF0B5	IO	DIFFIO_RX60n		J1	L3	N3	T2			HIGH
B5	VREF0B5	IO	DIFFIO_RX60p		J2	M3	N4	T1			HIGH
B5	VREF1B5	IO	DIFFIO_TX59n		M6	N6	N7	T9			HIGH
B5	VREF1B5	IO	DIFFIO_TX59p		M5	M6	N8	T10			HIGH
B5	VREF1B5	IO	DIFFIO_RX59n		J3	P4	M2	T3			HIGH
B5	VREF1B5	IO	DIFFIO_RX59p		J4	N4	M3	T4			HIGH
B5	VREF1B5	IO	DIFFIO_TX58n		M8	R5	P9	R5			HIGH
B5	VREF1B5	IO	DIFFIO_TX58p		M7	P5	P10	R6			HIGH
B5	VREF1B5	IO	DIFFIO_RX58n		H1	M4	L2	R3			HIGH
B5	VREF1B5	IO	DIFFIO_RX58p		H2	L4	L3	R4			HIGH
B5	VREF1B5	IO	DIFFIO_TX57n		L10	M5	N5	R8			HIGH
B5	VREF1B5	IO	DIFFIO_TX57p		L9	N5	N6	R7			HIGH

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B5	VREF1B5	IO	DIFFIO_RX57n/RDN5		H3	K3	M4	P3			HIGH
B5	VREF1B5	IO	DIFFIO_RX57p/RUP5		H4	K4	M5	P4			HIGH
B5	VREF1B5	IO	DIFFIO_TX56n		L5	M8	N10	P5			HIGH
B5	VREF1B5	IO	DIFFIO_TX56p		L6	L8	N9	P6			HIGH
B5	VREF1B5	IO	DIFFIO_RX56n		G1	J1	L1	R2			HIGH
B5	VREF1B5	IO	DIFFIO_RX56p		G2	H1	K2	P1			HIGH
B5	VREF1B5	VREF1B5			K9	N10	L8	P11			
B5	VREF1B5	IO	DIFFIO_TX55n		L8	M7	M8	P7			HIGH
B5	VREF1B5	IO	DIFFIO_TX55p		L7	L7	M9	P8			HIGH
B5	VREF1B5	IO	DIFFIO_RX55n		G4	G1	J2	P2			HIGH
B5	VREF1B5	IO	DIFFIO_RX55p		G3	F1	J1	N2			HIGH
B5	VREF1B5	IO	DIFFIO_TX54n		K7	L5	M6	N5			HIGH
B5	VREF1B5	IO	DIFFIO_TX54p		K8	K5	M7	N6			HIGH
B5	VREF1B5	IO	DIFFIO_RX54n		F1	H2	K4	N4			HIGH
B5	VREF1B5	IO	DIFFIO_RX54p		F2	J2	K3	N3			HIGH
B5	VREF1B5	IO	DIFFIO_TX53n		J7	H5	L6	N8			HIGH
B5	VREF1B5	IO	DIFFIO_TX53p		J8	J5	L7	N7			HIGH
B5	VREF1B5	IO	DIFFIO_RX53n		F3	G2	J3	M1			HIGH
B5	VREF1B5	IO	DIFFIO_RX53p		F4	F2	J4	M2			HIGH
B5	VREF1B5	IO	DIFFIO_TX52n		K5	F5	K5	M6			HIGH
B5	VREF1B5	IO	DIFFIO_TX52p		K6	G5	K6	M5			HIGH
B5	VREF1B5	IO	DIFFIO_RX52n		E1	J3	H1	M3			HIGH
B5	VREF1B5	IO	DIFFIO_RX52p		E2	H3	H2	M4			HIGH
B5	VREF2B5	IO	DIFFIO_TX51n		J6	L6	K8	L5			HIGH
B5	VREF2B5	IO	DIFFIO_TX51p		J5	K6	K7	L6			HIGH
B5	VREF2B5	IO	DIFFIO_RX51n		D1	G3	G1	L1			HIGH
B5	VREF2B5	IO	DIFFIO_RX51p		D2	F3	G2	L2			HIGH
B5	VREF2B5	IO	DIFFIO_TX50n		H8	J6	J5	M7			HIGH
B5	VREF2B5	IO	DIFFIO_TX50p		H7	H6	J6	M8			HIGH
B5	VREF2B5	IO	DIFFIO_RX50n			J4	H3	L3			HIGH

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B5	VREF2B5	IO	DIFFIO_RX50p			H4	H4	L4			HIGH
B5	VREF2B5	IO	DIFFIO_TX49n		H6	G6	J7	K5			HIGH
B5	VREF2B5	IO	DIFFIO_TX49p		H5	F6	J8	K6			HIGH
B5	VREF2B5	IO	DIFFIO_RX49n			G4	F1	K2			HIGH
B5	VREF2B5	IO	DIFFIO_RX49p			F4	F2	K1			HIGH
B5	VREF2B5	IO	DIFFIO_TX48n		G5	K8	H5	L8			HIGH
B5	VREF2B5	IO	DIFFIO_TX48p		G6	J8	H6	L7			HIGH
B5	VREF2B5	IO	DIFFIO_RX48n			E2	G3	K3			HIGH
B5	VREF2B5	IO	DIFFIO_RX48p			D2	G4	K4			HIGH
B5	VREF2B5	VREF2B5			E5	M10	F6	N11			
B5	VREF2B5	IO	DIFFIO_TX47n		F6	K7	H8	K7			HIGH
B5	VREF2B5	IO	DIFFIO_TX47p		F5	J7	H7	K8			HIGH
B5	VREF2B5	IO	DIFFIO_RX47n		C1	E3	F3	J3			HIGH
B5	VREF2B5	IO	DIFFIO_RX47p		C2	D3	F4	J4			HIGH
B5	VREF2B5	IO	DIFFIO_TX46n		D3	H7	G6	J7			HIGH
B5	VREF2B5	IO	DIFFIO_TX46p		D4	G7	G5	J8			HIGH
B5	VREF2B5	IO	DIFFIO_RX46n				E2	H2			LOW
B5	VREF2B5	IO	DIFFIO_RX46p				E1	H1			LOW
B5	VREF2B5	IO	DIFFIO_TX45n		E3	G8	G7	M9			HIGH
B5	VREF2B5	IO	DIFFIO_TX45p		E4	H8	G8	M10			HIGH
B5	VREF2B5	IO	DIFFIO_RX45n				F5	G2			LOW
B5	VREF2B5	IO	DIFFIO_RX45p				E4	G1			LOW
B5	VREF2B5	IO						N9			
B5	VREF2B5	IO						N10			
B5	VREF2B5	FPLL10CLKn				D1	L5	J1			
B5	VREF2B5	FPLL10CLKp				E1	L4	J2			
		GNDG_PLL10				K9	E3	L9			
		VCCG_PLL10				J9	D3	L10			
		GNDA_PLL10				M9	D1	K9			
		GND									

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
		VCCA_PLL10				L9	D2	J9			
B4	VREF0B4	IO				D4	F8	F7			
B4	VREF0B4	IO	DQ0T0		A4	C4	D5	C6	DQ0T0	DQ0T0	
B4	VREF0B4	IO			G7		F7	C4			
B4	VREF0B4	IO	DQ0T1		A3	C5	C3	B6	DQ0T1	DQ0T1	
B4	VREF0B4	IO				E4	J9	E5			
B4	VREF0B4	IO	DQ0T2		B3	D5	E5	C7	DQ0T2	DQ0T2	
B4	VREF0B4	IO				H9	G9	B4			
B4	VREF0B4	IO	DQS0T		D5	B4	C5	B7			
B4	VREF0B4	IO			F7	E5	H9	E6			
B4	VREF0B4	IO	DQ0T3		B5	B5	C4	A7	DQ0T3	DQ0T3	
B4	VREF0B4	IO				C2	K9	G7			
B4	VREF0B4	IO	DQ0T4		B4	B3	D4	C8	DQ0T4	DQ0T4	
B4	VREF0B4	VREF0B4			E7	K10	E6	L11			
B4	VREF0B4	IO				J10	F9	D6			
B4	VREF0B4	IO	DQ0T5		C4	C3	A4	A6	DQ0T5	DQ0T5	
B4	VREF0B4	IO			G8	F7	L9	G8			
B4	VREF0B4	IO	DQ0T6		A5	A5	B4	A8	DQ0T6	DQ0T6	
B4	VREF0B4	IO			J9		K10	D5			
B4	VREF0B4	IO	DQ0T7		C5	A4	B3	B8	DQ0T7	DQ0T7	
B4	VREF0B4	IO				F8	H10	G9			
B4	VREF0B4	IO			F8			B5			
B4	VREF0B4	IO	DQ1T0		E6	E6	D6	C9	DQ0T8	DQ0T8	
B4	VREF0B4	IO				E7	J10	F8			
B4	VREF0B4	IO	DQ1T1		A6	C7	C6	B9	DQ0T9	DQ0T9	
B4	VREF0B4	IO					L10	C5			
B4	VREF1B4	IO	DQ1T2		B7	D7	B5	A9	DQ0T10	DQ0T10	
B4	VREF1B4	IO				H10	F10	E8			
B4	VREF1B4	IO	DQS1T		B6	C6	E7	B10	DQS0T		
B4	VREF1B4	IO			H9	G9	G10	A4			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B4	VREF1B4	IO	DQ1T3		D6	A6	C7	C11	DQ0T11	DQ0T11	
B4	VREF1B4	IO				L11	M10	E7			
B4	VREF1B4	IO	DQ1T4		A7	B6	A5	A10	DQ0T12	DQ0T12	
B4	VREF1B4	IO	DQ1T7		C7	B7	B6	B11	DQ0T15	DQ0T15	
B4	VREF1B4	IO	DQ1T5		D7	D6	D7	C10	DQ0T13	DQ0T13	
B4	VREF1B4	IO			G9	J11	K11	G10			
B4	VREF1B4	IO	DQ1T6		C6	A7	A6	A11	DQ0T14	DQ0T14	
B4	VREF1B4	IO					L11	D7			
B4	VREF1B4	VREF1B4			E9	K11	E8	L12			
B4	VREF1B4	IO				F9	J11	E9			
B4	VREF1B4	IO				E9	H11	E10			
B4	VREF1B4	IO						D8			
B4	VREF1B4	IO	DQ2T0		D8	B8	B7	A12	DQ1T0	DQ0T16	
B4	VREF1B4	IO					M11	F9			
B4	VREF1B4	IO	DQ2T1		C8	D9	D8	D12	DQ1T1	DQ0T17	
B4	VREF1B4	IO			F9	H11	G11	D9			
B4	VREF1B4	IO	DQ2T2		E8	E8	B8	E12	DQ1T2	DQ0T18	
B4	VREF1B4	IO				G10	K12	F10			
B4	VREF1B4	IO	DQS2T		C9	C8	A7	C12		DQS0T	
B4	VREF1B4	IO					L12	A5			
B4	VREF1B4	IO	DQ2T3		D9	C9	E9	E13	DQ1T3	DQ0T19	
B4	VREF1B4	IO					F11	F11			
B4	VREF1B4	IO	DQ2T4		B9	D8	A8	B12	DQ1T4	DQ0T20	
B4	VREF1B4	IO			H10	J12	J12	G11			
B4	VREF1B4	IO	DQ2T5		B8	A9	C9	B13	DQ1T5	DQ0T21	
B4	VREF1B4	IO	DQ2T6		A8	B9	C8	C13	DQ1T6	DQ0T22	
B4	VREF1B4	IO	DQ2T7		A9	A8	D9	D13	DQ1T7	DQ0T23	
B4	VREF2B4	IO	FCLK6		G10	F10	G12	D11			
B4	VREF2B4	IO	FCLK7		F10	F11	A14	G14			
B4	VREF2B4	IO			J10	G11	H12	D10			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B4	VREF2B4	IO						F12			
B4	VREF2B4	IO	DQ3T0		E10	B10	E11	C14	DQ1T8	DQ0T24	
B4	VREF2B4	IO					K13	G12			
B4	VREF2B4	IO	DQ3T1		A10	D10	B9	D14	DQ1T9	DQ0T25	
B4	VREF2B4	IO			F11	G12	F13	F13			
B4	VREF2B4	IO	DQ3T2		C10	E10	D10	E14	DQ1T10	DQ0T26	
B4	VREF2B4	IO			K10	H12	F12	G13			
B4	VREF2B4	IO	DQS3T		D10	C10	D11	C15	DQS1T		
B4	VREF2B4	IO			G12	L12	L14	E11			
B4	VREF2B4	VREF2B4			E11	K12	E10	L13			
B4	VREF2B4	IO	DQ3T3		B10	D11	C10	A14	DQ1T11	DQ0T27	
B4	VREF2B4	IO				H13	B14	G15			
B4	VREF2B4	IO	DQ3T4		A11	E11	A9	B14	DQ1T12	DQ0T28	
B4	VREF2B4	IO				J13	H13	F14			
B4	VREF2B4	IO	DQ3T5		C11	B11	B11	B15	DQ1T13	DQ0T29	
B4	VREF2B4	IO	DEV_OE		J11	F12	L13	P16			
B4	VREF2B4	IO	RUP4		H11	F13	G13	F15			
B4	VREF2B4	IO	RDN4		G11	E14	J13	E16			
B4	VREF2B4	IO	DQ3T7		B11	A10	B10	D15	DQ1T15	DQ0T31	
B4	VREF2B4	IO					C14	G16			
B4	VREF2B4	IO	DQ3T6		D11	C11	C11	E15	DQ1T14	DQ0T30	
B4	VREF2B4	IO	DQ4T0		B12	D12	A11	A16			
B4	VREF2B4	IO		nWS	K11	F14	D14	F16			
B4	VREF2B4	IO	DQ4T1		C12	E12	B12	D16			
B4	VREF2B4	IO					H14	F17			
B4	VREF2B4	IO	DQ4T2		D12	A12	C12	A17			
B4	VREF2B4	IO				G13	K14	G17			
B4	VREF2B4	IO	DQS4T		A13	C12	D12	C16			
B4	VREF3B4	IO		DATA0	H12	E15	E14	M17			
B4	VREF3B4	IO	DQ4T3		B13	B12	C13	B16			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B4	VREF3B4	IO				G14	J14	C18			
B4	VREF3B4	IO	DQ4T4		E12	C13	D13	B17			
B4	VREF3B4	IO			L11	L14	L15	D18			
B4	VREF3B4	IO	DQ4T5		C13	D13	E13	D17			
B4	VREF3B4	IO		DATA1	F12	C16	F14	J17			
B4	VREF3B4	IO	DQ4T6		D13	E13	A13	E17			
B4	VREF3B4	IO					J15	E18			
B4	VREF3B4	IO	DQ4T7		E13	B13	B13	C17			
B4	VREF3B4	IO			M11	L16	K15	F18			
B4	VREF3B4	IO		DATA2	J12	F15	F15	K18			
B4	VREF3B4	VREF3B4				K13	E12	L14			
B4	VREF3B4	TMS		TMS	F13	D16	E15	F19			
B4	VREF3B4	TRST		TRST	L12	G15	G15	H19			
B4	VREF3B4	TCK		TCK	K12	F16	G14	E20			
B4	VREF3B4	IO		DATA3	M12	G17	C16	P21			
B4	VREF3B4	IO						H18			
B4	VREF3B4	IO						G18			
B4	VREF3B4	TDI		TDI	G13	E16	D16	F20			
B4	VREF3B4	TDO		TDO	H13	G16	F16	G20			
B4	VREF3B4	IO	CLK12n		J13	B14	A15	A18			
B4	VREF3B4	CLK12p			K13	A14	B15	B18			
B4	VREF3B4	IO	CLK13n/PLL11_OUT		L13	D14	C15	C19			
B4	VREF3B4	CLK13p			M13	C14	D15	D19			
		VCCA_PLL11				J14	E16	K19			
		GND									
		GNDA_PLL11				H14	E17	J19			
		VCCG_PLL11				H15	H16	L19			
		GNDG_PLL11				J15	H15	M19			
		TEMPDIODEp			B14	E17	E18	F21			
		TEMPDIODEn			C14	F17	F18	H21			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
		VCCA_PLL5			F14	J17	G17	L21			
		GND									
		GNDA_PLL5			G14	H16	F17	M21			
		VCCG_PLL5			D14	K15	J16	L20			
		GNDG_PLL5			E14	K17	L16	M20			
B9		VCC_PLL5_OUTA			F15	L18	H17	J20			
B10		VCC_PLL5_OUTB			G16	J18	L17	K21			
B9	VREF0B3	IO	PLL5_OUT0p		E15	B16	B16	C21			
B9	VREF0B3	IO	PLL5_OUT0n		D15	A16	A16	D21			
B9	VREF0B3	IO	PLL5_OUT1p		K14	B15	B17	C20			
B9	VREF0B3	IO	PLL5_OUT1n		K15	A15	A17	D20			
B9	VREF0B3	IO	PLL5_FBp		H14	D15	D17	B19			
B9	VREF0B3	IO	PLL5_FBn		H15	C15	C17	A19			
B10	VREF0B3	IO	PLL5_OUT2p		C15	D17	B18	B21			
B10	VREF0B3	IO	PLL5_OUT2n		B15	C17	A18	A21			
B10	VREF0B3	IO	PLL5_OUT3p		K16	B17	D18	A20			
B10	VREF0B3	IO	PLL5_OUT3n		J16	A17	C18	B20			
B3	VREF0B3	nSTATUS		nSTATUS	M16	E18	G16	N21			
B3	VREF0B3	nCONFIG		nCONFIG	L16	F19	J18	L22			
B3	VREF0B3	DCLK		DCLK	F16	F18	E19	G21			
B3	VREF0B3	CONF_DONE		CONF_DONE	G17	G18	G18	H22			
B3	VREF0B3	CLK14p			K17	A18	A19	B22			
B3	VREF0B3	IO	CLK14n		J17	B18	B19	A22			
B3	VREF0B3	CLK15p			M17	C18	C19	D22			
B3	VREF0B3	IO	CLK15n		L17	D18	D19	C22			
B3	VREF0B3	VREF0B3			E18	K18	E21	L25			
B3	VREF0B3	IO						G22			
B3	VREF0B3	IO						E22			
B3	VREF0B3	IO		DATA4	H17	G19	G19	L23			
B3	VREF0B3	IO						F22			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B3	VREF0B3	IO						E21			
B3	VREF0B3	IO						F23			
B3	VREF0B3	IO						G23			
B3	VREF0B3	IO			L18	H19	H19	H23			
B3	VREF0B3	IO	DQ5T0		D16	B19	A20	B23			
B3	VREF0B3	IO					K18	F24			
B3	VREF0B3	IO	DQ5T1		C16	C19	B20	E23			
B3	VREF0B3	IO		DATA5	K18	F20	J19	J23			
B3	VREF1B3	IO	DQ5T2		E16	D19	C20	D23			
B3	VREF1B3	IO					F19	G24			
B3	VREF1B3	IO	DQS5T		A16	C20	D20	C23			
B3	VREF1B3	IO						H24			
B3	VREF1B3	IO	DQ5T3		B16	E19	E20	A23			
B3	VREF1B3	IO		DATA6	H18	F21	K19	E24			
B3	VREF1B3	IO	DQ5T4		E17	A20	B21	A24			
B3	VREF1B3	IO				J19	F20	F25			
B3	VREF1B3	IO	DQ5T5		D17	B20	C21	B24			
B3	VREF1B3	IO			M18	H20	L18	G25			
B3	VREF1B3	IO	DQ5T6		B17	D20	D21	C24			
B3	VREF1B3	IO					L20	H25			
B3	VREF1B3	IO	DQ5T7		C17	E20	A22	D24			
B3	VREF1B3	IO	DQ6T1		C18	C21	C22	E25	DQ2T1	DQ1T1	
B3	VREF1B3	IO			F17	L19	K20	H26			
B3	VREF1B3	IO	DQ6T0		A18	B21	B22	B25	DQ2T0	DQ1T0	
B3	VREF1B3	IO	RUP3		J18	F22	F21	P23			
B3	VREF1B3	IO	RDN3		K19	F24	L19	M24			
B3	VREF1B3	VREF1B3				K19	E23	L26			
B3	VREF1B3	IO		DATA7	G18	G20	J20	P25			
B3	VREF1B3	IO	DQ6T2		D18	A22	B23	D25	DQ2T2	DQ1T2	
B3	VREF1B3	IO					H20	F27			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B3	VREF1B3	IO	DQS6T		B18	C22	D22	C25	DQS2T		
B3	VREF1B3	IO						F26			
B3	VREF1B3	IO	DQ6T3		A19	D21	C23	A26	DQ2T3	DQ1T3	
B3	VREF1B3	IO		CLKUSR	J19	F23	H21	J25			
B3	VREF1B3	IO	DQ6T4		B19	E21	A24	B26	DQ2T4	DQ1T4	
B3	VREF1B3	IO					G20	G27			
B3	VREF1B3	IO	DQ6T5		C19	B22	E22	C26	DQ2T5	DQ1T5	
B3	VREF1B3	IO	DQ6T6		E19	D22	B24	D26	DQ2T6	DQ1T6	
B3	VREF1B3	IO	DQ6T7		D19	E22	D23	E26	DQ2T7	DQ1T7	
B3	VREF2B3	IO	FCLK0		F19	E23	F22	G26			
B3	VREF2B3	IO	FCLK1		G19	E25	G22	D29			
B3	VREF2B3	IO						F28			
B3	VREF2B3	IO			H19	J20	K21	H27			
B3	VREF2B3	IO	DQ7T0		B20	A23	D24	B27	DQ2T8	DQ1T8	
B3	VREF2B3	IO						F29			
B3	VREF2B3	IO	DQ7T1		A20	B23	A25	C27	DQ2T9	DQ1T9	
B3	VREF2B3	IO						E29			
B3	VREF2B3	IO	DQ7T2		C20	A24	C24	D27	DQ2T10	DQ1T10	
B3	VREF2B3	IO				G21	J21	G28			
B3	VREF2B3	IO	DQS7T		D20	C24	B26	C28		DQS1T	
B3	VREF2B3	IO					L21	F30			
B3	VREF2B3	IO	DQ7T3		A21	C23	B25	E27	DQ2T11	DQ1T11	
B3	VREF2B3	IO				H21	G21	D30			
B3	VREF2B3	IO	DQ7T4		B21	D24	C25	B28	DQ2T12	DQ1T12	
B3	VREF2B3	IO					H22	G29			
B3	VREF2B3	IO	DQ7T5		C21	B24	D25	A28	DQ2T13	DQ1T13	
B3	VREF2B3	IO			J20	L21	L22	G30			
B3	VREF2B3	VREF2B3			E20	K20	E25	L27			
B3	VREF2B3	IO	DQ7T6		D21	D23	A26	D28	DQ2T14	DQ1T14	
B3	VREF2B3	IO						D31			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B3	VREF2B3	IO	DQ7T7		E21	E24	E24	E28	DQ2T15	DQ1T15	
B3	VREF2B3	IO			H20	J21	J22	D32			
B3	VREF2B3	IO						A35			
B3	VREF2B3	IO					K22	F31			
B3	VREF2B3	IO						E30			
B3	VREF2B3	IO	DQ8T1		A22	C25	A28	B29	DQ3T1	DQ1T17	
B3	VREF2B3	IO			F18	G22	F23	E31			
B3	VREF2B3	IO	DQ8T2		C22	B25	A27	C29	DQ3T2	DQ1T18	
B3	VREF2B3	IO	DQ8T0		B22	A25	C26	A29	DQ3T0	DQ1T16	
B3	VREF2B3	IO	DQS8T		D23	C26	B27	B30	DQS3T		
		GND			G20	D28	H24	E32			
B3	VREF3B3	IO					G23	D33			
B3	VREF3B3	IO	DQ8T3		D22	D25	D26	C30	DQ3T3	DQ1T19	
B3	VREF3B3	IO			F20	H22	J23	A36			
B3	VREF3B3	IO	DQ8T4		A23	A26	C27	A30	DQ3T4	DQ1T20	
B3	VREF3B3	IO					L23	F32			
B3	VREF3B3	IO	DQ8T5		C23	B26	B28	A31	DQ3T5	DQ1T21	
B3	VREF3B3	IO						B35			
B3	VREF3B3	IO	DQ8T6		E23	E26	D27	B31	DQ3T6	DQ1T22	
B3	VREF3B3	IO			G21	G23	H23	G31			
B3	VREF3B3	IO	DQ8T7		B23	D26	E26	C31	DQ3T7	DQ1T23	
B3	VREF3B3	IO						D34			
B3	VREF3B3	IO			G22	H23	K23	G32			
B3	VREF3B3	IO	DQ9T0		A24	B27	A29	A32	DQ3T8	DQ1T24	
B3	VREF3B3	IO						E33			
B3	VREF3B3	IO	DQ9T1		C25	C27	B29	C32	DQ3T9	DQ1T25	
B3	VREF3B3	IO				J22	F24	B36			
B3	VREF3B3	IO	DQ9T2		A25	A27	B30	B32	DQ3T10	DQ1T26	
B3	VREF3B3	IO				E27	L24	D35			
B3	VREF3B3	VREF3B3			E22	K21	E27	L28			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
B3	VREF3B3	IO	DQS9T		C24	B28	C28	B33			
B3	VREF3B3	IO					G24	C35			
B3	VREF3B3	IO	DQ9T3		D24	D27	C29	A34	DQ3T11	DQ1T27	
B3	VREF3B3	IO			F21	F25	F25	E34			
B3	VREF3B3	IO	DQ9T4		B24	A28	D29	A33	DQ3T12	DQ1T28	
B3	VREF3B3	IO					K24	G33			
B3	VREF3B3	IO	DQ9T5		B25	C28	D28	C33	DQ3T13	DQ1T29	
B3	VREF3B3	IO						F33			
B3	VREF3B3	IO	DQ9T6		A26	C29	C30	C34	DQ3T14	DQ1T30	
B3	VREF3B3	IO			F22	C30	F26	C36			
B3	VREF3B3	IO	DQ9T7		B26	B29	E28	B34	DQ3T15	DQ1T31	
B3	VREF3B3	IO				E28	J24	E35			
		VCCIO2			B28	C31	C31	C39			
		VCCIO2			M28	N31	C32	R39			
		VCCIO2			P20	T23	M32	W35			
		VCCIO2					T23	V25			
		VCCIO2						H33			
		VCCIO1			R20	U20	AA32	AA25			
		VCCIO1			U28	W31	AK31	Y32			
		VCCIO1			AG28	AJ31	AK32	AE39			
		VCCIO1					U23	AU39			
		VCCIO1						AM33			
		VCCIO8			Y15	AL29	AC17	AW37			
		VCCIO8			AH17	AL19	AM21	AW25			
		VCCIO8			AH27	Y17	AM30	AR21			
		VCCIO8						AE22			
		VCCIO8						AM30			
		VCCIO7			Y14	AC16	AC16	AE19			
		VCCIO7			AH2	AL13	AM12	AM20			
		VCCIO7			AH12	AL3	AM3	AW15			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
		VCCIO7						AW3			
		VCCIO7						AM10			
		VCCIO6			R9	AJ1	AA1	AU1			
		VCCIO6			U1	W1	AK1	AM7			
		VCCIO6			AG1	U12	AK2	AE1			
		VCCIO6					U10	AA5			
		VCCIO6						AB15			
		VCCIO5			B1	T9	C1	W15			
		VCCIO5			M1	N1	C2	Y8			
		VCCIO5			P9	C1	M1	R1			
		VCCIO5					T10	H7			
		VCCIO5						C1			
		VCCIO4			A2	A3	A12	A3			
		VCCIO4			A12	A13	A3	A15			
		VCCIO4			J14	J16	K16	E19			
		VCCIO4						R18			
		VCCIO4						H10			
		VCCIO3			A17	M17	A21	H20			
		VCCIO3			A27	A19	A30	R21			
		VCCIO3			J15	A29	K17	A25			
		VCCIO3						A37			
		VCCIO3						H30			
		VCCINT			M14	AA12	M12	AA16			
		VCCINT			N11	AA14	M14	AA18			
		VCCINT			N13	AA20	M19	AA22			
		VCCINT			N15	L13	M21	AA24			
		VCCINT			N17	L20	N13	AB17			
		VCCINT			P12	M11	N15	AB19			
		VCCINT			P14	M13	N18	AB21			
		VCCINT			P16	M15	N20	AB23			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
		VCCINT			R13	M19	P12	AB25			
		VCCINT			R15	M21	P14	AC16			
		VCCINT			R17	N12	P16	AC18			
		VCCINT			T12	N14	P17	AC20			
		VCCINT			T14	N16	P19	AC22			
		VCCINT			T16	N18	P21	AC24			
		VCCINT			T18	N20	R13	AD15			
		VCCINT			U11	P11	R15	AD17			
		VCCINT			U13	P13	R18	AD19			
		VCCINT			U15	P14	R20	AD21			
		VCCINT			U17	P15	T14	AD23			
		VCCINT			V12	P17	T16	AD25			
		VCCINT			V16	P19	T17	AE16			
		VCCINT				P21	T19	AE18			
		VCCINT				R12	U14	AE20			
		VCCINT				R13	U16	AE24			
		VCCINT				R14	U17	R16			
		VCCINT				R18	U19	R20			
		VCCINT				R19	V13	R22			
		VCCINT				R20	V15	R24			
		VCCINT				T11	V18	T15			
		VCCINT				T13	V20	T17			
		VCCINT				T19	W14	T19			
		VCCINT				T21	W16	T21			
		VCCINT				U10	W17	T23			
		VCCINT				U14	W19	T25			
		VCCINT				U18	Y13	U16			
		VCCINT				U22	Y15	U18			
		VCCINT				V11	Y18	U20			
		VCCINT				V13	Y20	U22			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
		VCCINT				V15		U24			
		VCCINT				V17		V15			
		VCCINT				V19		V17			
		VCCINT				V21		V19			
		VCCINT				W12		V21			
		VCCINT				W14		V23			
		VCCINT				W16		W16			
		VCCINT				W18		W18			
		VCCINT				W20		W22			
		VCCINT				Y11		W24			
		VCCINT				Y13		Y15			
		VCCINT				Y15		Y17			
		VCCINT				Y19		Y23			
		VCCINT				Y21		Y25			
		GND			A14	A1	A10	A13			
		GND			A15	A11	A2	A2			
		GND			AA16	A2	A23	A27			
		GND			AC15	A21	A31	A38			
		GND			AF26	A30	AA16	AA15			
		GND			AF3	A31	AA17	AA17			
		GND			AG2	AA17	AC1	AA23			
		GND			AG27	AA18	AC32	AA7			
		GND			AH14	AB16	AD17	AB16			
		GND			AH15	AD18	AF17	AB18			
		GND			B2	AK1	AL1	AB20			
		GND			B27	AK2	AL2	AB22			
		GND			C26	AK30	AL31	AB24			
		GND			C3	AK31	AL32	AC15			
		GND			G15	AL1	AM10	AC17			
		GND			H16	AL11	AM2	AC19			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
		GND			L14	AL2	AM23	AC21			
		GND			L15	AL21	AM31	AC23			
		GND			M15	AL30	B1	AC25			
		GND			N12	AL31	B2	AD16			
		GND			N14	B1	B31	AD18			
		GND			N16	B2	B32	AD20			
		GND			N18	B30	H18	AD22			
		GND			P1	B31	J17	AD24			
		GND			P11	H17	K1	AE15			
		GND			P13	H18	K32	AE17			
		GND			P15	K16	M13	AE21			
		GND			P17	L15	M15	AE23			
		GND			P18	L17	M16	AE25			
		GND			P28	M1	M17	AG1			
		GND			R1	M12	M18	AG39			
		GND			R11	M14	M20	AK10			
		GND			R12	M16	N12	AK20			
		GND			R14	M18	N14	AK22			
		GND			R16	M20	N16	AK30			
		GND			R18	M31	N17	AL21			
		GND			R28	N11	N19	AM32			
		GND			T11	N13	N21	AM8			
		GND			T13	N15	P13	AN21			
		GND			T15	N17	P15	AU3			
		GND			T17	N19	P18	AU37			
		GND				N21	P20	AV1			
		GND			U14	P12	R14	AV2			
		GND			U16	P16	R16	AV38			
		GND				P18	R17	AV39			
		GND			V13	P20	R19	AW13			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
		GND			V14	R11	T12	AW2			
		GND			V15	R15	T13	AW27			
		GND			V17	R17	T15	AW38			
		GND				R21	T18	B1			
		GND				T10	T20	B2			
		GND				T12	T21	B38			
		GND				T14	U12	B39			
		GND				T18	U13	C3			
		GND				T20	U15	C37			
		GND				T22	U18	G19			
		GND				U11	U20	H32			
		GND				U13	U21	H8			
		GND				U15	V14	J21			
		GND				U17	V16	K10			
		GND				U19	V17	K20			
		GND				U21	V19	K22			
		GND				V12	W13	K30			
		GND				V14	W15	N1			
		GND				V16	W18	N39			
		GND				V18	W20	R15			
		GND				V20	Y14	R17			
		GND				W11	Y16	R19			
		GND				W13	Y17	R23			
		GND				W15	Y19	R25			
		GND				W17		T16			
		GND				W19		T18			
		GND				W21		T20			
		GND				Y1		T22			
		GND				Y12		T24			
		GND				Y14		U15			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
		GND				Y16		U17			
		GND				Y18		U19			
		GND				Y20		U21			
		GND				Y31		U23			
		GND						U25			
		GND						V16			
		GND						V18			
		GND						V20			
		GND						V22			
		GND						V24			
		GND						W17			
		GND						W23			
		GND						W25			
		GND						W33			
		GND						Y10			
		GND						Y16			
		GND						Y18			
		GND						Y22			
		GND						Y24			
		GND						Y30			
		NC				AA22	AG27	AA12			
		NC				AB10	V12	AA13			
		NC				AB18		AA14			
		NC				K14		AA26			
		NC				K22		AA27			
		NC				L10		AA6			
		NC				P22		AB10			
		NC				V10		AB11			
		NC						AB12			
		NC						AB13			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
		NC						AB14			
		NC						AB26			
		NC						AB27			
		NC						AB28			
		NC						AB29			
		NC						AB7			
		NC						AC10			
		NC						AC11			
		NC						AC12			
		NC						AC13			
		NC						AC14			
		NC						AC26			
		NC						AC27			
		NC						AC28			
		NC						AC29			
		NC						AC30			
		NC						AC31			
		NC						AC9			
		NC						AD11			
		NC						AD12			
		NC						AD13			
		NC						AD14			
		NC						AD26			
		NC						AD27			
		NC						AD28			
		NC						AD29			
		NC						AE10			
		NC						AE11			
		NC						AE12			
		NC						AE13			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
		NC						AE14			
		NC						AE26			
		NC						AE27			
		NC						AE28			
		NC						AE30			
		NC						AE31			
		NC						AE9			
		NC						AF10			
		NC						AF12			
		NC						AF13			
		NC						AF14			
		NC						AF15			
		NC						AF17			
		NC						AF18			
		NC						AF19			
		NC						AF20			
		NC						AF21			
		NC						AF22			
		NC						AF24			
		NC						AF25			
		NC						AF26			
		NC						AF27			
		NC						AF28			
		NC						AF30			
		NC						AF31			
		NC						AF9			
		NC						AG12			
		NC						AG13			
		NC						AG14			
		NC						AG15			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
		NC						AG16			
		NC						AG17			
		NC						AG18			
		NC						AG19			
		NC						AG22			
		NC						AG23			
		NC						AG24			
		NC						AG25			
		NC						AG26			
		NC						AG27			
		NC						AG28			
		NC						AH12			
		NC						AH13			
		NC						AH14			
		NC						AH15			
		NC						AH16			
		NC						AH17			
		NC						AH18			
		NC						AH22			
		NC						AH25			
		NC						AH26			
		NC						AH27			
		NC						AH28			
		NC						AH29			
		NC						AJ11			
		NC						AJ16			
		NC						AJ17			
		NC						AJ18			
		NC						AJ22			
		NC						AJ24			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
		NC						AJ25			
		NC						AK11			
		NC						AK12			
		NC						AK13			
		NC						AK14			
		NC						AK15			
		NC						AK16			
		NC						AK18			
		NC						AK23			
		NC						AK24			
		NC						AK25			
		NC						AK26			
		NC						AK27			
		NC						AK28			
		NC						AK29			
		NC						AL10			
		NC						AL11			
		NC						AL12			
		NC						AL13			
		NC						AL14			
		NC						AL15			
		NC						AL16			
		NC						AL22			
		NC						AL24			
		NC						AL26			
		NC						AL27			
		NC						AL28			
		NC						AL29			
		NC						AL30			
		NC						AL34			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
		NC						AL35			
		NC						AL5			
		NC						AL6			
		NC						AM11			
		NC						AM12			
		NC						AM13			
		NC						AM14			
		NC						AM15			
		NC						AM16			
		NC						AM17			
		NC						AM18			
		NC						AM28			
		NC						AM29			
		NC						AM3			
		NC						AM31			
		NC						AM34			
		NC						AM35			
		NC						AM36			
		NC						AM37			
		NC						AM4			
		NC						AM5			
		NC						AM6			
		NC						AM9			
		NC						AN15			
		NC						AN3			
		NC						AN34			
		NC						AN35			
		NC						AN36			
		NC						AN37			
		NC						AN4			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
		NC						AN5			
		NC						AN6			
		NC						AP3			
		NC						AP34			
		NC						AP35			
		NC						AP36			
		NC						AP37			
		NC						AP4			
		NC						AP5			
		NC						AP6			
		NC						AR1			
		NC						AR2			
		NC						AR3			
		NC						AR36			
		NC						AR37			
		NC						AR38			
		NC						AR39			
		NC						AR4			
		NC						AT1			
		NC						AT2			
		NC						AT3			
		NC						AT36			
		NC						AT37			
		NC						AT38			
		NC						AT39			
		NC						AT4			
		NC						AU2			
		NC						AU38			
		NC						AV3			
		NC						AV37			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
		NC						B3			
		NC						B37			
		NC						C2			
		NC						C38			
		NC						D1			
		NC						D2			
		NC						D3			
		NC						D36			
		NC						D37			
		NC						D38			
		NC						D39			
		NC						D4			
		NC						E1			
		NC						E2			
		NC						E3			
		NC						E36			
		NC						E37			
		NC						E38			
		NC						E39			
		NC						E4			
		NC						F1			
		NC						F2			
		NC						F3			
		NC						F34			
		NC						F35			
		NC						F36			
		NC						F37			
		NC						F38			
		NC						F39			
		NC						F4			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
		NC						F5			
		NC						F6			
		NC						G3			
		NC						G34			
		NC						G35			
		NC						G36			
		NC						G37			
		NC						G4			
		NC						G5			
		NC						G6			
		NC						H11			
		NC						H12			
		NC						H13			
		NC						H14			
		NC						H15			
		NC						H16			
		NC						H17			
		NC						H28			
		NC						H29			
		NC						H3			
		NC						H31			
		NC						H34			
		NC						H35			
		NC						H36			
		NC						H37			
		NC						H4			
		NC						H5			
		NC						H6			
		NC						H9			
		NC						J10			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
		NC						J11			
		NC						J12			
		NC						J13			
		NC						J14			
		NC						J15			
		NC						J16			
		NC						J18			
		NC						J22			
		NC						J24			
		NC						J26			
		NC						J27			
		NC						J28			
		NC						J29			
		NC						J30			
		NC						J34			
		NC						J35			
		NC						J5			
		NC						J6			
		NC						K11			
		NC						K12			
		NC						K13			
		NC						K14			
		NC						K15			
		NC						K16			
		NC						K17			
		NC						K23			
		NC						K24			
		NC						K25			
		NC						K26			
		NC						K27			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
		NC						K28			
		NC						K29			
		NC						L15			
		NC						L16			
		NC						L17			
		NC						L18			
		NC						L24			
		NC						L29			
		NC						M11			
		NC						M12			
		NC						M13			
		NC						M14			
		NC						M15			
		NC						M16			
		NC						M18			
		NC						M22			
		NC						M23			
		NC						M25			
		NC						M26			
		NC						M27			
		NC						M28			
		NC						N12			
		NC						N13			
		NC						N14			
		NC						N15			
		NC						N16			
		NC						N17			
		NC						N18			
		NC						N19			
		NC						N20			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
		NC						N22			
		NC						N23			
		NC						N24			
		NC						N25			
		NC						N26			
		NC						N27			
		NC						N28			
		NC						P10			
		NC						P12			
		NC						P13			
		NC						P14			
		NC						P15			
		NC						P17			
		NC						P18			
		NC						P19			
		NC						P20			
		NC						P22			
		NC						P24			
		NC						P26			
		NC						P27			
		NC						P28			
		NC						P30			
		NC						P31			
		NC						P9			
		NC						R10			
		NC						R12			
		NC						R13			
		NC						R14			
		NC						R26			
		NC						R27			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
		NC						R28			
		NC						R29			
		NC						R30			
		NC						R31			
		NC						R9			
		NC						T11			
		NC						T12			
		NC						T13			
		NC						T14			
		NC						T26			
		NC						T27			
		NC						T28			
		NC						T29			
		NC						U10			
		NC						U11			
		NC						U12			
		NC						U13			
		NC						U14			
		NC						U26			
		NC						U27			
		NC						U28			
		NC						U29			
		NC						U30			
		NC						U31			
		NC						U9			
		NC						V10			
		NC						V11			
		NC						V12			
		NC						V13			
		NC						V14			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	F780	B956	F1020	F1508	DQS for x16	DQS for x32	DIFFIO Speed (1)
		NC						V26			
		NC						V27			
		NC						V28			
		NC						V29			
		NC						V30			
		NC						V33			
		NC						V9			
		NC						W13			
		NC						W14			
		NC						W26			
		NC						W27			
		NC						W28			
		NC						W29			
		NC						W30			
		NC						W34			
		NC						Y13			
		NC						Y14			
		NC						Y26			
		NC						Y27			

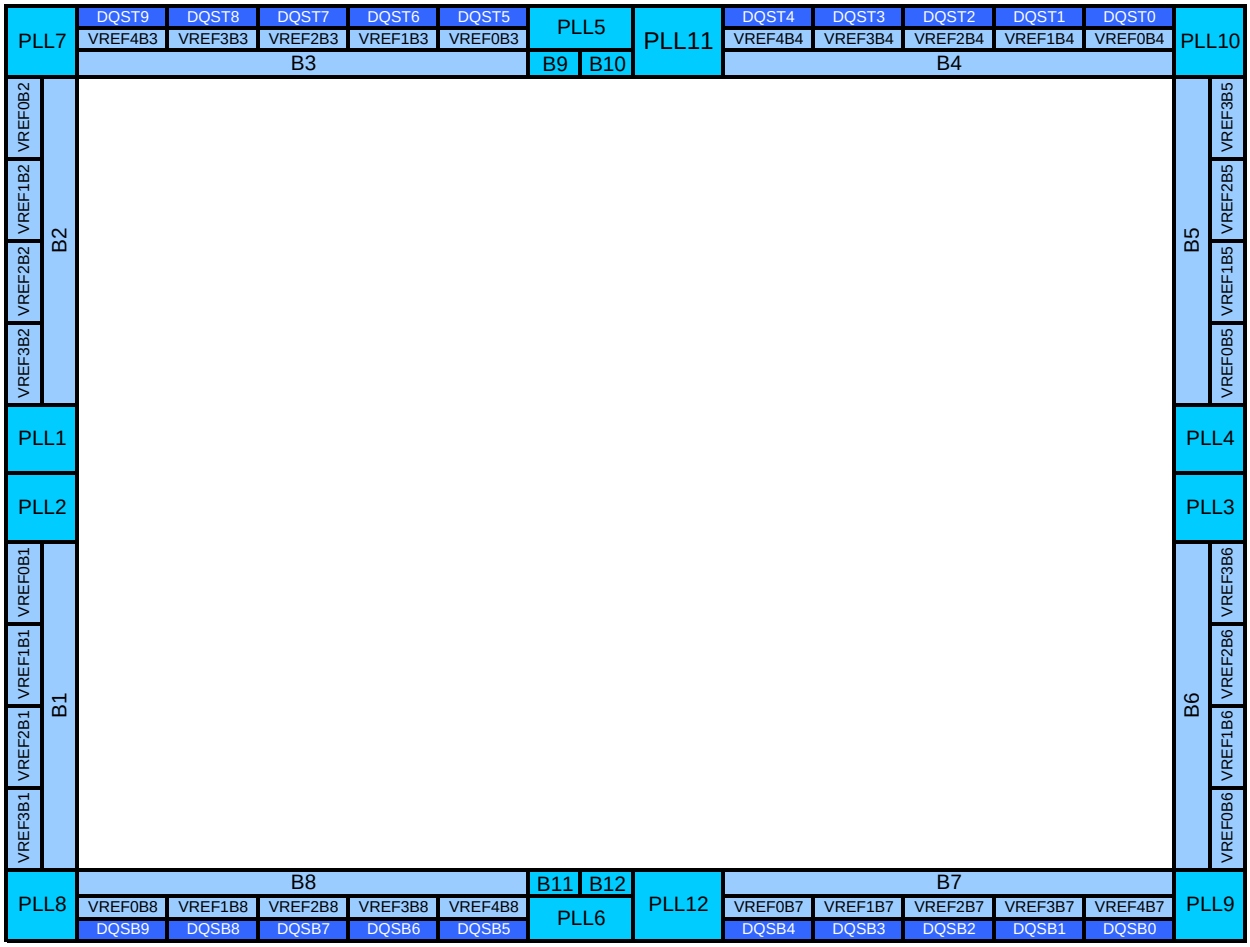
Note to Pin-List:

1) The wire bond and flip-chip packages will have different data rates for the high speed differential I/O channels. The following table shows the data rates as supported for each package.

Package	Package Type	High Speed Differential I/O Channel Performance (DIFFIO Speed)		Units
		High	Low	
F780	flip chip	840	N/A	Mbps
B956	flip chip	840	N/A	Mbps
F1020	flip chip	840	462	Mbps
F1508	flip chip	840	462	Mbps

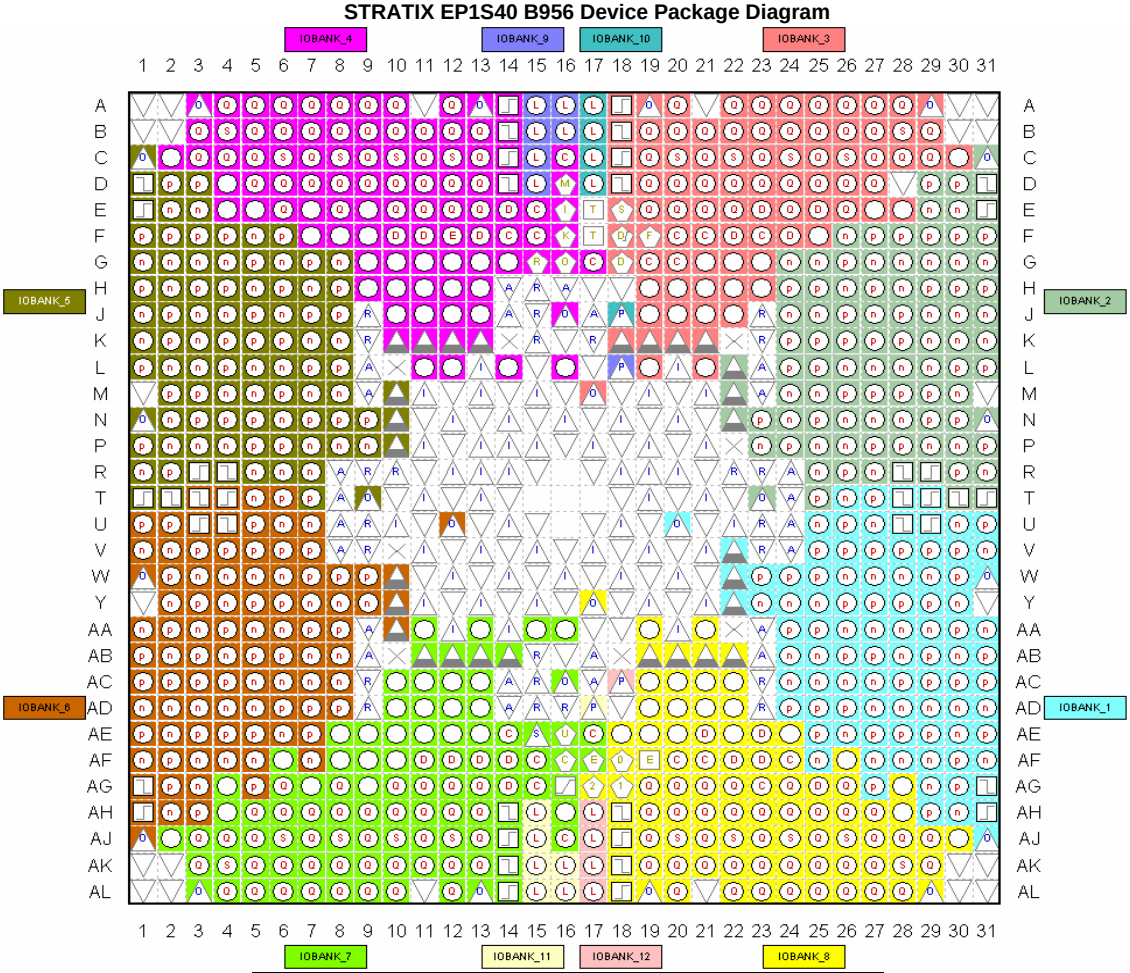
Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
		Supply and Reference Pins
VREF[1..4]B[1..8]	Input	Input reference voltage for bank 1. If a bank is used for a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for the bank. If VREF pins are not used, designers should connect them to either VCC or Gnd.
VCCIO[1..8]	Power	These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all I/O standards. VCCIO also supplies power to the input buffers used for the LVTTL, LVCMOS, 1.5-V, 1.8-V, 2.5-V, 3.3-V PCI, and 3.3-V PCI-X I/O standards.
VCCINT	Power	These are internal logic array voltage supply pins. VCCINT also supplies power to the input buffers used for the LVDS, LVPECL, 3.3-V PCML, HyperTransport™ technology, differential HSTL, GTL, GTL+, HSTL, SSTL, CTT, and 3.3-V AGP I/O standards.
VCC_PLL5_OUTA	Power	External clock output buffer power for PLL5 clock outputs PLL5_OUT[1..0]. The designer must connect this pin to the VCCIO of bank 9.
VCC_PLL5_OUTB	Power	External clock output buffer power for PLL5 clock outputs PLL5_OUT[3..2]. The designer must connect this pin to the VCCIO of bank 10.
VCC_PLL6_OUTA	Power	External clock output buffer power for PLL6 clock outputs PLL6_OUT[1..0]. The designer must connect this pin to the VCCIO of bank 11.
VCC_PLL6_OUTB	Power	External clock output buffer power for PLL6 clock outputs PLL6_OUT[3..2]. The designer must connect this pin to the VCCIO of bank 12.
VCCA_PLL[1..12]	Power	Analog power for PLLs[1..12]. The designer must connect this pin to 1.5 V, even if the PLL is not used.
GNDA_PLL[1..12]	Ground	Analog ground for PLLs[1..12]. The designer can connect this pin to the GND plane on the board.
VCCG_PLL[1..12]	Power	Guard ring power for PLLs[1..12]. The designer must connect this pin to 1.5 V, even if the PLL is not used.
GNDG_PLL[1..12]	Ground	Guard ring ground for PLLs[1..12]. The designer can connect this pin to the GND plane on the board.
NC	No Connect	Do not drive signals into these pins.
		Dedicated & Configuration/JTAG Pins
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration status pin; it is not available as a user I/O pin.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin; it is not available as a user I/O pin.
nCONFIG	Input	Dedicated configuration control input. A low transition resets the target device; a low-to-high transition begins configuration. All I/O pins tri-state when nCONFIG is driven low.
DCLK	Input	Clock input used to clock configuration data from an external source into the Stratix device. This is a dedicated pin used for configuration.
nIO_PULLUP	Input	IF nIO_PULLUP is driven high during configuration, the weak pull-ups on all user I/O pins are disabled. If driven low, the weak pull-ups are enabled during configuration. nIO_PULLUP can be pulled up to either 1.5, 1.8, 2.5, or 3.3 V.
PORSEL	Input	Dedicated input pin used to select POR delay times of 2 ms or 100 ms during powerup. When PORSEL is connected to ground, the POR time is 100 ms. When PORSEL is connected to 3.3 V, the POR time is 2 ms.
VCCSEL	Input	VCCSEL is used to select which input buffer is used on all configuration pins. VCCSEL will control whether the 3.3-/2.5-V input buffer or the 1.8-/1.5-V input buffer is used. A "0" means 3.3/2.5 V and a "1" means 1.8-/1.5 V. At powerup, VCCSEL accepts 3.3V and 2.5V TTL Levels. VCCSEL affects the following pins: TDI, TMS, TCK, TRST, MSEL0, MSEL1, MSEL2, nCONFIG, nCE, DCLK, CONF_DONE, nSTATUS, and PLL_ENA.
nCE	Input	Active-low chip enables. Dedicated chip enable input used to detect which device is active in a chain of devices. When nCE is low, the device is enabled. When nCE is high, the device is disabled.
nCEO	Output	Output that drives low when device configuration is complete. During multi-device configuration, this pin feeds a subsequent device's nCE pin.
TMS	Input	This is a dedicated JTAG input pin.
TDI	Input	This is a dedicated JTAG input pin.
TCK	Input	This is a dedicated JTAG input pin.
TDO	Output	This is a dedicated JTAG input pin.
TRST	Input	This is a dedicated JTAG input pin. Active low input, used to asynchronously reset the JTAG boundary scan circuit.
MSEL[2..0]	Input	Dedicated mode select control pins that set the configuration mode for the device.
TEMPDIODEp	Input	Pin used in conjunction with the temperature sensing diode (bias-high input) inside the Stratix device. If the temperature sensing diode is not used then connect this pin to GND.
TEMPDIODEn	Input	Pin used in conjunction with the temperature sensing diode (bias-low input) inside the Stratix device. If the temperature sensing diode is not used then connect this pin to GND.
		Clock and PLL Pins
PLL_ENA	Input	Dedicated input pin that drives the optional pllena port of all or a set of PLLs. If a PLL uses the pllena port, drive the PLL_ENA pin low to reset all PLLs including the counters to their default state. If VCCSEL = 0, then you must drive the PLL_ENA with a 3.3/2.5 V signal to enable the PLLs. If VCCSEL = 1, connect PLL_ENA to 1.8/1.5 V to enable the PLLs.
FCLK[7..0]	Bidirectional	Dedicated fast regional clock pins. FCLK pins can also be used as type input, output, or as bidirectional pins.
FPLL[10..7]CLKp	Input	Dedicated global clock inputs for fast PLLs (PLLs 7 through 10).
FPLL[10..7]CLKn	Input	Dedicated negative terminal associated with FPLL[10..7]CLKp pins.
CLK[15..0]p	Input	Dedicated global clock inputs 0 to 15.
CLK[15..0]n	I/O, Input	Optional negative terminal input for differential global clock input
PLL6_OUT[3..0]p	I/O, Output	Optional external clock outputs [3..0] from enhanced PLL 6. These pins can be differential (four output pin pairs) or single ended (eight clock outputs from PLL6).

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
PLL6_OUT[3..0]n	I/O, Output	Optional negative terminal for external clock outputs [3..0] from PLL6. If the clock outputs are single ended, then each pair of pins (i.e., PLL6_OUT0p and PLL6_OUT0n are considered one pair) can be either in phase or 180 degrees out of phase.
PLL5_OUT[3..0]p	I/O, Output	Optional external clock outputs [3..0] from enhanced PLL 5. These pins can be differential (four output pin pairs) or single ended (eight clock outputs from PLL5).
PLL5_OUT[3..0]n	I/O, Output	Optional negative terminal for external clock outputs [3..0] from PLL 5. If the clock outputs are single ended, then each pair of pins (i.e., PLL5_OUT0p and PLL5_OUT0n are considered one pair) can be either in phase or 180 degrees out of phase.
		Optional/Dual-Purpose Pins
DATA0	I/O, Input	Dual-purpose configuration data input pin. Can be used as an I/O pin after configuration is complete.
DIFFIO_TX[0..89]p/n	I/O, TX channel	Dual-purpose differential transmitter channels. These channels can be used for transmitting LVDS or HyperTransport compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFIO_RX[0..89]p/n	I/O, RX channel	Dual-purpose differential receiver channels. These channels can be used for receiving LVDS or HyperTransport compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
CLK6n, PLL12_OUT	I/O, Input (CLK6n), Output (PLL12_OUT)	This pin can be used as an I/O pin, CLK6n, as the PLL12_OUT pin. Only the EP1S40 and larger devices have this pin.
CLK13n, PLL11_OUT	I/O, Input (CLK13n), Output (PLL11_OUT)	This pin can be used as an I/O pin, CLK13n, or used as the PLL11_OUT pin. Only the EP1S40 and larger devices have this pin.
PLL5_FBp	I/O, Input	External feedback input pin for PLL5. This pin can be used as a user I/O pin if external feedback mode is not used.
PLL5_FBn	I/O, Input	Negative terminal input for external feedback input PLL5_FBp
PLL6_FBp	I/O, Input	External feedback input pin for PLL6
PLL6_FBn	I/O, Input	Negative terminal input for external feedback input PLL6_FBp
INIT_DONE	I/O, Output	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration.
DATA[7..1]	I/O, Input	Dual-purpose configuration input data pins. These pins can be used for configuration or as regular I/O pins. These pins can also be used as user I/O pins after configuration.
nRS	I/O, Input	Read strobe input pin. This pin can be used as a user I/O pin after configuration.
DEV_CLRn	I/O, Input	Optional pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as defined in the users design.
DEV_OE	I/O, Input	Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri stated; when this pin is driven high, all I/O pins behave as defined in the design.
CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. This pin can be used as a user I/O pin after configuration.
RDYnBSY	I/O, Output	Ready not busy output. A high output indicates that the target device is ready to accept another data byte. A low output indicates that the target device is not ready to receive another data byte. This pin can be used as a user I/O pin after configuration.
nCS,CS	I/O, Input	These are chip-select inputs that enable the Stratix device in the passive parallel asynchronous configuration mode. Drive nCS low and CS high to target a device for configuration. If a design requires an active high enable, use the CS pin and drive the nCS pin low. If a design requires an active low enable, use the nCS pin and drive the CS pin high. Configuration will be paused when either signal is inactive. Hold the nCS and CS pins active during configuration and initialization. The design can use these pins as user I/O pins after configuration.
nWS	I/O, Input	Active-low write strobe input to latch a byte of data on the DATA pins. This pin can be used as a user I/O pin after configuration.
PGM[2..0]	I/O, Output	These output pins control one of eight pages in the EPC16 configuration device when using remote update or local update configuration modes. When not using remote update or local update configuration modes, these pins are user I/O pins.
RUP[8..1]	I/O, Input	Reference pins for banks 8 to 1. The external precision resistors R_{UP} must be connected to the designated RUP pin on that I/O bank. If not required, these pins are regular I/O pins.
RDN[8..1]	I/O, Input	Reference pins for banks 8 to 1. The external precision resistors R_{DN} must be connected to the designated RDN pin on that I/O bank. If not required, these pins are regular I/O pins.
RUnLU	I/O, Input	Input control pin to select remote update or local update modes. If MSEL2 = 1, this is a input control pin to select remote update (RUnLU =1) or local update (RUnLU =0) modes. If MSEL2=0, the RUnLU pin is a user I/O pin.
CRC_ERROR	I/O, Output	Active high signal that indicates that the error detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error detection circuit is enabled.

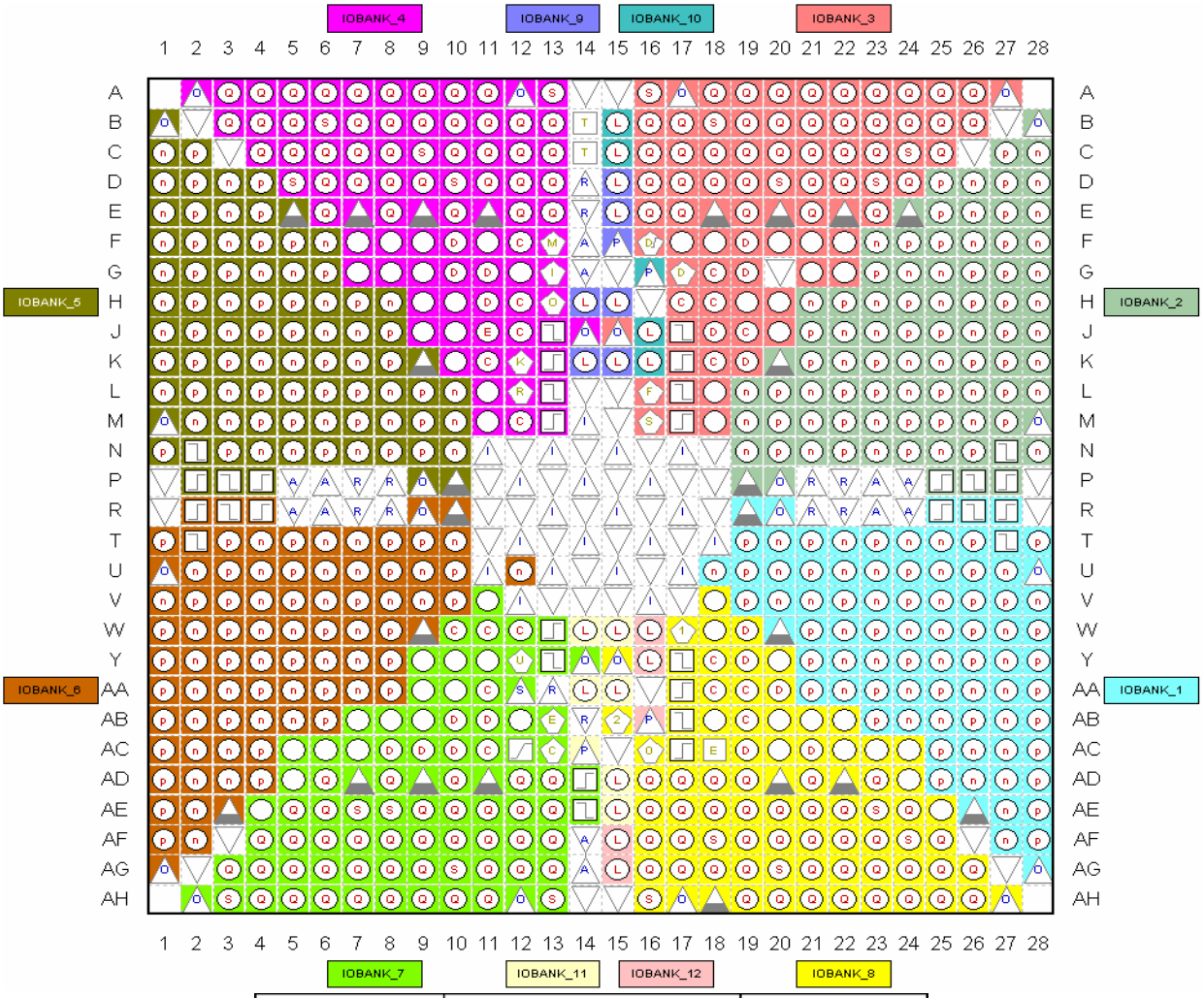


Notes:
1.This is a top view of the silicon die. For flip chip packages the die is mounted up-side down in the package.
2.This is a pictoral representation only to get an idea of placement on the device. Refer to the pin-list and the Quartus II for exact locations.

STRATIX EP1S40 B956 Device Package Diagram

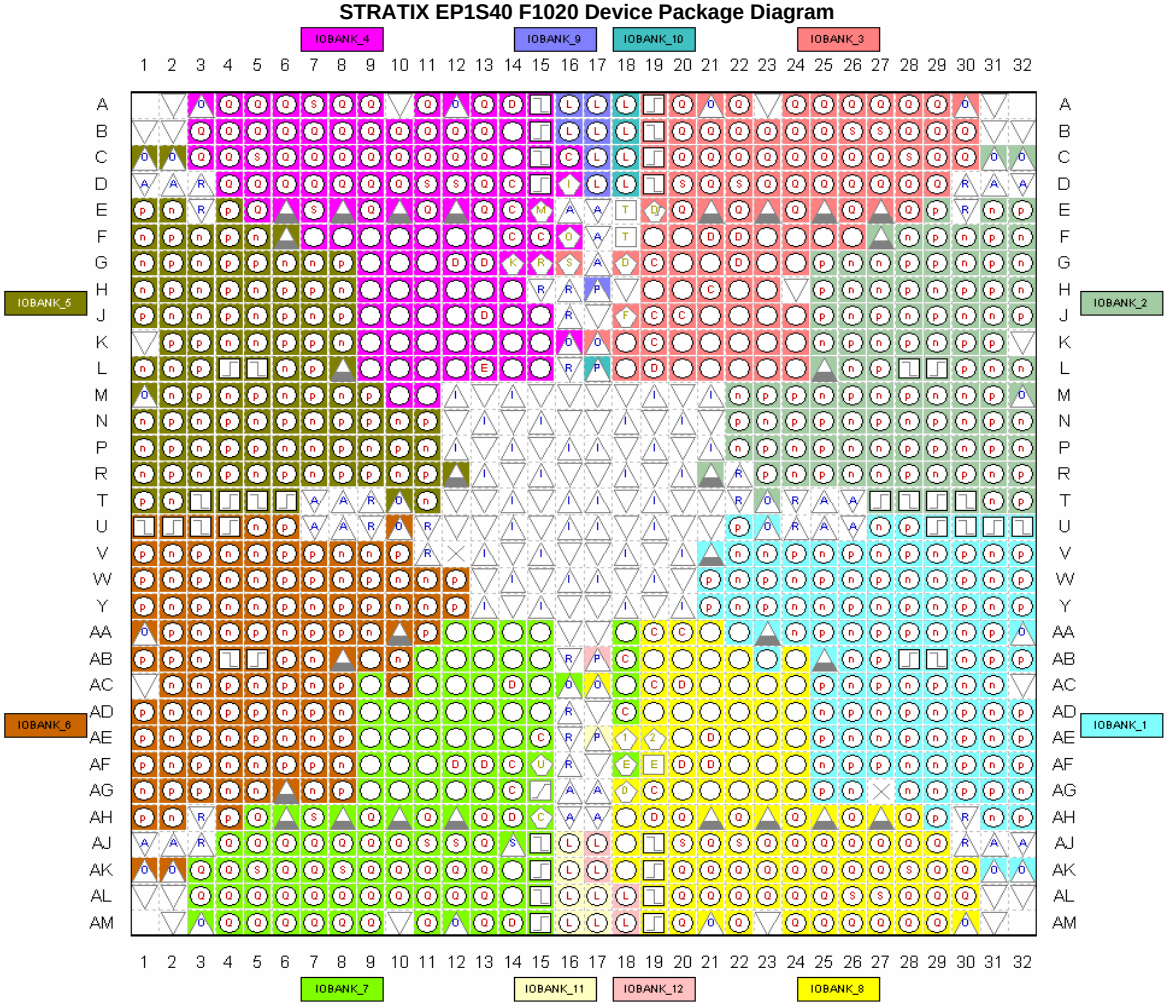


STRATIX EP1S40 F780 Device Package Diagram

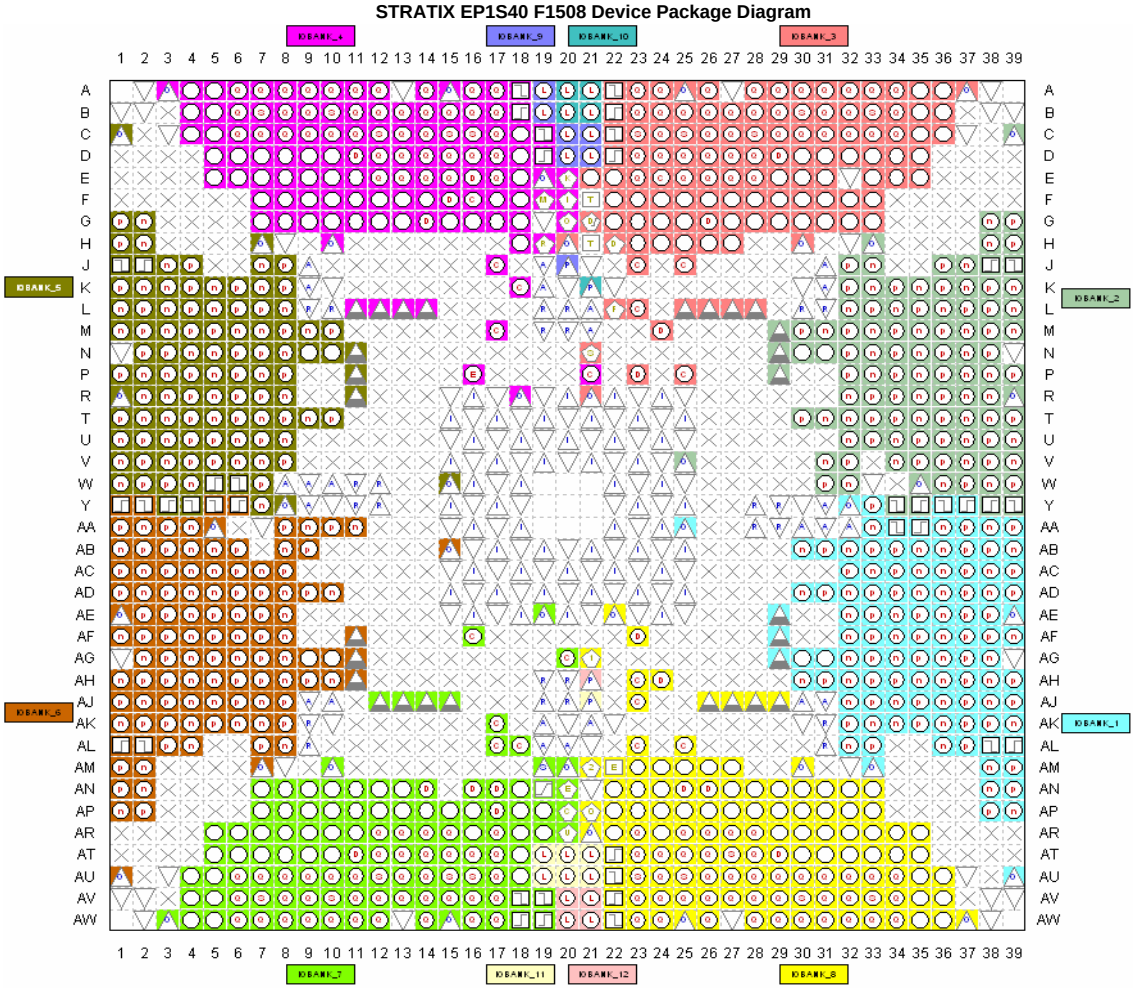


USER I/O PINS	DEDICATED PINS		POWER / GROUND PINS
USER IOs	CLK_p	nCEO	VCCA_PLL
DUAL PURPOSE PINS	CLK_n	nCE	VCCINT
OTHER CONFIGURATION	PORSEL	nCONFIG	VCCIO
DEV_OE	PLL_ENA	TDI	VCC_PLL_OUT
DIFF_n	TEMPDIODE	TCK	VCCG_PLL
DIFF_p	MSEL0	TMS	VCCSEL
DQ	MSEL1	TDO	VREF
DQS	MSEL2	TRST	GND
OTHER PLL	CONF_DONE	nSTATUS	GNDA_PLL
OTHER DUAL-PURPOSE	DCLK	nIO_PULLUP	GNDG_PLL
NO CONNECT			

STRATIX EP1S40 F1020 Device Package Diagram



STRATIX EP1S40 F1508 Device Package Diagram



USER I/O PINS	DEDICATED PINS		POWER / GROUND PINS
USER IOs	CLK_p	nCEO	VCCA_PLL
DUAL PURPOSE PINS	CLK_n	nCE	VCCINT
OTHER CONFIGURATION	PORSEL	nCONFIG	VCCIO
DEV_OE	PLL_ENA	TDI	VCC_PLL_OUT
DIFF_n	TEMPDIODE	TCK	VCCG_PLL
DIFF_p	MSEL0	TMS	VCCSEL
DQ	MSEL1	TDO	VREF
DQS	MSEL2	TRST	GND
OTHER PLL	CONF_DONE	nSTATUS	GNDA_PLL
OTHER DUAL-PURPOSE	DCLK	nIO_PULLUP	GNDG_PLL
NO CONNECT			

Clock Resources for High Speed Differential I/O (DIFFIO) Receiver and Transmitter channels. *Notes (5), (7)*										
Device	**Pin Count**	**Source FAST PLL**	**Rx Channels** ***Note (1)***		**Tx channels** ***Note (2)***		**Overlapped Rx Channels** ***Note (3)***		**Overlapped Tx Channels** ***Note (4)***	
			High *(6)*	**Low *(6)***	**High *(6)***	**Low *(6)***	**High *(6)***	**Low *(6)***	**High *(6)***	**Low *(6)***
EP1S40	780	PLL1	[23-39]	-	[25-42]	-	-	-	-	-
		PLL2	[7-22]	-	[4-19]	-	-	-	-	-
		PLL3	[67-82]	-	[70-85]	-	-	-	-	-
		PLL4	[50-66]	-	[47-64]	-	-	-	-	-
		PLL7	*(8)*	*(8)*	*(8)*	*(8)*	*(8)*	*(8)*	*(8)*	*(8)*
		PLL8	*(8)*	*(8)*	*(8)*	*(8)*	*(8)*	*(8)*	*(8)*	*(8)*
		PLL9	*(8)*	*(8)*	*(8)*	*(8)*	*(8)*	*(8)*	*(8)*	*(8)*
		PLL10	*(8)*	*(8)*	*(8)*	*(8)*	*(8)*	*(8)*	*(8)*	*(8)*
	956	PLL1	[23-42]	-	[25-42]	-	[25-42]	-	[25-42]	-
		PLL2	[3-22]	-	[3-19]	-	[3-19]	-	[3-19]	-
		PLL3	[67-86]	-	[70-86]	-	[70-86]	-	[70-86]	-
		PLL4	[47-66]	-	[47-64]	-	[47-64]	-	[47-64]	-
		PLL7	[25-42]	-	[25-44]	-	[25-42]	-	[25-42]	-
		PLL8	[3-19]	-	[0-19]	-	[3-19]	-	[3-19]	-
		PLL9	[70-86]	-	[70-89]	-	[70-86]	-	[70-86]	-
		PLL10	[47-64]	-	[45-64]	-	[47-64]	-	[47-64]	-
	1020	PLL1	[23-42]	-	[25-42]	[23-24]	[25-42]	-	[25-42]	-
		PLL2	[3-22]	-	[3-19]	[65-66]	[3-19]	-	[3-19]	-
		PLL3	[67-86]	-	[70-86]	[20-22]	[70-86]	-	[70-86]	-
		PLL4	[47-66]	-	[47-64]	[67-69]	[47-64]	-	[47-64]	-
		PLL7	[25-42]	[43-44]	[25-44]	-	[25-42]	-	[25-42]	-
		PLL8	[3-19]	[0-2]	[0-19]	-	[3-19]	-	[3-19]	-
		PLL9	[70-86]	[87-89]	[70-89]	-	[70-86]	-	[70-86]	-
		PLL10	[47-64]	[45-46]	[45-64]	-	[47-64]	-	[47-64]	-
	1508	PLL1	[23-42]	-	[25-42]	[23-24]	[25-42]	-	[25-42]	-
		PLL2	[3-22]	-	[3-19]	[65-66]	[3-19]	-	[3-19]	-
		PLL3	[67-86]	-	[70-86]	[20-22]	[70-86]	-	[70-86]	-

		PLL4	[47-66]	-	[47-64]	[67-69]	[47-64]	-	[47-64]	-
		PLL7	[25-42]	[43-44]	[25-44]	-	[25-42]	-	[25-42]	-
		PLL8	[3-19]	[0-2]	[0-19]	-	[3-19]	-	[3-19]	-
		PLL9	[70-86]	[87-89]	[70-89]	-	[70-86]	-	[70-86]	-
		PLL10	[47-64]	[45-46]	[45-64]	-	[47-64]	-	[47-64]	-

Notes:
1. These Rx channels can be clocked by the PLL listed in the "FAST PLL Source location" column.
2. These Tx channels can be clocked by the PLL listed in the "FAST PLL Source location" column.
3. These Rx channels can be driven by the PLL listed in the "FAST PLL Source location" or alternatively be driven by the other adjacent FAST PLL. See the PLL & Bank Diagram for PLL locations.
4. These Tx channels can be driven by the PLL listed in the "FAST PLL Source location" or alternatively be driven by the other adjacent FAST PLL. See the PLL & Bank Diagram for PLL locations.
5. Each range of channel numbers are shown in [ ] brackets.
6. Data channels designated as "high" speed support a maximum data rate of 840 Mbps for -5 and -6 speed grade devices and 624 Mbps for -7 speed grade devices. Data channels designated as "low" speed support a maximum data rate of 462 Mbps for all speed grades.
7. The high speed differential I/O (DIFFIO) channels span across two banks on both sides of the device. Each Fast PLL can normally only feed channels in one bank. However, the center PLLs can also clock the channels associated with the adjacent center PLL on the same side of the device through a mux that is shown in figures 5-16 and 5-17 in volume 2 of the Stratix Device Handbook. These channels are called "cross-bank" channels. When cross-bank channels are used only one center PLL on each side can be used.
8. PLLs 7, 8, 9, and 10 are not available for the EP1S30 and EP1S40 devices in the F780 package.

Version Number	Date	Changes Made
3.4	2/4/2005	Revised package diagrams.
3.5	11/14/2005	Update all package diagram for EP1S40.
3.6	3/2/2006	Added CRC_ERROR pin in Pin List and Pin Definition