Intel® 600 Series Chipset Family Platform Controller Hub (PCH)

Specification Update

Revision 007

July 2023

Document Number: 681906

Contents

Tables

Revision History

Revision Number	Description	Revision Date
001	• Initial release	October 2021
002	• Added Specification Changes: GPP_S Group Internal Pull-up/Pull-down Value Support • Updated Errata: 004	January 2022
003	• Added Errata: 010, 011, 012, 013, 014, 015, 016 • Updated Errata: 004	July 2022
004	• Added Errata: 017	January 2023
005	• Added Desktop Intel® IOTG Embedded Chipset R680E, Q670E and H610E, Mobile Intel® Chipset WM690 and HM670 identification • Added Errata: 018	May 2023
006	• Added Errata: 019	June 2023
007	• Added Errata: 020 and 021	July 2023

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1 Preface

This document is an update to the specifications contained in the documents listed in the following Affected Documents table. This document is a compilation of device and document errata and specification clarifications and changes. It is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into the specification update and are no longer published in other documents. This document may also contain information that has not been previously published.

1.1 Affected Documents

Document Title	Document Number
Intel® 600 Series Chipset Family Platform Controller Hub (PCH) Datasheet, Volume 1 of 2	648364
Intel® 600 Series Chipset Family Platform Controller Hub (PCH) Datasheet, Volume 2 of 2	680836
12th Gen Intel® Core™ Processors Family (Formerly Known as Alder Lake -S) for IoT Platforms Datasheet Addendum	710371

1.2 Nomenclature

Errata are design defects or errors. Errata may cause the behavior of the PCH to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present in all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

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2 Identification Information

2.1 Marking

Table 2-1. PCH Lines Component Identification

PCH Stepping	Top Marking (S-Spec)	Notes
B1	SRKZW	Desktop Intel® Chipset H610
B1	SRKZX	Desktop Intel® Chipset B660
B1	SRKZY	Desktop Intel® Chipset H670
B1	SRL01	Desktop Intel® Chipset Q670
B1	SRKZZ	Desktop Intel® Chipset Z690
B1	SRL00	Entry Workstation Intel® Chipset W680
B1	SRL02	Workstation Intel® Chipset W790
B1	SRL2S	Desktop Intel® IOTG Embedded Chipset R680E
B1	SRL2R	Desktop Intel® IOTG Embedded Chipset Q670E
B1	SRL2T	Desktop Intel® IOTG Embedded Chipset H610E
B1	SRL2Z	Mobile Intel® Chipset WM690
B1	SRL2Y	Mobile Intel® Chipset HM670

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3 Summary Tables of Changes

The following tables indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes, which apply to the product. Intel may fix some of the errata in a future stepping of the component and account for the other outstanding issues through documentation or specification changes as noted. These tables use the following notations:

3.1 Codes Used in Summary Table

Stepping	Description
X	Erratum exists in the stepping indicated. Specification Change that applies to the stepping indicated.
(No mark) or (Blank Box)	This erratum is fixed or not applicable in listed stepping or Specification Change does not apply to listed stepping.

Status	Description
Doc	Document change or update that is implemented.
Planned Fix	This erratum may be fixed in a future stepping of the product.
Fixed	This erratum has been previously fixed in Intel® hardware, firmware, or software.
No Fix	There are no plans to fix this erratum.

3.2 Errata Summary Table

Erratum ID	Stepping	Errata
	B1	
001	No Fix	SATA Enclosure Management LED Messaging
002	No Fix	eSPI SBLCL Register Bit Not Cleared by PLTRST#
003	No Fix	PCIe Clock and PCIe Reference Clock to Processor Maximum Rising/Falling Edge Rate and VCROSS
004	No Fix	USB Audio Offload Traffic with Full-Speed Device Behind Hub

Erratum ID	Stepping	Errata
	B1	
005	No Fix	Integrated GbE Controller Reset on D3 Exit
006	No Fix	xHCI Link Protocol Field Value - USB 3.2 Gen 1x2 and 2x2
007	No Fix	xHCI Force Header Command Incorrect Return Code
008	No Fix	USB VTIO Device Capabilities Field Length
009	No Fix	SLP_A# Minimum Assertion Width Timer During G3 Exit
010	Fixed	USB 2.0 Device Interrupt IN Endpoint Split Transaction Error
011	Fixed	System Hang During G3 Exit Following RTC Reset
012	No Fix	xHCI Dropped ACK Packet after Upstream Truncated Packet with DPPABORT OS
013	No Fix	Processor C-States with USB Full-speed or Low-speed Device Hotplug
014	No Fix	Timed GPIO Event May Have a Mismatched Time Stamp
015	No Fix	USB 3.2 Gen 1x1 Port Does Not Send 16 Polling LFPS Burst
016	Fixed	USB 3.2 Device Re-enumeration with USB 2.0 DCI.DBC Enabled
017	No Fix	USB 2.0 Full-speed Device Enumeration With Certain Cables
018	No Fix	Precision Time Measurement (PTM) Interpretation Capability Bit Incorrect Register Offset
019	No Fix	eSPI_CS1#, eSPI_CS2#, and eSPI_CS3# Floating Following Initial eSPI Reset Deassertion
020	Fixed	USB Low-Speed or Full-Speed Device Enumeration Failures During Hot-Plug
021	Fixed	DMI Receiver PHY Adjustment Framing Errors

3.3 Specification Changes

No.	Specification Changes
1	GPP_S Group Internal Pull-up/Pull-down Value Support

3.4 Specification Clarifications

No.	Specification Clarifications
	No specification clarifications for this revision of the specification update.

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4 Errata Details

001	**SATA Enclosure Management LED Messaging**
Problem	When sending a SATA enclosure LED message and all SATA ports are either idle or disabled, the PCH may not transmit the LED message due to an internal clock gating issue.
Implication	The LED status for SATA enclosure may be incorrect.
Workaround	None identified. Enclosure Management SW can poll the Enclosure Management (EM_CTL) - Offset 20h bit 8 register for a 0 value immediately before writing LED messages.
Status	For the steppings affected, refer to the Summary Table of Changes.

002	**eSPI SBLCL Register Bit Not Cleared by PLTRST#**
Problem	The IOSF-SB eSPI Link Configuration Lock (SBLCL) bit (offset 4000h, bit 27 in eSPI PCR space) is reset by RSMRST# assertion instead of PLTRST# assertion.
Implication	If the SBLCL bit is set to 1, software will not be able to access the eSPI device Capabilities and Configuration register in the reserved address range (0h - 7FFh) until RSMRST# asserts.
Workaround	If software needs to access the eSPI device reserved range 0h - 7FFh while SBLCL bit is set to 1, a RSMRST# assertion should be performed.
Status	For the steppings affected, refer to the Summary Table of Changes.

003	**PCIe Clock and PCIe Reference Clock to Processor Maximum Rising/Falling Edge Rate and VCROSS**
Problem	The PCIe Clock Output signals (CLKOUT_PCIE_P/N) and PCIe reference clock signals to processor (CLKOUT_CPUPCIBCLK_P/N) may not meet the maximum Rising/Falling Edge Rate and VCROSS specifications as defined in the PCI Express Card Electromechanical Specification Revision 3.0, section 2.1.3, REFCLK AC Specifications.
Implication	There are no known functional failures due to this erratum.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

004	**USB Audio Offload Traffic with Full-Speed Device Behind Hub**
Problem	If USB audio offload is enabled for a USB Full-Speed Isochronous audio device connected behind a USB 2.0 or later hub and there is an active concurrent bulk transfer to another device on any port of the xHCI controller or behind the hub, the controller may stall the offloaded audio traffic and a split transaction error may occur.
Implication	The USB audio offload playback may stop. Audio may be recovered if the audio stream is paused and restarted, the audio device is removed and reconnected, or the audio application is restarted.

Workaround	None identified. A mitigation for this erratum is available with a combination of Microsoft Windows 11 OS Release and Intel® Smart Sound Technology version 10.29.00.5574 or later. This mitigation will disable audio offload functionality for USB audio devices connected behind a hub.
Status	For the steppings affected, refer to the Summary Table of Changes.

005	**Integrated GbE Controller Reset on D3 Exit**
Problem	Upon GbE controller D3 exit, the GbE host driver performs a controller reset. During this reset, software accesses to the GbE MMIO registers may not complete.
Implication	The system may hang. Note: This erratum has only been observed in a synthetic environment.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

006	**xHCI Link Protocol Field Value - USB 3.2 Gen 1x2 and 2x2**
Problem	The xHCI Host Controller reports the value of 0h for the Link Protocol (LP) bits [15:14] in register XECP_SUPP_USB3_6 (MMIO offset 8038h) and XECP_SUPP_USB3_7 (MMIO offset 803Ch), which does not meet the xHCI specification revision 1.2.
Implication	There are no known functional failures due to this erratum.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

007	**xHCI Force Header Command Incorrect Return Code**
Problem	The xHCI controller does not return the correct completion code for the Force Header Command as defined in the Section 4.6.16 of the eXtensible Host Controller Interface for Universal Serial Bus (xHCI) Requirements Specification Rev 1.2.
Implication	xHCI CV TD4.12 - Force Header Command Test may report an error. Intel has obtained a waiver for TD 4.12. The Force Header Command is only used by the USB-IF Command Verifier (xHCI CV) tool for device testing. There are no known functional failures due to this erratum.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

008	**USB VTIO Device Capabilities Field Length**
Problem	The xHCI spec version 1.2 defines the PCI Express Capability structure offset 04h Device Capabilities (DVSEC) field to be 8 bytes. The USB Virtualization Based Trusted IO (VTIO) Management controller implements the DVSEC field as 12 bytes.
Implication	An USB controller driver may not be able to enable the USB VTIO controller.
Workaround	None identified. To mitigate this erratum, an Independent Software Vendor could account for the field length in the USB controller driver.

Status	For the steppings affected, refer to the Summary Table of Changes.

009	**SLP_A# Minimum Assertion Width Timer During G3 Exit**
Problem	Setting the Disable SLP_X Stretching After SUS Well Power Up (DIS_SLP_X_STRCH_SUS_UP) bit (offset 1020h, bit 12 in PMC_MMIO space) to 1 does not disable the SLP_A# Minimum Assertion Width (SLP_A_MIN_ASST_WDTH) timer (offset 1020h, bit 17 and 16 in PMC_MMIO space).
Implication	G3 exit duration may be extended by the value programmed in the SLP_A_MIN_ASST_WDTH register.
Workaround	None identified. To mitigate the issue for platforms that do not require SLP_A# stretching, BIOS should program SLP_A_MIN_ASST_WDTH to 0.
Status	For the steppings affected, refer to the Summary Table of Changes.

010	**USB 2.0 Device Interrupt IN Endpoint Split Transaction Error**
Problem	When a USB Full-speed or Low-speed (with an Interrupt IN Endpoint) device is connected behind a USB hub and a USB bulk device is also connected to any port on the xHCI controller, a split transaction error may occur on the USB Full-speed or Low-speed device.
Implication	The USB Controller driver may reset the USB Full-speed or Low-speed Interrupt IN Endpoint. The observed behavior is USB device specific. For example, a delay in response may be observed from a Low-speed USB mouse or keyboard device.
Workaround	A BIOS code change has been identified and may be implemented as a workaround for this erratum. For a more power optimized solution, a xHCI controller driver may dynamically clear the xHCI MMIO offset 0x8144 bit 8 when a USB Full-speed or Low-speed device is not connected behind a USB Hub and ensure the bit is set as configured by the BIOS.
Status	For the steppings affected, refer to the Summary Table of Changes.

011	**System Hang During G3 Exit Following RTC Reset**
Problem	Following a RTC Reset the PCH debug subsystem may enter an unsupported state if Delayed Authentication Mode (DAM) and DCI are disabled. Note: This issue may be observed only from PMC version 160.02.00.1029 to 160.02.00.1031.
Implication	The system may hang while exiting G3 and requires reflashing the system IFWI to recover.
Workaround	A BIOS code change has been identified and may be implemented as a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

012	**xHCI Dropped ACK Packet after Upstream Truncated Packet with DPPABORT OS**
Problem	If a USB 3.2 Gen 1x1 hub sends an upstream truncated packet with DPPABORT OS (Data Packet Payload Abort Order Set) framing followed by an ACK packet for a previous OUT transfer from the xHCI controller, the ACK packet may be dropped by the xHCI controller.
Implication	A timeout may be observed for the OUT transfer packet. Per the xHCI spec, a xHCI controller driver will issue a warm port reset to the device causing a device re-enumeration.

Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

013	**Processor C-States with USB Full-speed or Low-speed Device Hotplug**
Problem	When doing a hotplug on a USB hub with two or more USB Full-speed or Low-speed devices each with a 1 ms service interval interrupt endpoint, a race condition may occur between the PMC and the xHCI controller.
Implication	The processor may fail to enter C3 or deeper package C-States. Note: This erratum has only been observed in a synthetic environment.
Workaround	None identified. This condition is recovered after the xHCI controller has successfully entered D3.
Status	For the steppings affected, refer to the Summary Table of Changes.

014	**Timed GPIO Event May Have a Mismatched Time Stamp**
Problem	When a Timed GPIO event is counted in the Event Counter Capture (TGPIOECCV) register (offset 1238h, bits 31 to 0 in PWRMBASE space), the Time Capture (TGPIOTCV) register (offset 1230h, bits 31 to 0 in PWRMBASE space) value is not immediately updated after that event is counted.
Implication	A Timed GPIO event may have a mismatched time stamp.
Workaround	None identified. A Timed GPIO driver can partially mitigate for this erratum by detecting that a TGPIOECCV register change has occurred without a TGPIOTCV register change and then repeatedly re-read the TGPIOTCV register until a change does occur.
Status	For the steppings affected, refer to the Summary Table of Changes.

015	**USB 3.2 Gen 1x1 Port Does Not Send 16 Polling LFPS Burst**
Problem	On USB 3.2 Gen 1x1 only capable ports, including ports configured as USB 3.2 Gen 1x1 by soft strap, the xHCI controller may send only 15 LFPS signals instead of a burst of 16 LFPS signals as specified by the USB 3.2 specification.
Implication	There are no known functional implications due to this erratum. LFPS handshake requires the receiver link partner to only detect 2 LFPS signals. This issue may impact the SuperSpeed compliance test case which checks for the 16 LFPS burst requirements: TD6.4, TD6.5, and TD7.31.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

016	**USB 3.2 Device Re-enumeration with USB 2.0 DCI.DBC Enabled**
Problem	When USB 2.0 DCI.DBC is enabled and the DCI.DBC connection is established, a race condition may prevent the xHCI controller from correctly exiting the U1 or U2 link state.
Implication	A USB 3.2 device may get re-enumerated if the USB device initiates a U1 or U2 link state exit.

Workaround	A BIOS code change has been identified and may be implemented as a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

017	**USB 2.0 Full-speed Device Enumeration With Certain Cables**
Problem	The xHCI controller may not complete the detection of the End of Packet Single Ended 0 (EOP SE0) when a USB Full-speed device is connected through a USB 2.0 cable that has a connector-to-connector propagation delay greater than 15.6 ns.
Implication	Due to this erratum, the USB 2.0 Full-speed device may fail to enumerate.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

018	**Precision Time Measurement (PTM) Interpretation Capability Bit Incorrect Register Offset**
Problem	The PTM Propagation Delay Adaptation Interpretation B (PTMPDAIB) Bit is implemented at Configuration Space (CFG) Offset 158h instead of at 50h as documented in the PCI-SIG PTM Byte Ordering Adaptation Engineering Change Notice (ECN).
Implication	Due to this erratum, End Point Device (EPD) software that implements the PTM Byte Ordering Adaptation ECN will not be able to program their PTMPDAIB Bit correctly since it is located at a different register offset.
Workaround	None identified. To mitigate this issue, EPD software that implements the PTM Byte Ordering Adaptation ECN must access PTMPDAIB at CFG Offset 158h.
Status	For the steppings affected, refer to the Summary Table of Changes.

019	**ESPI_CS1#, ESPI_CS2#, and ESPI_CS3# Floating Following Initial eSPI Reset Deassertion**
Problem	During Deep Sx exit or booting from G3 state, ESPI_CS1#, ESPI_CS2#, and ESPI_CS3# are momentarily high impedance and may float low following the initial ESPI_RESET# deassertion.
Implication	Due to this erratum, unexpected system behavior may occur on systems with more than one eSPI device.
Workaround	Implement 10 kohm external pull-up resistors to the VCCPRIM_1P8 voltage rail on ESPI_CS1#, ESPI_CS2#, and ESPI_CS3#.
Status	For the steppings affected, refer to the Summary Table of Changes.

020	**USB Low-Speed or Full-Speed Device Enumeration Failures During Hot-Plug**
Problem	During the hot-plug of a USB 2.0 hub with Low-Speed or Full-Speed device connected behind the hub, a split transaction error may occur during the enumeration of the USB Low-Speed or Full-Speed device.
Implication	Due to this erratum, the USB Low-Speed or Full-Speed device may fail to enumerate when connected to the USB 2.0 hub. This condition is recovered after the xHCI controller has been reset (for example, software setting the xHCI Host Controller Reset (HCRST) bit or by performing a power button override).
Workaround	A BIOS code change has been identified and may be implemented as a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

021	**DMI Receiver PHY Adjustment Framing Errors**
Problem	During increased DMI traffic PCH DMI framing errors may occur due to Receiver Variable Gain Amplifier (VGA) PHY adjustments.
Implication	Due to this erratum, the system may hang with an Internal Timeout Error Machine Check (MCACOD 04A5h or 0402h).
Workaround	A BIOS code change has been identified and may be implemented as a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

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5 Specification Changes

1. GPP_S Group Internal Pull-up/Pull-down Value Support

The GPP_S group only supports 5 kohm internal pull-up/pull-down programmed via the corresponding GPIO TERM bits, instead of 20 kohm pull-up/pull-down as documented.

The TERM register bit description for GPP_S group in the Intel® 600 Series Chipset Family Platform Controller Hub (PCH) Datasheet Volume 2 of 2 (#680836) already reflected the 5 kohm pull-up/pull-down support.

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6 Specification Clarification

There are no specification clarifications for this revision of the Specification Update.

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