12th Generation Intel® Core™ Processor

Specification Update

Supporting 12th Generation Intel® Core™ Processor for S, H, U, P, and HX Processor Line Platforms, formerly known as Alder Lake

Revision 025

April 2024

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Revision History

Revision	Description	Revision Date
001	• Initial Release	October 2021
002	• Added Errata: ADL025, ADL026	December 2021
003	• Added Errata: ADL027, ADL028, ADL029 • Removed Errata: ADL011, ADL022	January 2022
004	• Added Errata: ADL030, ADL031, ADL032, ADL033, ADL034 • Added H Processor Line	February 2022
005	• Added Errata: ADL035, ADL036, ADL037	March 2022
006	• Added Erratum: ADL038 • Added P and U Processor Lines	April 2022
007	• Added Errata: ADL039, ADL040, ADL041, ADL042	May 2022
008	• Added HX Processor Line • Updated Erratum: ADL029	June 2022
009	• Added Errata: ADL043, ADL044, ADL045	July 2022
010	• Added Errata: ADL046, ADL047 • Removed Erratum: ADL003	September 2022
011	• Added Errata: ADL048, ADL049	November 2022
012	• Added Errata: ADL050, ADL051	January 2023
013	• Added Erratum: ADL052	March 2023
014	• Added Erratum: ADL053	April 2023
015	• Added Errata: ADL054, ADL055	May 2023
016	• Added Erratum: ADL056	June 2023
017	• Added Errata: ADL057, ADL058, ADL059	July 2023
018	• Added Errata: ADL060, ADL061, ADL062, ADL063	August 2023
019	• Added Erratum: ADL064 • Updated Errata: ADL060, ADL062, ADL063	September 2023
020	• Added Erratum: ADL065	October 2023
021	• Added Erratum: ADL066	November 2023
022	• Added Erratum: ADL067	December 2023
023	• Added Erratum: ADL068, ADL069	January 2024
024	• Added Erratum: ADL070	March 2024
025	• Added Errata: ADL071, ADL072, ADL073	April 2024

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1 Preface

This document is an update to the specifications contained in the documents listed in the following Affected Documents/Related Documents table. It is a compilation of device and document errata and specification clarifications and changes, and is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this updated document and are no longer published in other documents. This document may also contain information that has not been previously published.

1.1 Affected Documents

Document Title	Document Number
12th Generation Intel® Core™ Processors Datasheet, Volume 1 of 2	655258
12th Generation Intel® Core™ Processors Datasheet, Volume 2 of 2	655259

1.2 Related Documents

Document Title	Document Number/Location
AP-485, Intel® Processor Identification and the CPUID Instruction	http://www.intel.com/design/processor/applnots/241618.htm
Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 1: Basic Architecture Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 2A: Instruction Set Reference Manual A-M Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 2B: Instruction Set Reference Manual N-Z Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3A: System Programming Guide Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3B: System Programming Guide Intel® 64 and IA-32 Intel® Architecture Optimization Reference Manual	http://www.intel.com/products/processor/manuals/index.htm
Intel® 64 and IA-32 Architectures Software Developer's Manual Documentation Changes	http://www.intel.com/content/www/us/en/processors/architectures-software-developer-manuals.html
Intel® Virtualization Technology Specification for Directed I/O Architecture Specification	D51397-001
ACPI Specifications	www.acpi.info

1.3 Nomenclature

Errata – These are design defects or errors. Errata may cause the processor's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes – These are modifications to the current published specifications. These changes is incorporated in the next release of the specifications.

Specification Clarifications – This describe a specification in greater detail or further highlight a specifications impact to a complex design situation. These clarifications is incorporated in the next release of the specifications.

Documentation Changes – This include typos, errors, or omissions from the current published specifications. These changes are incorporated in the next release of the specifications.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications, and documentation changes are removed from the specification update, when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

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2 Identification Information

2.1 Component Identification via Programming Interface

The processor stepping is identified by the following register contents:

Table 1. Processor Lines Component Identification

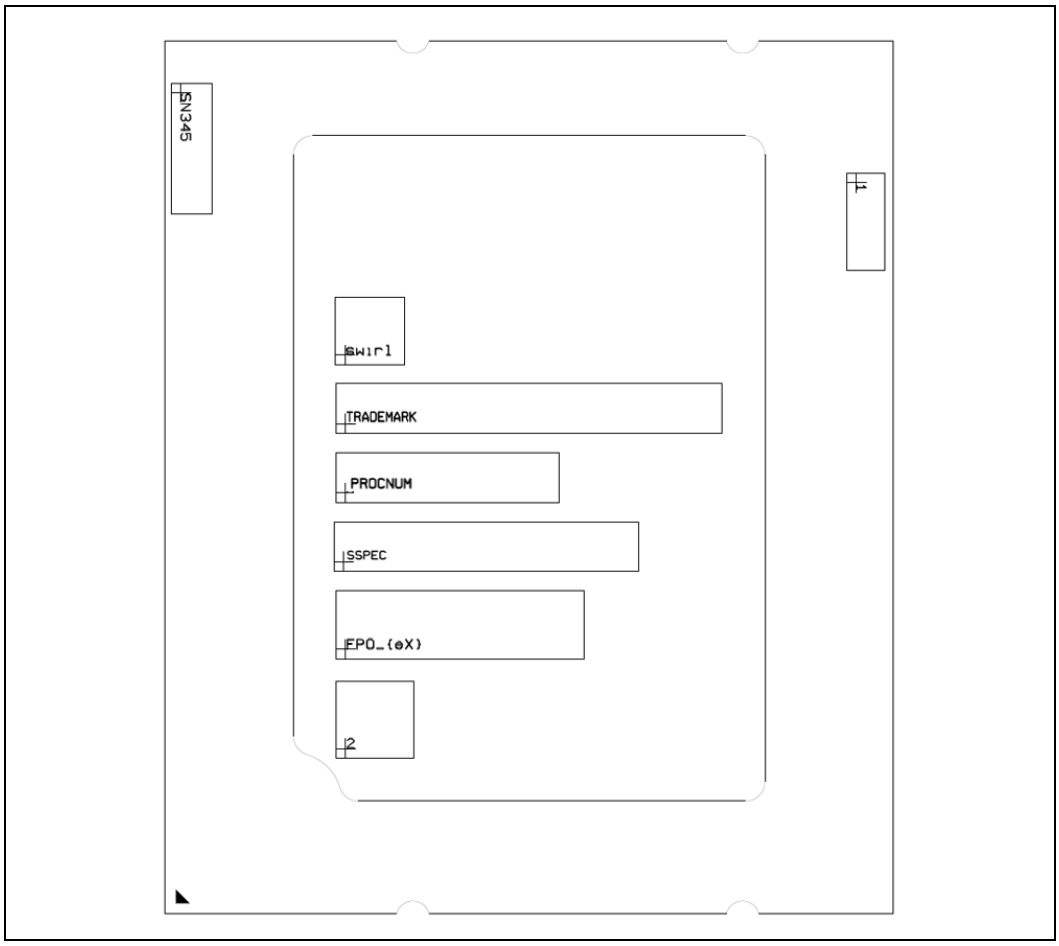
Processor	CPUID	Reserved [31:28]	Extended Family [27:20]	Extended Model [19:16]	Reserved [15:14]	Processor Type [13:12]	Family Code [11:8]	Model Number [7:4]	Stepping ID [3:0]
ADL-S 8+8 ADL-HX 8+8	0x90672	Reserved	0000000b	1001b	Reserved	00b	0110b	0111b	0010b
ADL-S 6+0	0x90675	Reserved	0000000b	1001b	Reserved	00b	0110b	0111b	0101b
ADL-H 6+8 ADL-P 6+8	0x906A3	Reserved	0000000b	1001b	Reserved	00b	0110b	1010b	0011b
ADL-U15W 2+8 ADL-U9W 2+8	0x906A4	Reserved	0000000b	1001b	Reserved	00b	0110b	1010b	0100b

1. The Extended Family, Bits [27:20] are used in conjunction with the Family Code, specified in Bits[11:8], to indicate whether the processor belongs to the Celeron®, Pentium®, or Intel® Core™ processor family.
2. The Extended Model, Bits [19:16] in conjunction with the Model Number, specified in Bits [7:4], are used to identify the model of the processor within the processor's family.
3. The Family Code corresponds to Bits [11:8] of the EDX register after RESET, Bits [11:8] of the EAX register after the CPUID instruction is executed with a 1 in the EAX register, and the generation field of the Device ID register accessible through Boundary Scan.
4. The Model Number corresponds to Bits [7:4] of the EDX register after RESET, Bits [7:4] of the EAX register after the CPUID instruction is executed with a 1 in the EAX register, and the model field of the Device ID register accessible through Boundary Scan.
5. The Stepping ID in Bits [3:0] indicates the revision number of that model. Refer table above for the processor stepping ID number in the CPUID information.
6. When EAX is initialized to a value of '1', the CPUID instruction returns the Extended Family, Extended Model, Processor Type, Family Code, Model Number and Stepping ID value in the EAX register. The EDX processor signature value after reset is equivalent to the processor signature output value in the EAX register.

Cache and TLB descriptor parameters are provided in the EAX, EBX, ECX and EDX registers after the CPUID instruction is executed with a 2 in the EAX register.

2.2 Component Marking Information

Figure 1. Processor Based on S Processor Line Chip Package LGA Top-Side Markings



Pin Count: 1700 Package Size: 45mm x 37.5mm

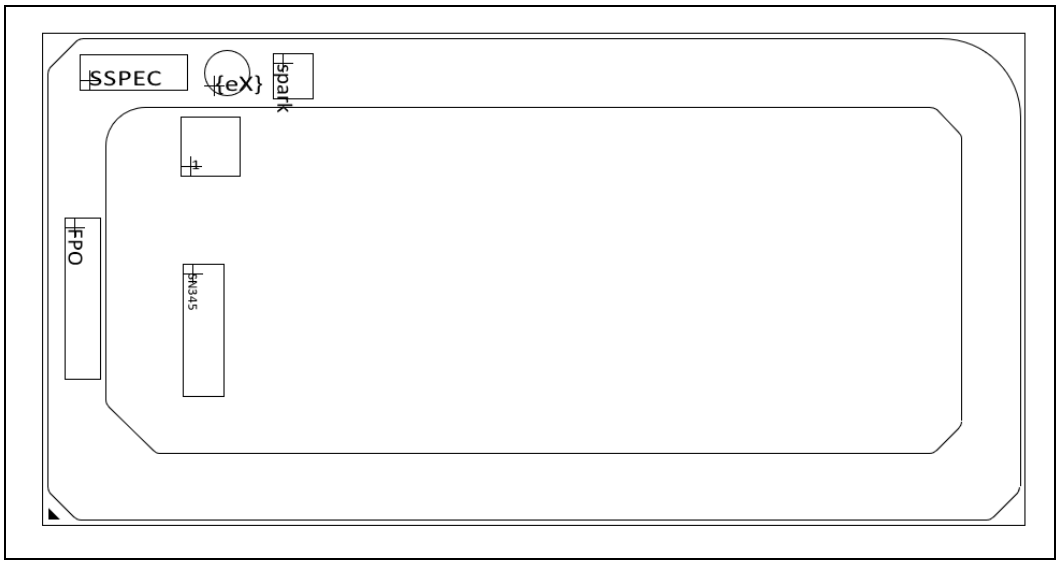
Production (SSPEC):

SWIRL (Intel logo)
TRADEMARK BRAND
PROCESSOR NUMBER
SSPEC
FPO {eX}

Note: "1" is unit visual ID (2D ID).

"2" is Pin 1 indicator on IHS.

Figure 2. Processor Based on H/P Processor Line Chip Package BGA Top-Side Markings



Pin Count: 1744 Package Size: 50mm x 25mm

Production (SSPEC):

SWIRL (Intel logo)
TRADEMARK BRAND
PROCESSOR NUMBER
SSPEC
FPO {eX}

Note: "1" is unit visual ID (2D ID).

"2" is Pin 1 indicator on IHS.

Figure 3. Processor Based on U15 Processor Line Chip Package BGA Top-Side Markings

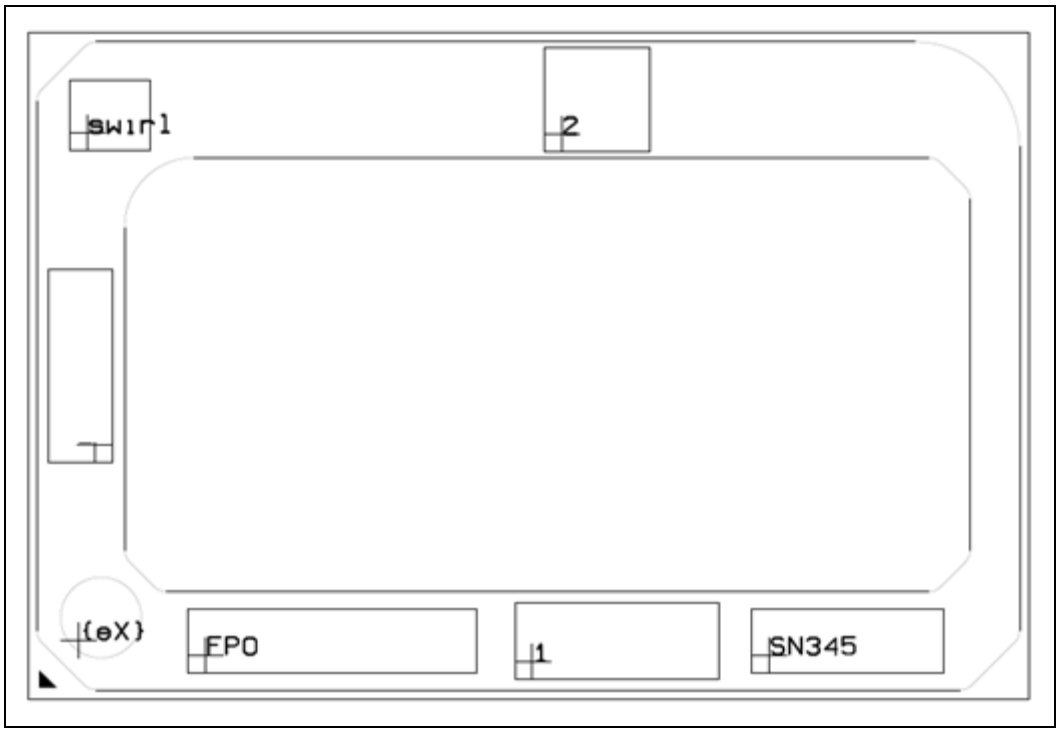
Pin Count: 1744 Package Size: 50mm x 25mm

Production (SSPEC):

Intel Logo
FPO
SSPEC
{eX}

Note: "1" is unit visual ID (2D ID).

Figure 4. Processor Based on U9 Processor Line Chip Package BGA Top-Side Markings



Pin Count: 1781 Package Size: 28.5mm x 19mm

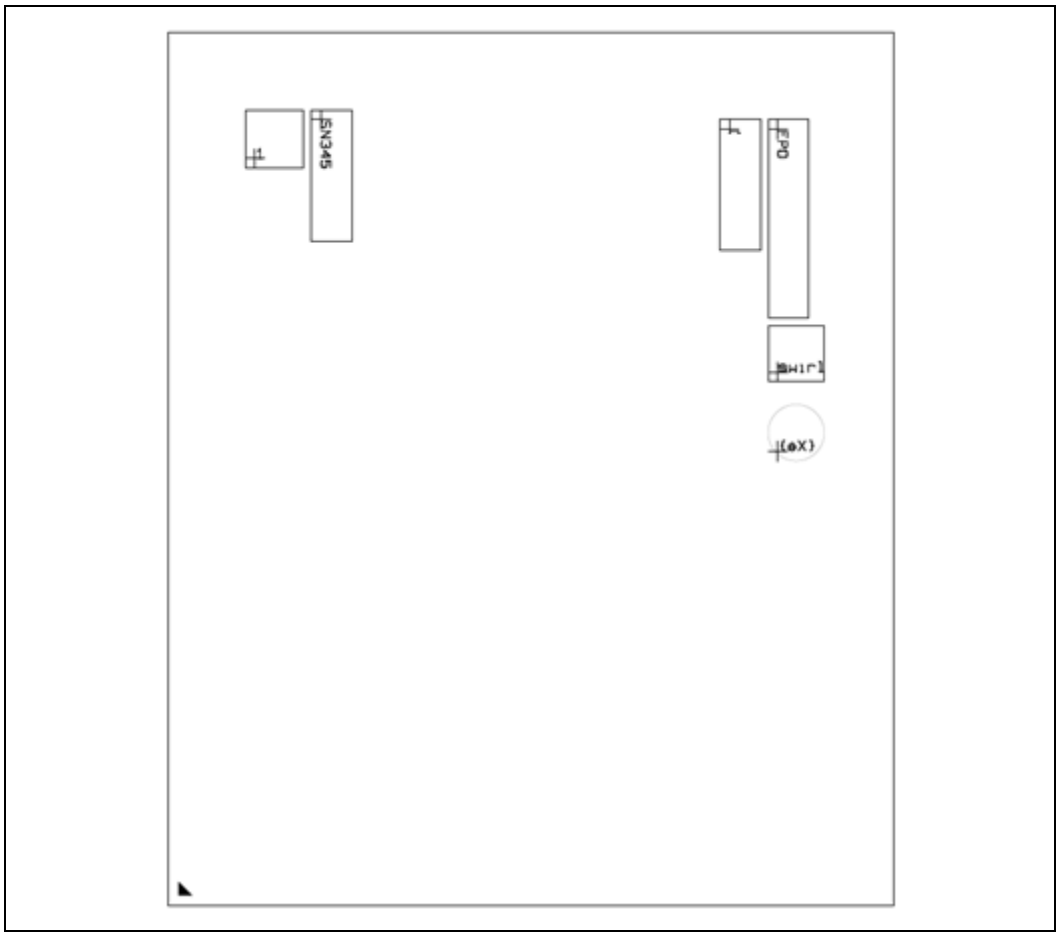
Production (SSPEC):

Intel Logo
FPO
SSPEC
{eX}

Note: "1" is unit visual ID (2D ID).

"2" is Pin 1 indicator on IHS.

Figure 5. Processor Based on HX Processor Line Chip Package BGA Top-Side Markings



Pin Count: 1964 Package Size: 37.5mm x 45mm

Production (SSPEC):

Intel Logo
FPO
SSPEC
{eX}

Note: "1" is unit visual ID (2D ID).

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3 Summary Tables of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes, which apply to the listed processor stepping. Intel® intends to fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

3.1 Codes Used in Summary Table

Stepping	Description
(No mark) or (Blank Box)	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Status	Description
Doc	Document change or update that is implemented.
Plan Fix	This erratum may be fixed in a future hardware stepping, firmware, or software update.
Fixed	This erratum has been previously fixed in Intel® hardware, firmware, or software.
No Fix	There are no plans to fix this erratum.

3.2 Errata Summary Table

ID	Processor Line				Title
	S	H/P	U	HX	
ADL001	No Fix	No Fix	No Fix	No Fix	X87 FDP Value May be Saved Incorrectly
ADL002	No Fix	No Fix	No Fix	No Fix	Debug Exceptions May Be Lost or Misreported When MOV SS or POP SS Instruction is Not Followed By a Write to SP
ADL003	N/A	N/A	N/A	N/A	N/A. Erratum has been removed.
ADL004	No Fix	No Fix	No Fix	No Fix	BMI1, BMI2, LZCNT, ADXC, and ADOX Instructions May Not Generate an #UD
ADL005	No Fix	No Fix	No Fix	No Fix	Exit Qualification For EPT Violations on Instruction Fetches May Incorrectly Indicate That The Guest-physical Address Was Writeable
ADL006	No Fix	No Fix	No Fix	No Fix	Processor May Generate Spurious Page Faults On Shadow Stack Pages
ADL007	No Fix	No Fix	No Fix	No Fix	Processor May Hang if Warm Reset Triggers During BIOS Initialization
ADL008	No Fix	No Fix	No Fix	No Fix	System May Hang When Bus-Lock Detection Is Enabled And EPT Resides in Uncacheable Memory

ID	Processor Line				Title
	S	H/P	U	HX	
ADL009	No Fix	No Fix	No Fix	No Fix	Processor May Generate Malformed TLP
ADL010	No Fix	No Fix	No Fix	No Fix	No #GP Will be Signaled When Setting MSR_MISC_PWR_MGMT.ENABLE_SDC if MSR_MISC_PWR_MGMT.LOCK is Set
ADL011	N/A	N/A	N/A	N/A	N/A. Erratum has been removed.
ADL012	No Fix	No Fix	No Fix	No Fix	Last Branch Records May Not Survive Warm Reset
ADL013	No Fix	No Fix	No Fix	No Fix	PCIe Link May Fail to Train Upon Exit From L1.2
ADL014	No Fix	No Fix	No Fix	No Fix	Incorrectly Formed PCIe Packets May Generate Correctable Errors
ADL015	No Fix	No Fix	No Fix	No Fix	#UD May be Delivered Instead of Other Exceptions
ADL016	N/A	No Fix	No Fix	No Fix	Type-C Host Controller Does Not Support Certain Qword Accesses
ADL017	No Fix	No Fix	No Fix	No Fix	#GP May be Serviced Before an Instruction Breakpoint
ADL018	No Fix	No Fix	No Fix	No Fix	Unexpected #PF Exception Might Be Serviced Before a #GP Exception
ADL019	No Fix	No Fix	No Fix	No Fix	WRMSR to Reserved Bits of IA32_L3_QOS_Mask_15 Will Not Signal a #GP
ADL020	No Fix	No Fix	No Fix	No Fix	VMX-Preemption Timer May Not Work if Configured With a Value of 1
ADL021	No Fix	No Fix	No Fix	No Fix	Setting MISC_FEATURE_CONTROL.DISABLE_THREE_STRIKE_CNT Does Not Prevent The Three-strike Counter From Incrementing
ADL022	N/A	N/A	N/A	N/A	N/A. Erratum has been removed.
ADL023	No Fix	No Fix	No Fix	No Fix	Unable to Transmit Modified Compliance Test Pattern at 2.5 GT/S or 5.0 GT/s Link Speeds
ADL024	Fixed	N/A	N/A	N/A	Single Core Configurations May Hang on S3/S4 Resume
ADL025	No Fix	No Fix	No Fix	No Fix	Single Step on Branches Might be Missed When VMM Enables Notification On VM Exit
ADL026	No Fix	No Fix	No Fix	No Fix	Reading The PPERF MSR May Not Return Correct Values
ADL027	No Fix	No Fix	No Fix	No Fix	Incorrect #CP Error Code on UIRET
ADL028	Fixed	N/A	N/A	N/A	Processor May Not Wake From TPAUSE/UMWAIT in Limited Situations
ADL029	Fixed	Fixed	Fixed	Fixed	Platform May Not Resume From G3/S3/S4/S5
ADL030	No Fix	No Fix	No Fix	No Fix	Intel® Processor Trace PSB+ Packets May Contain Unexpected Packets
ADL031	No Fix	No Fix	No Fix	No Fix	Intel® PT Trace May Drop Second Byte of CYC Packet
ADL032	No Fix	No Fix	No Fix	No Fix	VM Entry That Clears TraceEn May Generate a FUP

ID	Processor Line				Title
	S	H/P	U	HX	
ADL033	No Fix	No Fix	No Fix	No Fix	Unsynchronized Cross-Modifying Code Operations Can Cause Unexpected Instruction Execution Results
ADL034	N/A	No Fix	No Fix	No Fix	Processor May Hang When PROCHOT# is Active
ADL035	No Fix	No Fix	No Fix	No Fix	CPUID Reports Incorrect Number of Ways For The Load DTLB
ADL036	Fixed	Fixed	Fixed	Fixed	Unaligned CET-SS Stack Token Does Not Signal #GP
ADL037	No Fix	No Fix	No Fix	No Fix	Intel® PT Trace May Contain Incorrect Data When Configured With Single Range Output Larger Than 4KB
ADL038	No Fix	No Fix	No Fix	No Fix	OFFCORE_REQUESTS_OUTSTANDING Performance Monitoring Events May be Inaccurate
ADL039	No Fix	No Fix	No Fix	No Fix	On Instructions Longer Than 15 Bytes, #GP Exception is Prioritized and Delivered Over #CP Exception
ADL040	No Fix	No Fix	No Fix	No Fix	Mismatch on DR6 Value When Breakpoint Match is on Bitmap Address
ADL041	No Fix	No Fix	No Fix	No Fix	Processor Loads PERF_GLOBAL_CTRL MSR Value From SMM Transfer VMCS Upon STI When STM is Configured
ADL042	No Fix	No Fix	No Fix	No Fix	RTM Abort Status May be Incorrect For INT1/INT3 Instructions
ADL043	No Fix	No Fix	No Fix	No Fix	Incorrect MCACOD For L2 Prefetch MCE
ADL044	No Fix	No Fix	No Fix	No Fix	Call Instruction Wrapping Around The 32-bit Address Boundary May Return to Incorrect Address
ADL045	No Fix	No Fix	No Fix	No Fix	USB 3.2 Gen 1x1 Port Does Not Send 16 Polling LFPS Burst
ADL046	No Fix	No Fix	No Fix	No Fix	Crashlog and Telemetry BAR May Not Function Correctly
ADL047	Fixed	Fixed	Fixed	Fixed	LFENCE Instruction May Not Prevent FSFP Forwarding
ADL048	Fixed	Fixed	Fixed	Fixed	IA32_SPEC_CTL Bits IPRED_DIS_U, IPRED_DIS_S And BHI_DIS_S May Not Function Correctly
ADL049	No Fix	No Fix	No Fix	No Fix	VM Exit Qualification May Not be Correctly Set on APIC Access While Serving a User Interrupt
ADL050	Fixed	Fixed	Fixed	N/A	Processor Exiting Package C6 or C8 May Hang
ADL051	No Fix	No Fix	No Fix	No Fix	GPU Hang When Async Compute is Enabled
ADL052	Fixed	Fixed	Fixed	Fixed	Unexpected System Hang During Enhanced Intel SpeedStep Transitions
ADL053	Fixed	Fixed	Fixed	Fixed	Branch Predictor May Produce Incorrect Instruction Pointer
ADL054	Fixed	Fixed	Fixed	Fixed	Display Flickering May be Observed When The System is Idle
ADL055	No Fix	No Fix	No Fix	No Fix	Processor May Encrypt TME Exclude Range if Mapped to Remap Range
ADL056	No Fix	No Fix	No Fix	No Fix	Precision Time Measurement (PTM) Interpretation Capability Bit Incorrect Register Offset
ADL057	No Fix	No Fix	No Fix	No Fix	DDR5 Clock Jitter Out of Spec

ID	Processor Line				Title
	S	H/P	U	HX	
ADL058	No Fix	No Fix	No Fix	No Fix	IA32_MC2_ADDR And IA32_MC2_MISC MSRs Will be Cleared on Warm Reset
ADL059	No Fix	No Fix	No Fix	No Fix	xHCI Force Header Command Incorrect Return Code
ADL060	Fixed	Fixed	Fixed	Fixed	Machine Check Exception May be Observed During Package C6 Entry
ADL061	Fixed	Fixed	Fixed	Fixed	USB Type-C Monitor Removal May Result In System Hang
ADL062	Fixed	Fixed	Fixed	Fixed	The Time-Stamp Counter May Report an Incorrect Value
ADL063	Fixed	Fixed	Fixed	Fixed	INVLPG May Invalidate Global TLB Entries Only For The Current PCID
ADL064	Fixed	Fixed	Fixed	Fixed	CPU May Not Load The Most Recent Data
ADL065	No Fix	No Fix	No Fix	No Fix	Performance Monitoring Event IDQ.MS_UOPS May Undercount
ADL066	No Fix	No Fix	No Fix	No Fix	Performance Monitoring Events TOPDOWN.BACKEND_BOUND_SLOTS and IDQ_BUBBLES May be Inaccurate
ADL067	N/A	No Fix	No Fix	N/A	Type-C Display May be Blank Following S3/S4/S5 Resume
ADL068	No Fix	No Fix	No Fix	No Fix	Performance Monitoring Event Branch Instruction Retired Will Not Count CALLs to Next Sequential Instruction
ADL069	No Fix	No Fix	No Fix	No Fix	Performance Monitoring Event Branch Instruction Retired Will Overcount on Certain Types of Branch and Complex Instructions
ADL070	No Fix	No Fix	No Fix	No Fix	Unexpected System Behavior When Re-Enabling Intel® HT
ADL071	No Fix	No Fix	No Fix	No Fix	A Write to The TSC_Deadline MSR May Cause an Unexpected Timer Interrupt
ADL072	No Fix	No Fix	No Fix	No Fix	Processor Trace May Generate PSB Packets Too Infrequently
ADL073	No Fix	No Fix	No Fix	No Fix	Processor Trace May Not Generate a CYC Packet Before MODE.EXEC Packets

3.3 Specification Changes

No.	Specification Changes
	None for this revision of this specification update.

3.4 Specification Clarifications

No.	Specification Clarifications
	None for this revision of this specification update.

3.5 Documentation Changes

No.	Documentation Changes
	None for this revision of this specification update.

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4 Errata Details

ADL001	X87 FDP Value May be Saved Incorrectly
Problem	Execution of the FSAVE, FNSAVE, FSTENV, or FNSTENV instructions in real-address mode or virtual-8086 mode may save an incorrect value for the x87 FDP (FPU data pointer). This erratum does not apply if the last non-control x87 instruction had an unmasked exception.
Implication	Software operating in real-address mode or virtual-8086 mode that depends on the FDP value for non-control x87 instructions without unmasked exceptions may not operate properly. Intel® has not observed this erratum in any commercially available software.
Workaround	None identified. Software should use the FDP value saved by the listed instructions only when the most recent non-control x87 instruction incurred an unmasked exception.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL002	Debug Exceptions May be Lost or Misreported When MOV SS or POP SS Instruction is Not Followed By a Write to SP
Problem	If a MOV SS or POP SS instruction generated a debug exception, and is not followed by an explicit write to the Stack Pointer (SP), the processor may fail to deliver the debug exception or, if it does, the DR6 register contents may not correctly reflect the causes of the debug exception.
Implication	Debugging software may fail to operate properly if a debug exception is lost or does not report complete information. Intel® has not observed this erratum with any commercially available software.
Workaround	Software should explicitly write to the stack pointer immediately after executing MOV SS or POP SS.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL003	N/A. Erratum has been removed.

ADL004	BMI1, BMI2, LZCNT, ADXC, And ADOX Instructions May Not Generate an #UD
Problem	BMI1, BMI2, LZCNT, ADXC, and ADOX instructions will not generate an #UD fault, even though the respective CPUID feature flags do not enumerate them as supported instructions.
Implication	Software that relies on BMI1, BMI2, LZCNT, ADXC, and ADOX instructions to generate an #UD fault, may not work correctly.

ADL004	BMI1, BMI2, LZCNT, ADXC, And ADOX Instructions May Not Generate an #UD
Workaround	None identified. Software should check CPUID reported instructions availability and not rely on the #UD fault behavior.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL005	Exit Qualification For EPT Violations on Instruction Fetches May Incorrectly Indicate That The Guest-physical Address Was Writeable
Problem	On EPT violations, bit 4 of the Exit Qualification indicates whether the guest-physical address was writeable. When EPT is configured as supervisory shadow-stack (both bit 60 in EPT paging-structure leaf entry and bit 0 in EPT paging-structure entries are set), non-executable (bit 2 in EPT paging-structure entries is cleared), and non-writeable (bit 1 in EPT paging-structure entries is cleared) a VMExit due to a guest instruction fetch to a supervisory page will incorrectly set bit 4 of the Exit Qualification. Bits 3, 5, and 6 of the Exit Qualification are not impacted by this erratum.
Implication	Due to this erratum, bit 4 of the Exit Qualification may be incorrectly set. Intel® has not observed this erratum on any commercially available software.
Workaround	EPT handlers processing an EPT violation due to an instruction fetch access on a present page should ignore the value of bit 4 of the Exit Qualification.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL006	Processor May Generate Spurious Page Faults On Shadow Stack Pages
Problem	When operating in a virtualized environment, if shadow stack pages are mapped over an APIC page, the processor will generate spurious page faults on that shadow stack page whenever its linear to physical address translation is cached in the Translation Look-aside Buffer.
Implication	When this erratum occurs, the processor will generate a spurious page fault. Intel® is not aware of any software that maps shadow stack pages over an APIC page.
Workaround	Software should avoid mapping shadow stack pages over the APIC page.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL007	Processor May Hang if Warm Reset Triggers During BIOS Initialization
Problem	Under complex micro-architectural conditions, when the processor receives a warm reset during BIOS initialization, the processor may hang with a machine check error reported in IA32_MCi_STATUS, with MCACOD (bits [15:0]) value of 0400H, and MSCOD (bits [31:16]) value of 0080H.
Implication	Due to this erratum, the processor may hang. Intel® has only observed this erratum in a synthetic test environment.
Workaround	None Identified.

ADL007	Processor May Hang if Warm Reset Triggers During BIOS Initialization
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL008	System May Hang When Bus-Lock Detection Is Enabled and EPT Resides in Uncacheable Memory
Problem	On processors that support bus-lock detection (CPUID.(EAX=7, ECX=0).ECX[24]) and have it enabled (bit 2 in the IA32_DEBUGCTL MSR (1D9h)), and employ an Extended Page Table (EPT) that is mapped to an uncacheable area (UC), and the EPT_AD is enabled (bit 6 of the EPT Pointer is set), if the VMM performs an EPT modification on a predefined valid page while a virtual machine is running, the processor may hang.
Implication	Due to this erratum, the system may hang when bus-lock detection is enabled. Intel® has not observed this erratum in any commercially available software.
Workaround	VMM should not map EPT tables to Uncacheable memory while using EPT_AD.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL009	Processor May Generate Malformed TLP
Problem	If the processor root port receives an FetchAdd, Swap, or CAS TLP (an atomic operation) that is erroneous, it should generate a UR completion to the downstream requestor. If the TLP has an operand size greater than 4 bytes, the generated UR completion will report an operand size of 4 bytes, which will be interpreted as a malformed transaction.
Implication	When this erratum occurs, the processor may respond with a malformed transaction.
Workaround	None Identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL010	No #GP Will be Signaled When Setting MSR_MISC_PWR_MGMT.ENABLE_SDC if MSR_MISC_PWR_MGMT.LOCK is Set
Problem	If the MSR_MISC_PWR_MGMT.LOCK (MSR 1AAh, bit13) is set, a General Protection Exception (#GP) will not be signaled when MSR_MISC_PWR_MGMT.ENABLE_SDC (MSR 1AAh, bit 10) is cleared while IA32_XSS.HDC (MSR DA0h, bit 13) is set and if IA32_PKG_HDC_CTL.HDC_PKG_Enable (MSR DB0h, bit 0) was set at least once before.
Implication	Due to this erratum, MSR_MISC_PWR_MGMT.ENABLE_SDC will be cleared even though a #GP was not signaled.
Workaround	None identified. Software should not attempt to clear MSR_MISC_PWR_MGMT.ENABLE_SDC if the above #GP conditions are met.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL011	N/A. Erratum has been removed.

ADL012	Last Branch Records May Not Survive Warm Reset
Problem	Last Branch Records (LBRs) are expected to survive warm reset according to Intel® architectures (SDM Vol3 Table 9-2). LBRs may be incorrectly cleared following warm reset if a valid machine check error was logged in one of the IA32_MCi_STATUS MSRs (401h, 405h, 409h, 40Dh).
Implication	Reading LBRs following warm reset may show zero value even though LBRs were enabled (IA32_LBR_CTL.LBREn[0]=1) before the warm reset.
Workaround	None Identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL013	PCIe Link May Fail to Train Upon Exit From L1.2
Problem	When the PCIe Link exits the L1.2 low-power link state, the link may fail to correctly train to L0.
Implication	Due to this erratum, a PCIe link may incur unexpected link recovery events or it may enter a Link_Down state.
Workaround	It may be possible for a BIOS code change to workaround this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL014	Incorrectly Formed PCIe Packets May Generate Correctable Errors
Problem	Under complex microarchitectural conditions, the PCIe controller may transmit an incorrectly formed Transaction Layer Packet (TLP), which will fail CRC checks.
Implication	When this erratum occurs, the PCIe end point may record correctable errors resulting in either a NAK or link recovery. Intel® has not observed any functional impact due to this erratum.
Workaround	None Identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL015	#UD May be Delivered Instead of Other Exceptions
Problem	An invalid instruction opcode that runs into another exception before fetching all instruction bytes (For example:A #GP due to the instruction being longer than 15 bytes or a CS limit violation) may signal a #UD despite not fetching all instruction bytes under some microarchitectural conditions.
Implication	Due to this erratum, a #UD exception may be serviced before other exceptions. This does not occur for valid instructions. Intel® has only observed this erratum in a synthetic test environment.

ADL015	#UD May be Delivered Instead of Other Exceptions
Workaround	None Identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL016	Type-C Host Controller Does Not Support Certain Qword Accesses
Problem	The Type-C controller does not properly support Qword accesses to its MSI-X interrupt table which may lead to unexpected behavior.
Implication	When this erratum occurs, Qword reads do not return Unsupported Request and may not return correct data and Qword writes may lead to unexpected behavior. Intel® has not observed this erratum to affect any commercially available software.
Workaround	Software should not utilize Qword access for the Type-C MSI-X table.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL017	#GP May be Serviced Before an Instruction Breakpoint
Problem	An instruction breakpoint should have the highest priority and needs to be serviced before any other exception. In case an instruction breakpoint is marked on an illegal instruction longer than 15 bytes that starts in bytes 0-16 of a 32B-aligned chunk, and that instruction does not complete within the same 32B-aligned chunk, a General Protection Exception (#GP) on the same instruction will be serviced before the breakpoint exception.
Implication	Due to this erratum, an illegal instruction #GP exception may be serviced before an instruction breakpoint.
Workaround	None Identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL018	Unexpected #PF Exception Might Be Serviced Before a #GP Exception
Problem	Instructions longer than 15 bytes should assert a General Protection Exception (#GP). For instructions longer than 15 bytes, a Page Fault Exception (#PF) from the subsequent page might be issued before the #GP exception in the following cases: 1. The GP instruction starts at byte 1 – 16 of the last 32B-aligned chunk of a page (starting the count at byte 0), and it is not a target of taken jump, and it does not complete within the same 32B-aligned chunk it started in. 2. The GP instruction starts at byte 17 of the last 32B-aligned chunk of a page.
Implication	Due to this erratum, an unexpected #PF exception might be serviced before a #GP exception.
Workaround	None Identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL019	WRMSR to Reserved Bits of IA32_L3_QOS_Mask_15 Will Not Signal a #GP
Problem	A General Protection Exception (#GP) will not be signaled when writing non-zero values to the upper 32 bits of IA32_L3_QOS_Mask_15 MSR (Offset C9FH) even though they are defined as reserved bits.
Implication	Due to this erratum, a #GP will not be signaled when the upper bits of IA32_L3_QOS_Mask_15 are written with a non-zero value.
Workaround	None Identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL020	VMX-Preemption Timer May Not Work if Configured With a Value of 1
Problem	Under complex micro-architectural conditions, the VMX-preemption timer may not generate a VM Exit if the VMX-preemption timer value is set to 1.
Implication	Due to this erratum, if the value configured to a value of 1, a VM exit may not occur.
Workaround	None identified. Software should avoid programming the VMX-preemption timer with a value of 1.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL021	Setting MISC_FEATURE_CONTROL.DISABLE_THREE_STRIKE_CNT Does Not Prevent The Three-strike Counter From Incrementing
Problem	Setting MISC_FEATURE_CONTROL.DISABLE_THREE_STRIKE_CNT (bit 11 in MSR 1A4h) does not prevent the three-strike counter from incrementing as documented; instead, it only prevents the signaling of the three-strike event once the counter has expired.
Implication	Due to this erratum, software may be able to see the three-strike logged in the MC3_STATUS (MSR 40Dh, MCACOD = 400h [bits 15:0]) even when MISC_FEATURE_CONTROL.DISABLE_THREE_STRIKE_CNT is set.
Workaround	None Identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL022	N/A. Erratum has been removed.

ADL023	Unable to Transmit Modified Compliance Test Pattern at 2.5 GT/S or 5.0 GT/s Link Speeds
Problem	The processor's PCIe port (Bus 0, Device 1, Function 0/1/2 or Bus 0, Device 6, Function 0) does not transmit the Modified Compliance Test Pattern when in either 2.5 GT/S or 5.0 GT/s link speeds.
Implication	Due to this erratum, PCIe compliance testing may fail at 2.5 GT/S or 5.0 GT/s link speeds when enabling the Modified Compliance Test Pattern.

ADL023	Unable to Transmit Modified Compliance Test Pattern at 2.5 GT/S or 5.0 GT/s Link Speeds
Workaround	None Identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL024	Single Core Configurations May Hang on S3/S4 Resume
Problem	When booting in a single core configuration, the system may hang when resuming from a S3/S4 or a warm reset.
Implication	Due to this erratum, the system may hang.
Workaround	It is possible for BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL025	Single Step on Branches Might be Missed When VMM Enables Notification On VM Exit
Problem	Under complex micro-architectural conditions, single step on branches (IA32_DEBUGCTLMSR (Offset 1D9h, bit [1]) and also TF flag in EFLAGS register is set) in guest might be missed when VMM enables notification on VM Exit (IA32_VMX_PROCBASED_CTLS2 MSR, Offset 48Bh, bit [31]) while the dirty access bit is not set for the code page (bit [6] in paging-structure entry).
Implication	When single step is enabled under the above condition, some single step branches will be missed. Intel® has only observed this erratum in a synthetic test environment.
Workaround	When enabling single step on branches for debugging, software should first set the dirty bit of the code page.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL026	Reading The PPERF MSR May Not Return Correct Values
Problem	Under complex micro-architectural conditions, RDMSR instruction to Productive Performance (MSR_PPERF) MSR (Offset 64eh) may not return correct values in the upper 32 bits (EDX register) if Core C6 is enabled.
Implication	Software may experience a non-monotonic value when reading the MSR_PPERF multiple times.
Workaround	None identified. Software should not rely on the upper bits of the MSR_PPERF when core C6 is enabled.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL027	Incorrect #CP Error Code on UIRET
Problem	If a #CP exception is triggered during a UIRET instruction execution, the error code on the stack will report NEAR-RET instruction (code 1) instead of FAR-RET instruction (code 2).
Implication	Due to this erratum, an incorrect #CP error code is logged when #CP is triggered during UIRET instruction.
Workaround	None Identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL028	Processor May Not Wake From TPAUSE/UMWAIT in Limited Situations
Problem	External interrupts should cause the processor to exit the implementation-dependent optimized state reached by the TPAUSE and UMWAIT instructions regardless of the value of RFLAGS.IF. Due to this erratum, an interrupt may not wake the processor from such a state when RFLAGS.IF is 0. Additionally, the processor may not exit from UMWAIT/TPAUSE sleep state if the virtualization execution control of Interrupt-Window Exiting is active (bit[2] of Primary Processor Based VM Execution Control is set to 1) or if Virtual-interrupt Delivery is active (bit[9] of Secondary Processor Based VM Execution Control is 1 & bit[31] of Primary Processor Based VM Execution Control is 1). **NOTE:** The only method to reach UMWAIT/TPAUSE sleep state with interrupt-window exiting pending is if the previous instruction is a STI, MOV SS, POP SS, or VM-entry which sets MOV/POP SS blocking or STI blocking.
Implication	If interrupts are masked because RFLAGS.IF = 0, arrival of an interrupt (or virtual interrupt) will not wake the processor from TPAUSE/UWMAIT. For operating systems that ensure that RFLAGS.IF = 1 whenever CPL > 0, this erratum applies only if TPAUSE or UMWAIT is used with interrupts disabled by RFLAGS.IF while CPL = 0. Intel® is not aware of production software affected by this erratum.
Workaround	It may be possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL029	Platform May Not Resume From G3/S3/S4/S5
Problem	Transient noise on the CPU crystal clock differential signals (CPU_NSSC_DP and CPU_NSSC_ DN) when resuming from G3/S3/S4/S5 may prevent the platform from booting.
Implication	Due to this erratum, the platform may fail boot when resuming from G3/S3/S4/S5.
Workaround	It may be possible for BIOS code changes to workaround this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL030	Intel® Processor Trace PSB+ Packets May Contain Unexpected Packets
Problem	Some Intel® Processor Trace packets should be issued only between TIP.PGE (Target IP Packet.Packet Generation Enable) and TIP.PGD (Target IP Packet.Packet Generation Disable) packets. Due to this erratum, when a TIP.PGE packet is generated it may be preceded by a PSB+ (Packet Stream Boundary) that incorrectly includes FUP (Flow Update Packet) and MODE.Exec packets.
Implication	Due to this erratum, FUP and MODE.Exec may be generated unexpectedly.
Workaround	Decoders should ignore FUP and MODE.Exec packets that are not between TIP.PGE and TIP.PGD packets.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL031	Intel® PT Trace May Drop Second Byte of CYC Packet
Problem	Due to a rare microarchitectural condition, the second byte of a 2-byte CYC (Cycle Count) packet may be dropped without an OVF (Overflow) packet.
Implication	A trace decoder may signal a decode error due to the lost trace byte.
Workaround	None identified. A mitigation is available for this erratum. If a decoder encounters a multi-byte CYC packet where the second byte has bit 0 (Ext) set to 1, it should assume that 4095 cycles have passed since the prior CYC packet, and it should ignore the first byte of the CYC and treat the second byte as the start of a new packet.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL032	VM Entry That Clears TraceEn May Generate a FUP
Problem	If VM entry clears Intel® PT (Intel® Processor Trace) IA32_RTIT_CTL.TraceEn (MSR 570H, bit 0) while PacketEn is 1 then a FUP (Flow Update Packet) will precede the TIP.PGD (Target IP Packet, Packet Generation Disable). VM entry can clear TraceEn if the VM-entry MSR-load area includes an entry for the IA32_RTIT_CTL MSR.
Implication	When this erratum occurs, an unexpected FUP may be generated that creates the appearance of an asynchronous event taking place immediately before or during the VM entry.
Workaround	The Intel® PT trace decoder may opt to ignore any FUP whose IP matches that of a VM entry instruction.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL033	Unsynchronized Cross-Modifying Code Operations Can Cause Unexpected Instruction Execution Results
Problem	The act of one processor or system bus master writing data into a currently executing code segment of a second processor with the intent of having the second processor execute that data as code is called cross-modifying code (XMC). XMC that does not force the second processor to execute a synchronizing instruction prior to execution of the new code is called unsynchronized XMC. Software using unsynchronized XMC to modify the instruction byte stream of a processor can see unexpected or unpredictable execution behavior from the processor that is executing the modified code.
Implication	In this case the phrase "unexpected or unpredictable execution behavior" encompasses the generation of most of the exceptions listed in the Intel® Architecture Software Developer's Manual Volume 3: System Programming Guide including a General Protection Fault (GPF) or other unexpected behaviors. In the event that unpredictable execution causes a GPF the application executing the unsynchronized XMC operation would be terminated by the operating system.
Workaround	None Identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL034	Processor May Hang When PROCHOT# is Active
Problem	When PROCHOT# is activated during BIOS initialization, the processor may hang with a machine check error reported in IA32_MCi_STATUS, with MCACOD (bits [15:0]) value of 0402H, and MSCOD (bits [31:16]) value of 0409H.
Implication	Due to this erratum, the processor may hang.
Workaround	None Identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL035	CPUID Reports Incorrect Number of Ways For The Load DTLB
Problem	CPUID leaf 18H sub-leaf 04H EBX [31:16] reports 4 ways instead of 6 ways for the Load DTLB.
Implication	Due to this erratum, software that relies upon the number of ways in the load DTLB may operate sub optimally.
Workaround	None Identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL036	Unaligned CET-SS Stack Token Does Not Signal #GP
Problem	On systems that enable Control-flow Enforcement Technology shadow-stack (CET-SS) in supervisor mode, an inter-privilege level far CALL or event delivery switches the shadow stack to a supervisor shadow stack. During this switch, the processor fails to signal a #GP exception if the 32-byte region comprised of 8 bytes containing the supervisor shadow stack token and the following 24-byte stack frame are not 32-byte aligned on the shadow stack.
Implication	Due to this erratum, on systems that enable CET-SS in supervisor mode, system software that fails to properly 32-byte align the supervisor shadow stack token may incorrectly mark the supervisor shadow stack token as busy, preventing re-entry into the supervisor thread by generating an unexpected #GP exception unrelated to stack token alignment.
Workaround	It may be possible for BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL037	Intel® PT Trace May Contain Incorrect Data When Configured With Single Range Output Larger Than 4KB
Problem	Under complex micro-architectural conditions, when using Intel® Processor Trace (Intel® PT) with single range output larger than 4KB, disabling PT and then enabling PT using the TraceEn bit in IA32_RTIT_CTL MSR (MSR 570h, bit 0) may cause incorrect output values to be recorded.
Implication	Due to this erratum, a PT trace may contain incorrect values.
Workaround	None identified. Software should avoid using PT with single range output larger than 4KB.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL038	OFFCORE_REQUESTS_OUTSTANDING Performance Monitoring Events May be Inaccurate
Problem	The OFFCORE_REQUESTS_OUTSTANDING.*DATA_RD performance monitoring event (Event 20h; UMask 08h) counts the number of off-core outstanding data read transactions each cycle. Due to this erratum, an inaccurate count may be observed when Intel® HyperThreading Technology is enabled and hardware prefetchers are enabled.
Implication	OFFCORE_REQUESTS_OUTSTANDING Performance Monitoring Events may be Inaccurate.
Workaround	None Identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL039	On Instructions Longer Than 15 Bytes, #GP Exception is Prioritized And Delivered Over #CP Exception
Problem	A #GP (global protection exception) that results from an instruction being longer than 15 bytes is prioritized and served before a #CP (Controlflow Protection exception) that was created due to a missing ENDBRx instruction at the target of an indirect branch.
Implication	Due to this erratum, during an indirect jump with ENDBRANCH tracking, if the processor lands on an illegal instruction with length longer than 15 bytes or that decodes to a CS limit, the processor will prioritize and deliver a #GP exception over the #CP exception.
Workaround	None Identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL040	Mismatch on DR6 Value When Breakpoint Match is on Bitmap Address
Problem	Under complex microarchitectural conditions, on systems with Control-flow Enforcement Technology (CET) enabled, hitting a predefined data breakpoint may not be reported in B0-B3 (bits 3:0) in the DR6 register if that breakpoint was set on the legacy code page bitmap.
Implication	Due to this erratum, software may not know which breakpoint triggered when setting breakpoints on the legacy code page bitmap.
Workaround	None Identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL041	Processor Loads PERF_GLOBAL_CTRL MSR Value From SMM Transfer VMCS Upon STI When STM is Configured
Problem	The processor will load the value of IA32_PERF_GLOBAL_CTRL (MSR 038Fh) from the SMM-transfer VMCS upon SMI (System Management Interrupt) when STM (SMM-transfer monitor) is configured.
Implication	Due to this erratum, Processor may enter STM with non-zero PERF_GLOBAL_CTRL MSR which may result in unexpected performance monitoring behavior.
Workaround	Software should clear IA32_PERF_GLOBAL_CTRL inside the SMM transfer VMCS before performing STM configuration.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL042	RTM Abort Status May be Incorrect For INT1/INT3 Instructions
Problem	When Intel® Transactional Synchronization Extensions (TSX) is enabled, and there is an RTM (Restricted Transactional Memory))abort due to an INT1 or INT3 instruction, bit 5 of the RTM abort status (nested transaction execution) will not be set even if the RTM was nested.

ADL042	RTM Abort Status May be Incorrect For INT1/INT3 Instructions
Implication	Due to this erratum, software that manages RTM aborts cannot determine whether an abort is nested.
Workaround	None Identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL043	Incorrect MCACOD For L2 Prefetch MCE
Problem	Under complex micro-architectural conditions, an L2 prefetch MCE that should be reported with MCACOD 165h in IA32_MC3_STATUS MSR (MSR 40dh, bits [15:0]) may be reported with an MCACOD of 101h.
Implication	Due to this erratum, the reported MCACOD for this MCE may be incorrect.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL044	Call Instruction Wrapping Around The 32-bit Address Boundary May Return to Incorrect Address
Problem	In 32-bit mode, a call instruction wrapping around the 32-bit address should save a return address near the bottom of the address space (low address) around address zero. Under complex micro-architectural conditions, a return instruction following such a call may return to the next sequential address instead (high address).
Implication	Due to this erratum, In 32-bit mode a return following a call instruction that wraps around the 32-bit address boundary may return to the next sequential IP without wrapping around the address, possibly resulting in a #PF. Intel® has not observed this behavior on any commercially available software.
Workaround	Software should not place call instructions in addresses that wrap around the 32-bit address space in 32-bit mode.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL045	USB 3.2 Gen 1x1 Port Does Not Send 16 Polling LFPS Burst
Problem	On USB 3.2 Gen 1x1 only capable ports, including ports configured as USB 3.2 Gen 1x1 by soft strap, the xHCI controller may send only 15 LFPS signals instead of a burst of 16 LFPS signals as specified by the USB 3.2 specification.
Implication	There are no known functional implications due to this erratum. LFPS handshake requires the receiver link partner to only detect 2 LFPS signals. This issue may impact the SuperSpeed compliance test case which checks for the 16 LFPS burst requirements: TD6.4, TD6.5, and TD7.31.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL046	Crashlog and Telemetry BAR May Not Function Correctly
Problem	The Crashlog and Telemetry PM_BAR register (Bus 0, Device 10, Function 0, Offset 10h) does not correctly implement the BAR sizing function. It reports a 32K BAR, but the BAR requires 64K memory alignment.
Implication	Due to this erratum, if PM_BAR is 32K aligned, but not 64K aligned, accesses to the BAR will fail.
Workaround	None identified. BIOS must ensure that this BAR is 64K aligned.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL047	LFENCE Instruction May Not Prevent FSFP Forwarding
Problem	When the Fast Store Forwarding Predictor (FSFP) is enabled, the LFENCE instruction may allow older stores to be predictively forwarded to younger loads.
Implication	Due to this erratum, software that relies on the LFENCE instruction to prevent FSFP forwarding may not behave as expected.
Workaround	It may be possible for BIOS to contain a workaround for this Erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL048	IA32_SPEC_CTL Bits IPRED_DIS_U, IPRED_DIS_S And BHI_DIS_S May Not Function Correctly
Problem	IA32_SPEC_CTL (MSR 48h) bits IPRED_DIS_U (bit 3), IPRED_DIS_S (bit 4) and BHI_DIS_S (bit 10) may not function correctly after leaving a C6 or deeper sleep state.
Implication	Due to this erratum, software that relies upon these bit values may not behave as intended.
Workaround	It may be possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL049	VM Exit Qualification May Not be Correctly Set on APIC Access While Serving a User Interrupt
Problem	A VM Exit that occurs while the processor is serving a user interrupt in non-root mode should set the "asynchronous to instruction execution" bit in the Exit Qualification field in the Virtual Machine Control Structure (bit 16). However, if a VM Exit occurs during processing a user interrupt due to an APIC access, the bit will not be set.
Implication	Due to this erratum, the "asynchronous to instruction execution" bit will not be set if an APIC Access VM Exit occurs while the processor is serving a user interrupt. Intel® has not observed this erratum with any commercially available software.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL050	Processor Exiting Package C6 or C8 May Hang
Problem	When the processor exits a package C6 or C8 power state, it may encounter a machine check exception (MCACOD=PCU internal Errors(0402h) / MSCOD=MESSAGE_CHANNEL_TIMEOUT (0409h) / PKGC_EXIT_SA_FIVR_UNLOBOTOMY_TIMEOUT (0441h) / PKGC_WATCHDOG_HANG_C2P2_RSP (0462h)).
Implication	Due to this erratum the system may hang with machine check exception.
Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL051	GPU Hang When Async Compute is Enabled
Problem	GPU may hang when Async Compute is enabled
Implication	Due to this erratum, the GPU may hang when running high bandwidth GFx application such as benchmarks and/or games.
Workaround	None identified. The Async Compute feature will be disabled in a graphics driver update. See GFx Driver Revenue SV2 PR5 (101.3616 or later) and release notes.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL052	Unexpected System Hang During Enhanced Intel SpeedStep® Transitions
Problem	Under complex microarchitectural conditions Enhanced Intel SpeedStep® transitions may lead to a system hang.
Implication	Due to this issue a system may hang with MCACODE GCACHEL2_ERR_ERR (010Ah).
Workaround	It is possible for a BIOS code change to workaround this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL053	Branch Predictor May Produce Incorrect Instruction Pointer
Problem	Under complex microarchitectural conditions, the branch predictor may produce an incorrect instruction pointer leading to unpredictable system behavior.
Implication	Due to this erratum, the system may exhibit unpredictable behavior.
Workaround	It may be possible for BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL054	Display Flickering May be Observed When The System is Idle
Problem	Display flickering may be observed When system is idle due to VCCSA being lower than expected.
Implication	Due to this erratum, display flickering may be observed when the system is Idle.
Workaround	It may be possible for BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL055	Processor May Encrypt TME Exclude Range if Mapped to Remap Range
Problem	The processor accesses to TME exclude range may be encrypted but not decrypted if mapped to remap range.
Implication	Due to this erratum, the processor exclude range it will be encrypted but will but not decrypted if mapped to remap range.
Workaround	It may be possible for BIOS to workaround this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL056	Precision Time Measurement (PTM) Interpretation Capability Bit Incorrect Register Offset
Problem	The PTM Propagation Delay Adaptation Interpretation B (PTMPDAIB) Bit is implemented at Configuration Space (CFG) Offset 158h instead of at 50h as documented in the PCI-SIG PTM Byte Ordering Adaptation Engineering Change Notice (ECN).
Implication	End Point Device (EPD) software that implements the PTM Byte Ordering Adaptation ECN will not be able to program their PTMPDAIB Bit correctly since it is located at a different register offset.
Workaround	None identified. To mitigate this issue, EPD software that implements the PTM Byte Ordering Adaptation ECN must access PTMPDAIB at CFG Offset 158h.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL057	DDR5 Clock Jitter Out of Spec
Problem	DDR5 Clock Jitter, as measured by jitter parameters Dj, Rj, and Tj (Dynamic/Random/Total jitter), may be beyond the JEDEC specification (JEDEC doc number JESD79-5B, Chapter 8.3) limits.
Implication	Due to this erratum Clock Jitter measurements may be out of spec. Intel® has not observed any functional implications due to this erratum.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL058	IA32_MC2_ADDR And IA32_MC2_MISC MSRs Will be Cleared on Warm Reset
Problem	A non-zero value written to IA32_MC2_ADDR (40Ah) and IA32_MC2_MISC(40Bh) MSRs will be incorrectly cleared following a warm reset.
Implication	Due to this erratum, software that relies on the IA32_MC2_ADDR and IA32_MC2_MISC MSR values may not function correctly after a warm reset. Intel® has not observed this erratum with any commercially available software.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL059	xHCI Force Header Command Incorrect Return Code
Problem	The xHCI controller does not return the correct completion code for the Force Header Command as defined in the Section 4.6.16 of the eXtensible Host Controller Interface for Universal Serial Bus (xHCI) Requirements Specification Rev 1.2.
Implication	xHCI CV TD4.12 - Force Header Command Test may report an error. Intel has obtained a waiver for TD 4.12. The Force Header Command is only used by the USB-IF Command Verifier (xHCI CV) tool for device testing. There are no known functional failures due to this erratum.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL060	Machine Check Exception May be Observed During Package C6 Entry
Problem	The processor may hang during a package C6 entry with a machine check (MCACOD = 0x0402, MCSCOD = 0x0485).
Implication	Due to this erratum the system may hang.
Workaround	It is possible for BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL061	USB Type-C Monitor Removal May Result In System Hang
Problem	Platform designs with discrete graphics may hang upon removal of a USB Type-C monitor from the system.
Implication	Due to this erratum the system may hang
Workaround	It is possible for BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL062	The Time-Stamp Counter May Report an Incorrect Value
Problem	Under complex micro-architectural conditions, the Time-Stamp Counter (TSC) may incorrectly report the time stamp to be less than the expected time stamp after exiting C6 power saving state.
Implication	Due to this erratum, systems that rely upon a monotonically increasing value reported by the TSC may exhibit unpredictable system behavior.
Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL063	INVLPG May Invalidate Global TLB Entries Only For The Current PCID
Problem	The INVLPG instruction should invalidate any global TLB entries for the specified linear address, regardless of PCID (Process-Context Identifier). Due to this erratum, INVLPG may fail to invalidate TLB entries for global pages with PCIDs different from the current PCID value. **NOTE:** On affected processors, the CPU will not use global TLB entries with PCIDs different from the current PCID value. This erratum does not apply in VMX non-root operation. It applies only when PCIDs are enabled and either in VMX root operation or outside VMX operation.
Implication	When this erratum occurs, TLB entries may incorrectly remain valid, leading to unpredictable system behavior, including unexpected exceptions. This erratum does not apply to a guest operating system running in VMX non-root operation.
Workaround	It may be possible for BIOS to contain a workaround for this erratum. Alternatively, this can be worked around by software using INVPCID type 2 instead of INVLPG.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL064	CPU May Not Load The Most Recent Data
Problem	Under complex microarchitectural conditions, a read on one logical processor may not receive the most recently stored data by another logical processor.
Implication	Due to this erratum, unpredictable system behavior or a system hang may occur. Intel has only observed this behavior in a synthetic test environment. Intel has not observed this erratum with any commercially available system.
Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL065	Performance Monitoring Event IDQ.MS_UOPS May Undercount
Problem	The performance monitoring events IDQ.MS_UOPS, IDQ.MS_SWITCHES, and IDQ.MS_CYCLES_ANY (Event 79h, UMask 30h) may undercount MS_UOPS that come from the Decode Stream Buffer (DSB).
Implication	Due to this erratum, performance monitoring counters may report counts lower than expected.

ADL065	Performance Monitoring Event IDQ.MS_UOPS May Undercount
Workaround	None identified. Performance monitoring event UOPS_RETIRED.MS may be used instead.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL066	Performance Monitoring Events TOPDOWN.BACKEND_BOUND_SLOTS and IDQ_BUBBLES May be Inaccurate
Problem	The performance monitoring events TOPDOWN.BACKEND_BOUND_SLOTS (Event A4h, UMask 02h) and IDQ_BUBBLES.* (Event 9Ch, UMask 01h) may not count when the processor is in the C0.2 power sub-state, which is entered via the TPAUSE or UWAIT instructions. This erratum also impacts the accuracy of MSR_PERF_METRICS fields Frontend Bound, Backend Bound, and Fetch Latency (MSR 329h, Bits [23:16], [31:24] and [55:48]).
Implication	Due to this erratum, these performance monitoring events and the fields in MSR_PERF_METRICS may be inaccurate.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL067	Type-C Display May be Blank Following S3/S4/S5 Resume
Problem	When switching between Type-C Display Alt Mode and a Multi-Function Device (MFD) while the system is in S3/S4/S5, the Display may not enumerate.
Implication	When this erratum occurs the Display may be blank. A device unplug and re-plug may be necessary to recover the display.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL068	Performance Monitoring Event Branch Instruction Retired Will Not Count CALLs to Next Sequential Instruction
Problem	A CALL instruction whose target is the next sequential instruction (the same address pushed onto the stack) will not increment the performance monitoring event BR_INST_RETIRED (Event: C4H, UMask: 00H, F9H).
Implication	Due to this erratum, software monitoring Branch Instruction Retired events may undercount. Since the CALL is to the next instruction, control flow tracing with the Last Branch Retired (LBR) records should not be affected.
Workaround	None identified
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL069	**Performance Monitoring Event Branch Instruction Retired Will Overcount on Certain Types of Branch and Complex Instructions**
Problem	On certain types of branch and complex instructions the performance monitoring event BR_INST_RETIRED (Event: C4H, UMask: 00H / 7EH / BFH / C0H / DFH / EBH / FBH / F9H) will overcount by 1. Affected instructions include FAR CALL/JMP, RETF, IRET, VMENTRY/VMEXIT/VMPTRLD and complex SGX/SMX/CSTATE instructions/flows.
Implication	Due to this erratum, software monitoring Branch Instruction Retired events may overcount.
Workaround	None identified
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL070	**Unexpected System Behavior When Re-Enabling Intel® HT**
Problem	When performing a warm reset as part of enabling of Intel® Hyper-Threading, machine check banks may not be initialized correctly.
Implication	Due to this erratum, software that relies on initialized values in machine check banks may not behave as expected.
Workaround	None identified. Software or BIOS can avoid this erratum by performing cold reset when re-enabling Intel® HT.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL071	**A Write to The TSC_Deadline MSR May Cause an Unexpected Timer Interrupt**
Problem	Under complex micro-architectural conditions, writing a non-zero value to the Time-Stamp Counter (TSC) Deadline counter, IA32-TSC_DEADLINE MSR (6E0h), may cause timer interrupt following the write.
Implication	Due to this erratum, a unexpected timer interrupt may be signaled.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL072	**Processor Trace May Generate PSB Packets Too Infrequently**
Problem	A Packet Stream Boundary (PSB) packet should be generated for every PSBFreq number of trace output bytes. Due to this erratum, PSB packets may be generated only after as many as four times that number of output bytes have been generated.
Implication	Due to this erratum, trace decoder software may see fewer PSB packets than expected. This may lead to the trace decoder software needing to search further to find a starting point to decode or, when used in circular mode, being unable to decode the trace due to lacking any PSB packets.

Workaround	None identified. Software can request more frequent PSB packets by programming PSBFreq (bits[27:24]) of IA32_RTIT_CTL MSR (570H) to a value 1/4 of the desired value.
Status	For the steppings affected, refer to the Summary Table of Changes.

ADL073	**Processor Trace May Not Generate a CYC Packet Before MODE.EXEC Packets**
Problem	When a Processor Trace MODE.EXEC packet is generated due to a change in RFLAGS.IF (interrupt flag) or the CS.L or CS.D bits, the processor may not generate a CYC packet before generating the MODE.EXEC packet.
Implication	Due to this erratum, trace decoder software will not be able to precisely determine when mode changes that involve changing the interrupt flag or the application's default operand size happened.
Workaround	None identified
Status	For the steppings affected, refer to the Summary Table of Changes.

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5 Specification Changes

None.

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6 Specification Clarification

None.

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7 Document-Only Change

None.

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