Intel® Iris® Xᵉ MAX Graphics Open Source

Programmer's Reference Manual

For the 2020 Discrete GPU formerly named "DG1"

Volume 4: Configurations

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Table of Contents

Configurations

This chapter contains configurations details for DG1 products, as described in the following sections:

- Product Mapping Table
- Device Attributes
- Steppings and Device IDs

Product Mapping Table

Product Configuration Attribute Table	
Product Family	**DG1**
SKU Name	**POR**
Global Attributes	
Render Engine	Xᵉ MAX 1x6x16
Media Engine	Media12
Display Engine	Display12
Chassis	PCI
LLC Size	N/A
In-Package Memory	N/A
Main Memory	LP4-4267 128bit (68GBps)

Device Attributes

The following table lists detailed GT device attributes for proposed Xᵉ MAX.

Product Configuration Attribute Table	
Product Family	**DG1**
Architectural Name	**1x6x16**
SKU Name	**POR**
Global Attributes	
Slice count	1
Dual-Subslice (DSS) Count	6
EU/DSS	16
EU count (total)	96
Threads / EU	7
Thread Count (Total)	672
FLOPs/Clk - Half Precision, MAD (peak)	3072
FLOPs/Clk - Single Precision, MAD (peak)	1536
FLOPs/Clk - Double Precision, MAD (peak)	N/A
Unslice clocking (coupled/decoupled from Cr slice)	Coupled
GTI / Ring Interfaces	2
GTI bandwidth (bytes/unslice-clk)	r: 128
	w: 128
eDRAM Support	N/A
Graphics Virtual Address Range	48 bit
Graphics Physical Address Range (DM), Max Per Device Memory = 128 GB	37 bit
Graphics Physical Address Range (System memory)	39 bit
Caches & Dedicated Memories	
L3 Cache, total size (bytes)	16384k
L3 Cache, bank count	8
L3 Cache, bandwidth (bytes/clk)(1)	8x 64 R|W
L3 Cache, D$ Size (Kbytes)(2)	1408K
L3 Cache, Tile cache size (Kbytes)(2)	2048K
L3 Cache, Command buffer cache size (Kbytes)(2)	128K
URB Size (kbytes)(2)	768K
SLM Size (kbytes)	768k
LLC/L4 size (bytes)	3MB/core
Instruction Cache (instances, bytes ea.)	6x 48k
Color Cache (RCC, bytes)	3x 32k

Product Configuration Attribute Table	
Product Family	**DG1**
Architectural Name	**1x6x16**
SKU Name	**POR**
MSC Cache (MSC, bytes)	3x 16k
HiZ Cache (HZC, bytes)	3x 4k
Z Cache (RCZ, bytes)	3x 16k
Stencil Cache (STC, bytes)	3x 6k
Instruction Issue Rates	
FMAD, SP (ops/EU/clk)	8
FMUL, SP (ops/EU/clk)	8
FADD, SP (ops/EU/clk)	8
MIN,MAX, SP (ops/EU/clk)	8
CMP, SP (ops/EU/clk)	8
INV, SP (ops/EU/clk)	2
SQRT, SP (ops/EU/clk)	2
RSQRT, SP (ops/EU/clk)	2
LOG, SP (ops/EU/clk)	2
EXP, SP (ops/EU/clk)	2
POW, SP (ops/EU/clk)	1
IDIV, SP (ops/EU/clk)	1-6
TRIG, SP (ops/EU/clk)	2
FDIV, SP (ops/EU/clk)	1
Load/Store	
Data Ports (HDC)	6
L3 Load/Store - same addresses within msg (Bytes/clk)	384
L3 Load/Store - unique addresses within msg (Bytes/clk)	384
SLM Load//Store - same addresses within msg (Bytes/clk)	768
SLM Load//Store - unique addresses within msg (Bytes/clk)	768
Atomic, Local 32b - same addresses within msg (dwords/clk)	6
Atomic, Global 32b - unique addresses within msg (dwords/clk)	96
3D Attributes	
Geometry pipes	1
Samplers (3D)	6
2D Texel Rate, point, 32b (tex/clk)	48
2D Texel Rate, point, 64b (tex/clk)	48

Product Configuration Attribute Table	
Product Family	**DG1**
Architectural Name	**1x6x16**
SKU Name	**POR**
2D Texel Rate, point, 128b (tex/clk)	48
2D Texel Rate, bilinear, 32b (tex/clk)	48
2D Texel Rate, bilinear, 64b (tex/clk)	48
2D Texel Rate, bilinear, 128b (tex/clk)	12
2D Texel Rate, trilinear, 32b (tex/clk)	24
2D Texel Rate, trilinear, 64b (tex/clk)	24
2D Texel Rate, trilinear, 128b (tex/clk)	6
2D Texel Sample Rate, aniso 2x (MIP nearest), 32b (tex/clk)	48
2D Texel Sample Rate, aniso 4x (MIP nearest), 32b (tex/clk)	24
2D Texel Sample Rate, aniso 8x (MIP nearest), 32b (tex/clk)	12
2D Texel Sample Rate, aniso 16x (MIP nearest), 32b (tex/clk)	6
3D Texel Sample Rate, point, 32b (tex/clk)	48
3D Texel Sample Rate, point, 64b (tex/clk)	48
3D Texel Sample Rate, point, 128b (tex/clk)	24
3D Texel Sample Rate, bilinear, 32b (tex/clk)	24
3D Texel Sample Rate, bilinear, 64b (tex/clk)	24
3D Texel Sample Rate, bilinear, 128b (tex/clk)	6
HiZ Rate, (ppc)	3x128
IZ Rate, (ppc)	3x16
Stencil Rate (ppc)	3x128
(500 MHz, DDR-4267; Range depends on dynamic compression ratio)	
Pixel Rate, fill, 32bpp (pix/clk, RCC hit)	24
Pixel Rate, fill, 32bpp (pix/clk, LLC hit @ 1.0x unslice clk)	24
Pixel Rate, fill, 32bpp (pix/clk, LLC hit, @ 1.5x unslice clk)	N/A
Pixel Rate, fill, 32bpp (pix/clk, memory, @ 1.0x unslice clk)	24
Pixel Rate, fill, 32bpp (pix/clk, memory, @ 1.5x unslice clk)	N/A
(500 MHz, DDR-2400 or eDRAM; Range depends on dynamic compression ratio)	
Pixel Rate, blend, 32bpp (p/clk, RCC hit)	24
Pixel Rate, blend, 32bpp (p/clk, RCC miss, @ 1.0x unslice clk)	24
Pixel Rate, blend, 32bpp (p/clk, RCC miss, @ 1.5x unslice clk)	N/A

Product Configuration Attribute Table	
Product Family	**DG1**
Architectural Name	**1x6x16**
SKU Name	**POR**
Pixel Rate, blend, 32bpp (pix/clk, memory, @ 1.0x unslice clk)	17-24
Pixel Rate, blend, 32bpp (pix/clk, memory, @ 1.5x unslice clk)	N/A

Notes:

* Architectural Name = Slice Count x Subslice Count x EUs per Subslice

(1) L3 cache and URB share the write bandwidth. Read bandwidths of 64B/clk can be achieved independently

(2) URB/Data cache/Tile cache/Command buffer cache sizes are programmable. Indicative values presented in this table.

Device Attributes Media 12.1

Product Configuration Attribute Table	
Product Family	**DG1**
Architectural Name	**1x6x16**
SKU Name	**POR**
Media Attributes	
Samplers (VME)	6
Samplers (AVS)	6
VDBox Instances (See)	2
VEBox Instances	1
SFC Instances	2
WGBox Instances*	0

Notes:

- *WGBOX instances are removed across all SKUs

Device Attributes Display 12.1

Refer to the Display Overview chapter.

Steppings and Device IDs

SKUs and Device IDs

The following table details all currently planned SKUs. This information is subject to change at any time based on roadmap plans.

Index	Config	EUs	VDBoxes	TDP	Dev2 ID	RevID	Gfx String	SoC Version	Comments
4	1x6x16	96	2	25W	0x4905	0x1	Intel® Iris® Xe MAX Graphics	B0	DG1 Mobile mother board down
6	1x6x16	96	2	25W	0x4907	0x1	Intel Server GPU SG-18M	B0	SG1 Server SKU, no display