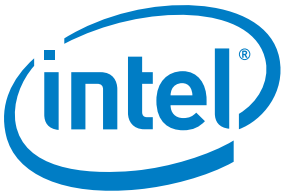


Product Marking Information for Intel® FPGA Arria® Devices

Arria II , Arria V

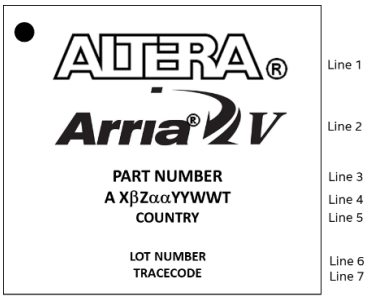
Version: **1.0**

Last updated: **August, 2020**

Reference Number: 11G-00016

Contents

1.0 Top Mark Layout for Intel FPGA Arria Devices



Line 1	Company (ALTERA®) logo
Line 2	Device Family logo
Line 3	Device Name
Line 4	Date Code
Line 5	Country where device is assembled (COO)
Line 6	Top ID* (FPO/Lot#)
Line 7	Top ID* (Tracecode)

*Certain packages (RQFP, EQUAD) will have the Top ID marked in a single line

Date Code: A Xβ Z αα YYWWT

A, X, β, Z, αα, T	Manufacturing Identifiers
YYWW	YY = Year, WW = Workweek in a 6-week date code window

Example:

Line 1	ALTERA®
Line 2	Arria® II
Line 3	EP2AZ225HF40I3N
Line 4	U HAF481913A
Line 5	MALAYSIA
Line 6	S908BP01
Line 7	3P2UA9D0P

6-week Date Code Scheme

Work Week	Date Code
1 – 6	YY01
7 – 12	YY07
13 – 18	YY13
19 – 24	YY19
25 – 30	YY25
31 – 36	YY31
37 – 42	YY37
43 – 48	YY43
49 – 53	YY49

2.0 Document Revision History

Date	Version	Changes
August 2020	1.0	Initial release.