WHITE PAPER

FPGA

The Breakthrough Advantage for FPGAs with Tri-Gate Technology

Transistor design transitions from traditional planar to 3-D structures provide a significant boost in the capabilities of high-performance programmable logic.

Authors

Ryan Kenny
Senior Product Marketing Manager
Intel Programmable Solutions Group

Jeff Watt
Technical Fellow
Intel Programmable Solutions Group

Table of Contents

Introduction

In February 2013, Altera® and Intel® Corporation jointly announced that the next generation of Altera's highest performance FPGA products would be produced using Intel's 14 nm 3-D Tri-Gate transistor technology exclusively. In December 2015, Intel completed the acquisition of Altera. This makes Intel the exclusive major FPGA provider of the most advanced, highest performance semiconductor technology available. To understand the impact of Tri-Gate technology on the capabilities of high-performance FPGAs, and how significant this advantage is in digital circuit speed, power, and production availability, a background on the development and state of Tri-Gate and related technologies is offered here.

Transistor design background

In 1947 the first transistor, a germanium 'point-contact' structure, was demonstrated at Bell Laboratories. Silicon was first used to produce bipolar transistors in 1954, but it was not until 1960 that the first silicon metal oxide semiconductor field-effect transistor (MOSFET) was built. The earliest MOSFETs were 2D planar devices with current flowing along the surface of the silicon under the gate. The basic structure of MOSFET devices has remained substantially unchanged for over 50 years.

Since the prediction or proclamation of Moore's Law in 1965, many additional enhancements and improvements have been made to the manufacture and optimization of MOSFET technology in order to enshrine Moore's Law in the vocabulary and product planning cycles of the semiconductor industry. In the last 10 years, the continued improvement in MOSFET performance and power has been achieved by breakthroughs in strained silicon, and High-K metal gate technology.

It was not until the publication of a paper by Digh Hisamoto and a team of other researchers at Hitachi Central Research Laboratory in 1991 that the potential for 3-D, or 'wraparound' gate transistor technology, to enhance MOSFET performance and eliminate short channel effects, was recognized. This paper called the proposed 3-D structure 'depleted lean-channel transistor', or DELTA [1]. In 1997 the Defense Advanced Research Projects Agency (DARPA) awarded a contract to a research group at the University of California, Berkeley, to develop a deep sub-micron transistor based on the DELTA concept. One of the earliest publications resulting from this research in 1999 dubbed the device a 'FinFET' for the fin-like structure at the center of the transistor geometry [2].

Important turning point in transistor technology

Continued optimization and manufacturability studies on 3-D transistor structures continued at research and development organizations in leading semiconductor companies. Some of the process and patent development has been published

and publicly shared, and some development remained in corporate labs.

The research investment interests of the semiconductor industry are driven by the International Technology Roadmap for Semiconductors (ITRS), which is coordinated and published by a consortium of manufacturers, suppliers, and research institutes. The ITRS defines transistor technology requirements to achieve continued improvement in performance, power, and density along with options which should be explored to achieve the goals. The ITRS and its public documentation captures conclusions and recommendations regarding manufacturing capabilities like strained silicon and High-K metal gate, and now the use of 3-D transistor technologies to maintain the benefits of Moore's law. Based on documents produced by the ITRS and an examination of academic papers and patent filings, research into 3-D transistor technologies has grown dramatically in the last decade.

Adoption and research

Two important pronouncements occurred in the last two years that have propelled the 3-D transistor structure into the industry spotlight, and into a permanent place in the technology story of MOSFET transistors.

The first announcement was by Intel Corporation on 4th of May, 2011, about their Tri-Gate transistor design that had been selected for the design and manufacture of their 22 nm semiconductor products. This was preceded by a decade of research and development taking advantage of the work of Hisamoto and others in FinFET development and optimization. It represented both a solid acknowledgment of the feasibility and cost-effectiveness of the Tri-Gate transistor structure in volume semiconductor production, as well as a continued declaration of leadership by Intel in semiconductor technology.

The second announcement was the publication of ITRS technology roadmaps, with contributions from many other semiconductor manufacturing companies that identified 3-D transistor technology as the primary enabler of all incremental semiconductor improvement beyond the 20 nm or 22 nm design node.

Primary advantages of Tri-Gate design

The 3-D geometry and structure of the Tri-Gate transistor provides a host of important improvements over the planar transistor structure, all related to the 'wrap-around' effect of the MOSFET 'gate' around the source-to-drain 'channel.' These advantages manifest in:

- Improved performance
- Reduced active and leakage power
- Transistor design density
- Reduced transistor susceptibility to charged particle single event upsets (SEU)

The key performance advantage of Tri-Gate transistor geometries over traditional planar geometries can be found in the effective width of the conducting channel. The current drive capability and performance of a transistor is directly proportional to its effective channel width. The effective channel width can be significantly enhanced in a 3-D

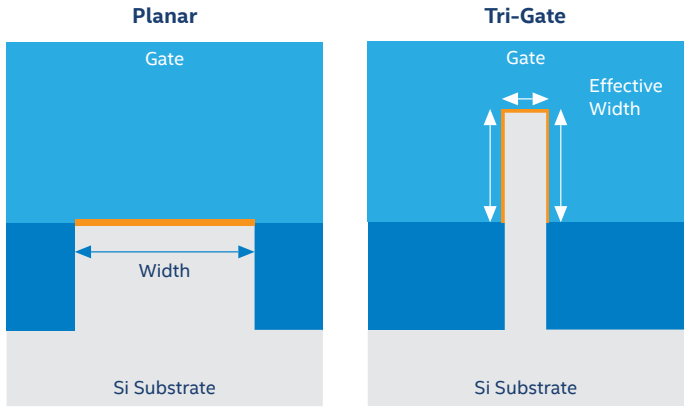

Figure 1. Effective Channel Widths of Planar and Tri-Gate Transistor Structures

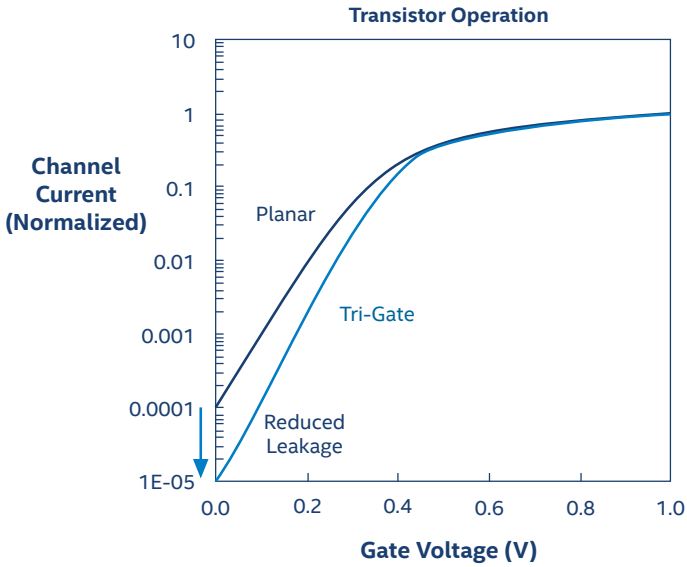

Figure 2. Tri-Gate Transistor Structures Provide Steeper Voltage Curves

transistor structure relative to a planar transistor because of the ability to extend the width in the third dimension without any impact on the layout area as shown in Figure 1. This provides the potential for both enhanced design flexibility for the designer of the transistor, as well as increased performance without the same penalties in 2-D area which exist when enhancing channel width in a planar transistor.

The power advantage results from the improved control of the channel by the gate's electric field on three sides of the fin. This reduces the sub threshold leakage current from source to drain in the 'off' state as compared to a planar transistor. In addition, the power supply voltage can be significantly reduced with Tri-Gate transistors while maintaining superior speed due to the increased effective width compared to a planar transistor. The combination of lower supply voltage and reduced leakage current results in substantial power savings.

As explained by Intel Corporation at their Intel Developer Forums (2011, 2012), this power advantage is created by an effectively steeper transistor voltage curve for Tri-Gate transistors, as shown in Figure 2. Transistor designers can take advantage of this steeper curve with either a significant

reduction in leakage current for the same performance of a planar transistor, or substantially higher performance (transistor operation speed), or a combination of both.

Each new generation of silicon manufacturing technology generally involves a geometry shrink, or reduction in overall gate and transistor structure, that results in higher density and more capable silicon. The 3-D Tri-Gate structure itself also accommodates higher density transistor designs by extending the transistor width characteristic into the third dimension. This allows designers the ability to trade off the size and width of the transistor 'fin' based on performance, power, and transistor density packing objectives. In the case of the move to 14 nm Tri-Gate design, Intel will benefit from both the transistor geometry shrink to 14 nm, and from further density improvements allowed by 3-D Tri-Gate transistor design.

The SEU advantage results from the small cross-sectional area connecting the fin to the substrate in the Tri-Gate structure. This creates a smaller area over which charge generated by ionizing particles can be collected than in a planar transistor structure. The reduced probability of charged particles causing bit-flips in transistor-based circuits is supported by early testing on Intel's 22 nm implementation of Tri-Gate transistors in their products.

Tri-Gate devices now in production

While the advantages of Tri-Gate transistors have been studied and known for some time, adoption and implementation is driven ultimately by technology and manufacturability, as well as cost-effectiveness.

The advanced state of semiconductor manufacturing at very small geometries (40 nm, 28 nm, 22 nm or 20 nm and beyond) requires research and development expenditures that now limit this technology to a handful of companies with capital expenditure capabilities in the billions of dollars. As a result, only a handful of manufacturers are able to capitalize on the known advantages of 3-D transistor technology. Intel Corporation is the only company to have made this design and manufacturing transition in 22 nm technology, and can provide data on the overall maturity and manufacturability of Tri-Gate transistors on a mass production scale. This data, as of the third quarter of 2014, includes over 500 million units of Tri-Gate transistor-based products.

Several known issues and characteristics of the 3-D gate structure have been acknowledged and addressed to achieve manufacturing and design maturity with the technology. These include the modeling of new parasitic capacitance values not modeled in traditional planar designs, layout dependent effects, and the use of double-patterning techniques using current lithographic equipment to form closely spaced fins.

The electronic design automation (EDA) community is also an important factor in the maturity and usability of FinFET and Tri-Gate design technology to the semiconductor designer. Starting in 2013, EDA companies began a great deal of publicity and user education revolving around the impact of Tri-Gate rules and flexibility in the design of future semiconductor products.

Impact on FPGA and other semiconductor device performance

The primary advantage of Tri-Gate technology to FPGA-based electronic product designer is the continuation of Moore's Law in the steady march of improvements in transistor density, performance, power, and cost-per-transistor. This sustains an industry of consumer electronics, computing platform development, software complexity advances, memory and storage growth, mobile device creativity and development, and business automation and productivity.

In addition, control over the static and active power dissipation of semiconductors improves tremendously with this technology. For users of FPGAs, this makes programmable logic that advances to 14 nm technology and beyond both power competitive with ASIC and ASSP design solutions on available competing design nodes, with even more significant advantages in programmability, performance, flexibility, Open Computing Language (OpenCL™)[§] software design entry, and integration of DSP, transceiver, hardened processor, and configurable I/Os.

- For more information, refer to the Meeting the Performance and Power Imperative of the Zettabyte Era with Generation 10 FPGAs and SoCs white paper.

Intel Corporation has provided data to their general investor community on distinct benefits they have achieved based on the production rollout of Tri-Gate technology on their microprocessor products. This data includes a reduction of over 50 percent in active power per transistor moving from 32 nm planar to 22 nm Tri-Gate design [(3)], improved defect density curves in 22 nm Tri-Gate as compared to 32 nm planar design [(3)], and reductions in SEU incidence rates from four times to ten times when moving from 32 nm planar to 22 nm Tri-Gate design [(4)].

Intel's leadership in transistor technologies

In several public forums, including the Intel Developer's Forums and investor's conferences, Intel identifies where they have demonstrated technology leadership in a variety of advances that have sustained the pace of Moore's Law. As shown in Figure 3, Intel has identified the number of years of production leadership they have achieved in bringing strained silicon and High-K metal gate technology to full production. In the case of 3-D Tri-Gate transistor technology, Intel estimates a lead of up to four years based on their production rollout of Tri-Gate technology at 22 nm in 2011.

According to former Intel CEO, Paul Otellini in their 16 April 2013 Earnings Call [(8)]:

"In the first quarter [of 2013], we shipped our 100 millionth 22 nanometer [Tri-Gate] processor, using our revolutionary 3-D transistor technology, while the rest of the industry works to ship its first unit."

Intel announced volume production of 14 nm Tri-Gate devices in August 2014, well ahead of competing foundries.

Another leadership advantage that will be held by Intel in their rollout of 14 nm technology can be traced to their very public 'tick-tock' strategy in process and microarchitecture

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introduction. Intel describes its tick-tock model here: With every "tick" cycle, Intel looks to advance manufacturing process technology and continue to deliver the expected benefits of Moore's Law to users. The typical increase in transistor density enables new capabilities, higher performance levels, and greater energy efficiency—all within a smaller, more capable version of the previous "tock" microarchitecture. In alternating "tock" cycles, expect Intel to use the previous "tick" cycle's manufacturing process technologies to introduce the next big innovation in processor microarchitecture.

Intel is firmly committed to a full process shrink in their move from 22 nm to 14 nm. Other competing foundries rolling out 16 nm or 14 nm FinFET process technologies are not implementing a full process node shrink to reduce the rollout risk of their first generation of FinFET technology.

Accessing the benefits of Tri-Gate technology through Intel FPGAs

Taking advantage of the significant benefits of the Tri-Gate technology is only possible for users of Intel high-density and high-performance FPGAs on the 14 nm technology process. This is the result of an exclusive manufacturing partnership between the two companies referenced in the introduction to this paper.

The substantial advantages of Tri-Gate silicon technologies will allow Intel to deliver previously unimaginable performance in FPGA and SoC products. This will include a historic doubling of core performance as compared to other high-end FPGAs, bringing FPGAs to the Gigahertz performance level. Overall active and static power numbers will reduce by up to 70 percent through a combination of process, architecture, and software advances, as well as efficiencies gained by consolidating multiple devices into fewer devices.

Intel FPGA users can begin designs today that take advantage of the significant performance and power efficiency benefits of Tri-Gate technology in FPGAs. This is possible by beginning designs with the Arria® 10 portfolio of 20 nm FPGA devices. Users can then take advantage of pin migration pathways from Arria 10 FPGA and SoC products to Intel Stratix® 10 FPGA and SoC (formerly Altera® Stratix 120 FPGAs and SoCs) products as they become available.

This allows FPGA users and system architects to begin designing products that can accommodate both the Arria 10 and Intel Stratix 10 product families with minimal board changes. This will allow you to get products to market with the highest performance and lowest power FPGAs that leverage 20 nm process technology and power reduction techniques, then advance these same products to the previously unimaginable performance and power efficiency of Intel's 14 nm Tri-Gate manufacturing process.

Conclusion

Identifying the highest performance FPGA products has historically been a subjective and parametric benchmarking process. But beginning with 14 nm Tri-Gate technology, the highest performance FPGAs will simply be the ones built on demonstrably superior transistor technology. Only Intel's 14 nm Tri-Gate Process offers a second generation of proven production technology. Only Intel's 14 nm process provides both the benefit of the Tri-Gate technology as well as the benefits of a full transistor process shrink. And, Intel is the only major FPGA company with access to this technology. Designing systems using Tri-Gate based technology will ensure that designers can take advantage of this performance leadership.

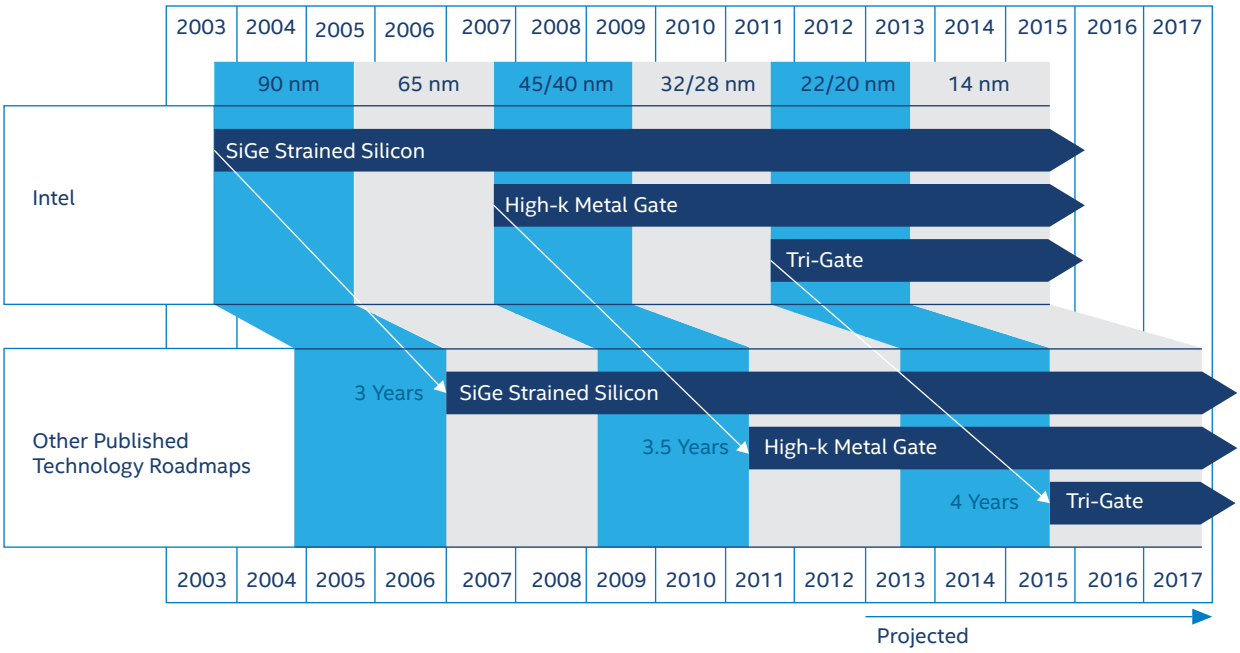

Figure 3. Intel's Demonstrated Transistor Technology Leadership

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Where to Get More Information

For more information about Intel and Intel Stratix 10 FPGAs, visit **https://www.altera.com/products/fpga/stratix-series/stratix-10/overview.html**