Backplane Applications with 28 nm FPGAs

WP-01185-1.1 White Paper

This white paper covers the challenges of backplane applications and how to use the features of Altera® Stratix® V GX and GS FPGAs to address the range of problems that are encountered in backplane applications such as 10GBASE-KR.

Introduction

As global communications and networking bandwidth demands continue to explode, communications equipment, servers, and other related equipment must continue to scale to meet the challenge. The latest generation of communication equipment utilizes sophisticated routing, switching, and transmission hardware to transfer data throughout networks and within datacenters. These systems integrate numerous line cards and other hardware typically residing on a backplane. The ability for FPGAs to drive backplanes is a key enabler for implementing these systems.

Backplane applications require transceivers that can drive electrical signals at high data rates upwards of 10.3125 Gbps per link on 10" to 40" backplanes. Increasing data rates and lengthening backplane channels pose significant challenges to designing backplane links and implementing transceivers, while maintaining low bit-error rate (BER) at the lowest power possible.

Altera's Stratix V GX/GS FPGAs transceivers offer a number of features designed to handle the challenges of backplane links, including high-speed backplane capable transceivers with low jitter at data rates up to 14.1 Gbps. These transceivers provide a variety of signal conditioning and equalization features, including:

- Transmit (TX) finite impulse response (FIR) pre-emphasis
- Continuous time linear equalization (CTLE)
- Decision feedback equalization (DFE)

These solutions are designed to provide the greatest flexibility and performance at the lowest power in an FPGA transceiver. This white paper covers the challenges of backplane applications and how to use the features of Stratix V GX and GS FPGAs to address the range of problems that are encountered in backplane applications such as 10GBASE-KR.

Backplane Characteristics and Solution Requirements

A high-speed backplane channel is a point-to-point connection that can be modeled as a long multi-layer, multi-link PCB channel to interconnect a transmitter and a receiver attached with connectors on either end, as illustrated in Figure 1. The overall PCB trace length can be as long as 1 m, its impedance must be controlled, and differential signaling is used.

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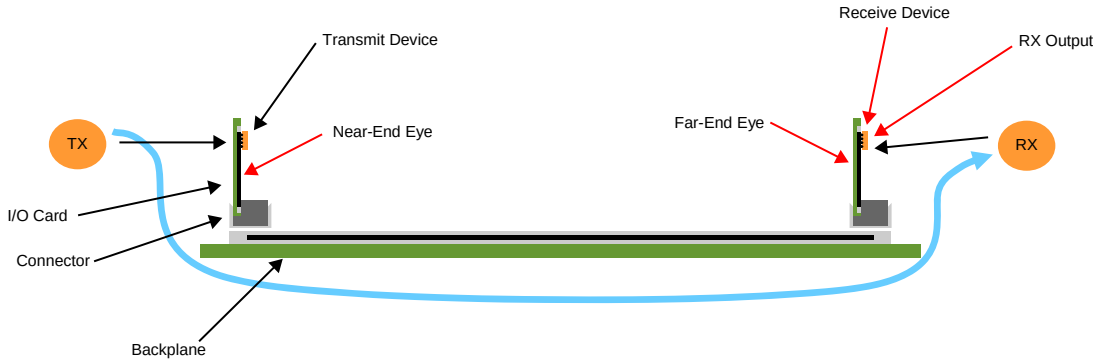
Figure 1. High-Speed Backplane Channel



The Backplane Challenge

When signal propagates from a transmitter to a receiver, signal quality degrades due to several undesirable electrical characteristics of the communication channel. Often times, a communication channel is constructed from PCB materials that are inherently lossy. In addition, there are various impedance discontinuities, each channel may induce noise to itself, and other neighboring signals may crosstalk into a given channel and appear as noise.

Mechanisms for Signal Degradation Across Backplanes

The mechanisms of signal degradation can be classified into the following causes:

- Insertion loss
  - Conductor loss
  - Dielectric loss
  - Return loss
  - Mode conversion
  - Radiation
- Polluted by noise
  - Induced by multiple reflections
  - Crosstalk from other channels

Although not exhaustive, this list will help designers to understand primary factors causing signal degradation, which can ultimately cause bit errors on a link. Once the cause of signal degradation in a design is known and understood, a range of transceiver tools can be used to mitigate the problem and ensure error free backplane links.

Insertion Loss

When travelling across a transmission medium such as PCB, electrical signals are attenuated as they propagate. The signal magnitude after propagating through a well-designed transmission line can be modeled as a frequency dependent relation, expressed by Equation 1.

Equation 1. Signal Magnitude Model

$$|v_{sig}(f)| = -20\log_{10}(e) \times (a_0 + a_1\sqrt{f} + a_2 f + a_3 f^2 + a_4 f^3)$$

Where f is the frequency of interest, and the coefficients a_0, a_1, and a_2 are the model factors. The factors a_0 and a_1 are due to conductor loss, and a_2 is due to dielectric loss. The factors a_3 and a_4 are due to other second- and third-order factors.

Conductor Loss

Copper is the primary metal material used to construct transmission line. Metal's DC resistance causes signal loss modeled by the coefficient a_0 which is proportional to the cross sectional area of the transmission line. For higher frequencies, the effective cross-sectional area decreases due to skin effect (the majority of the current tends to flow closer to the metal's surface) resulting in larger signal loss as modeled by the coefficient a_1. Smoothness or roughness of the metal surface also affects the signal loss amount due to skin effect.

Dielectric Loss

When the propagating signal changes its polarity, the polarization of the insulating laminate (dielectric material) also changes. The dielectric material's polarity change, however, lags behind the signal polarity change at high frequencies, which causes signal loss. The amount of this signal loss depends on dielectric material, and whose characteristic is indicated by dissipation factor Df or loss tangent tan δ. The coefficient a_2 is proportional to the tan δ (or dissipation factor), and therefore the dielectric signal loss is smaller with smaller tan δ PCB material. The tan δ of typical FR4 type laminate is 0.02. Nelco 4000-13 SI laminate with 0.008 tan δ is more suited for high-speed applications, and the Megtron-6 laminate with 0.002 tan δ provides supreme performance.

Other Loss Factors

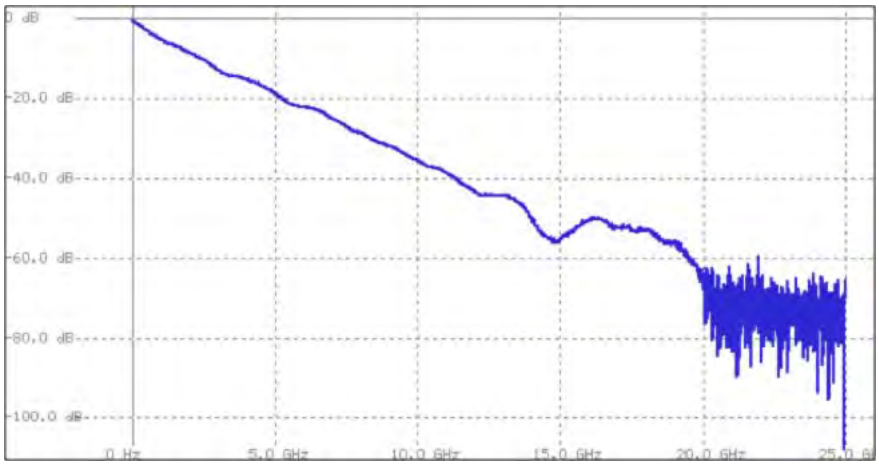
Although conductor loss and dielectric loss are primary loss factors, when transmission line design is not ideal several other loss factors need to be considered.

- *Return loss*—Return loss is a measure of signal energy loss due to reflection. When impedance discontinuity exists, part of the signal is reflected back at the impedance discontinuity point, thus reducing the signal energy being transmitted.
- *Mode conversion*—A balanced pair of transmission lines is used to send a differential signal. When the balance is broken, part of the differential signal is converted to a common mode signal, resulting in the energy loss of the differential signal.

- *Radiation*—Because all of the signals discussed here are electromagnetic waves, they can radiate into the air, resulting in the signal energy loss. Since a standing wave is the primary source of radiation in the backplane application, impedance control is the key to minimizing radiation. In addition, a stripline structure can be used instead of a microstrip structure for transmission line design. Reducing radiation is also important from EMI point of view.

Regardless of the mechanism, loss in backplanes is typically measured in terms of dB at the Nyquist frequency of the data stream, or Fs/2. For a 10.3125 Gbps system, Fs/2 is 5.15 GHz. Figure 2 shows an example insertion loss plot for a 30" Nelco 4000-13 SI backplane channel.

Figure 2. Insertion Loss Plot for 30" Nelco 4000-13 SI Backplane



Noise Degradation

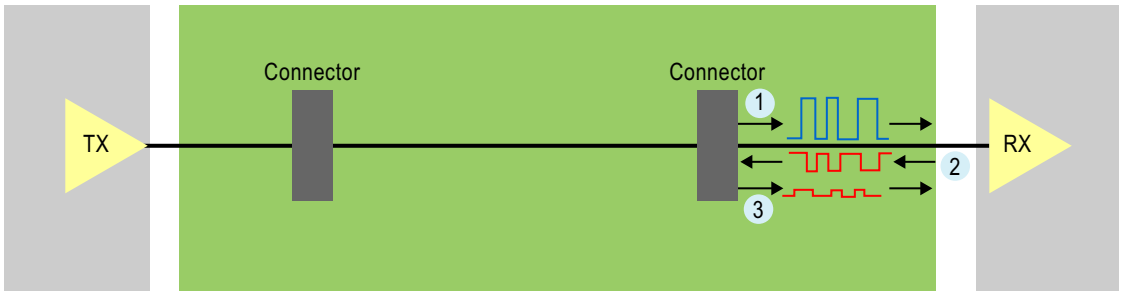
Aside from losses, other factors can contribute to signal degradation including noise induced by multiple reflections and crosstalk from neighboring channels that degrade the overall signal-to-noise ratio (SNR) in a link.

Noise Induced by Multiple Reflections

Though return loss is about impedance discontinuity and resulting reflection, this parameter does not directly tell its consequence on signal integrity. When there is more than one impedance discontinuity in a channel, which is often the case, multiple reflections occur among them, and the multiple-reflected signal is superimposed on the primary signal as noise. This self-induced noise in a channel degrades the signal quality.

This is illustrated in Figure 3. Signal (1) coming from the TX through the far end connector will reach a discontinuity. This could be a pin, via, or any other electrical discontinuity. Some of the original signal gets reflected at the discontinuity (2). Finally reflected signal will again reflect off of the connector with a time delay (3) and get superimposed at the RX input creating a composite signal 1+3.

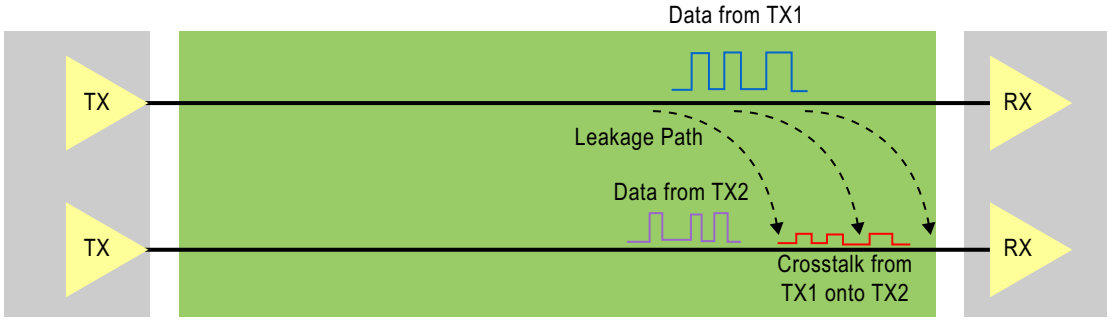
Figure 3. Mechanism for Noise Induced by Multiple Reflections



Crosstalk Noise from Other Channels

Daughterboards usually have multiple transceivers working together or independently, which include multiple differential pairs running in parallel on a backplane PCB. When these signals come close to each other, they leak and appear as noise as illustrated in Figure 4. Data from TX 1 can crosstalk onto the transmission line for TX 2.

Figure 4. Mechanism for Crosstalk Noise from Other Channels



Transceiver Requirements for Backplane Applications

To overcome the degradation across backplane links, Altera Stratix V transceivers offer a number of equalization tools to help compensate for channel non-idealities and ensure that a signal is received without error. Equalization can be employed at both the TX and receive (RX) ends of a link.

Three main equalization tools are offered:

- TX FIR, sometimes referred to as TX pre-emphasis
- CTLE on the RX side
- DFE on the RX side

General Strategy for Equalization

The transmission medium is a linear system, which creates an inverse transfer function. When this inverse transfer function is added to the transfer function of the link, the goal is to have a resultant transfer function that is relatively "flat" up to the required frequency. Figure 5 shows this simplified concept in a frequency domain.

Figure 5. Simplified Conceptual Equalization Scheme

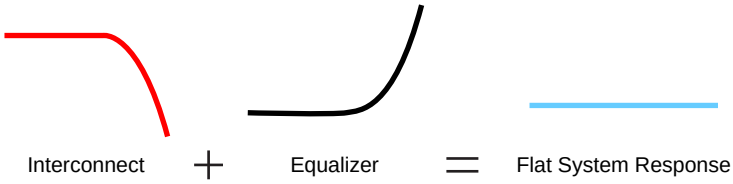
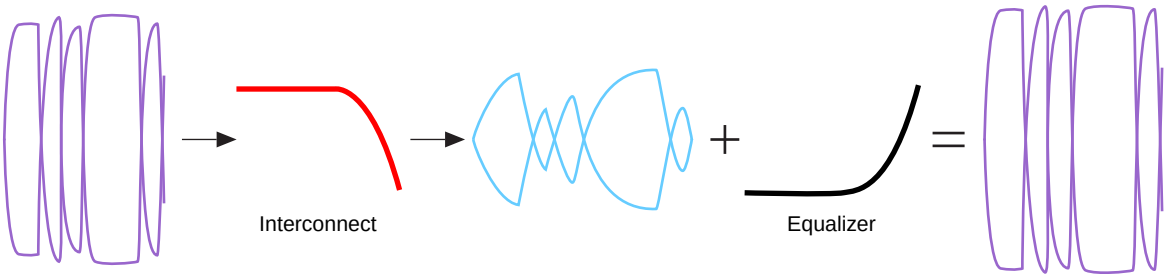


Figure 6 shows eye diagrams at three key points in the link. The first (left) is a launched signal from a transmitter. As this signal goes through the backplane, the resulting signal is attenuated (center). After the attenuated signal is sent through the equalizer, the original eye is restored (right). The attenuation in a link also causes high frequency transitions to spill into low frequency transitions creating inter-symbol interference (ISI).

Figure 6. Signals After Equalization



It is useful to note that since passive backplane links are linear systems, equalization can be applied at either the TX or RX side of the link to attain the desired effect of compensating for ISI.

A complicating factor is that the link may not have a simple attenuation curve. There may be multiple poles in the transfer function, as well as reflections, crosstalk, and resonances at some frequencies. Therefore, it is important to choose the right equalization method from the wide variety of available signal-conditioning techniques, such as TX pre-emphasis/de-emphasis, CTLE, and DFE.

TX Pre-Emphasis/De-Emphasis

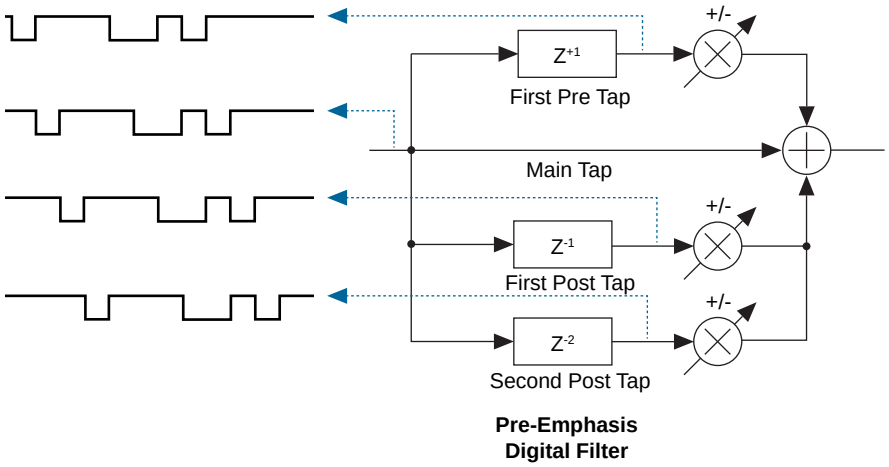
To equalize a signal, the transmitter can be pre-distorted so that after going through the interconnect, the resulting signal is clean for recovery at the receiver. This type of signal conditioning is called "emphasis," of which there are two types: pre-emphasis and de-emphasis.

TX pre-emphasis/de-emphasis is implemented at the TX driver by pre-conditioning the signal before it is launched into the channel so that the signal's high-frequency content is amplified (pre-emphasis) or the signal's low-frequency content is reduced (de-emphasis). The benefit of this method is relative simplicity and low power.

Figure 6 shows how a block diagram of how TX pre-emphasis and de-emphasis is conducted. All of the sampled data is available at the TX device. Delayed versions of transmitted data are created to be spaced apart by one unit interval (UI). This is accomplished by placing a bank of registers that holds both prior and upcoming serial data bits. Each delay bank is referred to as a "tap."

In addition to the main tap, Stratix V GX/GS FPGA transceivers provide one pre-tap to address pre-cursor ISI, and two post-taps to compensate for post-cursor ISI. This provides a total of four taps in the circuit, as shown in Figure 7. In addition, the coefficients on all four taps can be programmed individually, as well as the signs of pre- and second-post-taps. Fractional sampled data (1/2 UI) is available by taking information from the intermediate latch stages that commonly are used to create registers. Since both prior and upcoming (future) data bits are available, this signal-conditioning technique addresses both pre- and post-cursor ISI.

Figure 7. Block Diagram of Pre-Emphasis Implementation



The single pulse response in Figure 8 shows the time domain pre-emphasis response. It has pre-tap, followed by a main pulse and two post-taps.

Figure 8. Single Pulse Response of Pre-Emphasis Block

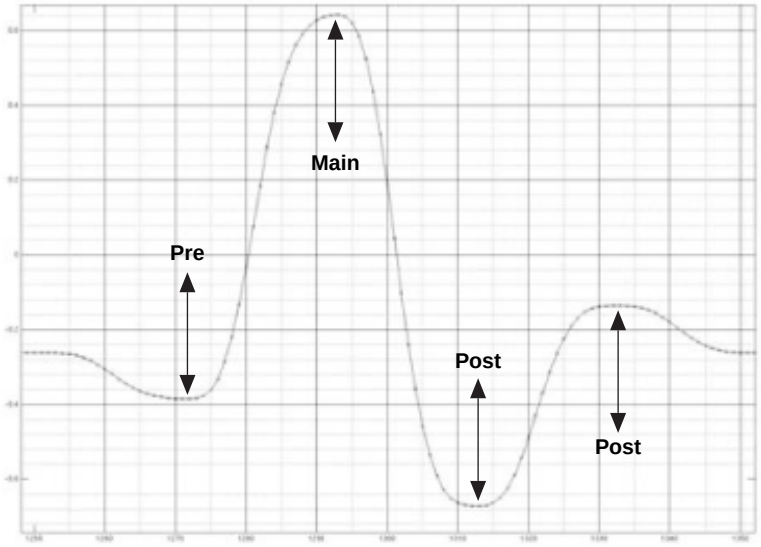
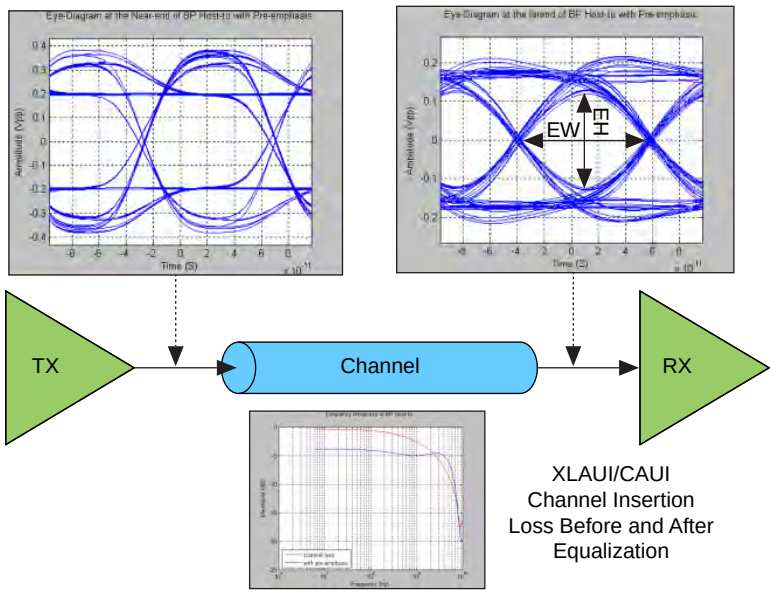


Figure 9 shows the pre-emphasis at the channel input and the open eye at the channel output for the XLAUI/CAUI channel-defined 40G/100G D1.0 specification operating at 10.3125 Gbps.

Figure 9. TX Pre-Emphasis at Near and Far Ends at 10.3125 Gbps with XLAUI/CAUI Channel



While it is a relatively simple technique, the main disadvantage of signal conditioning on the TX side is that TX pre-emphasis may increase the amount of crosstalk in backplane systems with substantial coupling between channels. Pre-conditioning a signal on the TX side will inject additional high-frequency content. After travelling through a lossy channel, the resulting signal has balanced high- and low-frequency content. The consequence is that in multiple serial link systems, the increased high-frequency content tends to escape into adjacent links, causing crosstalk. Nonetheless, if coupling in a channel is relatively low, pre-emphasis can be a very powerful, low-power solution to equalizing a backplane link.

CTLE

A complementary equalization technique, CTLE is typically implemented on the RX side of a link. Following the equalization theory, the linear equalizer simplifies the design, because non-sampled (that is, continuous time) implementations suffice. As a result, CTLE-based signal conditioning is usually the lowest power choice. Similar to TX pre-emphasis, CTLE addresses pre- and post-cursor ISI but in continuous time versus being limited to a pre-set number of TX sample points (taps).

Figure 10 shows an example of a first-order CTLE transfer function. A zero is inserted to compensate the poles in channel transfer function. This simple implementation has very low power consumption.

Figure 10. Example of a CTLE Transfer Function

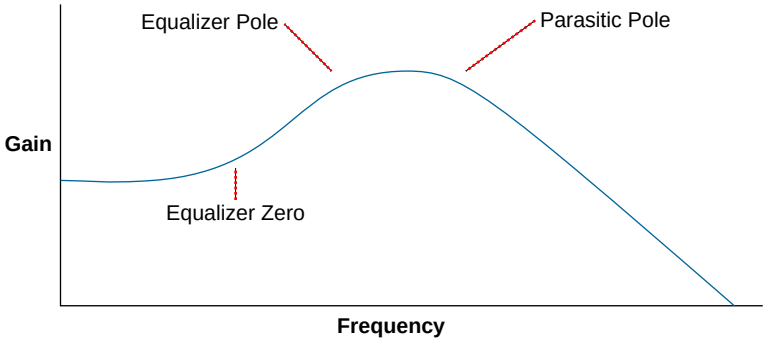
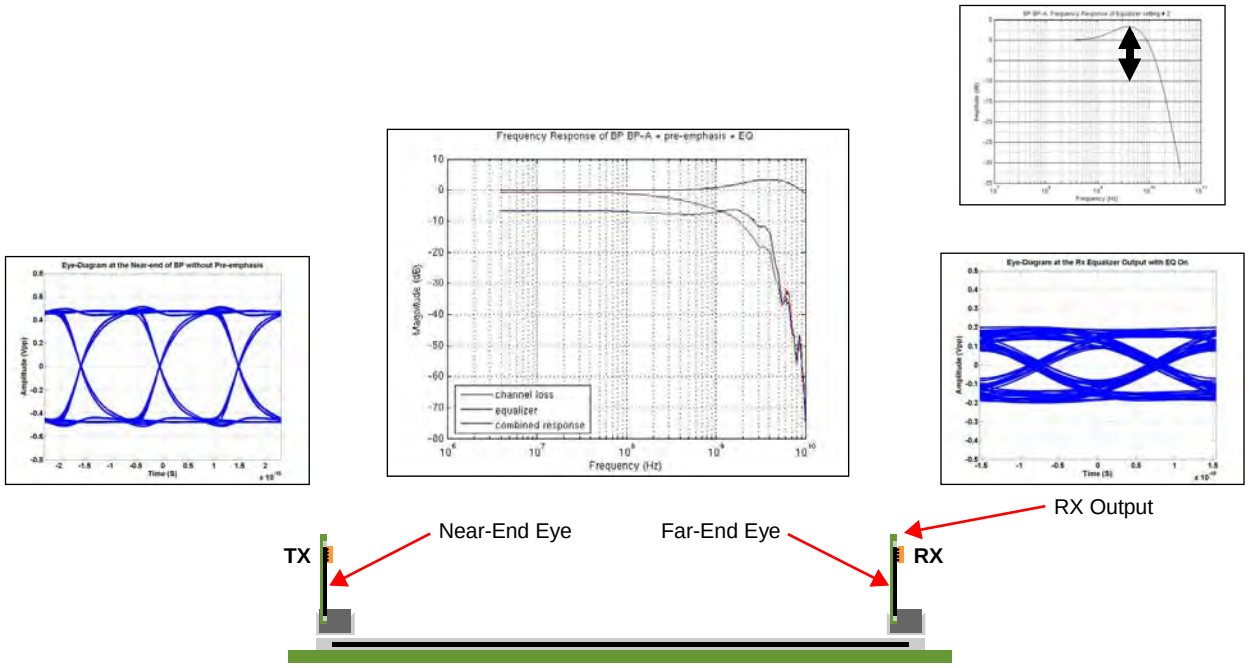


Figure 11 illustrates an example of using CTLE. For a given near-end TX signal, the far end shows an open eye when internal CTLE is enabled. It is clear that the amount of crosstalk is not increased in a system with CTLE versus TX emphasis, because of the reduced high frequency content at the TX driver.

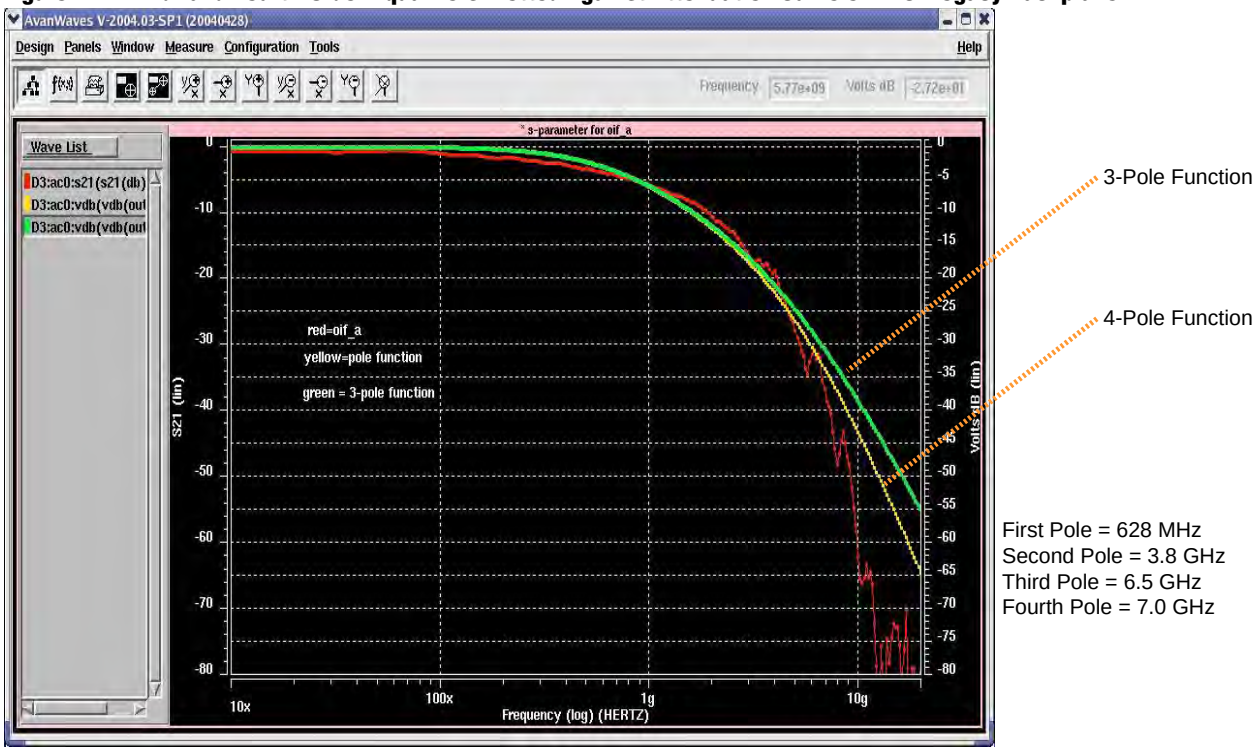
Figure 11. CTLE at Near End and Far End



As opposed to a single, first-order stage, multiple equalizer stages can be utilized for a given link at a selected data rate. Multiple stages not only increase the order of the resulting equalizer but also increase the maximum boost achieved in a given frequency interval.

Figure 12 shows the attenuation of the 40" XAUI legacy backplane, with third- and fourth-order pole functions also plotted. At 6.5 Gbps, a third-order function does a relatively good job of fitting the attenuation curve, while at 10 Gbps, a fourth-order function is required. Curve fitting with the number of poles tells the number of zeroes required in the equalization to undo the poles of the backplane. (High-level modeling is required to model the design exactly.)

Figure 12. Third- and Fourth-Order Equalizers Plotted Against Attenuation Curve of XAUI Legacy Backplane *(1)*

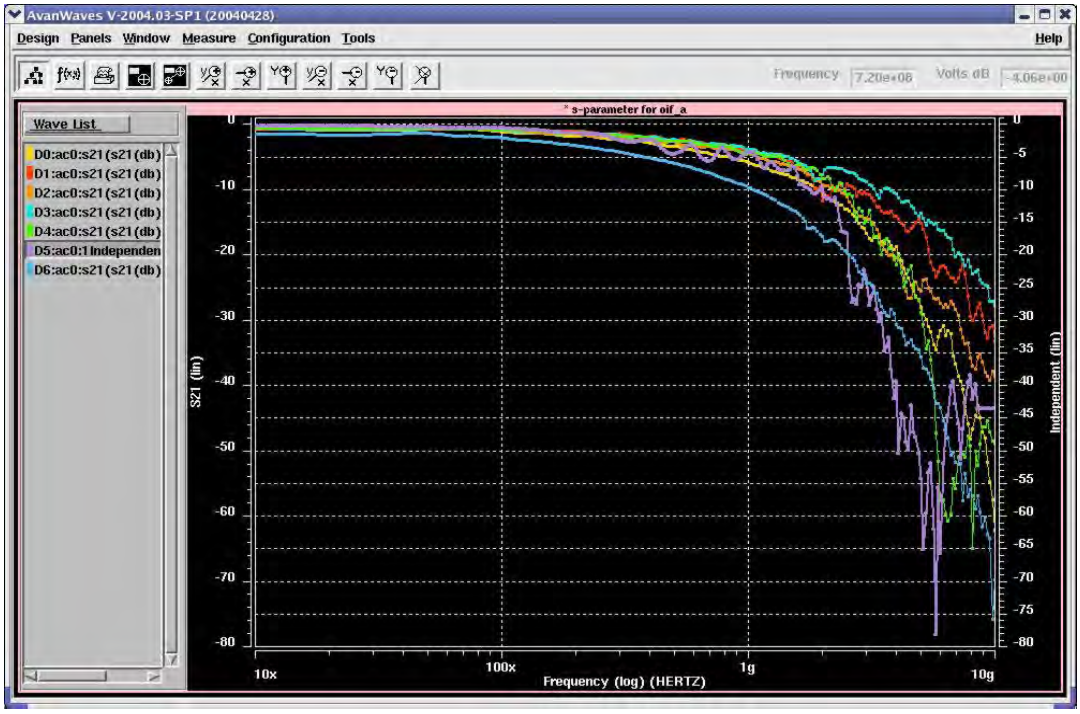


NOTE:

(1) A minimum of three zeros is required to enable 6 Gbps; four zeros are preferred to improve flexibility.

The few backplanes shown in Figure 13 have quite different attenuation characteristics, so the same equalization transfer curve will not fit all of these designs perfectly. An equalization scheme flexible enough to fit a majority of these curves is required.

Figure 13. Attenuation Curves of Sample Customer Backplanes *(1)*



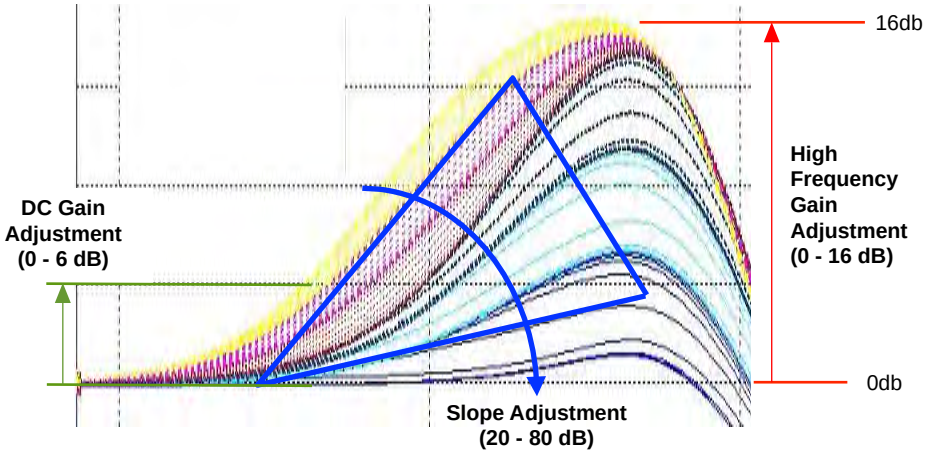
NOTE:

(1) Pole locations vary with different backplanes, cannot use the same pole function, and need greater flexibility.

Analysis of a database of backplanes up to 10.3125 Gbps shows that many equalizer needs are supported by a maximum slope of 80 dB/dec. Hence, RX CTLE has a minimum requirement of four equalizer stages, each with a 20 dB/dec slope and independent control over zero placement, to achieve the overall required curve fit. Each stage contributes a zero in the transfer function. Additionally, each stage is controlled independently to allow tuning of the zero location as well as the slope of the boost.

Stratix V FPGAs offer a wide range of CTLE boost settings to handle both long-reach applications, such as backplanes, as well as short-reach, chip-to-chip applications. The CTLE structure also supports DC gain adjustment. DC gain adjustment serves as a variable gain amplifier (VGA), which can also be leveraged in non-linear equalization schemes to increase the envelope of low frequency content for an optimal equalization solution. Integrating the variable DC gain into CTLE saves on circuit resources and lowers power consumption. Figure 14 shows a few of the over 240 possible ranges of boost and possible slopes using this architecture.

Figure 14. Equalization Curves of 4-Stage CTLE



It is important to note that a system that uses CTLE is well suited for real-time adaptation, since the signal information after the channel is readily available for processing and reconditioning at the RX side. Stratix V FPGAs offer CTLE capability with programmable bandwidth as well as automatic adaptation.

DFE

While CTLE is a very powerful tool for equalization, it will not provide sufficient equalization capability in all cases. In addition, CTLE can boost high frequency noise indiscriminately compared to the desired signal content. In the presence of crosstalk on a multi-lane backplane link or in the case of very high insertion loss where the SNR at the RX input is low, it is worthwhile to consider a scheme that can boost high-frequency signal content without boosting noise.

Unlike prior equalization schemes, DFE is a non-linear system, and must not only sample the data but also compute the new coefficient prior to the next sample. DFE works by actively shifting the incoming signal based on the history of the RX data. DFE removes signal energy that leaks from one bit to the following bit. This scheme allows DFE to cancel out post-cursor ISI. The advantage of DFE is to boost the power of highest frequency component of RX data without increasing noise power.

Stratix V FPGAs provide a DFE solution that consists of five taps and can compensate for an ISI tail or energy spilling out up to five UIs. Since the DFE system bases its decisions on prior bits, it only addresses post-cursor ISI and leaves the pre-cursor ISI uncompensated. As a result, CTLE is still required in a DFE system to accommodate the pre-cursor ISI. As such, CTLE and DFE are a good combination to address RX side equalization.

As shown in the conceptual diagram of Figure 15, DFE stores delayed versions of the data. The stored bit is multiplied by a coefficient and then summed with the incoming signal. The polarity of each coefficient is programmable.

Figure 15. Diagram of DFE Scheme

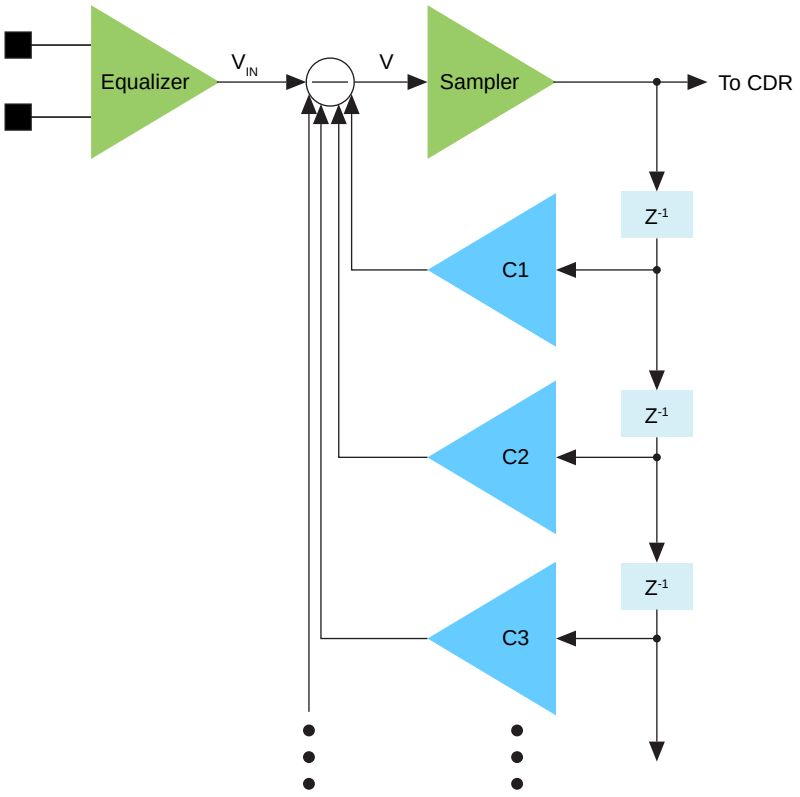
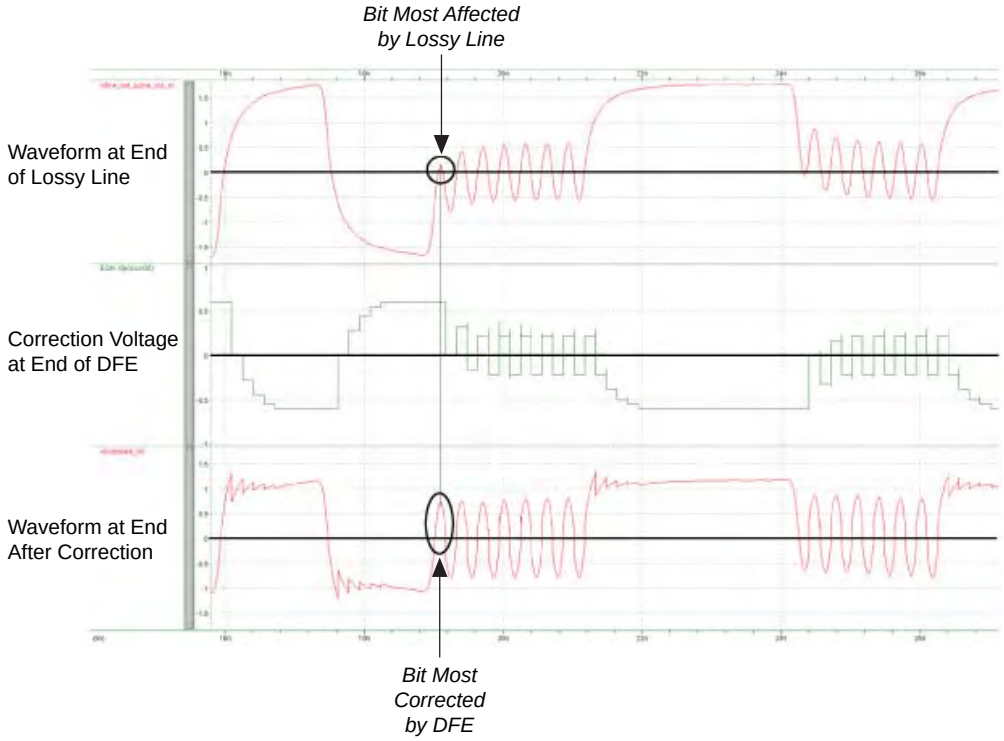


Figure 16 shows an incoming attenuated signal. The first bit after a long run of consecutive identical digits (CID) is most affected by the backplane attenuation and shows a baseline distortion. The correction voltage from DFE is summed with the incoming signal and generates a waveform after DFE that is much cleaner in terms of amplitude and timing. Although not shown, additional CTLE could help to further equalize the signal amplitude if required.

Figure 16. Diagram Showing Summation of Incoming Signal and DFE Feedback

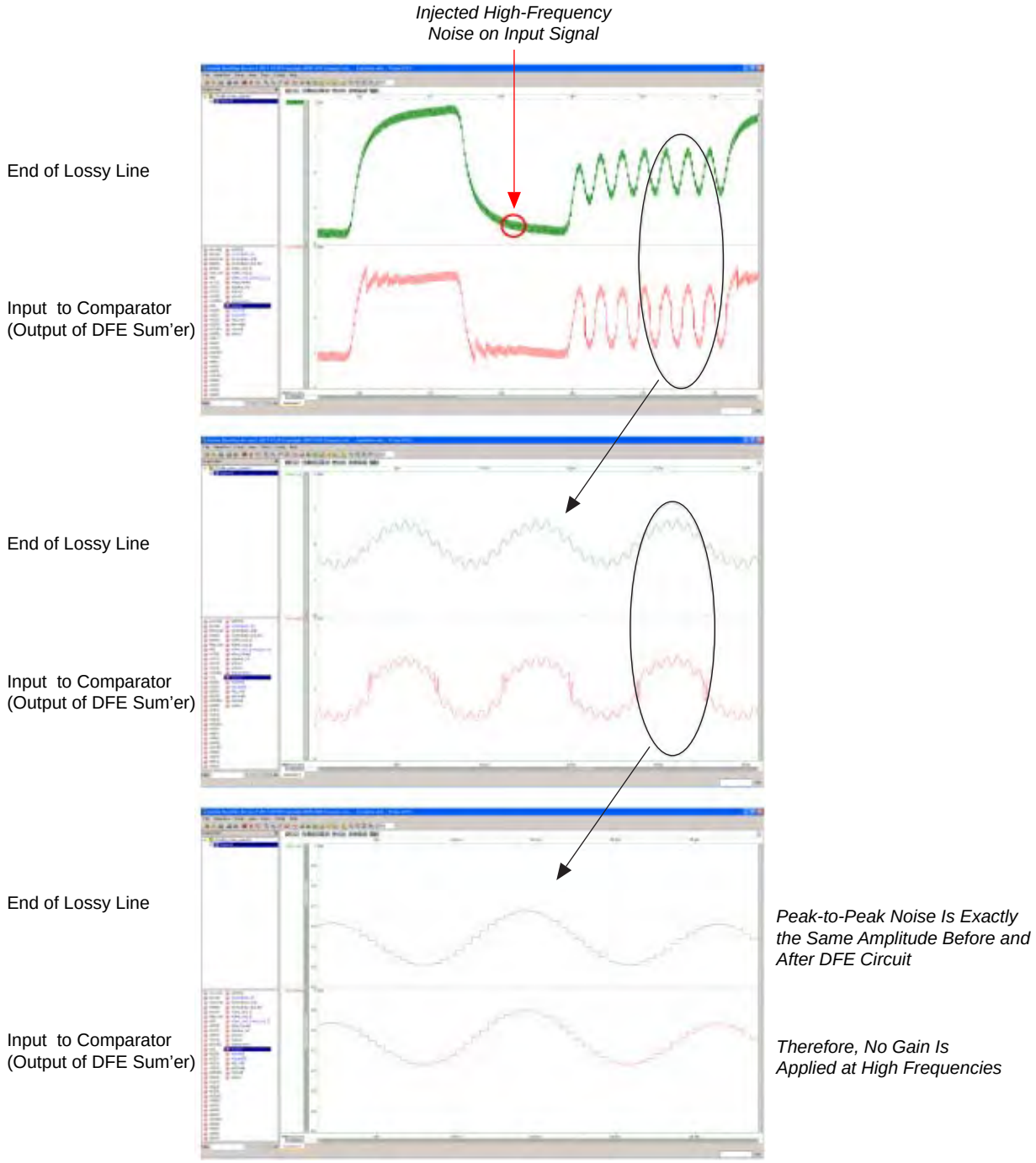


The major benefit of DFE is improved immunity in the case of crosstalk, especially when it is assumed to be additive white Gaussian noise (AWGN). The benefit of DFE in an AWGN system is understood by considering the SNR for cases of CTLE and DFE. The system has predominately post-cursor ISI (since DFE does not address pre-cursor ISI). The SNR is computed as a ratio of signal power to noise power. Since CTLE is continuous in time and does not really "know" or "need to know" the incoming signal spectral density, it boosts both signal and noise by equal amounts within a given frequency band.

One key assumption of an AWGN system is that noise power is equally distributed across a given frequency spectrum. The signal, unlike the AWGN, is limited in spectrum to the data rate and harmonics of the data rate. In the case when DFE is used to equalize the signal, the SNR improves. This is because DFE operates on sampled data, and not on the whole spectrum. Even though both signal and noise are present in the frequency spectrum of data and are boosted by DFE, boosting the fixed frequency spectrum improves the overall SNR.

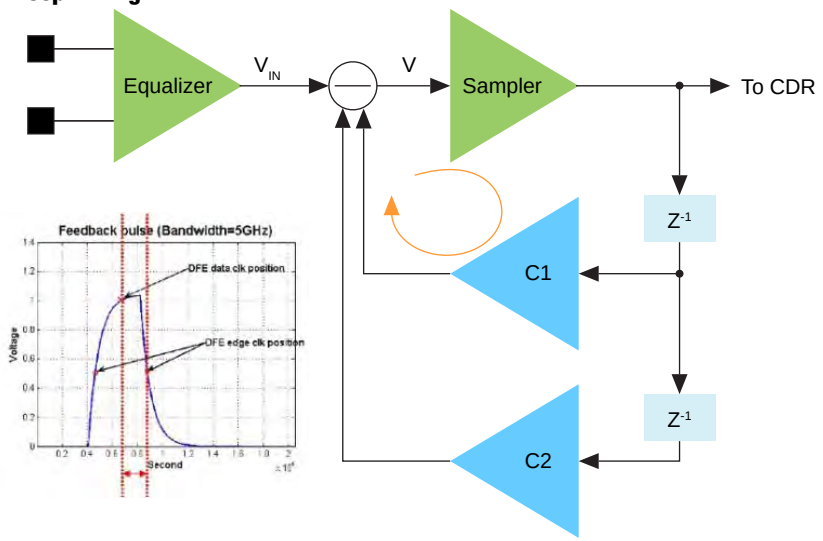
Figure 17 shows the previous attenuated signal and high-frequency noise superimposed on it. DFE boosts the signal based on the sampled data frequency harmonics, but a close inspection of the waveform shows that the peak-to-peak noise is not amplified. Hence, the SNR is actually improved by DFE. DFE has the advantage of improved SNR relative to CTLE, which can be an important parameter for systems with high crosstalk. However, the effectiveness of DFE in handling it can be reduced due to perform practical implementation challenges.

Figure 17. Waveforms Showing the Boosting of Intended Symbols and Not High Frequency Noise



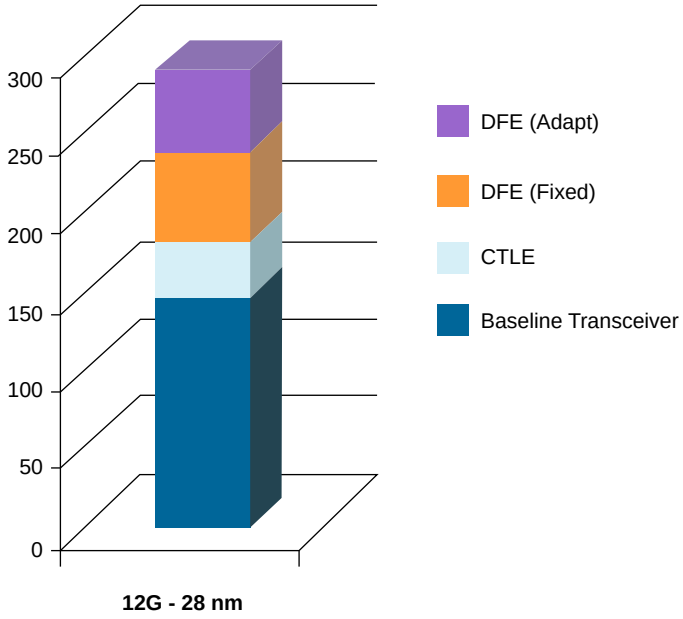
Timing closure in DFE hardware is often challenging. In many published high-speed applications, the first tap is not even available due to timing. As illustrated in Figure 18, the feedback loop timing is extremely tight. It is necessary to slice a bit, multiply by the coefficient, and sum it back to the input signal within 0.5 UI. At 10 Gbps, this is leaves 50 ps for the first successful tap operation. Additionally, the clock must be recovered from the serial datastream using the transceiver's CDR. The CDR introduces additional jitter, resulting in further reduction of the available timing margin, and further complicating the design. Many proprietary techniques are employed in DFE to meet these timing constraints.

Figure 18. Loop Timing



In addition to the timing constraints, a DFE system is rather complex and therefore requires a large amount of power compared to CTLE. DFE can easily increase transceiver power consumption by up to 2X, as shown in Figure 19. This amount of power consumption might be prohibitive for very dense backplane applications.

Figure 19. Additive Power Consumption for Various Equalization Features



The Need for Adaptive Equalization

One reason DFE is attractive is adaptive equalization, the assumed ability of the DFE engine to automatically compute coefficients for incoming bits based on the history of RX bits. The key feature of adaptive equalization is that it computes coefficients in real time without any prior channel or data pattern knowledge. As mentioned previously, above 8 Gbps data rate, the number of programmable signal conditioning settings is very large. Although it consumes more power, adaptive equalization is a very powerful tool as it is both fast and automatic. CTLE adaptation takes less than 250 µs to converge on a solution, while DFE adaptation typically takes about 10 µs. In Stratix V FPGAs, adaptive equalization is supported for both CTLE and DFE.

Both CTLE and DFE have one-time- and continuous-adaptation selections. One-time adaptation is intended for additional power savings, and is enabled during initial link training. However, it could be enabled periodically either over predetermined time intervals or by observing degradation in the system BER over time. In this setting, power is used only during the adaptation process, as once convergence is detected, the settings are frozen. Continuous adaptation constantly monitors the link in mission mode without disturbing normal traffic. Equalization settings adapt to track not only link aging but also voltage and temperature variations on both sides of the link.

Another goal of adaptive equalization is to make the system easy to use. Each link in the customer's design has different characteristics, so the amount of equalization required varies with backplane length, materials, data rate, and a host of other variables. With CTLE, the adaptation engine examines the output of all equalizer stages and adjusts the equalizer to increase or decrease the amount of equalization. In DFE, adaptation is used to automatically calculate tap coefficients.

Link Training

To setup a link using adaptive capabilities, the receiver must set up its settings automatically using some method. This process is referred to as link training. Ideally blind equalization, which means that no specific training pattern is required, is also one of the goals. In practice, however, the data must be DC balanced, and have reasonable transition density and run lengths.

The ideal patterns would be similar to PRBS-7 or PRBS-11 patterns or other 64b/66b encoded patterns with high transition density. This usually matches most customer applications very well, but for those customers with sub-optimal data patterns, a training pattern may still be used. In situations where an optimal solution cannot be found, the ability to read out adaptation values is provided inside the FPGA. These values are used as a starting point for manual adjustment.

Backplane Case Studies

Depending on a given backplane design, different equalization schemes will provide optimal results. To tackle the most aggressive backplanes, TX pre-emphasis, RX CTLE, and DFE might all be used in conjunction. Two cases and an example application are considered here.

Case 1: Loss Dominant Backplanes

For channels where insertion loss is the dominant mechanism for signal degradation, linear equalization schemes such as TX pre-emphasis and CTLE are the preferred method of equalization, as these solutions draw the least amount of power and provide substantial boost to compensate for loss. Stratix V FPGAs allow for up to 16 dB of CTLE gain and 4-tap TX pre-emphasis providing up to 12 dB of boost. Overall this is the lowest power solution for a given scenario drawing approximately 170 mW per channel at 10.3125 Gbps.

Case 2: Crosstalk Dominant Backplanes

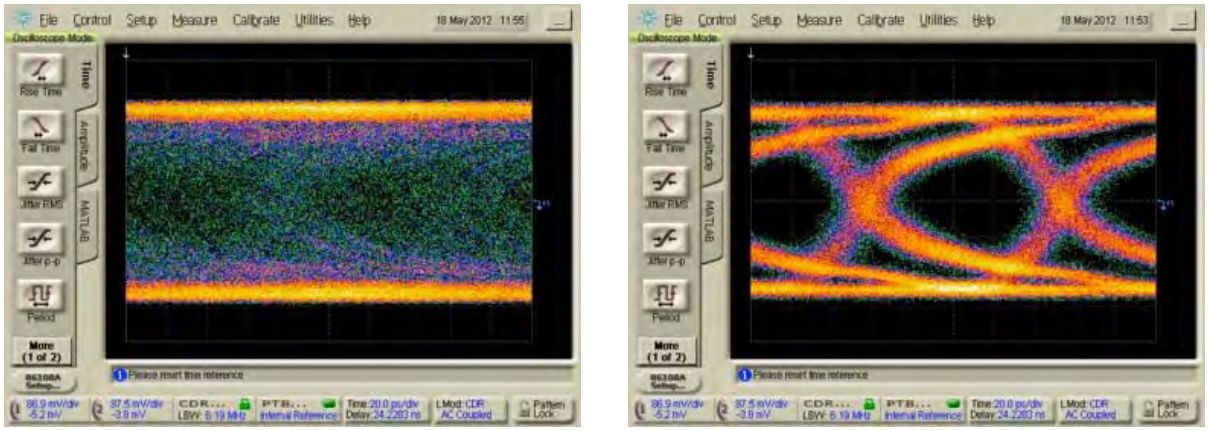
For channels where crosstalk and/or reflections are the dominant mechanism for signal degradation, DFE is often the preferred method of equalization. In these channels, crosstalk and reflections appear as noise relative to the signal of interest. Linear equalization schemes boost signal and noise equally, whereas DFE can boost signal with minimal boosting of noise which improves the SNR of the RX signal, thereby decreasing the chance for bit errors. Stratix V GX/GS FPGAs support a 5-tap DFE architecture in the situations where crosstalk and/or reflections are dominant. Although this can increase power up to 250 mW per channel, this architecture is well suited for this application when needed.

Example Application: 10GBASE-KR

The 10GBASE-KR standard is a common standard for backplane implementations. Figure 20 shows an eye diagram before and after equalization. The signal is a 10.3125 Gbps, PRBS-31 data pattern that is going through a 10GBASE-KR backplane with over 25 dB loss. The eye diagrams are observed at a pre-CDR reverse serial loopback diagnostic connection point just after the DFE circuit of a Stratix V FGPA. Without any equalization, no meaningful eye diagram can be recovered, as shown on the eye diagram on the left. After applying CTLE followed by adaptive DFE, the eye diagram on the right shows that this signal can be equalized and recovered with plenty of margin.

Figure 20. Eye Diagrams in a 10GBASE-KR Before and After Adaptive Equalization

RX Eye Diagram Without Equalization *RX Eye Diagram With CTLE+DFE Equalization*



Summary

Altera's Stratix V GX and GS FPGAs with transceivers offer a wide range of benefits for handling the most demanding backplane applications. These benefits include:

- Maximum data rate of 14.1 Gbps
- 4-tap TX pre-emphasis, the most TX pre-emphasis capability
- 16 dB CTLE gain, the highest gain CTLE solution with programmable bandwidth, covering the most backplane protocols
- Over 22 dB CTLE + DFE gain at 10.3125 Gbps with CTLE and DFE auto-adaptation
- Over 25 dB total system gain using TX pre-emphasis, CTLE, and DFE

All these solutions combined with the lowest power transceivers with the highest data rates in a backplane-capable FPGA make Altera Stratix V FPGAs the preferred option for multichannel backplane applications including 10GBASE-KR.

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Document Revision History

Table 1 shows the revision history for this document.

Table 1. Document Revision History

Date	Version	Changes
December 2012	1.1	Minor text edits.
October 2012	1.0	Initial release.