Stratix IV GT FPGA Features

		Maximum Resource Count for Stratix IV GT FPGAs (0.95 V)[1]					
		EP4S40G2	EP4S40G5	EP4S100G2	EP4S100G3	EP4S100G4	EP4S100G5
Resources	ALMs	91,200	212,480	91,200	116,480	141,440	212,480
	LEs (K)	228	531	228	291	354	531
	Registers[2]	182,400	424,960	182,400	232,960	282,880	424,960
	M9K memory blocks	1,235	1,280	1,235	936	1,248	1,280
	M144K memory blocks	22	64	22	36	48	64
	MLAB memory (Kb)	2,850	6,640	2,850	3,640	4,420	6,640
	Embedded memory (Kb)	14,283	20,736	14,283	13,608	18,144	20,736
	18 x 18 multipliers	1,288	1,024	1,288	832	1,024	1,024
Architectural Features	Global clock networks	16					
	Regional clock networks	64	88	64	88	88	88
	Periphery clock networks	88	112	88	112	112	112
	PLLs	8	8	8	12	12	12
	Design security	✓					
	Others	Plug and play signal integrity, programmable power technology					
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3[3]					
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, SSTL-18 (1 and II), SSTL-15 (I and II), SSTL-2 (I and II), HSTL-18 (I and II), HSTL-15 (I and II), HSTL-12 (I and II), Differential SSTL-18 (I and II), Differential SSTL-15 (I and II), Differential SSTL-2 (I and II), Differential HSTL-18 (I and II), Differential HSTL-15 (I and II), Differential HSTL-12 (I and II), Differential HSUL-12					
	Emulated LVDS channels, 1,100 Mbps	192	256	192	256	256	256
	LVDS channels, 1,600 Mbps (receive/transmit)	46/46					
	Embedded DPA circuitry	✓					
	OCT	Series, parallel, and differential					
	Transceiver count[4] (11.3 Gbps/8.5 Gbps/6.5 Gbps)	12/12/12	12/12/12	24/0/12	24/8/16	24/8/16	32/0/16
	PCIe hard IP blocks	2	2	2	4	4	4
	Memory devices supported	DDR3, DDR2, DDR, QDR II, QDR II+, RLDRAM 2, SDR					

Notes:

1. Available in industrial temperatures only (0oC to 100oC).

2. The base core logic register count is shown. The ALM can support three registers when used in LUTREG mode, which increases total register count by an additional 50%.

3. 3.3 V compliant, requires a 3.0 V power supply.

4. The total transceiver count is the sum of the 11.3, 8.5, and 6.5 Gbps transceivers.

Stratix IV GX FPGA Features

		Maximum Resource Count for Stratix IV GX FPGAs (0.9 V)						
		EP4SGX70	EP4SGX110	EP4SGX180	EP4SGX230	EP4SGX290	EP4SGX360	EP4SGX530
Resources	ALMs	29,040	42,240	70,300	91,200	116,480	141,440	212,480
	LEs (K)	73	106	176	228	291	354	531
	Registers[1]	58,080	84,480	140,600	182,400	232,960	282,880	424,960
	M9K memory blocks	462	660	950	1,235	936	1,248	1,280
	M144K memory blocks	16	16	20	22	36	48	64
	MLAB memory (Kb)	908	1,320	2,197	2,850	3,640	4,420	6,640
	Embedded memory (Kb)	6,462	8,244	11,430	14,283	13,608	18,144	20,736
	18 x 18 multipliers	384	512	920	1,288	832	1,040[2]	1,024
Architectural Features	Global clock networks	16						
	Regional clock networks	64	64	64	64	88	88	88
	Periphery clock networks	56	56	88	88	88	88	112
	PLLs	4	4	8	8	12	12	12
	Design security	✓						
	Others	Plug and play integrity, programmable power technology						
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3[3]						
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, SSTL-18 (1 and II), SSTL-15 (I and II), SSTL-2 (I and II), HSTL-18 (I and II), HSTL-15 (I and II), HSTL-12 (I and II), Differential SSTL-18 (I and II), Differential SSTL-15 (I and II), Differential SSTL-2 (I and II), Differential HSTL-18 (I and II), Differential HSTL-15 (I and II), Differential HSTL-12 (I and II), Differential HSUL-12						
	Emulated LVDS channels, 1,100 Mbps	128	128	192	192	256	256	256
	LVDS channels, 1,600 Mbps (receive/transmit)	56/56	56/56	88/88	88/88	98/98	98/98	98/98
	Embedded DPA circuitry							
	OCT	Series, parallel, and differential						
	Transceiver count (8.5 Gbps/6.5 Gbps)[4]	16/8	16/8	24/12	24/12	32/16	32/16	32/16
	PCIe hard IP blocks	2	2	2	2	4	4	4
	Memory devices supported	DDR3, DDR2, DDR, QDR II, QDR II+, RLDRAM 2, SDR						

Notes:
1. The base core logic register count is shown. The ALM can support three registers when used in LUTREG mode, which increases the total register count by an additional 50%.
2. The EP4SGX360N device has 1,024 18 x 18 multipliers.
3. 3.3 V compliant, requires a 3.0 V power supply.
4. The total transceiver count is the sum of 8.5 and 6.5 Gbps transceivers.

Stratix IV E FPGA Features

		Maximum Resource Count for Stratix IV E FPGAs (0.9 V)			
		EP4SE230	EP4SE360	EP4SE530	EP4SE820
Resources	ALMs	91,200	141,440	212,480	325,220
	LEs (K)	228	354	531	813
	Registers[1]	182,400	282,880	424,960	650,440
	M9K memory blocks	1,235	1,248	1,280	1,610
	M144K memory blocks	22	48	64	60
	MLAB memory (Kb)	2,850	4,420	6,640	10,163
	Embedded memory (Kb)	14,283	18,144	20,736	23,130
	18 x 18 multipliers	1,288	1,040	1,024	960
Architectural Features	Global clock networks	16			
	Regional clock networks	64	88	88	88
	Periphery clock networks	88	88	112	132
	PLLs	4	12	12	12
	Design security	✓			
	Others	Programmable power technology			
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3[2]			
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, SSTL-18 (1 and II), SSTL-15 (I and II), SSTL-2 (I and II), HSTL-18 (I and II), HSTL-15 (I and II), HSTL-12 (I and II), Differential SSTL-18 (I and II), Differential SSTL-15 (I and II), Differential SSTL-2 (I and II), Differential HSTL-18 (I and II), Differential HSTL-15 (I and II), Differential HSTL-12 (I and II), Differential HSUL-12			
	Emulated LVDS channels, 1,100 Mbps	128	256	256	288
	LVDS channels, 1,600 Mbps (receive/transmit)	56/56	88/88	112/112	132/132
	Embedded DPA circuitry	✓			
	OCT	Series, parallel, and differential			
	Memory devices supported	DDR3, DDR2, DDR, QDR II, QDR II+, RLDRAM 2, SDR			

Notes:
1. Base core logic register count is shown. The ALM can support three registers when used in LUTREG mode, which can increase the total register count by an additional 50%.
2. 3.3 V compliant, requires a 3.0 V power supply.

Stratix IV FPGA Series Package and I/O Matrices

		FBGA (F)[1]					
		780 pin 29 x 29 (mm) 1.0 mm pitch	**1,152 pin** 35 x 35 (mm) 1.0 mm pitch	**1,152 pin** 35 x 35 (mm) 1.0 mm pitch	**1,517 pin** 40 x 40 (mm) 1.0 mm pitch	**1,760 pin** 42.5 x 42.5 (mm) 1.0 mm pitch	**1,932 pin** 45 x 45 (mm) 1.0 mm pitch
Stratix IV GT FPGAs (0.95 V)	EP4S40G2				646 12+12+12		
	EP4S40G5				646[4] 12+12+12		
	EP4S100G2				646 24+0+12		
	EP4S100G3						769 24+8+16
	EP4S100G4						769 24+8+16
	EP4S100G5				646[4] 24+0+12		769 32+0+16
Stratix IV GX FPGAs (0.9 V)[2]	EP4SGX70	368 8+0		480 16+8			
	EP4SGX110	368 8+0	368 16+0	480 16+8			
	EP4SGX180	368 8+0	560 16+0	560 16+8	736 24+12		
	EP4SGX230	368 8+0	560 16+0	560 16+8	736 24+12		
	EP4SGX290	288[3] 16+0	560 16+0	560 16+8	736 24+12	864 24+12	904 32+16
	EP4SGX360	288[3] 16+0	560 16+0	560 16+8	736 24+12	864 24+12	904 32+16
	EP4SGX530			560[4] 16+8	736[4] 24+12	864 24+12	904 32+16
Stratix IV E FPGAs	EP4SE820		736[4]		960[4]	1,104	
	EP4SE530		736[4]		960[4]	960	
	EP4SE360	480[2]	736				
	EP4SE230	480					

Notes:
1. FineLine ball grid array.
2. I/O count does not include dedicated clock inputs that can be used as data inputs.
3. Hybrid package (flip chip) FBGA: 35 x 35 (mm) 1.0 mm pitch.
4. Hybrid package (flip chip) FBGA: 42.5 x 42.5 (mm) 1.0 mm pitch.

| 636
12+12+12 | Values on top indicate available user I/O pins; values on bottom indicate the sum of 11.3, 8.5, and 6.5 Gbps transceiver count. |

| 636
8+0 | Values on top indicate available user I/O pins; values at the bottom indicate the sum of 8.5 and 6.5 Gbps transceiver count. |

| 288 | Number indicates available user I/O pins. |

Vertical migration (same V_{cc}, GND, ISP, and input pins). For vertical migration, the number of user I/O pins may be less than the number stated in the table.
Stratix series devices are offered in commercial and industrial temperatures and RoHS-compliant packages. Stratix IV GT devices are only offered in industrial temperatures (0 ˚C to 100 ˚C).