40Gbps Ethernet MACPHY IP Hardware Demo Design using QSFP

Title

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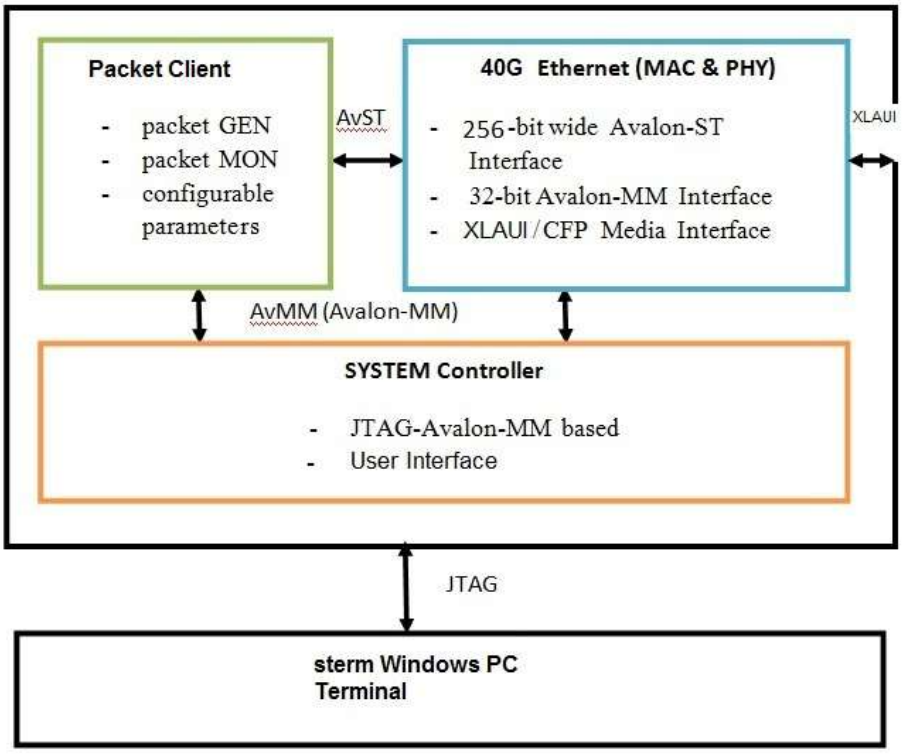
Introduction

This hardware demo design demonstrates the operation of Altera® 40-Gbps Ethernet MAC and PHY IP solution on a Stratix V device (5SGXEA7K2F40C2N). It is configured to demonstrate on a Stratix V GX FPGA Development Kit, also called PCIe Dev Kit using Altera development tool Quartus II 15.0 production release. This design provides a flexible test and demonstration platform which effectively control, test, and monitor 40Gbps Ethernet packets using internal serial PMA loopback and external optical loopback, MAC client side RX to TX parallel loopback.

This hardware demonstration reference design offers the following features:



• Stand-alone and easy-to-use design example with flexibility to dynamically select traffic profile.

• Uses a standard 256-bit Avalon-ST interface to connect to the Ethernet Packet Generator and Monitor.

• Provides both random and fixed size packet generator.

• System console GUI based flexible, reusable, and extendable user control interface allows users to dynamically configure and monitor any configuration registers provided by this demo design.

System Overview

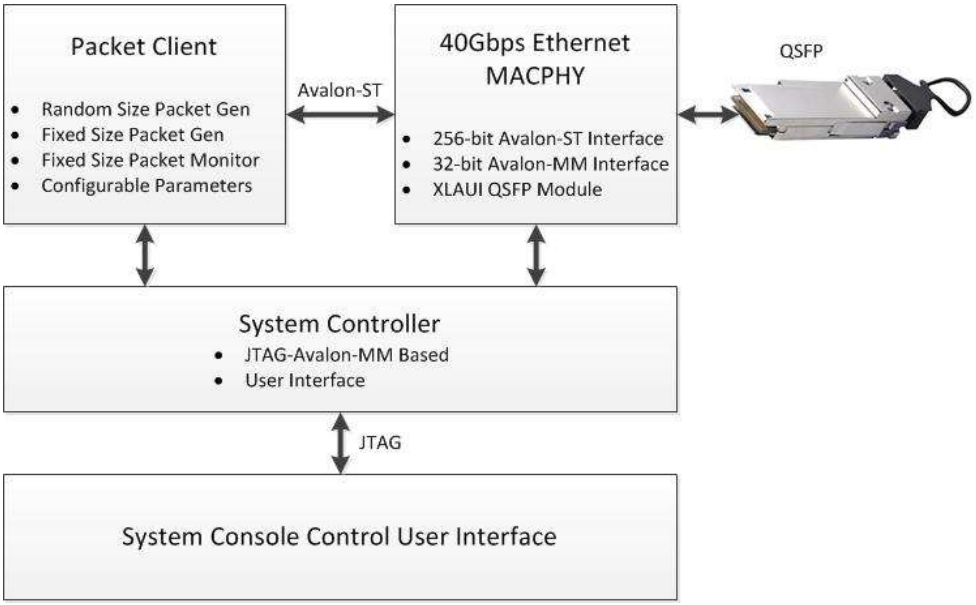
The hardware platform consists of three sub-systems:

• The 40G Ethernet MAC and PHY IP

• Packet Client with random and fixed size packet Generator and Monitor

• System console GUI for configuration and control of the system

This system can be represented by the following diagram:



40-Gbps Ethernet MAC and PHY IP

The Altera 40G Ethernet MAC and PHY IP core is implemented in compliance with the IEEE 803.3ba 2010 Higher Speed Ethernet Standard. This module handles the frame encapsulation and flow of data between a client logic and Ethernet network via a 40GbE Ethernet PCS and PMA (PHY). In the TX direction, the MAC accepts client frames, inserts inter-packet gap (IPG), preamble, start of frame delimiter (SFD), header, padding, and checksum before passing them to the PHY. The PHY encodes the MAC frame as required for reliable transmission over the media to the remote end. Similarly, in the RX direction, the

MAC accepts frames from the PHY, performs checks, updates statistics counters, strips out the CRC, preamble, and SFD, and passes the rest of the frame to the client.

Packet Client with Random Size Packet Generator and Monitor

The Packet Client includes a Packet Generator and a simple Packet Monitor. These modules have 256-bit Avalon-ST interface for the data-path and connect to the 40G Ethernet MAC. There is also a 32-bit Avalon-MM configuration and status interface associated with both the generator and the monitor. The generator can generate random packets. Monitor parses all packets received from MAC and checks the integrity of the packets.

Fixed Size Packet Generator and Monitor

The traffic generator is able to generate fixed size packets with length from 33-byte to 32768-byte. This traffic generator can be operated in two modes: continuous mode and burst mode. The packet payload be configured as either incremental or configurable fixed. The traffic monitor is able to check packet sequence number, packet length.

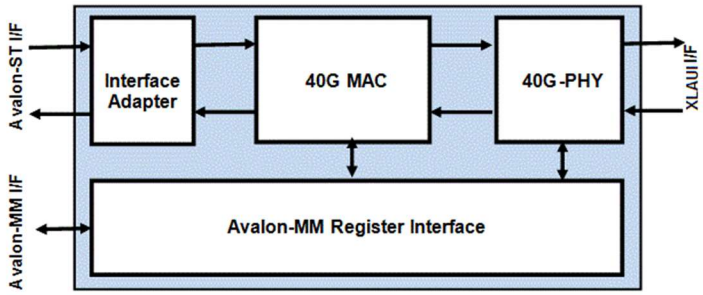
System Console Control Panels

This hardware demo design use System Console to run TCL script which is platform independent, can run on a PC (windows based operating system) or any Linux Machine.

There are four system console control panels designed for this hardware demo with straight forward hardware status monitoring and simple mouse click operation.

100G Ethernet MAC & PHY IP

As mentioned in previous sections, the 40G Ethernet sub-system consists of 40G MAC and PHY sub-modules. The MAC client side data path interface has two options: Avalon ST interface and Custom ST interface. This reference design uses an Avalon-ST interface which includes interface adapter. This adapter then provides a standard Avalon-ST interface for the MAC client. The MAC connects to the PHY core over XLGMII interface. The 40G Ethernet IP core can be demonstrated as the following simplified diagram:



Additional Functional Details of 40GE Ethernet IP Core

The additional details of the IP core can be found in the User guide. The IP core evaluation package and the user guide can be downloaded from here:40 Gbps and 100 Gbps Ethernet MegaCore Function

Start Guide for Hardware Demo design

The hardware demo design setup essentially consists of three parts:

- Stratix V GX FPGA Development Kit hardware setup
- Stratix V GX FPGA Development Kit software v12.0 setup, full installation of all files including reference manual, user guide, quick-start guide, BOM, layout, PCB, schematics, Board Update Portal example file, Board Test System example file, and others.
- Quartus II 15.0 and SignalTap II Logic Analyzer setup

The relevant setups for each of these components are provided in detail as shown below:

Stratix V GX FPGA Development Kit Hardware Setup

The Stratix V GX FPGA development board requires minimum hardware setup. A one time setting is required to ensure the following:

1. A QSFP module is plugged into an QSFP optical cage.

2. The DIP switches SW1 are pushed all to 8'b11111111.

3. The DIP switches SW3 are pushed all to 4'b0000.

4. The DIP switches SW4 [1:6] should be set as 6'b000110.

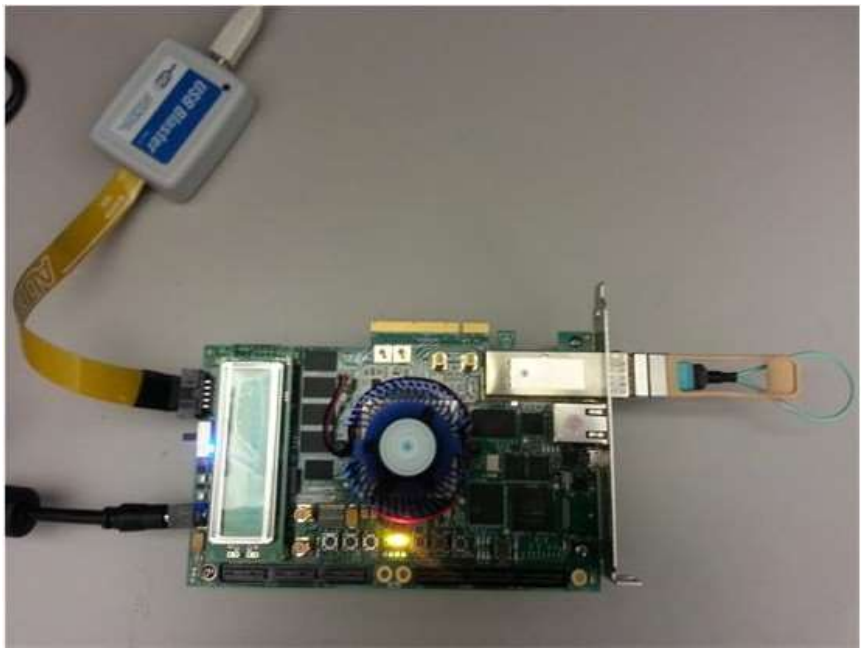
5. The DIP switch SW5 [1:4] should be set as 4'b1011.

6. The DIP switch SW6 [1:4] should be set as 4'b0001.

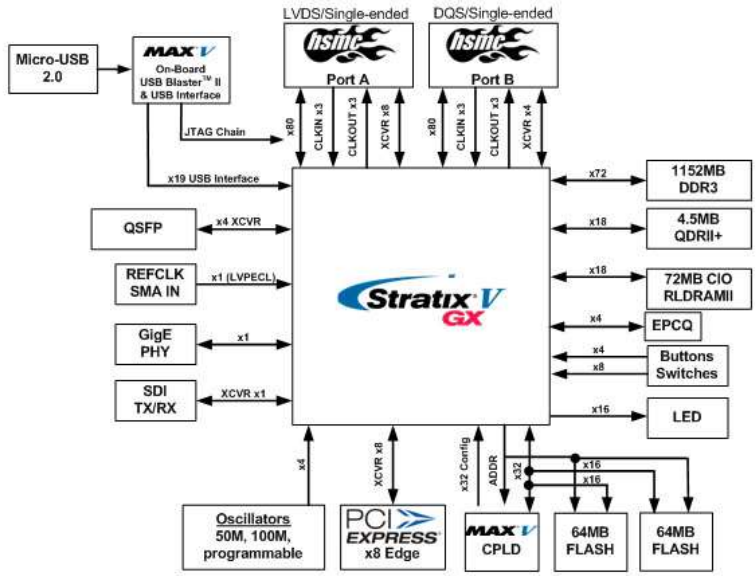
Before turning on power switch at the middle left of the development board, two cables are required to connect to development kit:

1. Power supply cable with adaptor to provide 19V DC voltage.

2. USB blaster cable connected between PC and development board.



Below is functional block diagram of Stratix V GX FPGA Development Kit.

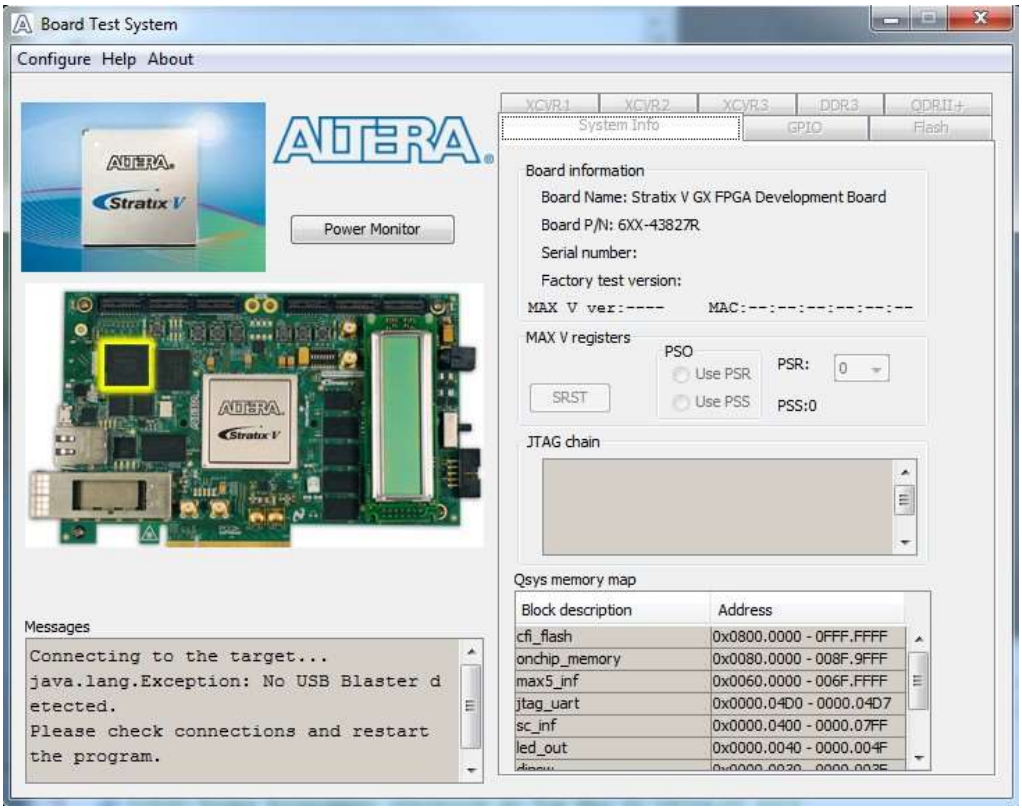


Stratix V GX FPGA Development Kit - Stratix V GX Edition v12.0 Software Setup

The Stratix V GX FPGA development kit – Stratix V GX Edition v12.0 Software from Stratix V GX FPGA Development Kit is required to be installed in order to use the Stratix V GX FPGA development board.

Full installation after running setup of v12.0 includes reference manual, user guide, quick-start guide, BOM, layout, PCB, schematics, Board Update Portal example file, Board Test System example file, and others. It also includes softwares for board test and clock control.

The Board Test System GUI is shown below:



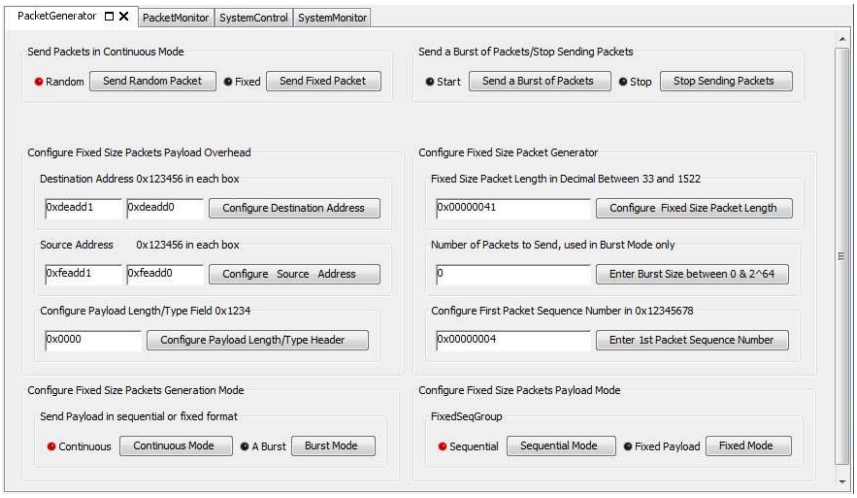
Quartus II 15.0 and System Console

After installing Quartus II 15.0, download the 40Gbps Hardware Demo Quick Start Guide which provides step by step instruction on how to open project, load SOF file and start system console.

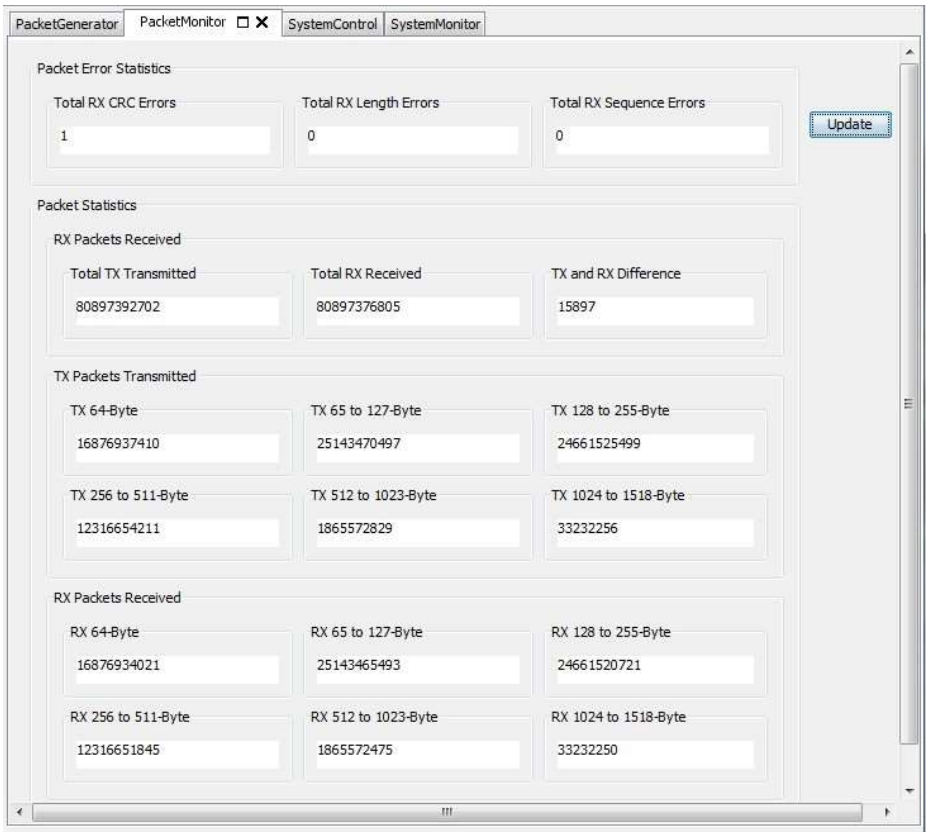
System Console GUI Control Panels

This hardware demo offers four GUI control panels using system console:

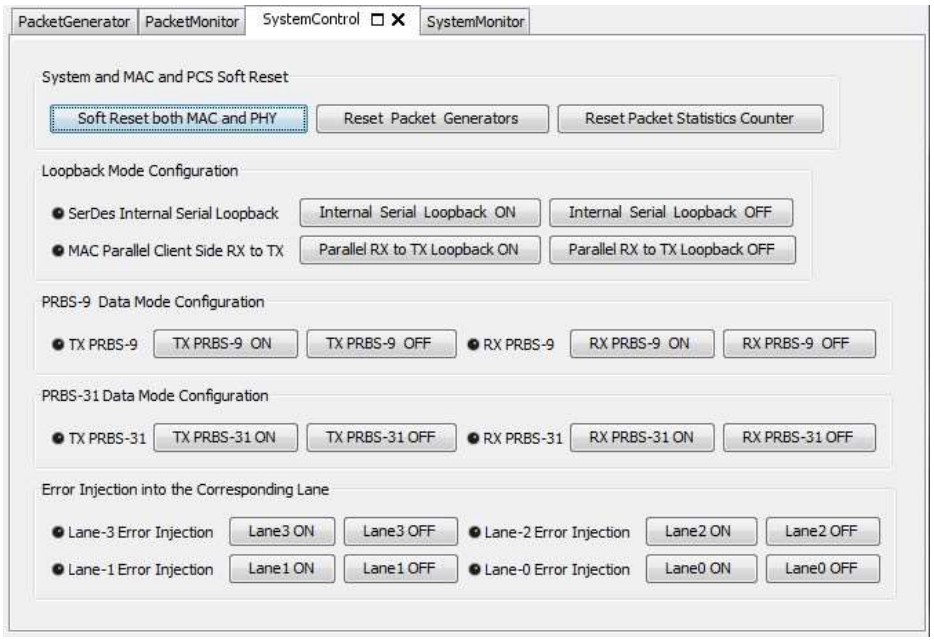
1. PacketGenerator GUI panel provides push button easy configuration on using fixed size and random size packet generators



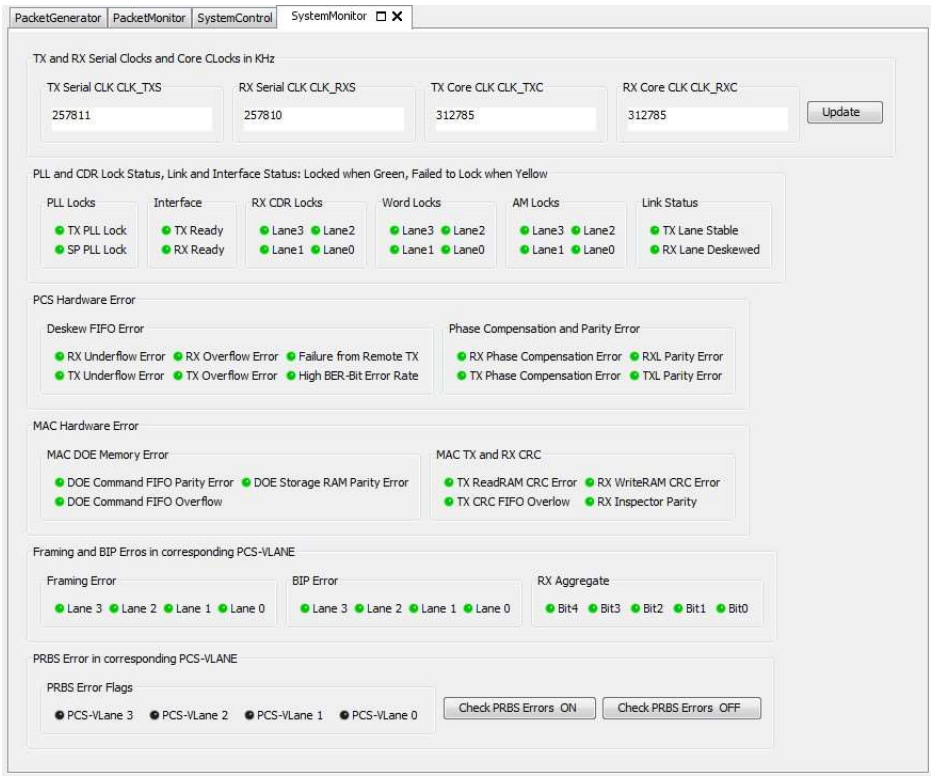
2. PacketMonitor GUI panel provides straight forward packet statitics of transmission and receiving



3. SystemControl GUI panel helps to set system using various loopback and PRBS



4.SystemMonitor GUI panel provides straight forward link and system working conditions



Reference links

Altera 40- and 100-Gbps Ethernet MAC and PHY MegaCore Function User Guide (PDF)

Altera 100G Development Kit, Stratix V GX Edition (PDF)

Known Issue

Please note that the system is flexible testing platform. We have done a limited number of testing with an intention to demonstrate the inter-op of the two sub-systems. Additional test cases can be created by creating various kind of difference setting to the sub-system. Also note that the system console and TCL based scripting provides a flexible testing platform. We have done a limited number of testing with an intention to demonstrate the inter-op of the two sub-systems. Additional test cases can be created by creating various kind of difference setting to the sub-system.

History

Last Update: July 16, 2015