## 40Gbps Ethernet MACPHY IP Hardware Demo Design using QSFP

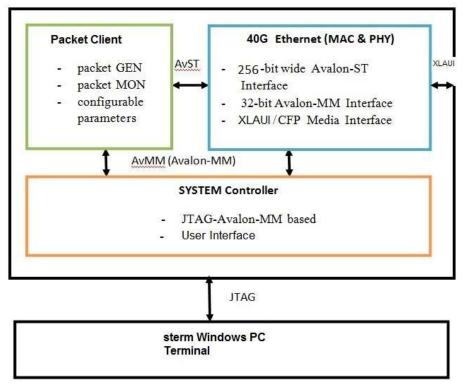
## Title

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## Introduction

This hardware demo design demonstrates the operation of Altera® 40-Gbps Ethernet MAC and PHY IP solution on a Stratix V device (5SGXEA7K2F40C2N). It is configured to demonstrate on a Stratix V GX FPGA Development Kit, also called PCIe Dev Kit using Altera development tool Quartus II 15.0 production release. This design provides a flexible test and demonstration platform which effectively control, test, and monitor 40Gbps Ethernet packets using internal serial PMA loopback and external optical loopback, MAC client side RX to TX parallel loopback.

# This hardware demonstration reference design offers the following features:



• Stand-alone and easy-to-use design example with flexibility to dynamically select traffic profile.

• Uses a standard 256-bit Avalon-ST interface to connect to the Ethernet Packet Generator and Monitor.

• Provides both random and fixed size packet generator.

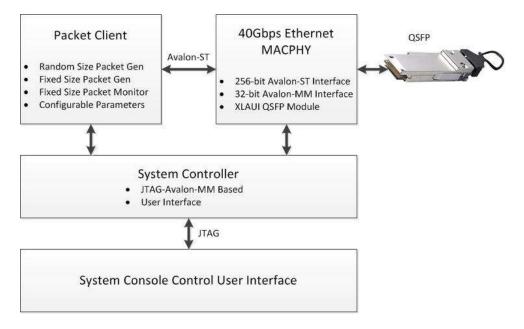
• System console GUI based flexible, reusable, and extendable user control interface allows users to dynamically configure and monitor any configuration registers provided by this demo design.

### **System Overview**

## The hardware platform consists of three sub-systems:

- The 40G Ethernet MAC and PHY IP
- Packet Client with random and fixed size packet Generator and Monitor
- System console GUI for configuration and control of the system

This system can be represented by the following diagram:



#### 40-Gbps Ethernet MAC and PHY IP

The Altera 40G Ethernet MAC and PHY IP core is implemented in compliance with the IEEE 803.3ba 2010 Higher Speed Ethernet Standard. This module handles the frame encapsulation and flow of data between a client logic and Ethernet network via a 40GbE Ethernet PCS and PMA (PHY). In the TX direction, the MAC accepts client frames, inserts inter-packet gap (IPG), preamble, start of frame delimiter (SFD), header, padding, and checksum before passing them to the PHY. The PHY encodes the MAC frame as required for reliable transmission over the media to the remote end. Similarly, in the RX direction, the

MAC accepts frames from the PHY, performs checks, updates statistics counters, strips out the CRC, preamble, and SFD, and passes the rest of the frame to the client.

#### Packet Client with Random Size Packet Generator and Monitor

The Packet Client includes a Packet Generator and a simple Packet Monitor. These modules have 256-bit Avalon-ST interface for the data-path and connect to the 40G Ethernet MAC. There is also a 32-bit Avalon-MM configuration and status interface associated with both the generator and the monitor. The generator can generate random packets. Monitor parses all packets received from MAC and checks the integrity of the packets.

#### **Fixed Size Packet Generator and Monitor**

The traffic generator is able to generate fixed size packets with length from 33-byte to 32768-byte. This traffic generator can be operated in two modes: continuous mode and burst mode. The packet payload be configured as either incremental or configurable fixed. The traffic monitor is able to check packet sequence number, packet length.

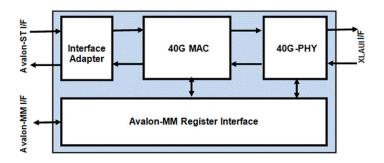
#### **System Console Control Panels**

This hardware demo design use System Console to run TCL script which is platform independent, can run on a PC (windows based operating system) or any Linux Machine.

There are four system console control panels designed for this hardware demo with straight forward hardware status monitoring and simple mouse click operation.

#### **100G Ethernet MAC & PHY IP**

As mentioned in previous sections, the 40G Ethernet sub-system consists of 40G MAC and PHY sub-modules. The MAC client side data path interface has two options: Avalon ST interface and Custom ST interface. This reference design uses an Avalon-ST interface which includes interface adapter. This adapter then provides a standard Avalon-ST interface for the MAC client. The MAC connects to the PHY core over XLGMII interface. The 40G Ethernet IP core can be demonstrated as the following simplified diagram:



#### Additional Functional Details of 40GE Ethernet IP Core

The additional details of the IP core can be found in the User guide. The IP core evaluation package and the user guide can be downloaded from here:40 Gbps and 100 Gbps Ethernet MegaCore Function

## Start Guide for Hardware Demo design

The hardware demo design setup essentially consists of three parts:

- Stratix V GX FPGA Development Kit hardware setup
- Stratix V GX FPGA Development Kit software v12.0 setup, full installation of all files including reference manual, user guide, quick-start guide, BOM, layout, PCB, schematics, Board Update Portal example file, Board Test System example file, and others.
- Quartus II 15.0 and SignalTap II Logic Analyzer setup

The relevant setups for each of these components are provided in detail as shown below:

## Stratix V GX FPGA Development Kit Hardware Setup

The Stratix V GX FPGA development board requires minimum hardware setup. A one time setting is required to ensure the following:

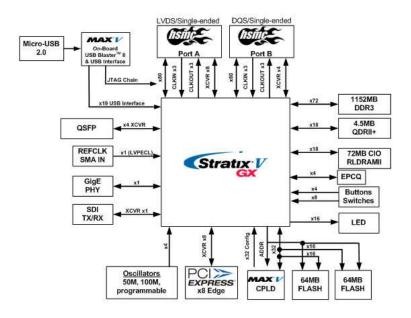
- 1. A QSFP module is plugged into an QSFP optical cage.
- 2. The DIP switches SW1 are pushed all to 8'b1111111.
- 3. The DIP switches SW3 are pushed all to 4'b0000.
- 4. The DIP switches SW4 [1:6] should be set as 6'b000110.
- 5. The DIP switch SW5 [1:4] should be set as 4'b1011.
- 6. The DIP switch SW6 [1:4] should be set as 4'b0001.

Before turning on power switch at the middle left of the development board, two cables are required to connect to development kit:

- 1. Power supply cable with adaptor to provide 19V DC voltage.
- 2. USB blaster cable connected between PC and development board.



Below is functional block diagram of Stratix V GX FPGA Development Kit.



## Stratix V GX FPGA Development Kit - Stratix V GX Edition v12.0 Software Setup

The Stratix V GX FPGA development kit – Stratix V GX Edition v12.0 Software from Stratix V GX FPGA Development Kit is required to be installed in order to use the Stratix V GX FPGA development board.

Full installation after running setup of v12.0 includes reference manual, user guide, quickstart guide, BOM, layout, PCB, schematics, Board Update Portal example file, Board Test System example file, and others. It also includes softwares for board test and clock control.



The Board Test System GUI is shown below:

## **Quartus II 15.0 and System Console**

After installing Quartus II 15.0, download the 40Gbps Hardware Demo Quick Start Guide which provides step by step instruction on how to open project, load SOF file and start system console.

## **System Console GUI Control Panels**

This hardware demo offers four GUI control panels using system console:

1. PacketGenerator GUI panel provides push button easy configuration on using fixed size and random size packet generators

nd Packets in Continuous Mode Random Send Random Packet Send Fixed Packet	Send a Burst of Packets/Stop Sending Pace Start Send a Burst of Packets	ekts Stop Stop Sending Packets
nfgure Fixed Size Packets Payload Overhead Destination Address 0x12345 in each box	Configure Fixed Size Packet Generator Fixed Size Packet Length in Decimal Bet	ween 33 and 1522
0xdeadd1 0xdeadd0 Configure Destination Address		Configure Fixed Size Packet Length
Source Address 0x123456 in each box	Number of Packets to Send, used in Bu	rst Mode only
0xfeadd1 0xfeadd0 Configure Source Address	þ	Enter Burst Size between 0 & 2^64
Configure Payload Length/Type Field 0x1234	Configure First Packet Sequence Numb	er in 0x12345678
0x0000 Configure Payload Length/Type Header	0x0000004	Enter 1st Packet Sequence Number
nfigure Fixed Size Packets Generation Mode end Payload in sequential or fixed format Continuous Continuous Mode A Burst Burst Mode	Configure Fixed Size Packets Payload Moo FixedSeqGroup Sequential Sequential Mode	e Fixed Payload Fixed Mode

2. PacketMonitor GUI panel provides straight forward packet statitics of transmission and receiving

acket Error Statistics			
Total RX CRC Errors	Total RX Length Errors	Total RX Sequence Errors	
1	0	0	Update
acket Statistics			
RX Packets Received			
Total TX Transmitted	Total RX Received	TX and RX Difference	
80897392702	80897376805	15897	
TX Packets Transmitted			
TX 64-Byte	TX 65 to 127-Byte	TX 128 to 255-Byte	
16876937410	25143470497	24661525499	
TX 256 to 511-Byte	TX 512 to 1023-Byte	TX 1024 to 1518-Byte	
12316654211	1865572829	33232256	
RX Packets Received			
RX 64-Byte	RX 65 to 127-Byte	RX 128 to 255-Byte	
16876934021	25143465493	24661520721	
RX 256 to 511-Byte	RX 512 to 1023-Byte	RX 1024 to 1518-Byte	
12316651845	1865572475	33232250	

3. SystemControl GUI panel helps to set system using various loopback and PRBS

Soft Reset both M	AC and PHY	Reset Packet	t Generators	set Packet Statistics Co	ounter
Loopback Mode Configu	ration				
SerDes Internal Ser	ial Loopback	Internal Serial L	oopback ON Inter	nal Serial Loopback O	FF
MAC Parallel Client	Side RX to TX	Parallel RX to TX I	Loopback ON Paral	el RX to TX Loopback C	DFF
PRBS-9 Data Mode Con • TX PRBS-9 TX F	RBS-9 ON	TX PRBS-9 OFF	• RX PRBS-9 R	(PRBS-9 ON R)	PRBS-9 OFF
TX PRBS-9     TX F     PRBS-31 Data Mode Cor	PRBS-9 ON				
TX PRBS-9     TX F     PRBS-31 Data Mode Cor	PRBS-9 ON	TX PRBS-9 OFF			X PRBS-9 OFF X PRBS-31 OFF
TX PRBS-9     TX F     PRBS-31 Data Mode Cor	PRBS-9 ON	TX PRBS-31 OFF			
TX PRBS-9     TX F PRBS-31 Data Mode Co     TX PRBS-31     TX F	RBS-9 ON	TX PRBS-31 OFF	• RX PRBS-31 R	PRBS-31 ON R	

4.SystemMonitor GUI panel provides straight forward link and system working conditions

		Control SystemMonitor	×⊔				
TX and RX Serial Clo	cks and Core CLock	s in KHz					
TX Serial CLK CLK	_TXS	RX Serial CLK CLK_RXS	ТХ	Core CLK CL	K_TXC	RX Core CLK CLK_RXC	
257811		257810	3	12785		312785	Update
PLL and CDR Lock S	tatus, Link and Inte	rface Status: Locked whe	n Green, <mark>Faile</mark> d	to Lock when	Yellow		
PLL Locks	Interface	RX CDR Locks	Word Locks		AM Locks	Link Status	
<ul> <li>TX PLL Lock</li> <li>SP PLL Lock</li> </ul>	<ul> <li>TX Ready</li> <li>RX Ready</li> </ul>	● Lane3 ● Lane2 ● Lane1 ● Lane0	Lane3     Lane1		<ul> <li>Lane3</li> <li>Lane3</li> <li>Lane1</li> <li>Lane0</li> </ul>		
PCS Hardware Error							
Deskew FIFO Erro	Error 💿 RX Overfl	ow Error 🧧 Failure from I		RX Phas	ensation and Parity B e Compensation Erro	Error r 🔹 RXL Parity Error	
TX Underflow	Error 9 TX Overfi	ow Error 🧧 High BER-Bit	Error Rate	TX Phas	e Compensation Erro	r 💿 TXL Parity Error	
		ow Error 🧕 High BER-Bit	Error Rate	• TX Phas	e Compensation Erro	r 🗧 TXL Parity Error	
TX Underflow     MAC Hardware Error     MAC DOE Memory	r	ow Error 🧕 High BER-Bit		• TX Phas	•	r 🔹 TXL Parity Error	
MAC Hardware Error MAC DOE Memor	r y Error	ODE Storage RAM Par	N ity Error	IAC TX and R	•	WriteRAM CRC Error	
MAC Hardware Error MAC DOE Memor DOE Comman DOE Comman	r y Error id FIFO Parity Error id FIFO Overflow	DOE Storage RAM Par	N ity Error	IAC TX and R	K CRC	WriteRAM CRC Error	
MAC Hardware Error MAC DOE Memor DOE Comman DOE Comman Framing and BIP Erro Framing Error	r y Error id FIFO Parity Error id FIFO Overflow	DOE Storage RAM Par PCS-VLANE BIP Error	N ity Error	IAC TX and R TX ReadRA TX CRC FI	X CRC MM CRC Error • RX 1 =0 Overlow • RX 1 RX Aggregate	WriteRAM CRC Error	
MAC Hardware Error MAC DOE Memor DOE Comman DOE Comman Framing and BIP Erro Framing Error	r y Error Id FIFO Parity Error Id FIFO Overflow os in corresponding ne 2 © Lane 1 © L	DOE Storage RAM Par PCS-VLANE BIP Error ane 0 Lane 3	ity Error	IAC TX and R TX ReadRA TX CRC FI	X CRC MM CRC Error • RX 1 =0 Overlow • RX 1 RX Aggregate	WriteRAM CRC Error Inspector Parity	

## **Reference links**

Altera 40- and 100-Gbps Ethernet MAC and PHY MegaCore Function User Guide (PDF)

Altera 100G Development Kit, Stratix V GX Edition (PDF)

## **Known Issue**

Please note that the system is flexible testing platform. We have done a limited number of testing with an intention to demonstrate the inter-op of the two sub-systems. Additional test cases can be created by creating various kind of difference setting to the sub-system. Also note that the system console and TCL based scripting provides a flexible testing platform. We have done a limited number of testing with an intention to demonstrate the inter-op of the two sub-systems. Additional test cases can be created by creating to the sub-system.

## History

Last Update: July 16, 2015