

40Gbps Ethernet Hardware Demo Quick Starter Guide



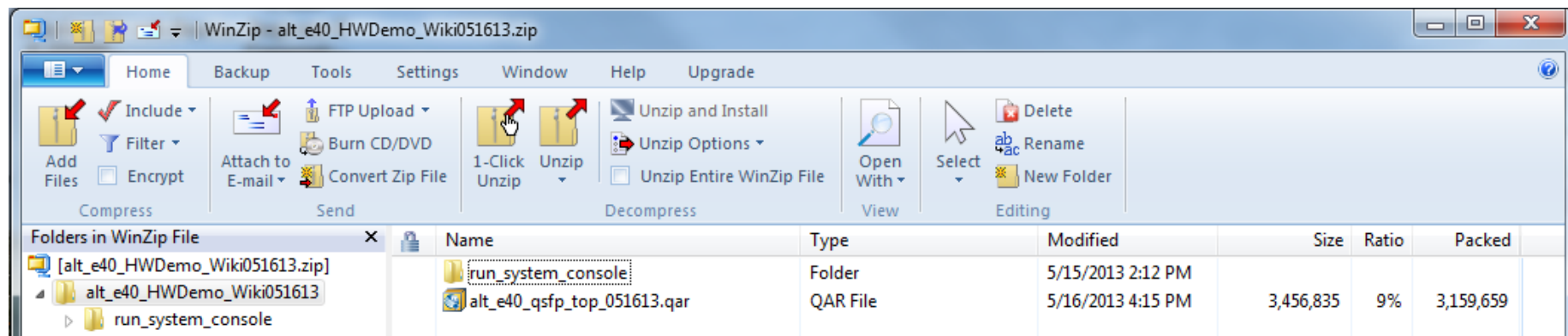
Download Design From AlteraWiki

■ Download Zipped Design from this link

- [http://www.alterawiki.com/wiki/40Gbps Ethernet MACPHY IP Hardware Demo Design using QSFP](http://www.alterawiki.com/wiki/40Gbps_Ethernet_MACPHY_IP_Hardware_Demo_Design_using_QSFP)

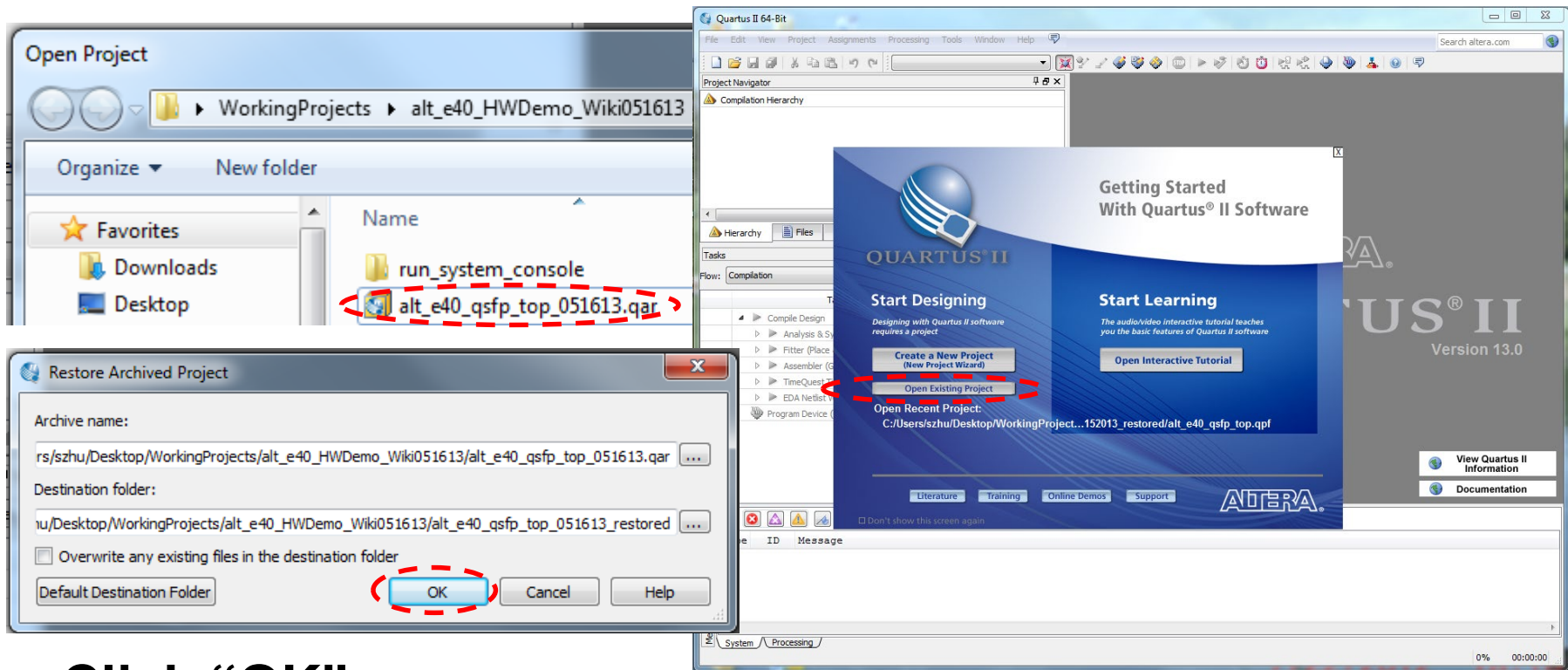
■ Unzip the compressed package

- There is a Quartus Archived design
- The directory “run_system_console” contains TCL scripts for this Demo



Start Quartus II and Load Project

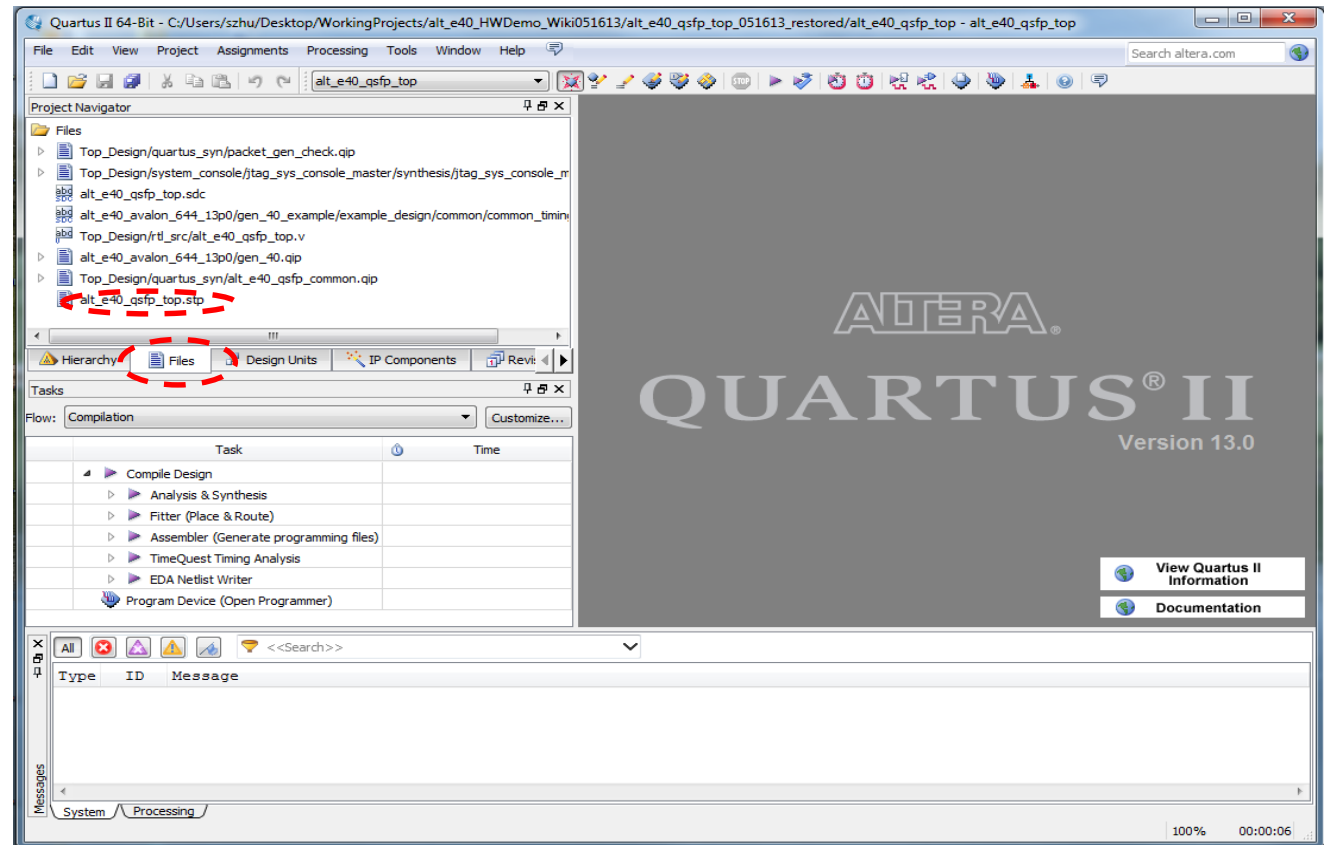
- Start Quartus II software 13.0 production release
- Click “Open Existing Project”
- Open “alt_e40_qsfp_top_051613.qar”



- Click “OK”

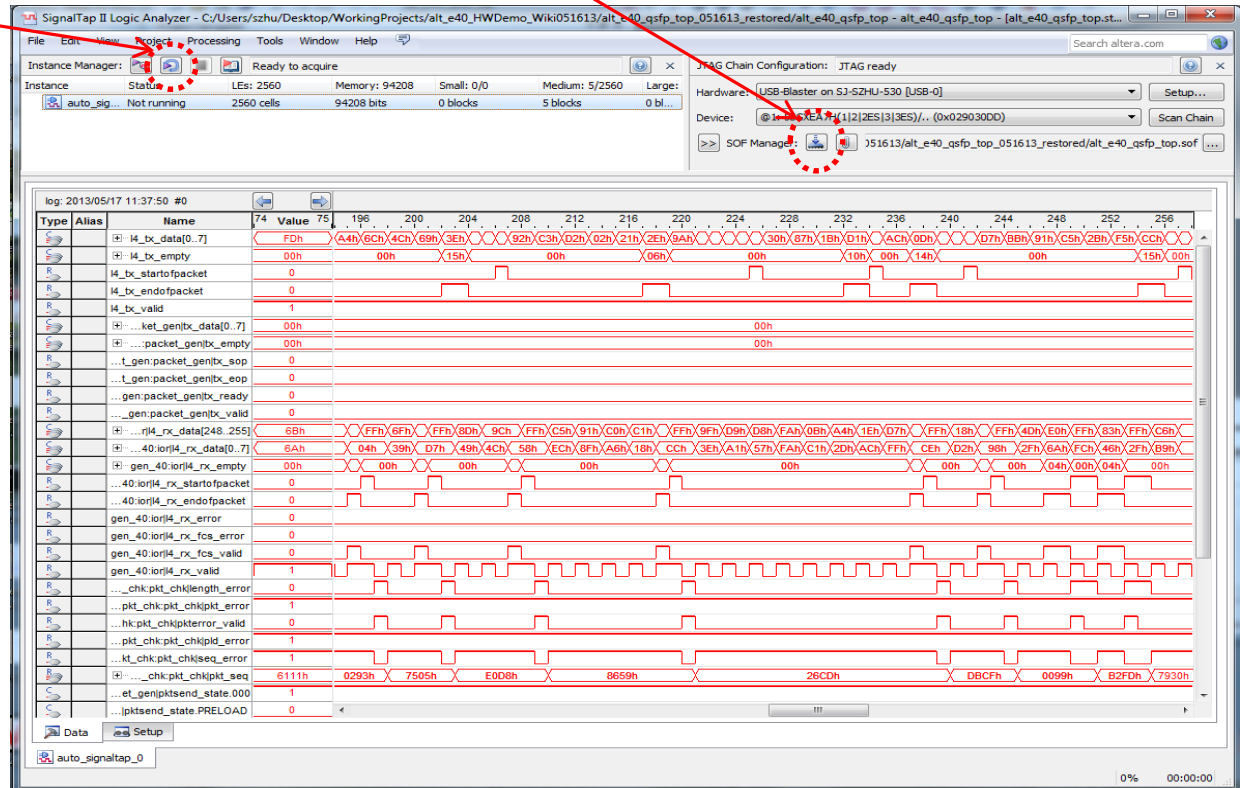
Open SignalTap II Logic Analyzer

- Click “Files”
- Double Click “alt_e40_qsfp_top.stp”



Program the Device

- Clicking “Program Device” button will program alt_e40_qsfp_top.sof into Stratix V FPGA
- Click “Autorun Analysis”



Start System Console

- **Start Qsys from Quartus II menu**
 - Tools -> Qsys
- **Start System Console from Qsys menu**
 - Tools -> System Console
- **Run**

- main_run.tcl

The screenshot displays the System Console - SystemMonitor application. The interface is divided into several sections:

- System Explorer:** A tree view on the left showing the project hierarchy, including connections, devices, and design instances.
- PacketGenerator, PacketMonitor, SystemControl, SystemMonitor:** A set of tabs at the top right.
- TX and RX Serial Clocks and Core Clocks in KHz:** A section with four input fields for clock frequencies: TX Serial CLK CLK_TXS (257811), RX Serial CLK CLK_RXS (257811), TX Core CLK CLK_TXC (312785), and RX Core CLK CLK_RXC (312785). An 'Update' button is present.
- PLL and CDR Lock Status, Link and Interface Status:** A section with a title 'Locked when Green, Failed to Lock when Yellow'. It contains several sub-sections with status indicators (green circles):
 - PLL Locks:** TX PLL Lock, SP PLL Lock.
 - Interface:** TX Ready, RX Ready.
 - RX CDR Locks:** Lane3 Lane2, Lane1 Lane0.
 - Word Locks:** Lane3 Lane2, Lane1 Lane0.
 - AM Locks:** Lane3 Lane2, Lane1 Lane0.
 - Link Status:** TX Lane Stable, RX Lane Deskewed.
- PCS Hardware Error:** A section with two sub-sections:
 - Deskew FIFO Error:** RX Underflow Error, TX Underflow Error, RX Overflow Error, TX Overflow Error, Failure from Remote TX, High BER-Bit Error Rate.
 - Phase Compensation and Parity Error:** RX Phase Compensation Error, TX Phase Compensation Error, RX Parity Error, TX Parity Error.
- MAC Hardware Error:** A section with two sub-sections:
 - MAC DOE Memory Error:** DOE Command FIFO Parity Error, DOE Storage RAM Parity Error, DOE Command FIFO Overflow.
 - MAC TX and RX CRC:** TX ReadRAM CRC Error, TX CRC FIFO Overflow, RX WriteRAM CRC Error, RX Inspector Parity.

At the bottom, the **Messages** pane shows system logs. A **Tcl Console** window is open at the bottom right, containing the following commands:

```
cd ../run_system_console
source main_run.tcl
Random Packets Generator is running in default
```

A red arrow points from the 'main_run.tcl' text in the list above to the 'source main_run.tcl' command in the Tcl Console window.

40Gbps Hardware Demo System Console Control Panels

■ There are four system console control panels

- Packet Generator
- Packet Monitor
- System Control
- System Monitor

The screenshot displays four overlapping windows from the 40Gbps Hardware Demo System Console:

- PacketGenerator:** Contains configuration options for sending packets (Random/Fixed), payload overhead (Destination/Source Address), payload length/type, and generation mode (Continuous/Burst).
- PacketMonitor:** Displays statistics for RX CRC Errors (0), Total RX Length (0), Total TX Transmitted (9365987170), Total RX Received (9365987163), TX Packets Transmitted (TX 64-Byte: 1953549921, TX 65 to 127-Byte: 2912400804, TX 256 to 511-Byte: 1425719159, TX 512 to 1023-Byte: 215957407), and RX Packets Received (RX 64-Byte: 1953549921, RX 65 to 127-Byte: 2912400800, RX 256 to 511-Byte: 1425719158, RX 512 to 1023-Byte: 215957406).
- SystemControl:** Features control buttons for 'Soft Reset both MAC and PHY', 'Reset Packet Generators', and 'Reset Packet Statistics Counter'. It also includes configuration for Loopback Mode (SerDes Internal Serial Loopback, MAC Parallel Client Side RX to TX) and PRBS-9 Data Mode.
- SystemMonitor:** Shows TX and RX Serial Clocks and Core Clocks in KHz (TX Serial CLK CLK_TXS: 257810, RX Serial CLK CLK_RXS: 257811, TX Core CLK CLK_TXC: 312785, RX Core CLK CLK_RXC: 312785). It also displays PLL and CDR Lock Status, PCS Hardware Error (Deskew FIFO, Phase Compensation and Parity), MAC Hardware Error (MAC DOE Memory, MAC TX and RX CRC), Framing and BIP Errors, and PRBS Error in corresponding PCS-VLANE.

Use System Monitor to Check System Working Condition

- **main_run.tcl auto checks all status twice after start**

- First check could show some error indicator in **RED**
- Second check should show all **GREEN**

- **System monitor does not auto check**

- **Click “Update” will check twice**

- **Right picture shows healthy normal system working condition**

The screenshot displays the System Monitor interface with the following sections:

- TX and RX Serial Clocks and Core Clocks in KHz:** TX Serial CLK CLK_TXS (257810), RX Serial CLK CLK_RXS (257811), TX Core CLK CLK_TXC (312785), RX Core CLK CLK_RXC (312785). An "Update" button is present.
- PLL and CDR Lock Status, Link and Interface Status:** Locked when Green, Failed to Lock when Yellow.
 - PLL Locks:** TX PLL Lock (Green), SP PLL Lock (Green).
 - Interface:** TX Ready (Green), RX Ready (Green).
 - RX CDR Locks:** Lane3 (Green), Lane2 (Green), Lane1 (Green), Lane0 (Green).
 - Word Locks:** Lane3 (Green), Lane2 (Green), Lane1 (Green), Lane0 (Green).
 - AM Locks:** Lane3 (Green), Lane2 (Green), Lane1 (Green), Lane0 (Green).
 - Link Status:** TX Lane Stable (Green), RX Lane Deskewed (Green).
- PCS Hardware Error:**
 - Deskew FIFO Error:** RX Underflow Error (Green), TX Underflow Error (Green), RX Overflow Error (Green), TX Overflow Error (Green), Failure from Remote TX (Green), High BER-Bit Error Rate (Green).
 - Phase Compensation and Parity Error:** RX Phase Compensation Error (Green), TX Phase Compensation Error (Green), RXL Parity Error (Green), TXL Parity Error (Green).
- MAC Hardware Error:**
 - MAC DOE Memory Error:** DOE Command FIFO Parity Error (Green), DOE Storage RAM Parity Error (Green), DOE Command FIFO Overflow (Green).
 - MAC TX and RX CRC:** TX ReadRAM CRC Error (Green), TX CRC FIFO Overflow (Green), RX WriteRAM CRC Error (Green), RX Inspector Parity (Green).
- Framing and BIP Errors in corresponding PCS-VLANE:**
 - Framing Error:** Lane 3 (Green), Lane 2 (Green), Lane 1 (Green), Lane 0 (Green).
 - BIP Error:** Lane 3 (Green), Lane 2 (Green), Lane 1 (Green), Lane 0 (Green).
 - RX Aggregate:** Bit4 (Green), Bit3 (Green), Bit2 (Green), Bit1 (Green), Bit0 (Green).
- PRBS Error in corresponding PCS-VLANE:** PCS-VLane 3 (Green), PCS-VLane 2 (Green), PCS-VLane 1 (Green), PCS-VLane 0 (Green). Buttons for "Check PRBS Errors ON" and "Check PRBS Errors OFF".



Thank You



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