



QUARTUS^{II}

DDR3 Using the MAX 10 FPGA Development Kit

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1. Description

The MAX 10 FPGA development kit has one 64-Mx16 1Gb DDR3 SDRAM and one 128-Mx8 1Gb DDR3 SDRAM. The MAX 10 FPGA provides full-speed support to a DDR3 300-MHz interface with error correction code (ECC) feature. This design example is used to check out a x24 DDR3 300MHz interface, please download the installer of MAX 10 development kit and use BTS GUI to try it out for a straightforward experience.

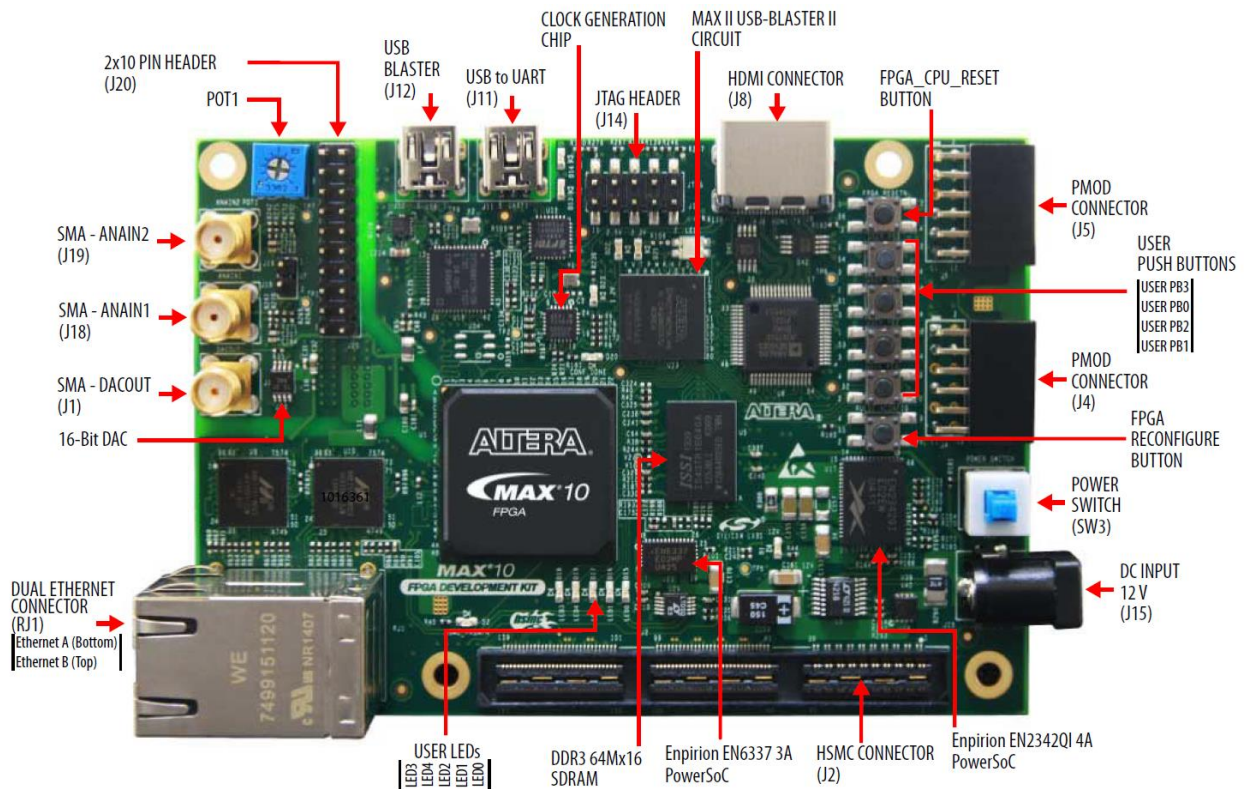


Fig: Max10 FPGA Development Kit

2. Operation of the Design:

This design example demonstrates the working of DDR3 interface by reading and writing to a selected amount of addresses.

Please note some address pins for DDR3 interface have been changed from Rev B to Rev C to fix pin assignment violation issue with v15.0 or later version. In addition, DDR3 dedicated reference clock is only working on Rev C kit. Please turn to the User Guide https://www.altera.com/content/dam/altera-www/global/en_US/pdfs/literature/ug/ug-max10m50-fpga-dev-kit.pdf for more details about DDR3 interface.

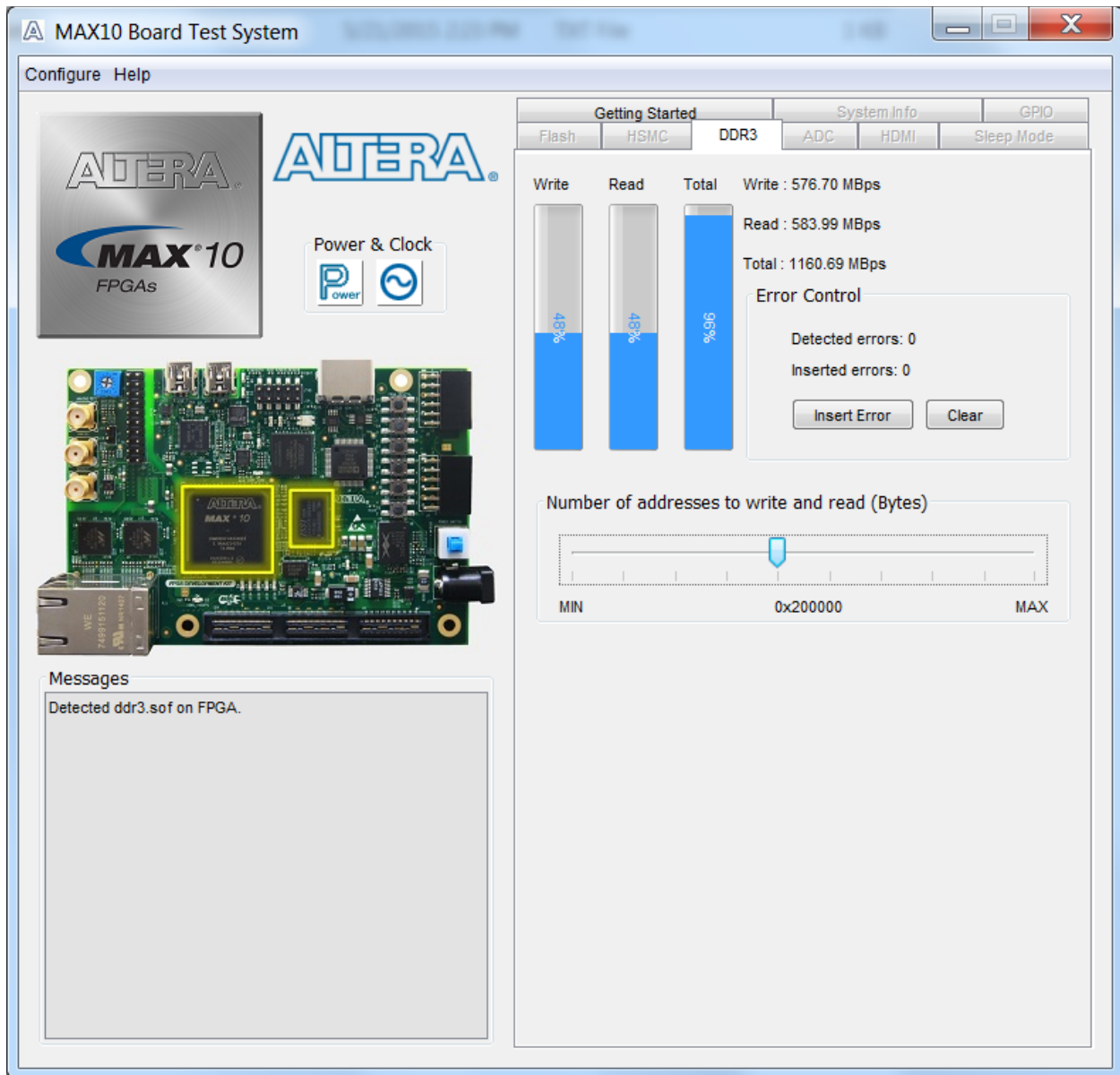
3. Reconstruct the Design:

This design example has a system Qsys component which includes DDR3 core, user-defined memory drive test component and JTAG-Avalon MM interface. It allows you to kick off the traffic test and monitor its status over memory components via system-console.

Use	Connections	Name	Description	Export	Clock	Base
<input checked="" type="checkbox"/>		sys_clk	Clock Source	sys_clk		
<input checked="" type="checkbox"/>		clk_in	Clock Input	reset	exported	
<input checked="" type="checkbox"/>		clk_in_reset	Reset Input			
<input checked="" type="checkbox"/>		clk	Clock Output			
<input checked="" type="checkbox"/>		clk_reset	Reset Output			
<input checked="" type="checkbox"/>		master_0	JTAG to Avalon Master Bridge			
<input checked="" type="checkbox"/>		clk	Clock Input		sys_clk	
<input checked="" type="checkbox"/>		clk_reset	Reset Input			
<input checked="" type="checkbox"/>		master	Avalon Memory Mapped Master			
<input checked="" type="checkbox"/>		master_reset	Reset Output		[clk]	
<input checked="" type="checkbox"/>		product_info_0	product_info			
<input checked="" type="checkbox"/>		clock_reset	Clock Input		sys_clk	
<input checked="" type="checkbox"/>		clock_reset_reset	Reset Input		[clock_reset]	
<input checked="" type="checkbox"/>		avalon_slave_0	Avalon Memory Mapped Slave			# 0x0000_0000
<input checked="" type="checkbox"/>		mSGDMA_0	mSGDMA			
<input checked="" type="checkbox"/>		cal_fail_mon	Conduit	msgdma_0_cal_fail_mon		
<input checked="" type="checkbox"/>		cal_success_mon	Conduit	msgdma_0_cal_success_mon		
<input checked="" type="checkbox"/>		clk	Clock Input		mem_if_ddr3_emif_0_afi_clk	
<input checked="" type="checkbox"/>		clk_0	Clock Input		sys_clk	
<input checked="" type="checkbox"/>		dispatcher_read_csr_irq	Interrupt Sender		[clk]	
<input checked="" type="checkbox"/>		dispatcher_write_csr_irq	Interrupt Sender		[clk]	
<input checked="" type="checkbox"/>		dma_read_master	Avalon Memory Mapped Master		[clk]	
<input checked="" type="checkbox"/>		dma_write_master	Avalon Memory Mapped Master		[clk]	
<input checked="" type="checkbox"/>		reset_source	Reset Output		[clk]	
<input checked="" type="checkbox"/>		mrm_bridge_slv	Avalon Memory Mapped Slave			# 0x0020_0000
<input checked="" type="checkbox"/>		reset	Reset Input			
<input checked="" type="checkbox"/>		reset_0	Reset Input			
<input checked="" type="checkbox"/>		status_mon_0_init_done_mon	Conduit	msgdma_0_status_mon_0_init_done_mon		
<input checked="" type="checkbox"/>		status_mon_in	Conduit			
<input checked="" type="checkbox"/>		master_driver_msgdma_0	master_driver_msgdma			
<input checked="" type="checkbox"/>		reset	Reset Output		[clock]	
<input checked="" type="checkbox"/>		clock	Conduit [conduit_end 15.0]		sys_clk	
<input checked="" type="checkbox"/>		csr	Interrupt Receiver		[clock]	# 0x0010_0000
<input checked="" type="checkbox"/>		interrupt_receiver	Interrupt Receiver		[clock]	
<input checked="" type="checkbox"/>		avalon_master	Avalon Memory Mapped Master		[clock]	
<input checked="" type="checkbox"/>		reset_source	Reset Output		[clock]	
<input checked="" type="checkbox"/>		conduit_end	Conduit	master_driver_msgdma_0_conduit_end	[clock]	
<input checked="" type="checkbox"/>		refclk_clock_bridge	Clock Bridge			
<input checked="" type="checkbox"/>		in_clk	Clock Input	refclk_clock_bridge_in_clk	exported	
<input checked="" type="checkbox"/>		out_clk	Clock Output		refclk_clock_bridge_out_clk	
<input checked="" type="checkbox"/>		mem_if_ddr3_emif_0	DDR3 SDRAM Controller with UniPHY			
<input checked="" type="checkbox"/>		pll_ref_clk	Clock Input			
<input checked="" type="checkbox"/>		global_reset	Reset Input			
<input checked="" type="checkbox"/>		soft_reset	Reset Input			
<input checked="" type="checkbox"/>		afi_clk	Clock Output			
<input checked="" type="checkbox"/>		afi_half_clk	Clock Output		mem_if_ddr3_emif_0_afi_clk	
<input checked="" type="checkbox"/>		afi_reset	Reset Output		[clock]	
<input checked="" type="checkbox"/>		afi_reset_export	Reset Output		mem_if_ddr3_emif_0_afi_half_clk	
<input checked="" type="checkbox"/>		memory	Conduit			
<input checked="" type="checkbox"/>		avl	Avalon Memory Mapped Slave	memory		# 0x0000_0000
<input checked="" type="checkbox"/>		status	Conduit		mem_if_ddr3_emif_0_afi_clk	
<input checked="" type="checkbox"/>		pll_sharing	Conduit			
<input checked="" type="checkbox"/>		csr	Avalon Memory Mapped Slave		mem_if_ddr3_emif_0_afi_clk	#

4. How to run the DDR3 design example on the MAX 10 Development kit

- 1) Download the ddr3.par from the design store.
- 2) Use the command **quartus_sh --platform_install -package <directory-path>/ddr3.par** to install the design template
- 3) Use the command **quartus_sh --platform -name ddr3** to unarchive the project and get all the design files.
- 4) Recompile the design or directly use SOF image at master_image folder
- 5) Power on the kit and configure SOF to MAX 10 FPGA
- 6) Double click "BoardTestSystem" at *\\examples\board_test_system\ to open BTS GUI to test this design.



Acknowledgment

This design is based on DDR3 components for MAX 10 FPGA Development Kit produced by Altera Corporation.

Document Revision History

Date	Version	Changes
May 2015	V1.0	Initial Release