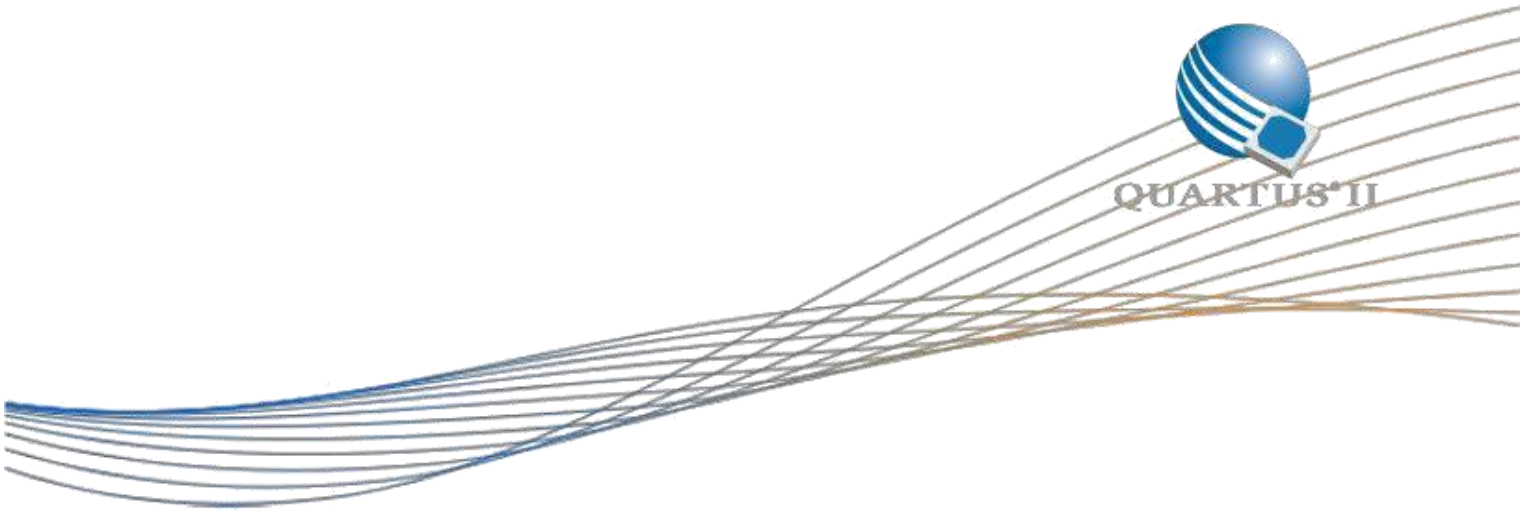


DDR3 Using the MAX 10 FPGA Development Kit

1. Description

The MAX 10 FPGA development kit has one 64-Mx16 1Gb DDR3 SDRAM and one 128-Mx8 1Gb DDR3 SDRAM. The MAX 10 FPGA provides full-speed support to a DDR3 300-MHz interface with error correction code (ECC) feature. This design example is used to check out a x24 DDR3 300MHz interface, please download the installer of MAX 10 development kit and use BTS GUI to try it out for a straightforward experience.

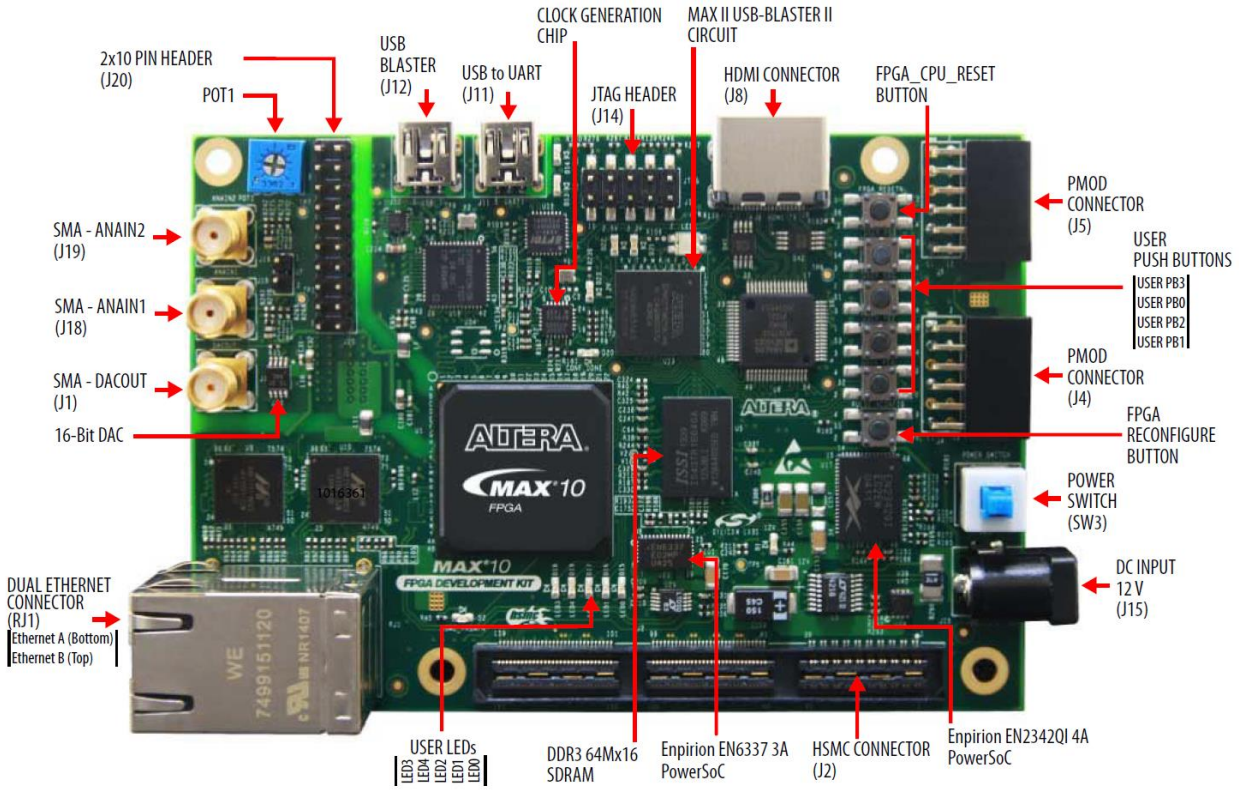


Fig: Max10 FPGA Development Kit

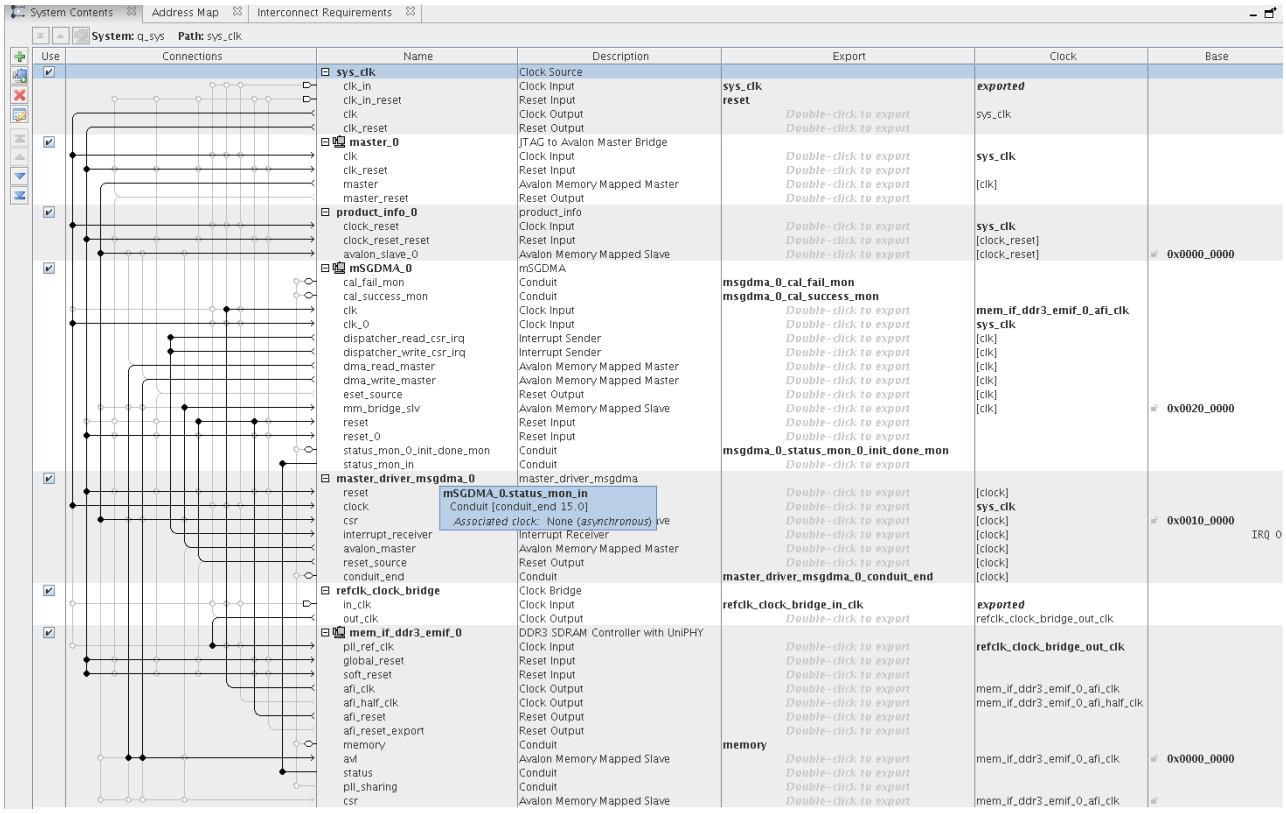
2. Operation of the Design:

This design example demonstrates the working of DDR3 interface by reading and writing to a selected amount of addresses.

Please note some address pins for DDR3 interface have been changed from Rev B to Rev C to fix pin assignment violation issue with v15.0 or later version. In addition, DDR3 dedicated reference clock is only working on Rev C kit. Please turn to the User Guide https://www.altera.com/content/dam/altera-www/global/en_US/pdfs/literature/ug/ug-max10m50-fpga-dev-kit.pdf for more details about DDR3 interface.

3. Reconstruct the Design:

This design example has a system Qsys component which includes DDR3 core, user-defined memory drive test component and JTAG-Avalon MM interface. It allows you to kick off the traffic test and monitor its status over memory components via system-console.



4. <u>How to run the DDR3 design example on the MAX 10 Development kit</u>

   1) Download the ddr3.par from the design store.
   2) Use the command "**quartus_sh --platform_install -package <directory-path>/ddr3.par**" to install the design template
   3) Use the command "**quartus_sh --platform -name ddr3**" to unarchive the project and get all the design files.
   4) Recompile the design or directly use SOF image at master_image folder
   5) Power on the kit and configure SOF to MAX 10 FPGA
   6) Double click "BoardTestSystem" at *\examples\board_test_system\ to open BTS GUI to test this design.

Acknowledgment
This design is based on DDR3 components for MAX 10 FPGA Development Kit produced by Altera Corporation.

Document Revision History

Date	Version	Changes
May 2015	V1.0	Initial Release