Stratix 10 Mailbox Client IP Core Design Example - QSPI flash Access and Remote System Update

Description:

This reference design implements the Mailbox Client Intel FPGA IP Core in Stratix 10 FPGA.

The Mailbox Client Intel FPGA IP is a bridge between a host and the Secure Device Manager(SDM). You use the Mailbox Client Intel FPGA IP to send commands and receive status from SDM peripheral clients. The Mailbox Client Intel FPGA IP is an Avalon MM slave component that must connect to an Avalon MM master.

In this reference design, JTAG-to-Avalon Master acts as the host controller connecting to Mailbox Client Intel FPGA IP core. The JTAG-to-Avalon Master Bridge IP translates the commands it receives from the System Console to Avalon Memory-Mapped (Avalon MM) format that the Mailbox Client Intel FPGA IP requires. Mailbox Client Intel FPGA IP: drives commands and receives responses from the SDM.

The rsu1.tcl script provides examples to perform the available command functions supported by SDM. You can run the functions available in the rsu1.tcl script via System Console of the Intel Quartus Prime software to perform the following operations,

- Read FPGA IDCODE

- Read FPGA CHIP ID

- QPSI flash access operations such as program QSPI flash with .rpd file.

- Remote System Update(RSU) operations such as reading RSU status and trigger reconfiguration from the data source which can be either an application image or factory image.

The rsu1.tcl script can be downloaded from the link provided below.
https://www.intel.com/content/dam/altera-www/global/en_US/others/support/devices/configuration/rsu1.tcl

For more details,
1. Refer to Mailbox Client Intel FPGA IP User Guide

https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/ug/ug-20087.pdf

2. Refer to Chapter 5. Remote System Update(RSU) in Intel Stratix 10 Configuration User Guide
https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/hb/stratix-10/ug-s10-config...