Agilex™ 7 FPGAs and SoCs M-Series Product Table

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Version 2024.01.09

Product Line		AGM 032	AGM 039
Resources	Logic elements (LEs)	3,245,000	3,851,520
	Adaptive logic modules (ALMs)	1,100,000	1,305,600
	ALM registers	4,400,000	5,222,400
	M20K memory blocks	15,932	18,960
	M20K memory size (Mb)	311	370
	MLAB memory count	55,000	65,280
	MLAB memory size (Mb)	33	40
	HBM2E High Bandwidth DRAM Memory (Gbytes) Size	16 / 32	16 / 32
	Fabric PLL	8	8
	I/O PLL	16	16
	Variable-precision digital signal processing (DSP) blocks	9,375	12,300
	18 x 19 multipliers	18,750	24,600
	Single-precison or half-precision tera floating point operations per second (TFLOPS)	14 / 28	18.4 / 37
	Maximum EMIF x72	4	4
Maximum Available Device Resources	Memory devices supported	LPDDR5, DDR5, DDR4, QDR IV	
	Maximum AIB Interfaces	4	
	Secure device manager (SDM)	Provides SHA-384 bitstream integrity, ECDSA 256/384 bitstream authentication, AES-256 bitstream encryption, physically unclonable function (PUF) protected key storage, side-channel attack resistance, SPDM attestation, cryptographic services, physical anti-tamper support	
	Hard processor system	Quad-core 64 bit Arm Cortex*-A53 up to 1.41GHz with 32KB I/D cache, Neon* coprocessor, 1 MB L2 Cache, direct memory access (DMA), system memory management unit, cache coherency unit, hard memory controllers, USB 2.0 x2, 1G EMAC x3, UART x2, SPI x4, I2C x5, general prupose timers x7, watchdog timer x4	
Tile Resources	F-Tile	PCI Express* (PCIe*) hard IP block (4.0 x16) or bifurcateable 2x PCIe 4.0 x8 (EP) or 4x 4.0 x4 (RP) Transciever channel count : - 4 channels at 116 Gbps (PAM4) / 58 Gbps (NRZ) - 16 channels at 32 Gbps (NRZ) /12 channels at 58 Gbps (PAM4) - RS & KP FEC Advanced networking support: - Bifurcatable 400 GbE hard IP block (10/25/50/100/200/400 GbE FEC/PCS/MAC) - Bifurcatable 200 Gb hard IP block (10/25/50/100/200 Gbs FEC/PCS) IEEE 1588 support PMA direct	
	R-Tile	Compute Express Interface (CXL) - Link width x16 lanes, x8 lanes PCI Express(PCIe) hard IP block (5.0 x16) or Bifurcateable 2x PCIe 5.0 x8 (EP) or 4x 5.0 x4 (RP) Virtualization (SR-IOV) supporting 8 PFs/2k VFs Scalable IOV VirtIO Support Precise Time Management PIPE Direct	

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Package Options (HBM2E Packages)	Tile Configuration	GPIO(LVDS) / F-Tile 32G NRZ (58G PAM4) / High-Speed Transceiver 58G NRZ (116G PAM4) / R- Tile 32G PCIe (CXL) Lanes	
4700A (56mm x 66mm, 0.92mm Hex)	F-Tile x3, R-Tile x1, HBM2E	768(384) / 48(36) / 8(8) / 16(16)	768(384) / 48(36) / 8(8) / 16(16)
4700B (56mm x 66mm, 0.92mm Hex)	F-Tile x4, HBM2E	768(384) / 64(48) / 8(8)	768(384) / 64(48) / 8(8)

Product Line		AGM 032	AGM 039
Package Options (Non-HBM2E Packages)	Tile Configuration	GPIO(LVDS) / F-Tile 32G NRZ (58G PAM4) / High-Speed Transceiver 58G NRZ (116G PAM4) / R- Tile 32G PCIe (CXL) Lanes	
3184B (56 mm x 45 mm, 0.92 mm Hex)	F-Tile x4	720(360) / 64(48) / 8(8)	720(360) / 64(48) / 8(8)

Note:
1. All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit www.intel.com/fpga.

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