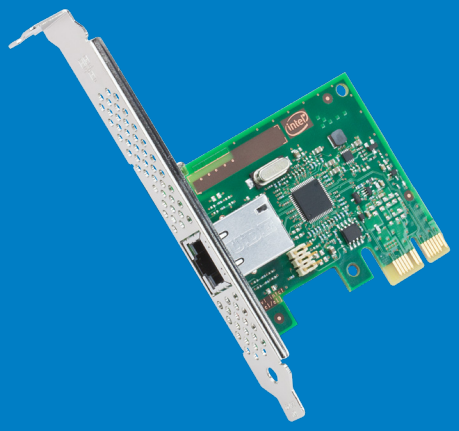
Product Brief

# Intel® Ethernet Server Adapter I210



## Single-port Gigabit Ethernet server adapter designed for entry-level servers and audio-video applications.

### Key Features

- Low-halogen[1] single-port PCI-Express 10/100/1000 Ethernet adapter
- Innovative power management features including Energy Efficient Ethernet (EEE), DMA Coalescing, ultra-compact design, and a unique ventilated bracket for increased efficiency and reduced power consumption
- The Intel Ethernet I210 Series implements a signed firmware authenticated capability to verify the firmware and critical device settings with built-in detection of corruption.
- IEEE 802.1Qav Audio-Video-Bridging (AVB) for tightly controlled media stream synchronization, buffering, and reservation
- High-performing design supporting PCI Express Gen 2.1 2.5GT/s
- Reliable and proven Gigabit Ethernet technology from Intel Corporation

### Overview

The Intel® Ethernet Server Adapter I210 builds on Intel's history of excellence in Ethernet Products. This adapter represents the next step in the Gigabit Ethernet (GbE) networking evolution for the enterprise and data centers offering Audio-Video-Bridging (AVB) support, along with power management technologies such as Energy Efficient Ethernet (EEE) and DMA Coalescing (DMAC).

## Audio-Video Bridging (AVB)

The Intel® Ethernet Server Adapter I210 supports IEEE 802.1Qav Audio-Video Bridging (AVB) for customers requiring tightly controlled media stream synchronization, buffering, and reservation. The 802.1Qav is part of the AVB specification that provides a way to guarantee bounded latency and latency variation for time sensitive traffic and includes:

- Timing and synchronization for time-specific applications (802.1AS) Stream Reservation (SR) protocol to guarantee the resources needed for Audio/Video (AV) streams (802.1Qat)
- Forwarding and queueing enhancements for time sensitive streams (802.1Qav).

## Performance Optimization

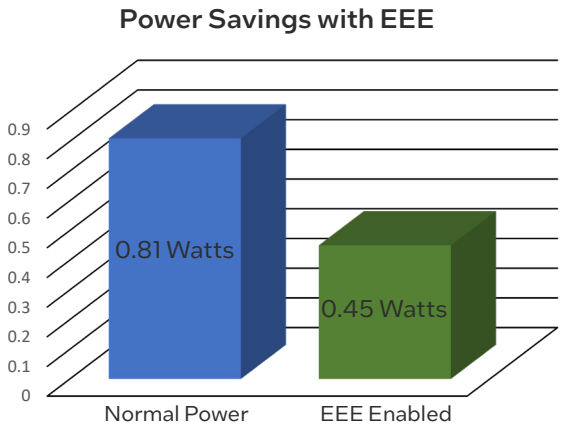
The I210 contains four transmit and four receive queues. These queues offer Error Correcting Memory (ECC) protection for improved data reliability. The adapter efficiently manages packets with minimum latency by combining parallel and pipelined logic architectures optimized for these independent transmit and receive queues. These queues, combined with Receive Side Scaling (RSS) and Message Signal Interrupt Extension (MSI-X) support, optimize the performance on servers with multi-core processors.

## Power Management Technologies

Intel has introduced new, Advanced Power Management Technologies (PMTs) that enable enterprises to configure power options on the adapter and more effectively manage power consumption.

### Energy Efficient Ethernet (EEE)

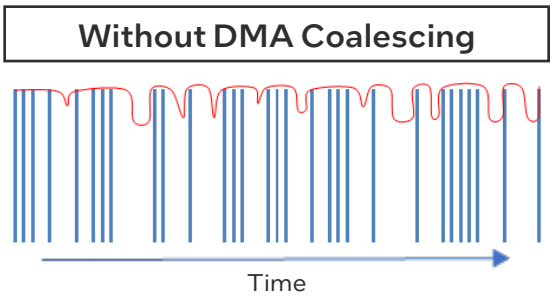
Supports the IEEE802.3az Energy Efficient Ethernet (EEE) standard. During periods of low network activity, EEE reduces the power consumption of an Ethernet connection by negotiating with a compliant EEE switch port to transition to a low power idle (LPI) state.



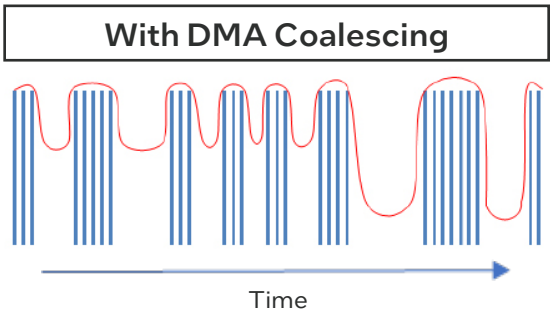

The controller power is reduced by approximately 50 percent of its normal operating power, saving power on the network port and the switch port. When increased network traffic is detected, the controller and the switch quickly come back to full power to handle the increased network traffic. EEE is supported for both 1000BASE-T and 100BASE-TX.

### DMA Coalescing

Another power management technology that can reduce power on the server platform is DMA Coalescing (DMAC). Typically, when a packet arrives at the adapter, a DMA request is initiated in order to place the packet into host (or server) memory. This transaction wakes up the processor, memory, and other system components from a lower power state in order to perform the tasks required to handle the incoming packet.




**No Coalescing.** As shown by the red line, components have less time between DMA calls to reach and stay in lower power.




**With Coalescing.** With more time between DMA calls, components can reach lower power states and remain in them longer.

Based on the configurable DMAC settings, incoming packets are buffered momentarily before any DMA calls are made. This buffering enables the controller to intelligently identify opportunities to batch multiple packets together. When components are wakened from lower power states they can efficiently handle the batched packets at the same time. Platform components are able to remain in lower power states longer, which can dramatically reduce platform energy consumption. DMAC synchronizes DMA calls across all controller ports to ensure maximum power savings.

## Environmentally Friendly Design

The I210 family is low halogen and lead-free to reduce the potential for environmental impact. Power management technologies, a unique ventilated bracket, and space-saving design make this adapter an ideal solution for compact workstations and entry-level servers.

| Features | Description |
|---|---|
| **General** | |
| Intel® Ethernet Controller I210 with PCI Express 2.1 Support | ▪ Industry-leading integrated MAC/PHY PCIe 2.0 GbE controller<br>▪ 2.5 GT/s support for x1 width (lane) |
| Low Halogen[1] | ▪ Leadership in an environmentally friendly ecosystem |
| Low profile single-port copper adapter | ▪ Compact design for high-density servers |
| Ships with full-height bracket installed; low-profile bracket included in package. Single-screw mount. | ▪ Streamlines installation |
| Ventilated bracket | ▪ Maximize airflow and cooling |
| **Ethernet** | |
| Audio-Video Bridging (AVB) Support (802.1Qav) | ▪ Dedicated Tx and Rx Queues for AVB traffic<br>▪ Supports forwarding and queuing enhancements for time-sensitive streams<br>▪ Supports time-based transmission |
| IEEE 802.3 autonegotiation | ▪ Automatic link configuration for speed duplex and flow control |
| 1 Gb/s Ethernet IEEE 802.3, 802.3u, 802.3ab PHY specifications compliant | ▪ Robust operation over installed base of CAT5 twisted-pair cabling |
| Integrated PHY for 10/100/1000 Mb/s for multi-speed, full, and half-duplex | ▪ Smaller footprint and lower power dissipation compared to multiple discrete MAC and PHYs |
| IEEE 802.3x and IEEE 802.3z compliant flow control support with software-controllable Rx thresholds and Tx pause frames | ▪ Local control of network congestion levels<br>▪ Frame loss reduced from receive overruns |
| Automatic cross-over detection function (MDI/ MDI-X) | ▪ The PHY automatically detects which application is being used and configures itself accordingly |
| IEEE 1588 protocol and 802.1AS implementation | ▪ Time-stamping and synchronization of time sensitive applications<br>▪ Distribute common time to media devices |
| **Power Management and Efficiency** | |
| IEEE 802.3az - Energy Efficient Ethernet (EEE) | ▪ Power consumption by the PHY is reduced by approximately 50%; link transitions to low power Idle (LPI) state as defined in the IEEE 802.3az (EEE) standard |
| DMA Coalescing | ▪ Reduces platform power consumption by coalescing, aligning, and synchronizing DMA<br>▪ Enables synchronizing port activity and power management of memory, CPU and RC internal circuitry |
| Smart power down (SPD) at S0 no link/Sx no link | ▪ PHY powers down circuits and clocks that are not required for detection of link activity |
| Active State Power Management (ASPM) | ▪ Optionality Compliance bit enables ASPM or runs ASPM compliance tests to support entry to L0s |
| LAN disable function | ▪ Option to disable the LAN Port and/or PCIe Function. Disabling just the PCIe function but keeping the LAN port that resides on it fully active (for manageability purposes and BMC pass-through traffic) |
| Full wake up support: | ▪ Advanced Power Management (APM) Support– [formerly Wake on LAN]<br>– APM - Designed to receive a broadcast or unicast packet with an explicit data pattern (Magic Packet) and assert a signal to wake up the system<br>▪ Advanced Configuration and Power Interface (ACPI) specification v2.0c<br>– ACPI - PCIe power management based wake-up that can generate system wake-up events from a number of sources<br>▪ Magic Packet wake-up enable with unique MAC address |
| ACPI register set and power down functionality supporting D0 and D3 states | ▪ A power-managed link speed control lowers link speed (and power) when highest link performance is not required |
| MAC Power Management controls | ▪ Power management controls in the MAC /PHY enable the device to enter a low-power state |
| Low Power Link Up - Link Speed Control | ▪ Enables a link to come up at the lowest possible speed in cases where power is more important than performance |
| Power Management Protocol Offload (Proxying) | ▪ Avoid spurious wake-up events and reduce system power consumption when the device is in D3 low power state and system in S3 or S4 low power states |

| Features | Description |
|---|---|
| **Stateless Offloads and Performance** | |
| TCP/UDP, IPv4 checksum offloads (Rx/ Tx/Large- send); Extended Tx descriptors) | ▪ More offload capabilities and improved CPU usage<br>▪ Checksum and segmentation capability extended to new standard packet type |
| IPv6 supports for IP/TCP and IP/UDP receives Checksum offload | ▪ Improved CPU usage |
| Transmit Segmentation Offloading (TSO) (IPv4, IPv6) | ▪ Increased throughput and lower processor usage |
| Interrupt throttling control | ▪ Limits maximum interrupt rate and improves CPU usage |
| Legacy and Message Signal Interrupt (MSI) | ▪ Interrupt mapping |
| Message Signal Interrupt Extension (MSI-X) | ▪ Dynamic allocation of up to 5 vectors per port |
| Intelligent interrupt generation | ▪ Enhanced software device driver performance |
| Receive Side Scaling (RSS) for Windows | ▪ Up to four queues per port |
| Scalable I/O for Linux environments (IPv4, IPv6, TCP/UDP) | ▪ Improves the system performance related to handling of network data on multiprocessor systems |
| Support for packets up to 9.5 KB (Jumbo Frames) | ▪ Enables faster and more accurate throughput of data |
| Low Latency Interrupts | ▪ Based on the sensitivity of the incoming data, the controller can bypass the automatic moderation of time intervals between the interrupts |
| Header/packet data split in receive | ▪ Helps the driver to focus on the relevant part of the packet without the need to parse it |
| PCIe 2.1 TLP Processing Hint Requester | ▪ Provides hints on a per transaction basis to facilitate optimized processing |
| Descriptor ring management hardware for Transmit and Receive | ▪ Optimized descriptor fetch and write-back for efficient system memory and PCIe bandwidth usage |
| **Remote Boot Options** | |
| Preboot Execution Environment (PXE) flash interface support) | ▪ Enables system boot via the EFI (32-bit and 64-bit)<br>▪ Flash interface for PXE 2.1 option ROM |
| Intel Boot Agent software--Linux boot via PXE or BOOTP, Windows Deployment Services, or UEFI | ▪ Enables networked computer to boot using a program code image supplied by a remote server<br>▪ Complies with the Preboot Execution Environment (PXE) Version 2.1 Specification |
| Descriptor ring management hardware for Transmit and Receive | ▪ Optimized descriptor fetch and write-back for efficient system memory and PCIe bandwidth usage |
| **Manageability** | |
| DMTF Network Controller Sideband Interface (NC-SI) Pass-through | ▪ Supports pass through traffic between BMC and Controller's LAN functions<br>▪ Meets RMII Spec, Revision 1.2 as a PHY-side device |
| Intel® System Management Bus (SMBus) Pass-through | ▪ Enables BMC to configure the Controller's filters and management related capabilities |
| Management Component Transport Protocol (MCTP) over SMBus and PCIe | ▪ Used for baseboard management controller (BMC) communication between add-in devices |
| OS2BMC Traffic support | ▪ Transmission and reception of traffic internally to communicate between the OS and local BMC |
| Private OS2BMC Traffic Flow | ▪ BMC may have its own private connection to the network controller and network flows are blocked |
| Firmware Based Thermal Management | ▪ Can be programmed via the BMC to initiate Thermal actions and report thermal occurrences |
| IEEE 802.3 MII Management Interface | ▪ Enables the MAC and software to monitor and control the state of the PHY |
| MAC/PHY Control and Status | ▪ Enhanced control capabilities through PHY reset, link status, duplex indication, and MAC Dx power state |
| Watchdog timer | ▪ Defined by the FLASHT register to minimize Flash updates |
| Extended error reporting | ▪ Messaging support to communicate multiple types/severity of errors |
| Controller Memory Protection | ▪ Main internal memories are protected by error-correcting code (ECC) or parity bits |
| Vital Product Data (VPD) Support | ▪ Support for VPD memory area |

## Specifications

| | |
|---|---|
| Connector | RJ45 |
| IEEE standard/ network topology | EEE 802.3 (10BASE-T, 100BASE-TX, 1000BASE-T) |
| Cabling | CAT3 or higher for 10BASE-T operation<br>CAT5 or higher for 100BASE-TX operation<br>CAT5e or higher for 1000BASE-T operation |
| Data rate supported per port | 10/100/1000 Mbps copper |
| Bus Type | PCIe 2.1 (2.5GT/s) |
| Bus Width | 1-lane PCIe; operable in x1 or greater slots |
| Interrupt levels | INTA, INTB, INTC, INTD, MSI, MSI-X |
| Hardware certifications | FCC B, UL CE, VCCI, BSMI, CTICK, KCC |
| Controller | Intel® Ethernet Controller I210 |
| Power consumption (active-typical) | 0.81 W |
| Operating temperature | 0 °C to 55 °C (32 °F to 131°F) |
| Storage temperature | -40 °C to 70 °C (-40 °F to 158 °F) |
| Storage humidity | 90% non-condensing relative humidity at 35 °C |
| Connect speed LED Indicators | Link/Activity LED: off = No Link; on = Link; Blinking = Activity<br>Speed LED: Not illuminated = 10Mb/s; green = 100Mb/s; amber = 1Gb/s |

## Physical Dimensions

| | |
|---|---|
| Length | 6.7 cm (2.64 inches) |
| (Bracket) Width | 1.8 cm (0.71 inches) |
| Full-height end bracket | 12.07 cm (4.76 inches) |
| Low-profile end bracket | 8 cm (3.15 inches) |

## Supported Operating Systems

For a complete list of supported network operating systems for Intel® Ethernet Network Adapters visit:
intel.com/support/EthernetOS

## Product Order Codes

| | |
|---|---|
| I210T1 | Single Pack |
| I210T1BLK | Bulk |

## Warranty

Intel limited lifetime warranty for retail Ethernet Products, 90-day money-back guarantee (US and Canada).

## Customer Support

For customer support options in North America visit:
intel.com/content/www/us/en/support/contact-support.html

## Product Information

For information about Intel® Ethernet Products and technologies, visit: intel.com/ethernetproducts

1. Low Halogen--Applies only to brominated and chlorinated flame retardants (BFRs/CFRs) and PVC in the final product. Intel components as well as purchased components on the finished assembly meet JS-709A requirements, and the PCB/Substrate meet IEC 61249-2-21 requirements. The replacement of halogenated flame retardants and/or PVC may not be better for the environment.



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