Product Marking Information for Agilex™ 7 and Agilex™ 5 FPGAs and SoCs

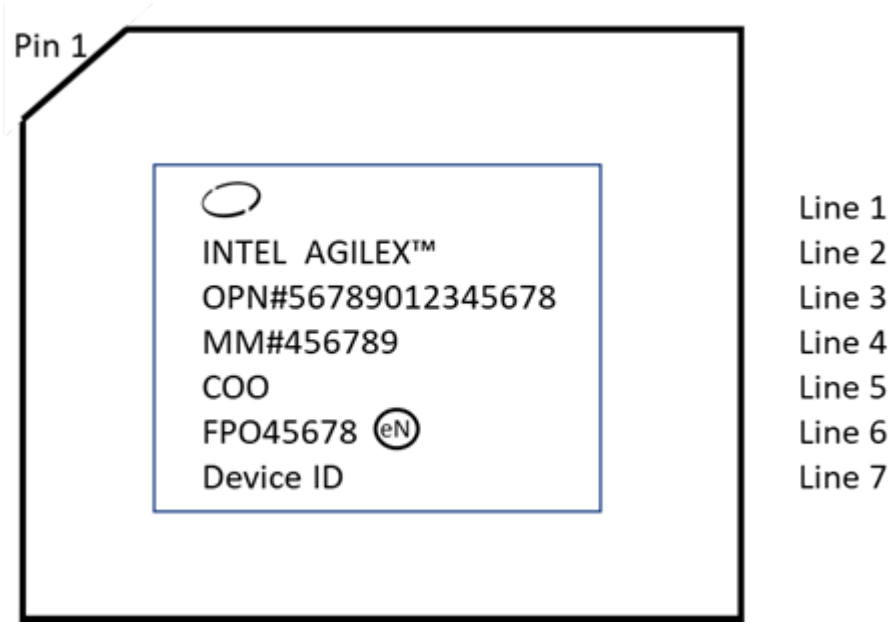
Version: **2.0**

Last updated: **November 2024**

Reference Number: 11G-00016

Contents

1.0 Top Mark Layout for Agilex™ 7 and Agilex™ 5 FPGAs and SoCs



Line 1	Intel swirl logo
Line 2	Family Name (Intel Agilex)
Line 3	Device Name (OPN)
Line 4	Unit Intel ID (MM)
Line 5	Country of Origin (COO)
Line 6	Lot number (Intel FPO) + 2nd level interconnect symbol e(N)
Line 7	Unit level ID (Device Visual ID)

2.0 Document Revision History

Date	Version	Changes
December 2021	1.0	Initial release.