

Product Marking Information for Intel® Max® 10 Devices

Version: 2.0

Last updated: February 2023

Reference Number: 11G-00016



You may not use or facilitate the use of this document in connection with any infringement or other legal analysis concerning Intel products described herein.

No license (express or implied, by estoppel or otherwise) to any intellectual property rights is granted by this document.

All information provided here is subject to change without notice. Contact your Intel representative to obtain the latest Intel product specifications and roadmaps.

The products described may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Intel, the Intel logo, Agilex, Altera, Arria, Cyclone, Enpirion, eASIC, easicopy, MAX, Nios, Quartus, Stratix words and logos are trademarks of Intel Corporation or its subsidiaries in the U.S. and/or other countries. Intel warrants performance of its FPGA and semiconductor products to current specifications in accordance with Intel's standard warranty but reserves the right to make changes to any products and services at any time without notice. Intel assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Intel. Intel customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.

*Other names and brands may be claimed as the property of others.

Copyright © 2023, Intel Corporation. All rights reserved.



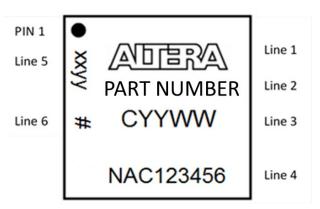
Contents

1.0 Top Mark Layout for Intel Max 10 Devices	4
- VBGA/YBGA Package	
- EQFP Package	
- MBGA Package	
- UBGA 169 Package	
- UBGA 324 Package	
- FBGA Package	
2.0 Document Revision History	10



1.0 Top Mark Layout for Intel Max 10 Devices

VBGA/YBGA Package



Marking Description		
Line 1	ALTERA® logo	
Line 2	Device Name (note 1)	
Line 3	Date code	
	(YY = last 2 digits of the	
	year; WW= Workweek)	
Line 4	Trace Code	
Line 5	Die coordinates in wafer map	
Line 6	Bin number	
Example		
Line 1	ALTERA®	
Line 2	10M08V81G (note 1)	
Line 3	C2249	
Line 4	S908BP01	
Line 5	46-48	
Line 6	В	

6-Week Datecode Scheme	
Work Week	Date Code
1 - 6	YY01
7 - 12	YY07
13 - 18	YY13
19 - 24	YY19
25 - 30	YY25
31 - 36	YY31
37 - 42	YY37
43 - 48	YY43
49 – 53	YY49

Note 1:

Shortened device or part number.

Example: "10M08V81G" for device 10M08SLV81I8G.



EQFP Package

Pin 1



	Marking Description
Line 1	ALTERA® logo
Line 2	Product Family logo
Line 3	Device Name
	(Example: 10M08SAE144I7G)
Line 4	Datecode
Line 5	Lot Code
Line 6	Trace Code

6-Week Datecode Scheme		
Work Week	Date Code	
1 - 6	YY01	
7 - 12	YY07	
13 - 18	YY13	
19 - 24	YY19	
25 - 30	YY25	
31 - 36	YY31	
37 - 42	YY37	
43 - 48	YY43	
49 - 53	YY49	



MBGA Package

Pin 1

Trace of Tr

Line 1

Line 2

Line 3

Line 4

Line 5

Line 6

Marking Description	
Line 1	Company (ALTERA®) logo
Line 2	Device Name
Line 3	(Example: 10M08SAM153I7G)
Line 4	Datecode
Line 5	
Line 6	Lot Code
Line 7	Tracecode

6-Week Datecode Scheme		
Work Week	Date Code	
1 - 6	YY01	
7 - 12	YY07	
13 - 18	YY13	
19 - 24	YY19	
25 - 30	YY25	
31 - 36	YY31	
37 - 42	YY37	
43 - 48	YY43	
49 - 53	YY49	



UBGA 169 Package

Pin 1



Line 1

Line 2

Line 3

Line 4

Line 5 Line 6

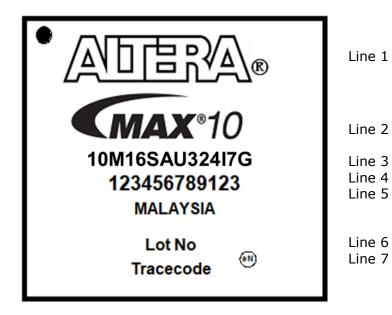
Marking Description	
Line 1	ALTERA® logo
Line 2	Device Name (Example: 10M02SCU169C8G)
Line 3	Datecode
Line 4	Country of Origin
Line 5	Lot Code
Line 6	Trace Code

6-Week Datecode Scheme		
Work Week	Date Code	
1 - 6	YY01	
7 - 12	YY07	
13 - 18	YY13	
19 - 24	YY19	
25 - 30	YY25	
31 - 36	YY31	
37 - 42	YY37	
43 - 48	YY43	
49 – 53	YY49	



UBGA 324 Package

Pin 1



Marking Description		
Line 1	ALTERA® logo	
Line 2	Product Family logo	
Line 3	Device Name	
	(Example: 10M16SAU324I7G)	
Line 4	Datecode	
Line 5	Country of Origin	
Line 6	Lot Code	
Line 7	Trace Code	

6-Week Datecode Scheme	
Work Week	Date Code
1 - 6	YY01
7 – 12	YY07
13 - 18	YY13
19 - 24	YY19
25 - 30	YY25
31 - 36	YY31
37 - 42	YY37
43 - 48	YY43
49 – 53	YY49

8



FBGA Package

Pin 1



Marking Description		
Line 1	ALTERA® logo	
Line 2	Product Family logo	
Line 3	Device Name	
	(Example: 10M40DCF672I7GAA)	
Line 4	Datecode	
Line 5	Country of Origin	
Line 6	Lot Code	
Line 7	Trace Code	

6-Week Datecode Scheme		
Work Week	Date Code	
1 - 6	YY01	
7 – 12	YY07	
13 - 18	YY13	
19 - 24	YY19	
25 - 30	YY25	
31 - 36	YY31	
37 - 42	YY37	
43 - 48	YY43	
49 - 53	YY49	



2.0 Document Revision History

Date	Version	Changes
August 2020	1.0	Initial release.
February 2023	2.0	Updated to add marking lay-outs of the different packages in the product family.