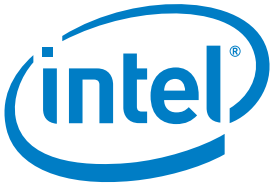

Intel® FPGA
Product Marking Information
Cyclone®, Cyclone® V, IV, III, II

Top Mark Layout for Intel® Cyclone®, Cyclone® V, IV, III, II

Line 1
Line 2
Line 3
Line 4
Line 5
Line 6
Line 7

Line 1 Company (Altera) logo
Line 2 Family logo
Line 3 Device Name
Line 4 Date Code
Line 5 Country where device is assembled
Line 6/
Line 7 Top ID (FPO/Lot# + Tracecode)
Certain packages (RQFP, EQUAD) will have the Top ID marked in a single line.

Datecode:
A Xβ Z αα YYWWT where:
A, X, β , Z, αα, T - Manufacturing Identifiers
YYWW - YY = Year, WW = Workweek in a 6-week datecode window

Example
Line 1 ALTERA®
Line 2 Cyclone®V
Line 3 5CEFA4M1317N
Line 4 U HAF481913A
Line 5 MALAYSIA
Line 6 S908BP01
Line 7 3P2UA9D0P

6-week Datecode Scheme

Work Week	Datecode
1 – 6	YY01
7 – 12	YY07
13 – 18	YY13
19 – 24	YY19
25 – 30	YY25
31 – 36	YY31
37 – 42	YY37
43 – 48	YY43
49 – 53	YY49

Revision History

Revision Number	Description	Revision Date
1.0	Initial release. Reference: 11G-00016.	