Agilex™ 7 FPGAs and SoCs I-Series Product Table

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Version 2024.02.08

	Product Line	AGI 019	AGI 023	AGI 022	AGI 027	AGI 035	AGI 040	AGI 041
Resources	Logic elements (LEs)	1,918,975	2,308,080	2,208,075	2,692,760	3,540,000	4,047,400	4,000,672
	Adaptive logic modules (ALMs)	650,500	782,400	748,500	912,800	1,200,000	1,372,000	1,356,160
	ALM registers	2,602,000	3,129,600	2,994,000	3,651,200	4,800,000	5,488,000	5,424,640
	High-performance crypto blocks	2	2	0	0	4	4	4
	eSRAM memory blocks	1	1	0	0	3	3	2
	eSRAM memory size (Mb)	18	18	0	0	54	54	36
	M20K memory blocks	8,500	10,464	10,900	13,272	14,931	19,908	17,136
	M20K memory size (Mb)	166	204	212	259	292	389	335
	MLAB memory count	32,525	39,120	37,425	45,640	60,000	68,600	67,808
	MLAB memory size (Mb)	20	24	23	28	37	42	42
	Fabric PLL	5	5	12	12	6	6	8
	I/O PLL	10	10	16	16	12	12	16
	Variable-precision digital signal processing (DSP) blocks	1,354	1,640	6,250	8,528	9,594	12,792	0
	18 x 19 multipliers	2,708	3,280	12,500	17,056	19,188	25,584	0
	Single-precison or half-precision tera floating point operations per second (TFLOPS)	2.4 / 4.9	2.4 / 4.9	9.4 / 18.8	12.8 / 25.6	14.3 / 28.7	19.1 / 38.3	0
Maximum Available Device Resources	Maximum EMIF x72[1]	3	3	4	4	4	4	4
	Maximum differential (RX or TX) pairs	240	240	360	360	288	288	372
	Maximum AIB Interfaces	4	4	4	4	6	6	4
	Memory devices supported	DDR4 and QDR IV						
	Secure device manager (SDM)	Provides SHA-384 bitstream integrity, ECDSA 256/384 bitstream authentication, AES-256 bitstream encryption, physically unclonable function (PUF) protected key storage, side-channel attack resistance, SPDM attestation, cryptographic services, physical anti-tamper support						
	Hard processor system	Quad-core 64 bit Arm Cortex*-A53 up to 1.50 GHz with 32 KB I/D cache , Neon* coprocessor, 1 MB L2 cache, direct memory access (DMA), system memory management unit, cache coherency unit, hard memory controllers, USB 2.0x2, 1G EMAC x3, UART x2, serial peripheral interface (SPI) x4, I2C x5, general purpose timers x7, watchdog timer x4				n/a		HPS support[2]
Tile Resources	F-Tile	PCI Express* (PCIe*) hard IP block (4.0 x16) or Bifurcateable 2x PCIe 4.0 x8 (EP) or 4x 4.0 x4 (RP) Transceiver channel count : - 4 channels at 116 Gbps (PAM4) / 58 Gbps (NRZ) - 16 channels at 32 Gbps (NRZ) /12 channels at 58 Gbps (PAM4) - RS & KP FEC Advanced networking support: - Bifurcatable 400 GbE hard IP block (10/25/50/100/200/400 GbE FEC/PCS/MAC) - Bifurcatable 200 Gb hard IP block (10/25/50/100/200 Gbs FEC/PCS) IEEE 1588 support PMA direct						
	R-Tile	Compute Express Interface (CXL) - Link width x16 lanes, x8 lanes PCIe hard IP block (5.0 x16) or Bifurcateable 2x PCIe 5.0 x8 (EP) or 4x 5.0 x4 (RP) Virtualization (SR-IOV) supporting 8 PFs/2k VFs Scalable IOV VirtIO support Precise time management PIPE direct						

Notes:
1. Max EMIF count achieved using AVST x8 mode Compact - Address/Cmd lane [3 lanes] configuration
2. Same HPS as AGI 027/022/023/019

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F-Tile - Package Options and I/O Pins	**Tile Configuration**	**GPIO (LVDS) / F-Tile 32G NRZ(58G PAM4) / High-Speed Transceiver 58G NRZ (116G PAM4) Channels**						
3184B (56 mm x 45 mm, 0.92 mm Hex)	F-Tile x4	480(240)/64(48)/8(8)	480(240)/64(48)/8(8)	720(360)/64(48)/8(8)	720(360)/64(48)/8(8)			732(366)/64(48)/8(8)
3948A (56mm x 56mm, 0.92 mm Hex)	F-Tile x6					576(288)/96(72)/24(24)	576(288/96(72)/24(24)	
F-Tile and R-Tile - Package Options and I/O Pins	**Tile Configuration**	**GPIO (LVDS) / F-Tile 32G NRZ(58G PAM4) / High-Speed Transceiver 58G NRZ(116G PAM4) Channels / R- Tile 32G PCIe (CXL) Lanes**						
1805A (42.5mm x 42.5mm, 1.025 mm Hex)	F-Tile x1 & R-Tile x 1	480(240)/16(12)/0(0)/16(16)	480(240)/16(12)/0(0)/16(16)					
2957A[3] (56 mm x 45 mm, 1.0 / 0.92 mm Hex)	F-Tile x1 & R-Tile x 3			720(360)/16(12)/4(4)/48(32)	720(360)/16(12)/4(4)/48(32)			720(360)/16(12)/4(4)/48(32)
3184A (56 mm x 45 mm, 0.92 mm Hex)	F Tile x3 & R-Tile x1			720(360)/48(36)/8(8)/16(16)	720(360)/48(36)/8(8)/16(16)			
3184E (56 mm x 45 mm, 0.92 mm Hex)	F Tile x2 & R-Tile x2							744(372)/32(24)/8(8)/32(32)

Notes:
3. Conditional pin migration from AGI 022/027 to AGI 041 device.
4. All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit www.intel.com/fpga.