Manufacturing with Intel® Stratix 10 Field Programmable Gate Arrays

Revision 1.1
Q1 2019

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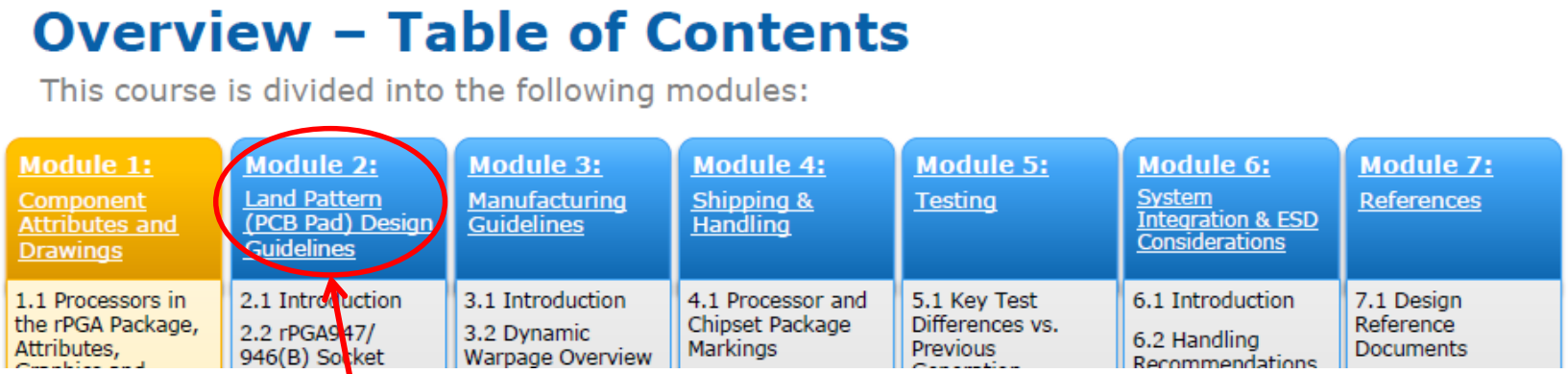
Introduction

- This Manufacturing Advantage Services (MAS) course shares Intel knowledge to facilitate customer manufacturing excellence as an advantage service.

Page Markings and Navigation Aids

Click on the house to go to a Table of Contents page.



These headers are links to modules.

Revision History

- **Revision 1.0**:
  - Original Document Release
- **Revision 1.1**:
  - Document title update

Module 1: Component Attributes and Drawings

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Overview – Table of Contents

This course is divided into the following modules:

Module 1:
Component Attributes, Drawings and Land Pattern (PCB Pad)

- 1.1 Recommended PCB Pad Patterns
- 1.2 Package Side Details (Informational)
- 1.3 Package Attributes
- 1.4 Board Side Recommendations

Module 2:
Manufacturing Guidelines

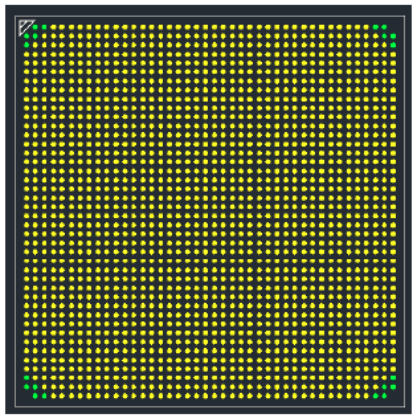
- 2.1 SMT Assembly Process Recommendations
- 2.2 Post Reflow Cleaning Risk
- 2.3 Proposed - Temporary Sealing Flip Chip Air Vent Process
- 2.4 SMT Rework Process Recommendations
- 2.5 Thermocouple Locations for Rework Thermal Reflow Profile
- 2.6 Intel® Lead-Free Rework Thermo Profile Graphic (for Stratix 10)
- 2.7 SMT Stencil Recommendations
- 2.7.1-.6 SMT & Rework Mini- Stencil F35, F43, F48, F50, F53, F55
- 2.8 X-Ray Exposure Time Recommendation*

Module 3:
References

- 3.1 Reference Documents
- 3.2 Intel® Learning Network access Information
- 3.3 Resource Design Center access Information

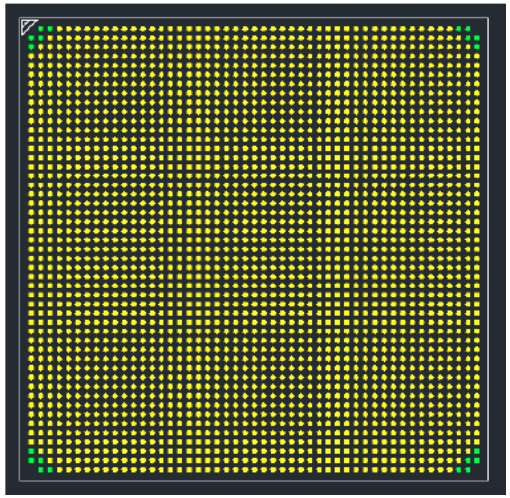
1.1 Recommended PCB Pad Patterns

F43 Package
(42x42) - 4 = 1760 balls



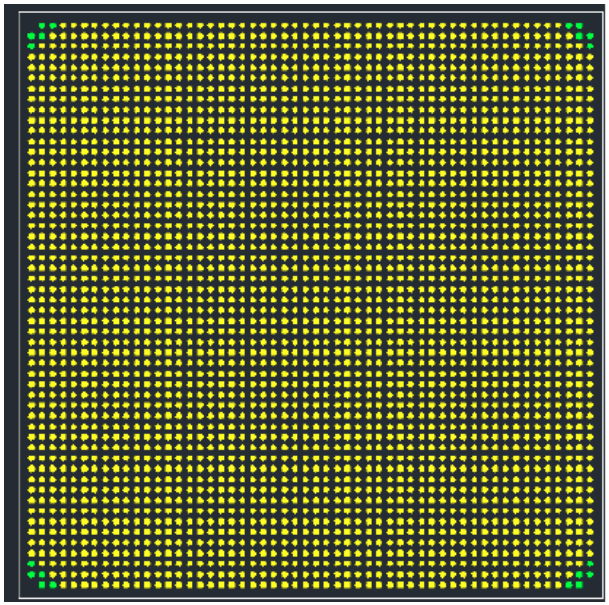
42x42 grid:
42.5x42.5mm package

F50 Package
(49x49) - 4 = 2397 balls



49x49 grid:
50x50mm package

F55 Package
(54x54) - 4 = 2912 balls

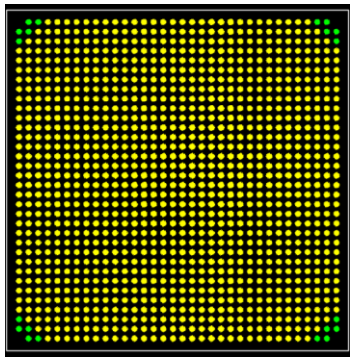


54x54 grid:
55x55mm package

Pad	Definition
Yellow Circle	Metal defined 20 mils (0.51 mm) round pad.
Green Circle	Solder Mask Defined – 20 mils (0.51 mm) SRO on a 24 mils (0.61 mm) round pad

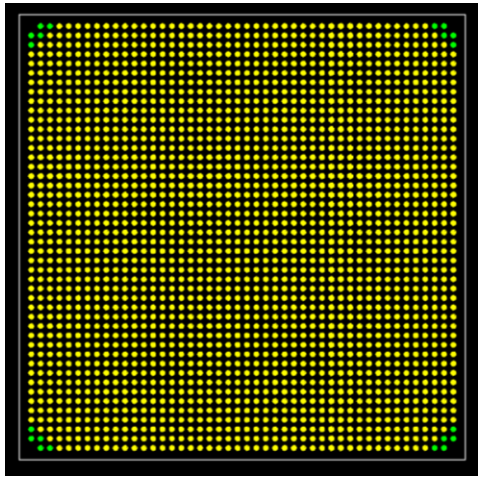
1.1 Recommended PCB Pad Patterns

F35 Package
(34x34) - 4 = 1152 balls



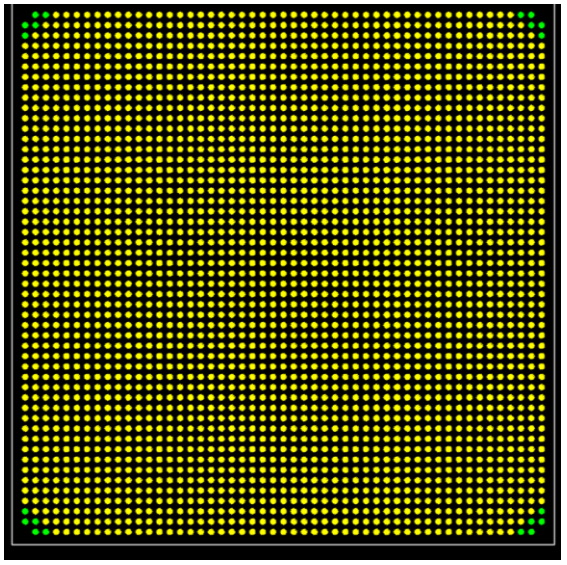
34x34 grid:
35x35mm package

F48 Package
(46x46) - 4 = 2112 balls



46x46 grid:
47.5x47.5mm package

F53 Package
(51x51) - 4 = 2597 balls



51x51 grid:
52.5x52.5mm package

Pad	Definition
Yellow Circle	Metal defined 20 mils (0.51 mm) round pad.
Green Circle	Solder Mask Defined – 20 mils (0.51 mm) SRO on a 24 mils (0.61 mm) round pad

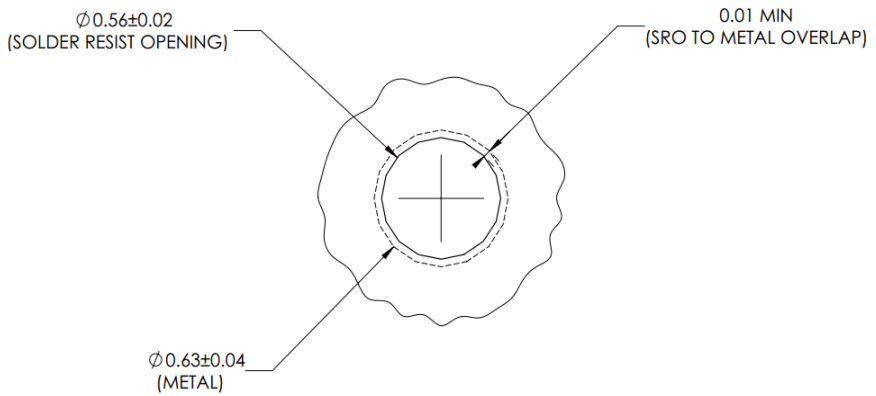
1.2 Package Side Details (Informational)

For all packages, package side pad Solder Resist Opening (SRO) is the same

- Function of the ball pitch

Pad definition on package

- 0.56mm (22.1 mil) SRO
- On a 0.63mm (24.8 mil) pad



1.3 Package Attributes

Attribute	F35	F43	F48	F50	F53	F55
	1	2	3	4	5	6
Package Size (mm)	35 x 35	42.5 x 42.5	47.5 x 47.5	50 x 50	52.5 x 52.5	55 x 55
Integrated Heat Spreader	Yes	Yes	Yes	Yes	Yes	Yes
Ball Count	1152	1760	2112	2397	2597	2912
Min Ball Pitch (mm)	1	1	1	1	1	1
Ball Diameter (Pre-attach) (um)	610	610	610	610	610	610

1.4 Board Side Recommendations

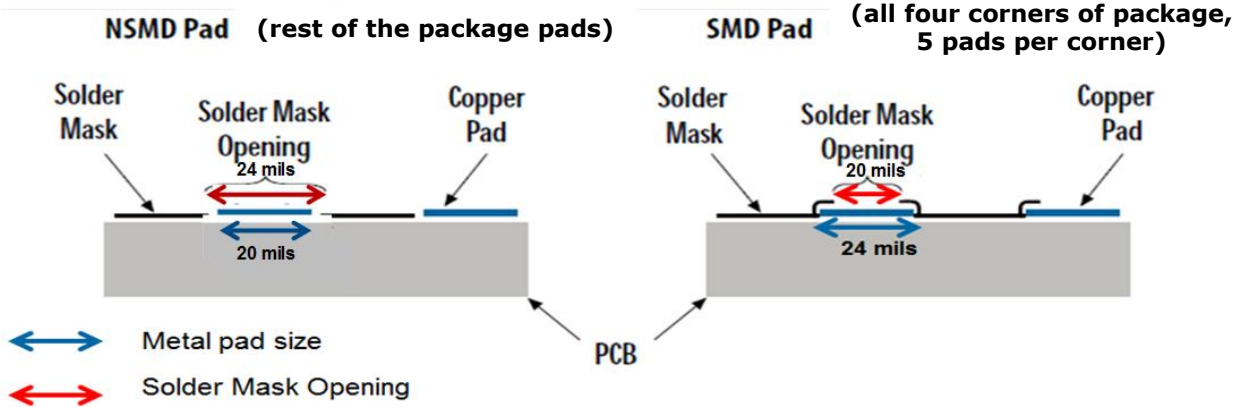
Starting with a 1.1:1 ratio (package pad area : board pad area) design intent, board side pad can be max of 0.51mm (20 mils)

- Choose max pad size to maximize Solder Joint Reliability (SJR)

Pad construction - Solder Mask Defined (SMD) and Non-Solder Mask Defined (NSMD)

- Choose NSMD metal defined pads wherever possible
- Choose SMD solder mask defined pads in the 5 outermost pads on each corner to maximize shock and bend reliability

Reliability considerations - especially Shock and Bend, corner joints are more susceptible to damage from use conditions that are emulated in standard reliability testing methodologies



Module 2: Assembly & Rework Process, Stencil Design and *X-Ray Exposure Time Recommendations

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- 2.8 X-Ray Exposure Time Recommendation*

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2.1 SMT Assembly Process Recommendations

Parameter		Recommendations for Customer Evaluation
Moisture		
Moisture Sensitivity Level (MSL)		MSL3
Solder Paste Print		
Intel Evaluated Solder Pastes		SAC 305, Type 3 or greater, no clean SMT paste (Shenmao PF606-P*)
Stencil Thickness & Aperture Design		Refer to stencil design recommendations
Pick and Place (PnP)		
Component Placement		100% ball recognition
Reflow		
Reflow Pallets		Refer to SMT Reflow Pallet Recommendations
Reflow Profile	Reflow Ambient	Air
	Rising (+) and Falling (-) Ramp Rate	< 3 °C/second
	Soak Temp and Time	Paste Dependent. Follow paste manufacturer's requirements
	Time Above ≥ 220°C	60 – 120 seconds
	Solder Joint Peak Reflow Temp	235 - 245°C
	Maximum Body and Substrate Temp	≤245°C
	Component Delta T (ΔT)	Control ΔT across component to <8°C for uniform heating

Notes:

- Intel's SMT process recommendation is for no clean SMT paste process, use of water-soluble flux/paste combined with deflux (wash process) could impact the mechanical and thermal integrity of the FPGA
- Except for body temp, all temperatures are measured with thermo-couples inside solder joints, for increased accuracy.
- This is Intel's reflow reference process practices and parameters are provided for reference purposes only, based on internal studies, and are not necessarily optimized. Mfg. processes are unique and may require unique solutions to ensure an acceptable level of quality, reliability, and mfg yield. Due to the differences in equipment and materials, process parameter modifications may be required to meet customer's quality, reliability, and manufacturing yield requirements.
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- *Other names and brands may be claimed as the property of others.

2.1.1 SMT Assembly Process Recommendations

Manufacturing Guidelines

General Information

- **Intel believes that following the process & material parameter recommendations outlined in IPC7095C* and in this module may be required to achieve acceptable SMT yields.**
  - Solder paste formulation and solder paste volume optimization are the two most effective ways to mitigate solder joint formation defects.
  - In order to increase SMT process margin and achieve acceptable SMT yields, Intel strongly recommends that customers select the right solder paste formulation
  - Intel has performed a higher level of SJQ characterization on the FCBGAs and this module contains the recommended solder paste formulations and stencil designs
  - Intel recognizes customer needs to optimize SMT yield across the entire motherboard and its components. This module serves to provide a starting guide for customers, and final optimization is specific to each customer design and process considerations
- **Intel believes that following the process & material parameter recommendations in this module may be required to achieve acceptable SMT yields.**

Failure to implement the recommendations in this module can lead to higher than expected SMT yield loss

Notes:
- See the Manufacturing with Intel® FCBGA Components for Solder Joint Quality MAS for deeper training of warpage fundamentals.
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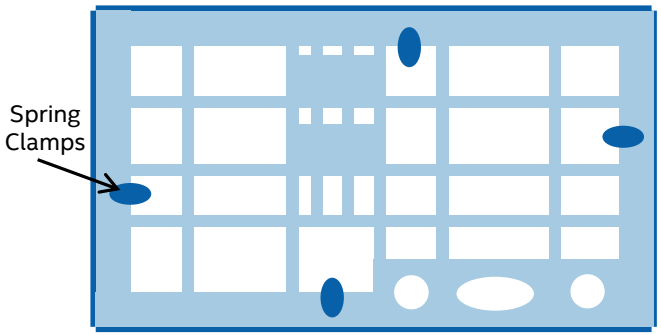
2.1.2 SMT Assembly Process Recommendations

SMT Reflow Pallet Recommendations

- ***Background:*** Pallets are typically used during SMT to keep the board "flat" to improve yield and/or to protect key components.
- ***Intel Recommendations:***
  1. Use a pallet for all reflow processes.
  2. Support board across the span to prevent sagging at high temperatures.
  3. Top of board height = top of pallet height (within tolerance ranges)
  4. Provide adequate clearance for thermal expansion of the PCB during reflow: 1mm (min) clearance from all board edges.
  5. Use edge low force spring clamps around the perimeter of the PCB.
  6. Evaluate the product board design to understand high-temperature flatness. See IPC 9641 *High Temperature Printed Board Flatness Guideline* for additional information.



Example Depiction of Pallet Design with Four Spring Clamps and adequate PCB span support

(a) (b)

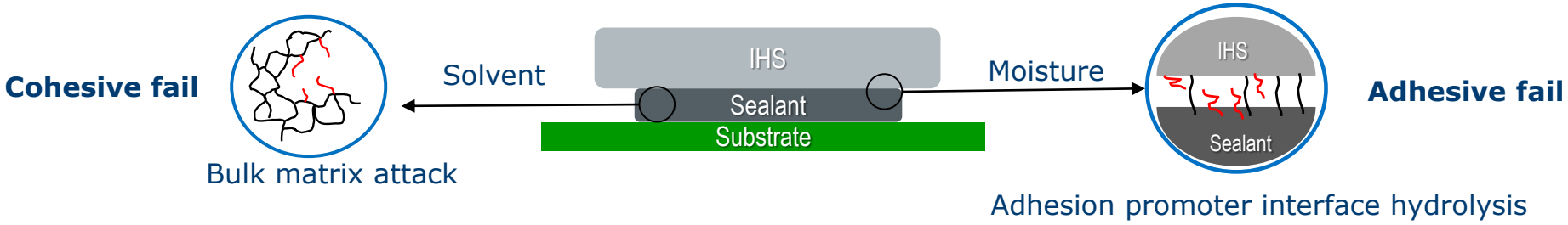
Example of Spring Clamp:
(a) Without Board and
(b) Clamping a Board

Minimizing board warpage to <50 µm (<2 mils) in the FCBGA area during reflow is strongly recommended. The use of a pallet[1] is one minimizing approach.

[1]Results may vary by pallet and board design features: Use of spring clamps, material type, unsupported spans near land area, etc.

2.2 Post Reflow Cleaning Risk

Intel recommendation to customers to exclude deflux/solvent wash post SMT based on known impact to adhesion degradation



- Intel flip chips are not hermetically sealed and exposure to cleaning solvents or excessive moisture during any step of board assembly could pose significantly impact to the mechanical & thermal integrity of the flip chips.
- Note: The integrated heat spreader (IHS) requires a small vent hole to allow for packaging material outgassing during assembly. If the flip chip is exposed to solvents or moisture they could seep into the IHS cavity and damage the underlying components.

  In particular three key risk arise:
  1. Degradation of the adhesion of the heat spreader sealant
  2. Degradation of the thermal interface material
  3. Corrosion of underlying components
- Therefore, Intel recommends using no-clean SMT with no post SMT cleaning to prevent any risk to the flip chip.
- If post SMT cleaning is **absolutely needed** in the process, the air vents must be closed temporarily just before the wash cycle, and open them after wash and before bake.
  - To prevent degradation/corrosion of components use of a water soluble paste and wash with deionized water in the deflux tooling. Please follow standard MSL baking requirements to ensure all moisture removed from the Flip Chip /board (typically 125C , 4-8 hours)
    - *Note: These are guidelines, please consultant with individual suppliers best know manufacturing practices*

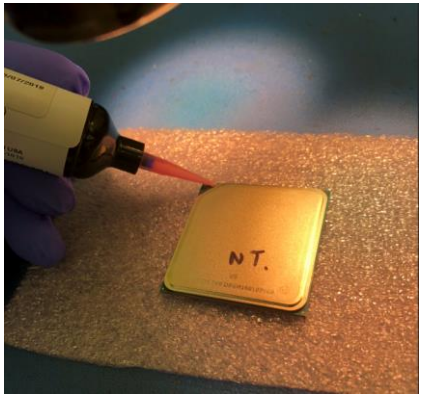
2.3 Proposed – Temporary Sealing Flip Chip Air Vent Process

- After SMT process, seal the air vent of the Flip Chip
- Cure the sealant material* under UV light for about 10 minutes.
- Go through the Wash Process
- After Wash Process, use oil-free air to dry and remove any excess water from the board/components.
- Peel off the air vent sealant with a tweezer
- Proceed to bake the board/components to ensure all moisture removed from the Flip Chip /board (typically 125C , 4-8 hours)

Notes:
- Commercially Available Sealant Materials – Dymax 725 SpeedMask Masking Resin and Dymax E-Max 906-B-Rev A

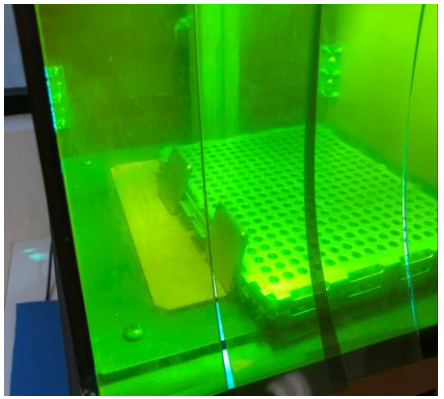
2.3 Temporary Sealing Flip Chip Air Vent Process

1



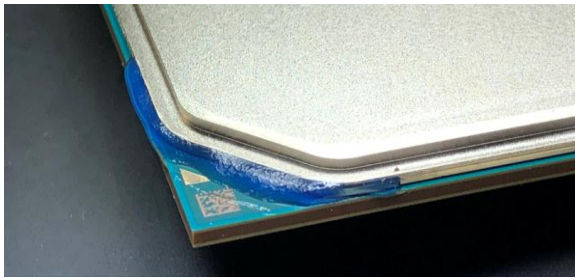
Sealing of air vent in pin #1 location

2



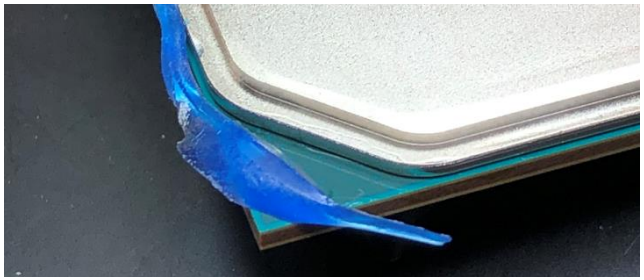
UV Curing of the sealant material

3



UV Cured Sealant at pin #1 location

4



Sealant peel-off after wash process

2.4 SMT Rework Process Recommendations

FCBGAs/Chipset	Flux-Only Application (applied on the PCB Pads)	Solder Paste Application (applied to the PCB Pads by Mini-Stencil)
Stratix 10	Recommended	Recommended

Rework recommendations for customer consideration.	
Parameters	**FCBGA & Chipset**
Solder Paste Formulation	SAC305 (LF) Type 3 or greater no clean SMT paste
Intel Evaluated Flux Formulation	Tacky Flux No-Clean Lead-Free Flux Alpha*PoP 707, Tacky flux, No-Clean Lead-Free Flux
Rework pallets	Case dependent - follow customer practice
Gap between nozzle & PCB surface (optimize air flow)	762 µm (30 mils)
Placement force	0 grams (paste application) 140 grams (flux application)
Rework Ambient	Air
Solder Joint Peak Reflow Temperature (PRT)	230 to 245°C
Time Above ≥ 217°C	60 to 120 seconds
Maximum Body Temperature	Never exceed component substrate temperature ≤ 245°C
Component Delta T (ΔT)	≤10°C
Soak Temp & Time	Paste dependant; consult paste manufacturer.
Rising Ramp Rate below 150°C (+)	0.5 to 2.5°C/sec
Rising Ramp Rate between 205°C and 215°C (+)	0.35 to 0.75°C/sec
Falling Ramp Rate (-)	0.50 to 2.0°C/sec

Notes:

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- Except for body temp, all temperatures are measured with thermo couples inside solder joints, for increased accuracy.
- This is Intel's rework reference process practices and parameters are provided for reference purposes only, based on internal studies, and are not necessarily optimized. Mfg. processes are unique and may require unique solutions to ensure an acceptable level of quality, reliability, and mfg yield. Due to the differences in equipments and materials, process parameter modifications may be required to meet customer's quality, reliability, and manufacturing yield requirements.
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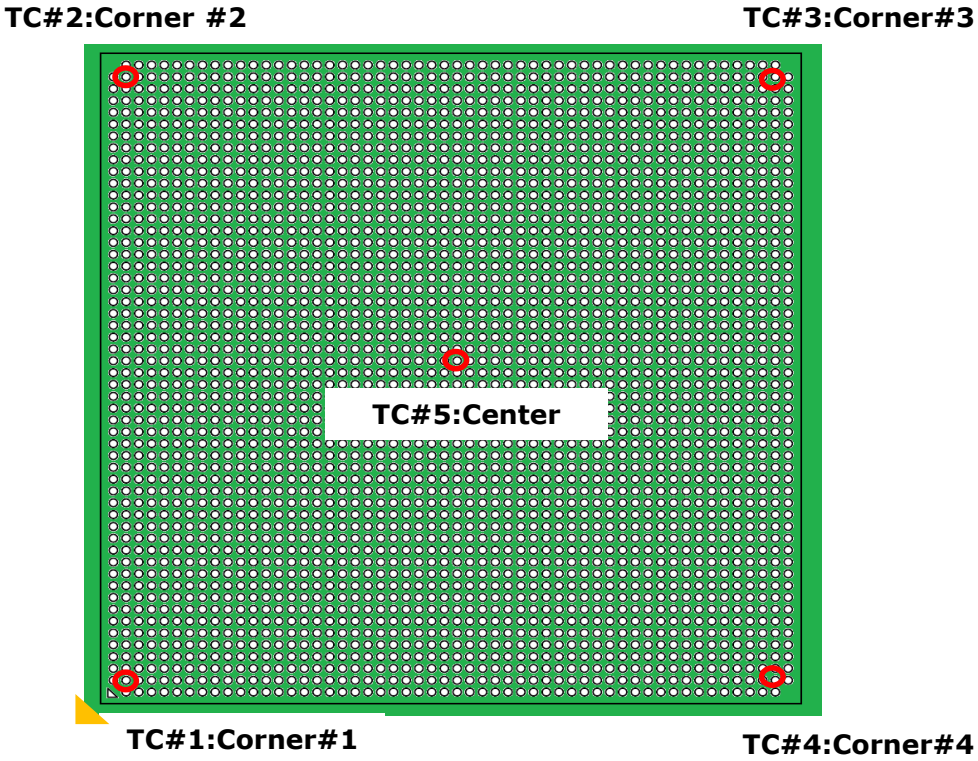
2.5 Thermocouple Locations for Rework Thermal Reflow Profile



Mounted into PCB Pads

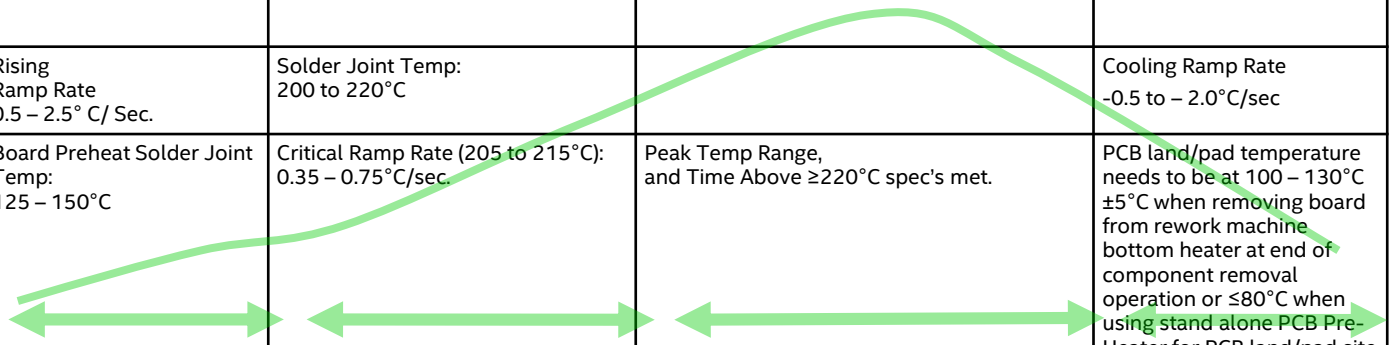
Comments: Drill holes in the RED PCB pads and mount the TC wire tips in the RED PCB pads shown on the image. Label TC connectors per TC # in above table.

TC #	Corner#
1	Corner#1
2	Corner#2
3	Corner#3
4	Corner#4
5	Center

Intel recommends the Lead Free component be thermo coupled at the specific locations in order to ensure an accurate reflow profile

2.6 Lead-Free Rework Thermo Profile Graphic (for Stratix 10)

Step 1 Board Preheat	Step 2 Soak Time	Step 3 Peak Reflow & Time Above 220 °C	Step 4 Cool Down
Start with solder joint temp ≤ 40°C	After nozzle is lowered prior to peak reflow (Soak Time: Paste dependant; consult paste manufacturer)	Solder Joint Temp 230 – 245°C Above ≥217°C 60 – 120 sec Max delta-t of solder joint temperature at peak reflow ≤10°C	Substrate MAX Temperature ≤245°C
Rising Ramp Rate 0.5 – 2.5° C/ Sec.	Solder Joint Temp: 200 to 220°C		Cooling Ramp Rate -0.5 to – 2.0°C/sec
Board Preheat Solder Joint Temp: 125 – 150°C	Critical Ramp Rate (205 to 215°C): 0.35 – 0.75°C/sec.	Peak Temp Range, and Time Above ≥220°C spec's met.	PCB land/pad temperature needs to be at 100 – 130°C ±5°C when removing board from rework machine bottom heater at end of component removal operation or ≤80°C when using stand alone PCB Pre-Heater for PCB land/pad site dress operation.
Preheat with bottom heater, before nozzle is lowered	Nozzle has lowered to reflow component	Nozzle is down during peak reflow	Nozzle raises to home position when solder joint reaches peak temp range



2.7 SMT Stencil Recommendations

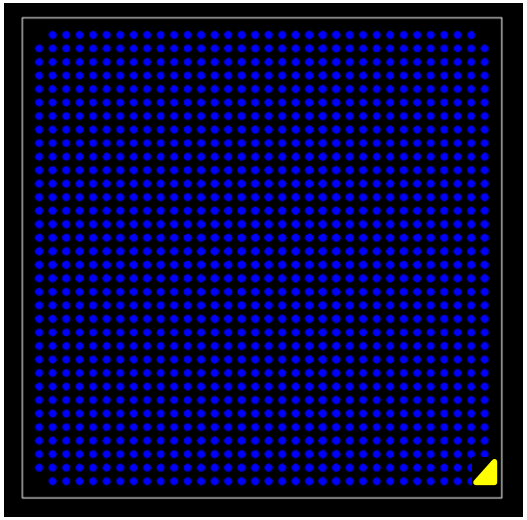
The stencil recommendations are based on Intel's experience with large packages

While you may have used a single stencil opening size in the past, these recommendations are considered to be the best way to mount Stratix 10 packages

These recommendations are intended to maximize the initial assembly yield and the long term reliability of the Stratix 10 board assembly

2.7.1 SMT & Rework Mini- Stencil Recommendations F35 (35mmx35mm)

Stencil Thickness: 127 µm (5 mils) option			
Stencil Design (Aperture)	**Over-printing**	**Solder Paste Volume Target**	**Area Ratio**
BGA Body Pads • Round 20mils	See notes	0.0257 cu. mm (1570 cu. mils)	1.00

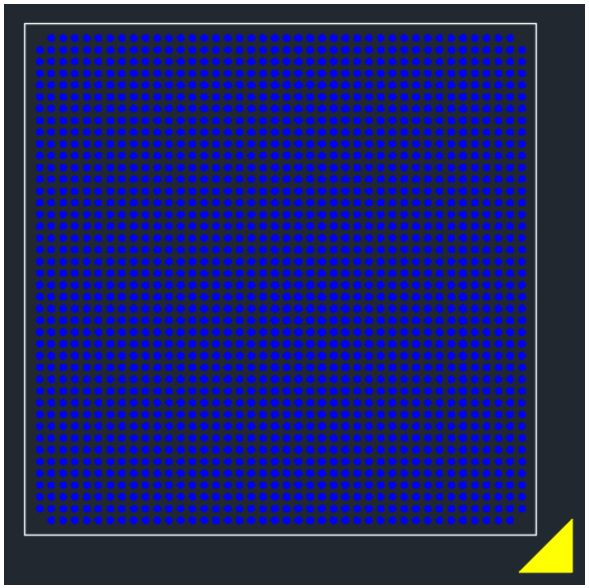


*For Step Top Lids

Notes:
- "Under print" in center of package to minimize paste volume to compensate for possible extra solder joint compression because of package mass and warpage.

2.7.2 SMT & Rework Mini- Stencil Recommendations F43 (42.5mmx42.5mm)

Stencil Thickness: 127 µm (5 mils) option			
Stencil Design (Aperture)	**Over-printing**	**Solder Paste Volume Target**	**Area Ratio**
BGA Body Pads • Round 20mils	See notes	0.0257 cu. mm (1570 cu. mils)	1.00

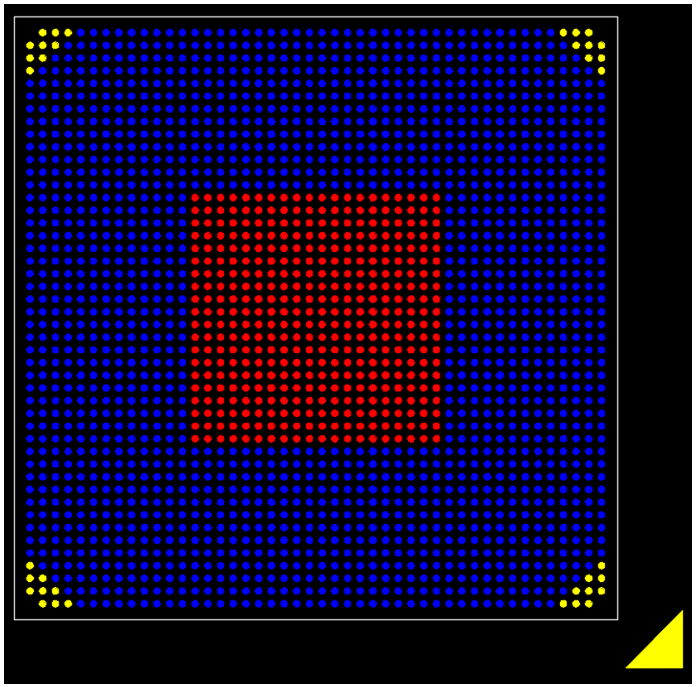


*For Step Top and Flat Top Lids

Notes:
- "Under print" in center of package to minimize paste volume to compensate for possible extra solder joint compression because of package mass and warpage.

2.7.3 SMT & Rework Mini- Stencil Recommendations F48 (47.5mmx47.5mm)

Stencil Thickness: 127 µm (5 mils) option			
Stencil Design (Aperture)	**Over-printing**	**Solder Paste Volume Target**	**Area Ratio**
BGA Body Pads Round 22mils (9 per corner)	See notes	0.0311 cu. mm (1900 cu. mils)	1.10
BGA Body Pads Round 18mils (20x20 grid)	See notes	0.0208 cu. mm (1272 cu. mils)	0.90
BGA Body Pads Round 25mils	See notes	0.0402 cu. mm (2453 cu. mils)	1.25

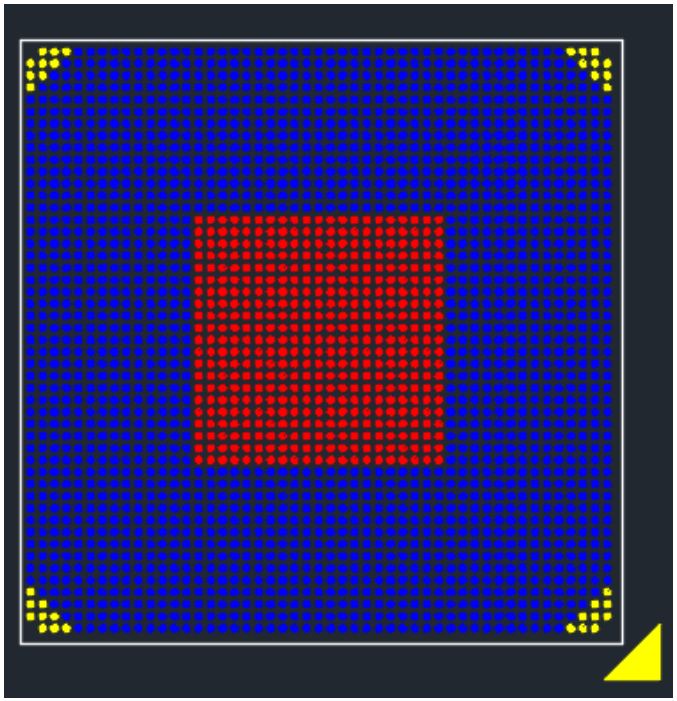


*For Step Top Lids

Notes:
- "Under print" in center of package to minimize paste volume to compensate for possible extra solder joint compression because of package mass and warpage.

2.7.4 SMT & Rework Mini- Stencil Recommendations F50 (50mmx50mm)

Stencil Thickness: 127 µm (5 mils) option			
Stencil Design (Aperture)	**Over-printing**	**Solder Paste Volume Target**	**Area Ratio**
BGA Body Pads Round 22mils (9 per corner)	See notes	0.0311 cu. mm (1900 cu. mils)	1.10
BGA Body Pads Round 18mils (21x21 grid)	See notes	0.0208 cu. mm (1272 cu. mils)	0.90
BGA Body Pads Round 25mils	See notes	0.0402 cu. mm (2453 cu. mils)	1.25

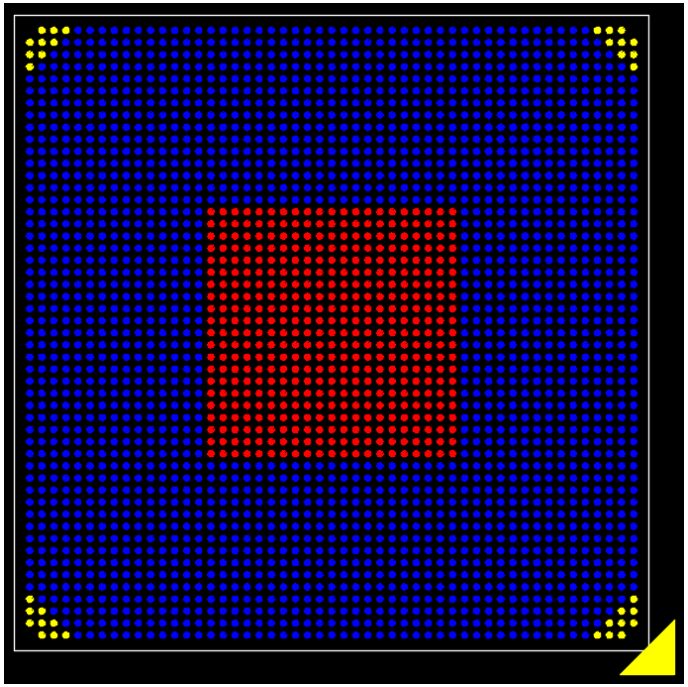


*For Step Top and Flat Top Lids

Notes:
- "Under print" in center of package to minimize paste volume to compensate for possible extra solder joint compression because of package mass and warpage.

2.7.5 SMT & Rework Mini- Stencil Recommendations F53 (52.5mmx52.5mm)

Stencil Thickness: 127 µm (5 mils) option			
Stencil Design (Aperture)	**Over-printing**	**Solder Paste Volume Target**	**Area Ratio**
BGA Body Pads Round 22mils (9 per corner)	See notes	0.0311 cu. mm (1900 cu. mils)	1.10
BGA Body Pads Round 18mils (21x21 grid)	See notes	0.0208 cu. mm (1272 cu. mils)	0.90
BGA Body Pads Round 25mils	See notes	0.0402 cu. mm (2453 cu. mils)	1.25

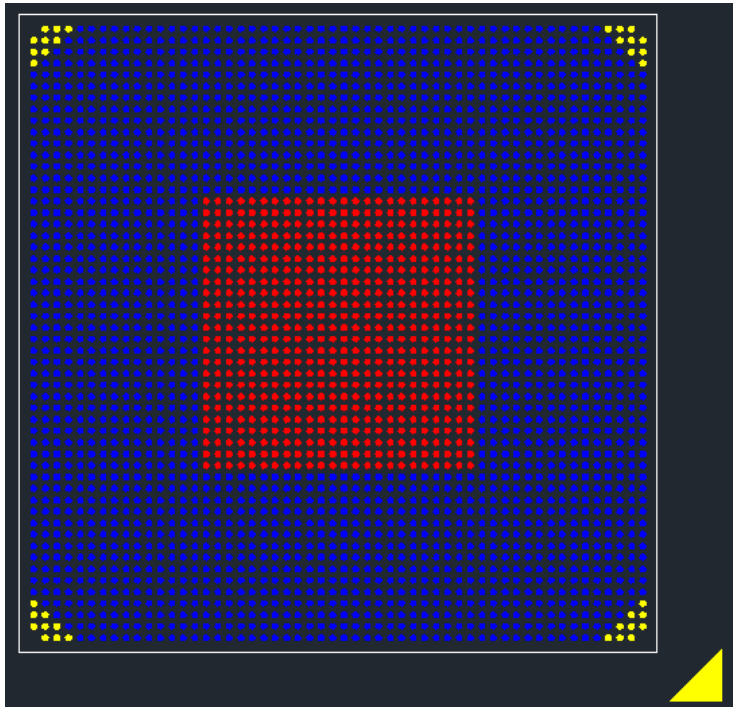


*For Step Top Lids

Notes:
- "Under print" in center of package to minimize paste volume to compensate for possible extra solder joint compression because of package mass and warpage.

2.7.6 SMT & Rework Mini- Stencil Recommendations F55 (55mmx55mm)

Stencil Thickness: 127 µm (5 mils) option			
Stencil Design (Aperture)	**Over-printing**	**Solder Paste Volume Target**	**Area Ratio**
BGA Body Pads Round 22mils (9 per corner)	See notes	0.0311 cu. mm (1900 cu. mils)	1.10
BGA Body Pads Round 18mils (24x24 grid)	See notes	0.0208 cu. mm (1272 cu. mils)	0.90
BGA Body Pads Round 25mils	See notes	0.0402 cu. mm (2453 cu. mils)	1.25



*For Step Top and Flat Top Lids

Notes:
- "Under print" in center of package to minimize paste volume to compensate for possible extra solder joint compression because of package mass and warpage.

2.8 X-Ray Exposure Time Recommendation (Only for MX Family Series)

Only applicable for Stratix 10 Devices with HBM (High Bandwidth Memory) DRAM Dies. MX Family Series.

- Please refer to document link: Customer Ready Summary Stratix 10 MX HBM X-Ray Exposure Recommendation

All other non HBM (High Bandwidth Memory) Stratix 10 Devices will follow normal X-Ray Operation

Module 3: References

Manufacturing with Intel® Stratix 10 Field Programmable Gate Arrays

MAS Revision 1.1

Q1 2019

Overview – Table of Contents

This course is divided into the following modules:

Module 1:
Component Attributes, Drawings and Land Pattern (PCB Pad)

- 1.1 Recommended PCB Pad Patterns
- 1.2 Package Side Details (Informational)
- 1.3 Package Attributes
- 1.4 Board Side Recommendations

Module 2:
Manufacturing Guidelines

- 2.1 SMT Assembly Process Recommendations
- 2.2 Post Reflow Cleaning Risk
- 2.3 Proposed - Temporary Sealing Flip Chip Air Vent Process
- 2.4 SMT Rework Process Recommendations
- 2.5 Thermocouple Locations for Rework Thermal Reflow Profile
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- 2.7.1-.6 SMT & Rework Mini- Stencil F35, F43, F48, F50, F53, F55
- 2.8 X-Ray Exposure Time Recommendation*

Module 3:
References

- 3.1 Reference Documents
- 3.2 Intel® Learning Network access Information
- 3.3 Resource Design Center access Information

Acronyms Found in this Module

MAS	Manufacturing Advantage Service
CNDA	Corporate Non-Disclosure Agreement
EDS	External Design Specification
IBP	Intel® Business Portal
PDG	Platform Design Guide
RDC	Resource Design Center
SJQ	Solder Joint Quality
TMDG	Thermal & Mechanical Design Guide

3.1 Reference Documents

The reader of this document should also be familiar with the material and concepts.

Title	Intel® Learning Network [1]	Document Number Searchable in RDC[2]
Manufacturing with Intel® Stratix 10 Field Programmable Gate Arrays [**THIS DOCUMENT**]	16950	603962
Intel® Stratix 10: MX Device, X-Ray Exposure Recommendation	TBD	TBD
Manufacturing with Intel® Products: Rework Guidance for Ball Grid Array (BGA), Package on Package (PoP), and Sockets	9699	541231

Notes:
- [1]Intel® Learning Network - http://learn.intel.com
- [2]If you type the provided document number into the search field of RDC it will retrieve the document.
- Contact your Intel representative for all document access questions.

3.2 How CNDA* Customers Access Documents from the Intel® Learning Network

1.Open your internet browser and go to http://learn.intel.com

2.Either log in using an existing account, or choose and 'click here' to setup a new account.

3.Register your new Intel® Learning Network account by setting up a username and password; complete the registration and profile requirements. Please use your company email address as part of the registration process.

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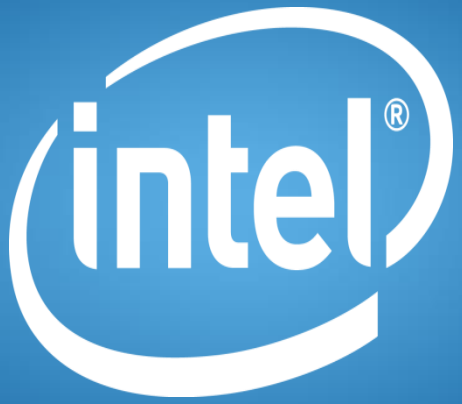
- Visit http://rdc.intel.com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