13th Generation Intel® Core™, Intel® Core™ 14th Generation, Intel® Core™ Processor (Series 1) and (Series 2), and Intel® Xeon™ E 2400 Processor, and Intel® Xeon™ 6300 Processor

Specification Update

Supporting 13th Generation Intel® Core™ Processor for S, H, P, HX, and U Processor Line Platforms, formerly known as Raptor Lake

Supporting Intel® Core™ 14th Generation Processor for S and HX Processor Line Platforms, formerly known as Raptor Lake Refresh

Supporting Intel® Core™ Processor (Series 1) for U Processor Line Platform, formerly known as Raptor Lake Refresh

Supporting Intel® Core™ Processor (Series 2) for H Processor Line Platform, formerly known as Raptor Lake Refresh

Supporting Intel® Xeon® E 2400 Processor and Intel® Xeon® 6300 Processor, formerly known As Raptor Lake−E Refresh

Revision 020

February 2025

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Revision History

Document Number	Revision Number	Description	Revision Date
740518	001	Initial Release • Errata Included: RPL001-RPL034	October 2022
	002	• Added Errata: RPL035, RPL036, RPL037	December 2022
	003	• Added H/P, U, and HX Processor Lines	January 2023
	004	• Added Errata: RPL038, RPL039	March 2023
	005	• Added Erratum: RPL040	May 2023
	006	• Added Errata: RPL041, RPL042	June 2023
	007	• Added Errata: RPL043, RPL044, RPL045, RPL046	July 2023
	008	• Added Errata: RPL047, RPL048, RPL049 • Updated Erratum: RPL042	August 2023
	009	• Added Erratum: RPL050	September 2023
	010	• Added Erratum: RPL051	October 2023
	011	• Added Erratum: RPL052	November 2023
	012	• Added Erratum: RPL053 • Initial revision for Intel® Xeon™ E2400 • Initial revision for Intel® Core™ 14th Generation Processor	December 2023
	013	• Added Erratum: RPL056 • Updated Erratum: RPL035, RPL050	March 2024
	014	• Added Errata: RPL057, RPL058	April 2024
	015	• Added Errata: RPL059, RPL060	May 2024
	016	• Added Errata: RPL061, RPL062, RPL063	October 2024
	017	• Added Errata: RPL064 • Updated Erratum: RPL063	November 2024
	018	• Added Errata: RPL054, RPL055, RPL065, RPL066 • Updated IDs for Errata RPL036-RPL037, RPL040-RPL049 • Added Processor Line naming conventions Intel® Core™ Processor (Series 1) and (Series 2) in Introduction • Initial revision for H Refresh Processor Line • Updated Errata Summary Table	December 2024
	019	• Added Errata: RPL067 • Updated IDs for Errata RPL054-RPL064	February 2025
	020	• Initial revision for E Refresh Processor Line	February 2025

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1 Preface

This document is an update to the specifications contained in the documents listed in the following Affected Documents/Related Documents table. It is a compilation of device and document errata and specification clarifications and changes, and is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this updated document and are no longer published in other documents. This document may also contain information that has not been previously published.

1.1 Affected Documents

Document Title	Document Number
13th Generation Intel® Core™ and Intel® Core™ 14th Generation Processors Datasheet, Volume 1 of 2	743844
13th Generation Intel® Core™ Processors Datasheet, Volume 2 of 2	743846

1.2 Related Documents

Document Title	Document Number/Location
AP-485, Intel® Processor Identification and the CPUID Instruction	http://www.intel.com/design/processor/applnots/241618.htm
Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 1: Basic Architecture Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 2A: Instruction Set Reference Manual A-M Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 2B: Instruction Set Reference Manual N-Z Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3A: System Programming Guide Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3B: System Programming Guide Intel® 64 and IA-32 Intel® Architecture Optimization Reference Manual	http://www.intel.com/products/processor/manuals/index.htm
Intel® 64 and IA-32 Architectures Software Developer's Manual Documentation Changes	http://www.intel.com/content/www/us/en/processors/architectures-software-developer-manuals.html
Intel® Virtualization Technology Specification for Directed I/O Architecture Specification	D51397-001
ACPI Specifications	www.acpi.info

1.3 Nomenclature

Errata – These are design defects or errors. Errata may cause the processor's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes – These are modifications to the current published specifications. These changes is incorporated in the next release of the specifications.

Specification Clarifications – This describe a specification in greater detail or further highlight a specifications impact to a complex design situation. These clarifications is incorporated in the next release of the specifications.

Documentation Changes – This include typos, errors, or omissions from the current published specifications. These changes are incorporated in the next release of the specifications.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications, and documentation changes are removed from the specification update, when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

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2 Identification Information

Processor line naming conventions in this document:
- S, H, P, HX, and U Processor Line when referring to 13th Generation Intel® Core™
- S Refresh, HX Refresh Processor when referring to Intel® Core™ 14th Generation
- U Refresh Processor when referring to Intel® Core™ Processor ("Series 1") and ("Series 2")
- H Refresh Processor when referring to Intel® Core™ Processor ("Series 2")
- E Processor when referring to Intel® Xeon® E 2400 Processor
- E Refresh Processor when referring to Intel® Xeon® 6300 Processor

2.1 Component Identification via Programming Interface

The processor stepping is identified by the following register contents:

Table 2-1. Processor Lines Component Identification

Processor	CPUID	Reserved [31:28]	Extended Family [27:20]	Extended Model [19:16]	Reserved [15:14]	Processor Type [13:12]	Family Code [11:8]	Model Number [7:4]	Stepping ID [3:0]
RPL-S 8P+16E	B0671h	Reserved	0000000b	1011b	Reserved	00b	0110b	0111b	0001b
RPL-S Refresh 8P+16E	B0671h	Reserved	0000000b	1011b	Reserved	00b	0110b	0111b	0001b
RPL-HX 8P+16E	B0671h	Reserved	0000000b	1011b	Reserved	00b	0110b	0111b	0001b
RPL-HX Refresh 8P+16E	B0671h	Reserved	0000000b	1011b	Reserved	00b	0110b	0111b	0001b
RPL-S 8P+8E	B06F2h	Reserved	0000000b	1011b	Reserved	00b	0110b	1111b	0010b
RPL-S Refresh 8P+8E	B06F2h	Reserved	0000000b	1011b	Reserved	00b	0110b	1111b	0010b
RPL-HX 8P+8E	B06F2h	Reserved	0000000b	1011b	Reserved	00b	0110b	1111b	0010b
RPL-S 6P+0E	B06F5h	Reserved	0000000b	1011b	Reserved	00b	0110b	1111b	0101b
RPL-S Refresh 6P+0E	B06F5h	Reserved	0000000b	1011b	Reserved	00b	0110b	1111b	0101b
RPL-P 6P+8E	B06A2h	Reserved	0000000b	1011b	Reserved	00b	0110b	1010b	0010b
RPL-H 6P+8E	B06A2h	Reserved	0000000b	1011b	Reserved	00b	0110b	1010b	0010b

Processor	CPUID	Reserved [31:28]	Extended Family [27:20]	Extended Model [19:16]	Reserved [15:14]	Processor Type [13:12]	Family Code [11:8]	Model Number [7:4]	Stepping ID [3:0]
RPL-H Refresh 6P+8E	B06A2h	Reserved	0000000b	1011b	Reserved	00b	0110b	1010b	0010b
RPL-U 2P+8E	B06A3h	Reserved	0000000b	1011b	Reserved	00b	0110b	1010b	0011b
RPL-U Refresh 2P+8E	B06A3h	Reserved	0000000b	1011b	Reserved	00b	0110b	1010b	0011b
RPL-E 8P+0E	B0671h	Reserved	0000000b	1011b	Reserved	00b	0110b	0111b	0001b
RPL-E Refresh 8P+0E	B0671h	Reserved	0000000b	1011b	Reserved	00b	0110b	0111b	0001b

1. The Extended Family, Bits [27:20] are used in conjunction with the Family Code, specified in Bits[11:8], to indicate whether the processor belongs to the Celeron®, Pentium®, or Intel® Core™ processor family.

2. The Extended Model, Bits [19:16] in conjunction with the Model Number, specified in Bits [7:4], are used to identify the model of the processor within the processor's family.

3. The Family Code corresponds to Bits [11:8] of the EDX register after RESET, Bits [11:8] of the EAX register after the CPUID instruction is executed with a 1 in the EAX register, and the generation field of the Device ID register accessible through Boundary Scan.

4. The Model Number corresponds to Bits [7:4] of the EDX register after RESET, Bits [7:4] of the EAX register after the CPUID instruction is executed with a 1 in the EAX register, and the model field of the Device ID register accessible through Boundary Scan.

5. The Stepping ID in Bits [3:0] indicates the revision number of that model. Refer table above for the processor stepping ID number in the CPUID information.

6. When EAX is initialized to a value of '1', the CPUID instruction returns the Extended Family, Extended Model, Processor Type, Family Code, Model Number and Stepping ID value in the EAX register. The EDX processor signature value after reset is equivalent to the processor signature output value in the EAX register.

Cache and TLB descriptor parameters are provided in the EAX, EBX, ECX and EDX registers after the CPUID instruction is executed with a 2 in the EAX register.

2.2 Component Marking Information

Figure 2-1. Processor Based on S/S-Refresh/E/E Refresh Processor Lines Chip Package LGA Top-Side Markings
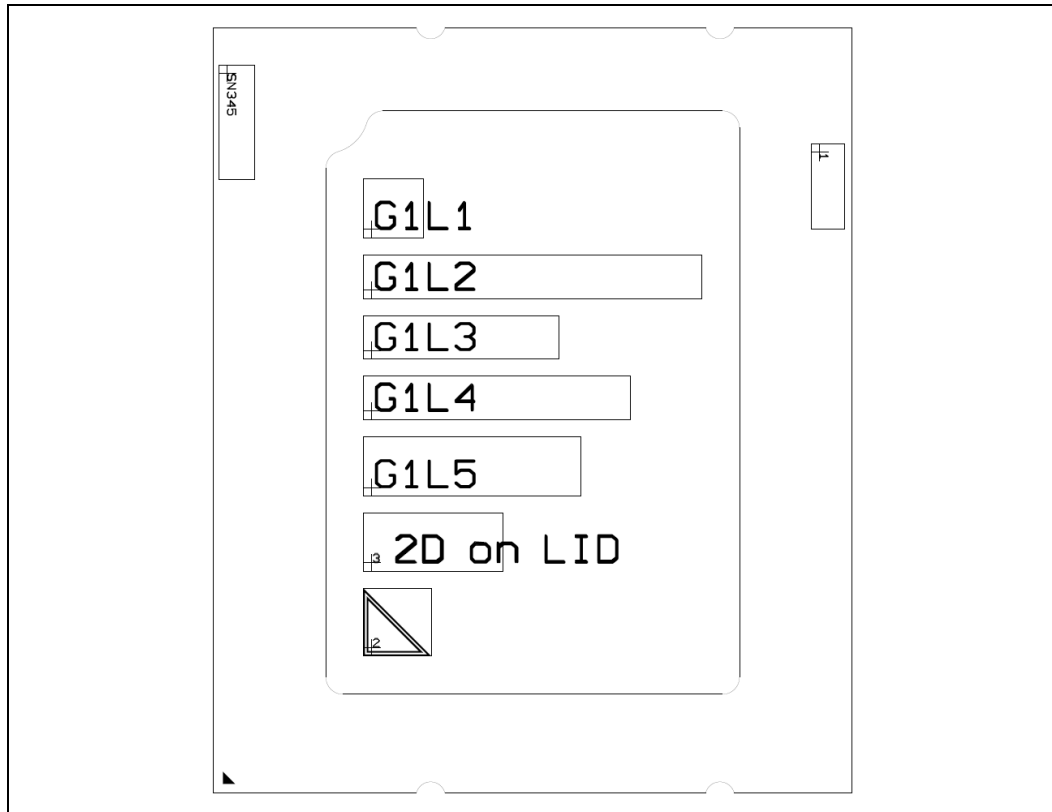
Pin Count: 1700   Package Size (width x height):   37.5mm x 45mm

Production (SSPEC):

- SN345
- G1L1: SPARK (Intel logo)
- G2L1: TRADEMARK BRAND
- G3L1: PROCESSOR NUMBER
- G4L1: SSPEC
- G5L1: FPO_{EX}

Note: "1" is used to extract the unit visual ID (2D ID).

"2" is Pin 1 indicator on IHS.

Figure 2-2. Processor Based on H/H-Refresh/P Processor Line Chip Package LGA Top-Side Markings

Pin Count: 1744   Package Size (width x height): 50mm x 25mm

Production (SSPEC):

- SN345
- G1L1: SPARK (Intel logo)
- G1L2: FPO
- G1L3: SSPEC
- G2L1: {ex}

Note: "1" is used to extract the unit visual ID (2D ID).

Figure 2-3. Processor Based on HX/HX-Refresh Processor Line Chip Package LGA Top-Side Markings
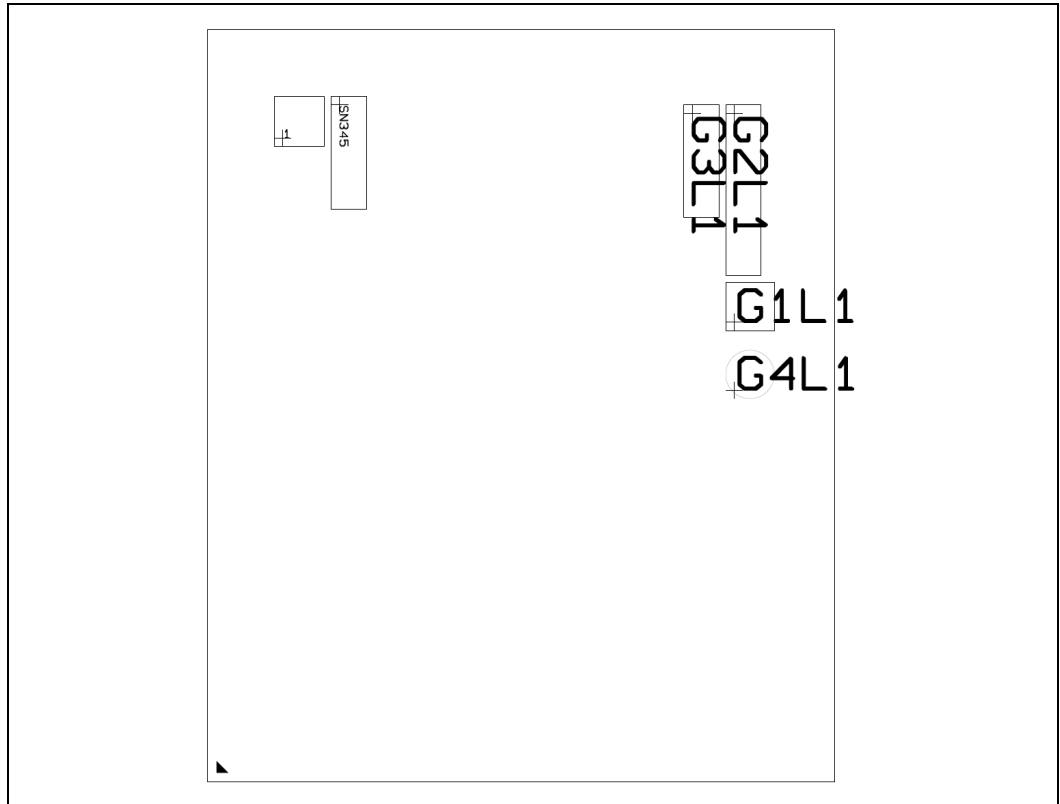
Pin Count: 1964   Package Size "(width x height)": 37.5mm x 45mm

Production (SSPEC):

- SN345
- G1L1: SPARK (Intel logo)
- G2L1: FPO
- G3L1: SSPEC
- G4L1: {eX}

Note: "1" is used to extract the unit visual ID (2D ID).

Figure 2-4. Processor Based on U/U-Refresh Processor Line Chip Package LGA Top-Side Markings

Pin Count: 1744   Package Size (width x height): 50mm x 25mm

Production (SSPEC):

- SN345
- G1L1: SPARK (Intel logo)
- G2L1: FPO
- G3L1: SSPEC
- G4L1: {eX}

Note: "1" is used to extract the unit visual ID (2D ID).

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3   *Summary Tables of Changes*

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes, which apply to the listed processor stepping. Intel® intends to fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

3.1   Codes Used in Summary Table

Stepping	Description
(No mark) or (Blank Box)	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Status	Description
Planned Fix	This erratum may be fixed in a future stepping of the product.
Fixed	This erratum has been previously fixed in Intel® hardware, firmware, or software.
No Fix	There are no plans to fix this erratum.

3.2   Errata Summary Table

Errata ID	Processor Line								Title
	S/S Refresh			E/E Refresh	P/H/H Refresh	HX/HX Refresh		U/U Refresh	
	8+16	8+8	6+0	8+0	6+8	8+16	8+8	2+8	
RPL001	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Intel® Processor Trace PSB+ Packets May Contain Unexpected Packets
RPL002	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	x87 FDP Value May be Saved Incorrectly
RPL003	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Debug Exceptions May Be Lost or Misreported When MOV SS or POP SS Instruction is Not Followed By a Write to SP
RPL004	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Intel® PT Trace May Drop Second Byte of CYC Packet
RPL005	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	BMI1, BMI2, LZCNT, ADXC, and ADOX Instructions May Not Generate an #UD

Errata ID	Processor Line								Title
	S/S Refresh			E/E Refresh	P/H/H Refresh	HX/HX Refresh		U/U Refresh	
	8+16	8+8	6+0	8+0	6+8	8+16	8+8	2+8	
RPL006	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Exit Qualification For EPT Violations on Instruction Fetches May Incorrectly Indicate That The Guest-physical Address Was Writeable
RPL007	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Processor May Generate Spurious Page Faults On Shadow Stack Pages
RPL008	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Processor May Hang if Warm Reset Triggers During BIOS Initialization
RPL009	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	System May Hang When Bus-Lock Detection Is Enabled And EPT Resides in Uncacheable Memory
RPL010	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Processor May Generate Malformed TLP
RPL011	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No #GP May be Signaled When Setting MSR_MISC_PWR_MGMT.ENABLE_SDC if MSR_MISC_PWR_MGMT.LOCK is Set
RPL012	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	PCIe Link May Fail to Train Upon Exit From L1.2
RPL013	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Incorrectly Formed PCIe Packets May Generate Correctable Errors
RPL014	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Single Step on Branches Might be Missed When VMM Enables Notification On VM Exit
RPL015	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Incorrect #CP Error Code on UIRET
RPL016	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	CPUID Reports Incorrect Number of Ways For The Load DTLB
RPL017	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Intel® PT Trace May Contain Incorrect Data When Configured With Single Range Output Larger Than 4KB
RPL018	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	IA32_PERF_CAPABILITIES.PERF_METRICS_AVAILABLE is Not Set
RPL019	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	OFFCORE_REQUESTS_OUTSTANDING Performance Monitoring Events May be Inaccurate
RPL020	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	On Instructions Longer Than 15 Bytes, #GP Exception is Prioritized And Delivered Over #CP Exception
RPL021	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Mismatch on DR6 Value When Breakpoint Match is on Bitmap Address
RPL022	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	RTM Abort Status May be Incorrect For INT1/INT3 Instructions

Errata ID	Processor Line								Title
	S/S Refresh			E/E Refresh	P/H/H Refresh	HX/HX Refresh		U/U Refresh	
	8+16	8+8	6+0	8+0	6+8	8+16	8+8	2+8	
RPL023	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Incorrect MCACOD For L2 Prefetch MCE
RPL024	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Call Instruction Wrapping Around The 32-bit Address Boundary May Return to Incorrect Address
RPL025	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	VM Entry That Clears TraceEn May Generate a FUP
RPL026	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	#UD May be Delivered Instead of Other Exceptions
RPL027	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	#GP May be Serviced Before an Instruction Breakpoint
RPL028	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Unexpected #PF Exception Might Be Serviced Before a #GP Exception
RPL029	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	WRMSR to Reserved Bits of IA32_L3_QOS_Mask_15 May Not Signal a #GP
RPL030	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	VMX-Preemption Timer May Not Work if Configured With a Value of 1
RPL031	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Setting MISC_FEATURE_CONTROL.DISABLE_THREE_STRIKE_CNT Does Not Prevent The Three-strike Counter From Incrementing
RPL032	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	VM Exit Qualification May Not be Correctly Set on APIC Access While Serving a User Interrupt
RPL033	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Unable to Transmit Modified Compliance Test Pattern at 2.5 GT/S or 5.0 GT/s Link Speeds
RPL034	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	USB 3.2 Gen 1x1 Port Does Not Send 16 Polling LFPS Burst
RPL035	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Unsynchronized Cross-Modifying Code Operations Can Cause Unexpected Instruction Execution Results
RPL036	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Type-C Host Controller Does Not Support Certain Qword Accesses
RPL037	N/A	N/A	N/A	N/A	No Fix	No Fix	No Fix	No Fix	GPU Hang When Async Compute is Enabled
RPL038	N/A	Fixed	Fixed	N/A	N/A	N/A	N/A	N/A	Processor Exiting Package C6 or C8 May Hang
RPL039	Fixed	Fixed	Fixed	Fixed	Fixed	Fixed	Fixed	Fixed	Unexpected System Hang During Enhanced Intel SpeedStep Transitions

Errata ID	Processor Line								Title
	S/S Refresh			E/E Refresh	P/H/H Refresh	HX/HX Refresh		U/U Refresh	
	8+16	8+8	6+0	8+0	6+8	8+16	8+8	2+8	
RPL040	Fixed	Fixed	Fixed	Fixed	Fixed	Fixed	Fixed	Fixed	The Time-Stamp Counter May Report an Incorrect Value
RPL041	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Processor May Encrypt TME Exclude Range if Mapped to Remap Range
RPL042	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Precision Time Measurement (PTM) Interpretation Capability Bit Incorrect Register Offset
RPL043	Fixed	Fixed	N/A	Fixed	Fixed	Fixed	Fixed	Fixed	INVLPG May Invalidate Global TLB Entries Only For The Current PCID
RPL044	Fixed	Fixed	Fixed	Fixed	Fixed	Fixed	Fixed	Fixed	Machine Check Exception May be Observed During Package C6 Entry
RPL045	N/A	Fixed	Fixed	N/A	N/A	N/A	Fixed	N/A	Branch Predictor May Produce Incorrect Instruction Pointer
RPL046	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	IA32_MC2_ADDR And IA32_MC2_MISC MSRs May be Cleared on Warm Reset
RPL047	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	xHCI Force Header Command Incorrect Return Code
RPL048	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	DDR5 Clock Jitter Out of Spec
RPL049	Fixed	N/A	N/A	Fixed	N/A	Fixed	N/A	N/A	IA32_SPEC_CTL Bits IPRED_DIS_U, IPRED_DIS_S And BHI_DIS_S May Not Function Correctly
RPL050	Fixed	Fixed	N/A	Fixed	Fixed	Fixed	Fixed	Fixed	CPU May Not Load The Most Recent Data
RPL051	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Performance Monitoring Event IDQ.MS_UOPS May Undercount
RPL052	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Performance Monitoring Events TOPDOWN.BACKEND_BOUND_SLOTS and IDQ_BUBBLES May be Inaccurate
RPL053	N/A	N/A	N/A	N/A	No Fix	N/A	N/A	No Fix	Type-C Display May be Blank Following S3/S4/S5 Resume
RPL054	No Fix	No Fix	No Fix	N/A	No Fix	No Fix	No Fix	No Fix	Performance Monitoring Event Branch Instruction Retired Will Not Count CALLs to Next Sequential Instruction
RPL055	No Fix	No Fix	No Fix	N/A	No Fix	No Fix	No Fix	No Fix	Performance Monitoring Event Branch Instruction Retired Will Overcount on Certain Types of Branch and Complex Instructions
RPL056	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Unexpected System Behavior When Re-Enabling Intel® HT

Errata ID	Processor Line								Title
	S/S Refresh			E/E Refresh	P/H/H Refresh	HX/HX Refresh		U/U Refresh	
	8+16	8+8	6+0	8+0	6+8	8+16	8+8	2+8	
RPL057	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Processor Trace May Generate PSB Packets Too Infrequently
RPL058	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Processor Trace May Not Generate a CYC Packet Before MODE.EXEC Packets
RPL059	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	Disabling The APIC While an Interrupt is Being Delivered May Cause a System Hang
RPL060	Fixed	Fixed	Fixed	N/A	N/A	Fixed	Fixed	Fixed	Split Load May Return Incorrect Data
RPL061	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	PCONFIG Error Reporting May be Incorrect
RPL062	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	No Fix	xHCI Out of Order ACK Due to LCRD1
RPL063	No Fix	N/A	N/A	N/A	N/A	No Fix	N/A	N/A	Incorrect Internal Voltage Request May Lead to Unpredictable System Behavior
RPL064	No Fix	No Fix	No Fix	No Fix	N/A	N/A	N/A	N/A	PCIe REFCLK Inactive Prior to PERST#
RPL065	No Fix	No Fix	No Fix	N/A	No Fix	No Fix	No Fix	No Fix	Display Artifacts With YUV420 Format
RPL066	Fixed	Fixed	Fixed	Fixed	Fixed	Fixed	Fixed	Fixed	VM Exit Following MOV to CR8 Instruction May Lead to Unexpected IDT Vectoring-Information
RPL067	No Fix	No Fix	N/A	N/A	No Fix	No Fix	No Fix	No Fix	Cache Level Wrongly Reported in Machine Check Banks

3.3 Specification Changes

No.	Specification Changes
	None for this revision of this specification update.

3.4 Specification Clarifications

No.	Specification Clarifications
	None for this revision of this specification update.

3.5 Documentation Changes

No.	Documentation Changes
	None for this revision of this specification update.

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4   *Errata Details*

RPL001	Intel® Processor Trace PSB+ Packets May Contain Unexpected Packets
Problem	Some Intel® Processor Trace packets should be issued only between TIP.PGE (Target IP Packet.Packet Generation Enable) and TIP.PGD (Target IP Packet.Packet Generation Disable) packets. Due to this erratum, when a TIP.PGE packet is generated it may be preceded by a PSB+ (Packet Stream Boundary) that incorrectly includes FUP (Flow Update Packet) and MODE.Exec packets.
Implication	Due to this erratum, FUP and MODE.Exec may be generated unexpectedly.
Workaround	Decoders should ignore FUP and MODE.Exec packets that are not between TIP.PGE and TIP.PGD packets.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL002	x87 FDP Value May be Saved Incorrectly
Problem	Execution of the FSAVE, FNSAVE, FSTENV, or FNSTENV instructions in real-address mode or virtual-8086 mode may save an incorrect value for the x87 FDP (FPU data pointer). This erratum does not apply if the last non-control x87 instruction had an unmasked exception.
Implication	Software operating in real-address mode or virtual-8086 mode that depends on the FDP value for non-control x87 instructions without unmasked exceptions may not operate properly. Intel® has not observed this erratum in any commercially available software.
Workaround	None identified. Software should use the FDP value saved by the listed instructions only when the most recent non-control x87 instruction incurred an unmasked exception.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL003	Debug Exceptions May Be Lost or Misreported When MOV SS or POP SS Instruction is Not Followed By a Write to SP
Problem	If a MOV SS or POP SS instruction generated a debug exception, and is not followed by an explicit write to the stack pointer (SP), the processor may fail to deliver the debug exception or, if it does, the DR6 register contents may not correctly reflect the causes of the debug exception.
Implication	Debugging software may fail to operate properly if a debug exception is lost or does not report complete information. Intel® has not observed this erratum with any commercially available software.
Workaround	Software should explicitly write to the stack pointer immediately after executing MOV SS or POP SS.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL004	Intel® PT Trace May Drop Second Byte of CYC Packet
Problem	Due to a rare microarchitectural condition, the second byte of a 2-byte CYC (Cycle Count) packet may be dropped without an OVF (Overflow) packet.
Implication	A trace decoder may signal a decode error due to the lost trace byte.
Workaround	None identified. A mitigation is available for this erratum. If a decoder encounters a multi-byte CYC packet where the second byte has bit 0 (Ext) set to 1, it should assume that 4095 cycles have passed since the prior CYC packet, and it should ignore the first byte of the CYC and treat the second byte as the start of a new packet.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL005	BMI1, BMI2, LZCNT, ADXC, and ADOX Instructions May Not Generate an #UD
Problem	BMI1, BMI2, LZCNT, ADXC, and ADOX instructions may not generate an #UD fault, even though the respective CPUID feature flags do not enumerate them as supported instructions.
Implication	Software that relies on BMI1, BMI2, LZCNT, ADXC, and ADOX instructions to generate an #UD fault, may not work correctly.
Workaround	None identified. Software should check CPUID reported instructions availability and not rely on the #UD fault behavior.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL006	Exit Qualification For EPT Violations on Instruction Fetches May Incorrectly Indicate That The Guest-physical Address Was Writeable
Problem	On EPT violations, bit 4 of the Exit Qualification indicates whether the guest-physical address was writeable. When EPT is configured as supervisory shadow-stack (both bit 60 in EPT paging-structure leaf entry and bit 0 in EPT paging-structure entries are set), non-executable (bit 2 in EPT paging-structure entries is cleared), and non-writeable (bit 1 in EPT paging-structure entries is cleared) a VMExit due to a guest instruction fetch to a supervisory page may incorrectly set bit 4 of the Exit Qualification. Bits 3, 5, and 6 of the Exit Qualification are not impacted by this erratum.
Implication	Due to this erratum, bit 4 of the Exit Qualification may be incorrectly set. Intel® has not observed this erratum on any commercially available software.
Workaround	EPT handlers processing an EPT violation due to an instruction fetch access on a present page should ignore the value of bit 4 of the Exit Qualification.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL007	Processor May Generate Spurious Page Faults On Shadow Stack Pages
Problem	When operating in a virtualized environment, if shadow stack pages are mapped over an APIC page, the processor may generate spurious page faults on that shadow stack page whenever its linear to physical address translation is cached in the Translation Look-aside Buffer.

RPL007	**Processor May Generate Spurious Page Faults On Shadow Stack Pages**
Implication	When this erratum occurs, the processor may generate a spurious page fault. Intel® is not aware of any software that maps shadow stack pages over an APIC page.
Workaround	Software should avoid mapping shadow stack pages over the APIC page.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL008	**Processor May Hang if Warm Reset Triggers During BIOS Initialization**
Problem	Under complex micro-architectural conditions, when the processor receives a warm reset during BIOS initialization, the processor may hang with a machine check error reported in IA32_MCi_STATUS, with MCACOD (bits [15:0]) value of 0400H, and MSCOD (bits [31:16]) value of 0080H.
Implication	Due to this erratum, the processor may hang. Intel® has only observed this erratum in a synthetic test environment.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL009	**System May Hang When Bus-Lock Detection Is Enabled And EPT Resides in Uncacheable Memory**
Problem	On processors that support bus-lock detection (CPUID.(EAX=7, ECX=0).ECX[24]) and have it enabled (bit 2 in the IA32_DEBUGCTL MSR (1D9h)), and employ an Extended Page Table (EPT) that is mapped to an uncacheable area (UC), and the EPT_AD is enabled (bit 6 of the EPT Pointer is set), if the VMM performs an EPT modification on a predefined valid page while a virtual machine is running, the processor may hang.
Implication	Due to this erratum, the system may hang when bus-lock detection is enabled. Intel® has not observed this erratum in any commercially available software.
Workaround	VMM should not map EPT tables to Uncacheable memory while using EPT_AD.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL010	**Processor May Generate Malformed TLP**
Problem	If the processor root port receives an FetchAdd, Swap, or CAS TLP (an atomic operation) that is erroneous, it should generate a UR completion to the downstream requestor. If the TLP has an operand size greater than 4 bytes, the generated UR completion may report an operand size of 4 bytes, which may be interpreted as a malformed transaction.
Implication	When this erratum occurs, the processor may respond with a malformed transaction.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL011	No #GP May be Signaled When Setting MSR_MISC_PWR_MGMT.ENABLE_SDC if MSR_MISC_PWR_MGMT.LOCK is Set
Problem	If the MSR_MISC_PWR_MGMT.LOCK (MSR 1AAh, bit13) is set, a General Protection Exception (#GP) may not be signaled when MSR_MISC_PWR_MGMT.ENABLE_SDC (MSR 1AAh, bit 10) is cleared while IA32_XSS.HDC (MSR DA0h, bit 13) is set and if IA32_PKG_HDC_CTL.HDC_PKG_Enable (MSR DB0h, bit 0) was set at least once before.
Implication	Due to this erratum, MSR_MISC_PWR_MGMT.ENABLE_SDC may be cleared even though a #GP was not signaled.
Workaround	None identified. Software should not attempt to clear MSR_MISC_PWR_MGMT.ENABLE_SDC if the above #GP conditions are met.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL012	PCIe Link May Fail to Train Upon Exit From L1.2
Problem	When the PCIe Link exits the L1.2 low-power link state, the link may fail to correctly train to L0.
Implication	Due to this erratum, a PCIe link may incur unexpected link recovery events or it may enter a Link_Down state.
Workaround	It may be possible for a BIOS code change to workaround this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL013	Incorrectly Formed PCIe Packets May Generate Correctable Errors
Problem	Under complex microarchitectural conditions, the PCIe controller may transmit an incorrectly formed Transaction Layer Packet (TLP), which may fail CRC checks.
Implication	When this erratum occurs, the PCIe end point may record correctable errors resulting in either a NAK or link recovery. Intel® has not observed any functional impact due to this erratum.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL014	Single Step on Branches Might be Missed When VMM Enables Notification On VM Exit
Problem	Under complex micro-architectural conditions, single step on branches (IA32_DEBUGCTLMSR (Offset 1D9h, bit [1]) and also TF flag in EFLAGS register is set) in guest might be missed when VMM enables notification on VM Exit (IA32_VMX_PROCBASED_CTLS2 MSR, Offset 48Bh, bit [31]) while the dirty access bit is not set for the code page (bit [6] in paging-structure entry).
Implication	When single step is enabled under the above condition, some single step branches may be missed. Intel® has only observed this erratum in a synthetic test environment.
Workaround	When enabling single step on branches for debugging, software should first set the dirty bit of the code page.

RPL014	**Single Step on Branches Might be Missed When VMM Enables Notification On VM Exit**
Status	For the steppings affected, refer to the <u>Summary Table of Changes</u>.

RPL015	**Incorrect #CP Error Code on UIRET**
Problem	If a #CP exception is triggered during a UIRET instruction execution, the error code on the stack may report NEAR-RET instruction (code 1) instead of FAR-RET instruction (code 2).
Implication	Due to this erratum, an incorrect #CP error code is logged when #CP is triggered during UIRET instruction.
Workaround	None identified.
Status	For the steppings affected, refer to the <u>Summary Table of Changes</u>.

RPL016	**CPUID Reports Incorrect Number of Ways For The Load DTLB**
Problem	CPUID leaf 18H sub-leaf 04H EBX [31:16] reports 4 ways instead of 6 ways for the Load DTLB.
Implication	Due to this erratum, software that relies upon the number of ways in the load DTLB may operate sub optimally.
Workaround	None identified.
Status	For the steppings affected, refer to the <u>Summary Table of Changes</u>.

RPL017	**Intel® PT Trace May Contain Incorrect Data When Configured With Single Range Output Larger Than 4KB**
Problem	Under complex micro-architectural conditions, when using Intel(r) Processor Trace (PT) with single range output larger than 4KB, disabling PT and then enabling PT using the TraceEn bit in IA32_RTIT_CTL MSR (MSR 570h, bit 0) may cause incorrect output values to be recorded.
Implication	Due to this erratum, a PT trace may contain incorrect values.
Workaround	None identified. Software should avoid using PT with single range output larger than 4KB.
Status	For the steppings affected, refer to the <u>Summary Table of Changes</u>.

RPL018	**IA32_PERF_CAPABILITIES.PERF_METRICS_AVAILABLE is Not Set**
Problem	PERF_METRICS_AVAILABLE indication inside IA32_PERF_CAPABILITIES MSR (bit 15 in MSR 345h) reports whether MSR_PERF_METRICS is available. This indication may not be set unless BIOS disables E-cores in the system.
Implication	When this erratum occurs, the PERF_METRICS are available even though IA32_PERF_CAPABILITIES.PERF_METRICS_AVAILABLE reports otherwise.
Workaround	None identified.

RPL018	**IA32_PERF_CAPABILITIES.PERF_METRICS_AVAILABLE is Not Set**
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL019	**OFFCORE_REQUESTS_OUTSTANDING Performance Monitoring Events May be Inaccurate**
Problem	The OFFCORE_REQUESTS_OUTSTANDING.*DATA_RD performance monitoring events (Event 20h; UMask 08h) counts the number of off-core outstanding data read transactions each cycle. Due to this erratum, an inaccurate count may be observed when Intel® HyperThreading Technology is enabled and hardware prefetchers are enabled.
Implication	OFFCORE_REQUESTS_OUTSTANDING Performance Monitoring Events may be Inaccurate.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL020	**On Instructions Longer Than 15 Bytes, #GP Exception is Prioritized And Delivered Over #CP Exception**
Problem	A #GP (global protection exception) that results from an instruction being longer than 15 bytes is prioritized and served before a #CP (Controlflow Protection exception) that was created due to a missing ENDBRx instruction at the target of an indirect branch.
Implication	Due to this erratum, during an indirect jump with ENDBRANCH tracking, if the processor lands on an illegal instruction with length longer than 15 bytes or that decodes to a CS limit, the processor may prioritize and deliver a #GP exception over the #CP exception.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL021	**Mismatch on DR6 Value When Breakpoint Match is on Bitmap Address**
Problem	Under complex microarchitectural conditions, on systems with Control-flow Enforcement Technology (CET) enabled, hitting a predefined data breakpoint may not be reported in B0-B3 (bits 3:0) in the DR6 register if that breakpoint was set on the legacy code page bitmap.
Implication	Due to this erratum, software may not know which breakpoint triggered when setting breakpoints on the legacy code page bitmap.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL022	**RTM Abort Status May be Incorrect For INT1/INT3 Instructions**
Problem	When Intel® Transactional Synchronization Extensions (TSX) is enabled, and there is an RTM (Restricted Transactional Memory))abort due to an INT1 or INT3 instruction, bit 5 of the RTM abort status (nested transaction execution) may not be set even if the RTM was nested.
Implication	Due to this erratum, software that manages RTM aborts cannot determine whether an abort is nested.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL023	**Incorrect MCACOD For L2 Prefetch MCE**
Problem	Under complex micro-architectural conditions, an L2 prefetch MCE that should be reported with MCACOD 165h in IA32_MC3_STATUS MSR (MSR 40dh, bits [15:0]) may be reported with an MCACOD of 101h.
Implication	Due to this erratum, the reported MCACOD for this MCE may be incorrect.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL024	**Call Instruction Wrapping Around The 32-bit Address Boundary May Return to Incorrect Address**
Problem	In 32-bit mode, a call instruction wrapping around the 32-bit address should save a return address near the bottom of the address space (low address) around address zero. Under complex micro-architectural conditions, a return instruction following such a call may return to the next sequential address instead (high address).
Implication	Due to this erratum, In 32-bit mode a return following a call instruction that wraps around the 32-bit address boundary may return to the next sequential IP without wrapping around the address, possibly resulting in a #PF. Intel® has not observed this behavior on any commercially available software.
Workaround	Software should not place call instructions in addresses that wrap around the 32-bit address space in 32-bit mode.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL025	**VM Entry That Clears TraceEn May Generate a FUP**
Problem	If VM entry clears Intel® PT (Intel® Processor Trace) IA32_RTIT_CTL.TraceEn (MSR 570H, bit 0) while PacketEn is 1 then a FUP (Flow Update Packet) may precede the TIP.PGD (Target IP Packet, Packet Generation Disable). VM entry can clear TraceEn if the VM-entry MSR-load area includes an entry for the IA32_RTIT_CTL MSR.
Implication	When this erratum occurs, an unexpected FUP may be generated that creates the appearance of an asynchronous event taking place immediately before or during the VM entry.
Workaround	The Intel® PT trace decoder may opt to ignore any FUP whose IP matches that of a VM entry instruction.

RPL025	VM Entry That Clears TraceEn May Generate a FUP
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL026	#UD May be Delivered Instead of Other Exceptions
Problem	An invalid instruction opcode that runs into another exception before fetching all instruction bytes (e.g. a #GP due to the instruction being longer than 15 bytes or a CS limit violation) may signal a #UD despite not fetching all instruction bytes under some microarchitectural conditions.
Implication	Due to this erratum, a #UD exception may be serviced before other exceptions. This does not occur for valid instructions. Intel® has only observed this erratum in a synthetic test environment.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL027	#GP May be Serviced Before an Instruction Breakpoint
Problem	An instruction breakpoint should have the highest priority and needs to be serviced before any other exception. In case an instruction breakpoint is marked on an illegal instruction longer than 15 bytes that starts in bytes 0-16 of a 32B-aligned chunk, and that instruction does not complete within the same 32B-aligned chunk, a General Protection Exception (#GP) on the same instruction may be serviced before the breakpoint exception.
Implication	Due to this erratum, an illegal instruction #GP exception may be serviced before an instruction breakpoint.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL028	Unexpected #PF Exception Might Be Serviced Before a #GP Exception
Problem	Instructions longer than 15 bytes should assert a General Protection Exception (#GP). For instructions longer than 15 bytes, a Page Fault Exception (#PF) from the subsequent page might be issued before the #GP exception in the following cases: 1. The GP instruction starts at byte 1 – 16 of the last 32B-aligned chunk of a page (starting the count at byte 0), and it is not a target of taken jump, and it does not complete within the same 32B-aligned chunk it started in. 2. The GP instruction starts at byte 17 of the last 32B-aligned chunk of a page.
Implication	Due to this erratum, an unexpected #PF exception might be serviced before a #GP exception.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL029	WRMSR to Reserved Bits of IA32_L3_QOS_Mask_15 May Not Signal a #GP
Problem	A General Protection Exception (#GP) may not be signaled when writing non-zero values to the upper 32 bits of IA32_L3_QOS_Mask_15 MSR (Offset C9FH) even though they are defined as reserved bits.
Implication	Due to this erratum, a #GP may not be signaled when the upper bits of IA32_L3_QOS_Mask_15 are written with a non-zero value.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL030	VMX-Preemption Timer May Not Work if Configured With a Value of 1
Problem	Under complex micro-architectural conditions, the VMX-preemption timer may not generate a VM Exit if the VMX-preemption timer value is set to 1.
Implication	Due to this erratum, if the value configured to a value of 1, a VM exit may not occur.
Workaround	None identified. Software should avoid programming the VMX-preemption timer with a value of 1.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL031	Setting MISC_FEATURE_CONTROL.DISABLE_THREE_STRIKE_CNT Does Not Prevent The Three-strike Counter From Incrementing
Problem	Setting MISC_FEATURE_CONTROL.DISABLE_THREE_STRIKE_CNT (bit 11 in MSR 1A4h) does not prevent the three-strike counter from incrementing as documented; instead, it only prevents the signaling of the three-strike event once the counter has expired.
Implication	Due to this erratum, software may be able to see the three-strike logged in the MC3_STATUS (MSR 40Dh, MCACOD = 400h [bits 15:0]) even when MISC_FEATURE_CONTROL.DISABLE_THREE_STRIKE_CNT is set.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL032	VM Exit Qualification May Not be Correctly Set on APIC Access While Serving a User Interrupt
Problem	A VM Exit that occurs while the processor is serving a user interrupt in non-root mode should set the "asynchronous to instruction execution" bit in the Exit Qualification field in the Virtual Machine Control Structure (bit 16). However, if a VM Exit occurs during processing a user interrupt due to an APIC access, the bit may not be set.
Implication	Due to this erratum, the "asynchronous to instruction execution" bit may not be set if an APIC Access VM Exit occurs while the processor is serving a user interrupt. Intel® has not observed this erratum with any commercially available software.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL033	**Unable to Transmit Modified Compliance Test Pattern at 2.5 GT/S or 5.0 GT/s Link Speeds**
Problem	The processor's PCIe port (Bus 0, Device 1, Function 0/1/2 or Bus 0, Device 6, Function 0) does not transmit the Modified Compliance Test Pattern when in either 2.5 GT/S or 5.0 GT/s link speeds.
Implication	Due to this erratum, PCIe compliance testing may fail at 2.5 GT/S or 5.0 GT/s link speeds when enabling the Modified Compliance Test Pattern.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL034	**USB 3.2 Gen 1x1 Port Does Not Send 16 Polling LFPS Burst**
Problem	On USB 3.2 Gen 1x1 only capable ports, including ports configured as USB 3.2 Gen 1x1 by soft strap, the xHCI controller may send only 15 LFPS signals instead of a burst of 16 LFPS signals as specified by the USB 3.2 specification.
Implication	There are no known functional implications due to this erratum. LFPS handshake requires the receiver link partner to only detect 2 LFPS signals. This issue may impact the SuperSpeed compliance test case which checks for the 16 LFPS burst requirements: TD6.4, TD6.5, and TD7.31.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL035	**Unsynchronized Cross-Modifying Code Operations Can Cause Unexpected Instruction Execution Results**
Problem	The act of one processor or system bus master writing data into a currently executing code segment of a second processor with the intent of having the second processor execute that data as code is called cross-modifying code (XMC). XMC that does not force the second processor to execute a synchronizing instruction prior to execution of the new code is called unsynchronized XMC. Software using unsynchronized XMC to modify the instruction byte stream of a processor can see unexpected or unpredictable execution behavior from the processor that is executing the modified code.
Implication	In this case the phrase "unexpected or unpredictable execution behavior" encompasses the generation of most of the exceptions listed in the Intel® Architecture Software Developer's Manual Volume 3: System Programming Guide including a General Protection Fault (GPF) or other unexpected behaviors. In the event that unpredictable execution causes a GPF the application executing the unsynchronized XMC operation would be terminated by the operating system.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL036	**Type-C Host Controller Does Not Support Certain Qword Accesses**
Problem	The Type-C controller does not properly support Qword accesses to its MSI-X interrupt table which may lead to unexpected behavior.

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RPL036	Type-C Host Controller Does Not Support Certain Qword Accesses
Implication	When this erratum occurs, Qword reads do not return Unsupported Request and may not return correct data and Qword writes may lead to unexpected behavior. Intel® has not observed this erratum to affect any commercially available software.
Workaround	Software should not utilize Qword access for the Type-C MSI-X table.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL037	GPU Hang When Async Compute is Enabled
Problem	GPU may hang when Async Compute is enabled
Implication	Due to this erratum, the GPU may hang when running high bandwidth GFx application such as benchmarks and/or games.
Workaround	None identified. The Async Compute feature may be disabled in a graphics driver update. See GFx Driver Revenue SV2 PR5 (101.3616 or later) and release notes.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL038	Processor Exiting Package C6 or C8 May Hang
Problem	When the processor exits a package C6 or C8 power state, it may encounter a machine check exception (MCACOD=PCU internal Errors(0402h) / MSCOD=MESSAGE_CHANNEL_TIMEOUT (0409h) / PKGC_EXIT_SA_FIVR_UNLOBOTOMY_TIMEOUT (0441h) / PKGC_WATCHDOG_HANG_C2P2_RSP (0462h)).
Implication	Due to this erratum the system may hang with machine check exception.
Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL039	Unexpected System Hang During Enhanced Intel® SpeedStep Transitions
Problem	Under complex microarchitectural conditions Enhanced Intel® SpeedStep transitions may lead to a system hang.
Implication	Due to this issue a system may hang with MCACODE GCACHEL2_ERR_ERR (010Ah).
Workaround	It is possible for a BIOS code change to workaround this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL040	The Time-Stamp Counter May Report an Incorrect Value
Problem	Under complex micro-architectural conditions, the Time-Stamp Counter (TSC) may incorrectly report the time stamp to be less than the expected time stamp after exiting C6 power saving state.
Implication	Due to this erratum, systems that rely upon a monotonically increasing value reported by the TSC may exhibit unpredictable system behavior.

RPL040	The Time-Stamp Counter May Report an Incorrect Value
Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL041	Processor May Encrypt TME Exclude Range if Mapped to Remap Range
Problem	The processor accesses to TME exclude range may be encrypted but not decrypted if mapped to remap range.
Implication	Due to this erratum, the processor exclude range it may be encrypted but may but not decrypted if mapped to remap range.
Workaround	It may be possible for BIOS to workaround this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL042	Precision Time Measurement (PTM) Interpretation Capability Bit Incorrect Register Offset
Problem	The PTM Propagation Delay Adaptation Interpretation B (PTMPDAIB) Bit is implemented at Configuration Space (CFG) Offset 158h instead of at 50h as documented in the PCI-SIG PTM Byte Ordering Adaptation Engineering Change Notice (ECN).
Implication	End Point Device (EPD) software that implements the PTM Byte Ordering Adaptation ECN may not be able to program their PTMPDAIB Bit correctly since it is located at a different register offset.
Workaround	None identified. To mitigate this issue, EPD software that implements the PTM Byte Ordering Adaptation ECN must access PTMPDAIB at CFG Offset 158h.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL043	INVLPG May Invalidate Global TLB Entries Only For The Current PCID
Problem	The INVLPG instruction should invalidate any global TLB entries for the specified linear address, regardless of PCID (Process-Context Identifier). Due to this erratum, INVLPG may fail to invalidate TLB entries for global pages with PCIDs different from the current PCID value. Note that, on affected processors, the CPU may not use global TLB entries with PCIDs different from the current PCID value. This erratum does not apply in VMX non-root operation. It applies only when PCIDs are enabled and either in VMX root operation or outside VMX operation.
Implication	When this erratum occurs, TLB entries may incorrectly remain valid, leading to unpredictable system behavior, including unexpected exceptions. This erratum does not apply to a guest operating system running in VMX non-root operation.
Workaround	It may be possible for BIOS to contain a workaround for this erratum. Alternatively, this can be worked around by software using INVPCID type 2 instead of INVLPG.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL044	Machine Check Exception May be Observed During Package C6 Entry
Problem	The processor may hang during a package C6 entry with a machine check (MCACOD = 0x0402, MCSCOD = 0x0485 or 0x046C).
Implication	Due to this erratum the system may hang.
Workaround	It is possible for BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL045	Branch Predictor May Produce Incorrect Instruction Pointer
Problem	Under complex microarchitectural conditions, the branch predictor may produce an incorrect instruction pointer leading to unpredictable system behavior.
Implication	Due to this erratum, the system may exhibit unpredictable behavior.
Workaround	It may be possible for BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL046	IA32_MC2_ADDR And IA32_MC2_MISC MSRs May be Cleared on Warm Reset
Problem	A non-zero value written to IA32_MC2_ADDR (40Ah) and IA32_MC2_MISC(40Bh) MSRs may be incorrectly cleared following a warm reset.
Implication	Due to this erratum, software that relies on the IA32_MC2_ADDR and IA32_MC2_MISC MSR values may not function correctly after a warm reset. Intel® has not observed this erratum with any commercially available software.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL047	xHCI Force Header Command Incorrect Return Code
Problem	The xHCI controller does not return the correct completion code for the Force Header Command as defined in the Section 4.6.16 of the eXtensible Host Controller Interface for Universal Serial Bus (xHCI) Requirements Specification Rev 1.2.
Implication	xHCI CV TD4.12 - Force Header Command Test may report an error. Intel® has obtained a waiver for TD 4.12. The Force Header Command is only used by the USB-IF Command Verifier (xHCI CV) tool for device testing. There are no known functional failures due to this erratum.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL048	DDR5 Clock Jitter Out of Spec
Problem	DDR5 Clock Jitter, as measured by jitter parameters Dj, Rj, and Tj (Dynamic/Random/Total jitter), may be beyond the JEDEC specification (JEDEC doc number JESD79-5B, Chapter 8.3) limits.

RPL048	DDR5 Clock Jitter Out of Spec
Implication	Due to this erratum Clock Jitter measurements may be out of spec. Intel has not observed any functional implications due to this erratum.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL049	IA32_SPEC_CTL Bits IPRED_DIS_U, IPRED_DIS_S And BHI_DIS_S May Not Function Correctly
Problem	IA32_SPEC_CTL (MSR 48h) bits IPRED_DIS_U (bit 3), IPRED_DIS_S (bit 4) and BHI_DIS_S (bit 10) may not function correctly after leaving a C6 or deeper sleep state.
Implication	Due to this erratum, software that relies upon these bit values may not behave as intended.
Workaround	It may be possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL050	CPU May Not Load The Most Recent Data
Problem	Under complex microarchitectural conditions, a read on one logical processor may not receive the most recently stored data by another logical processor.
Implication	Due to this erratum, unpredictable system behavior or a system hang may occur. Intel has only observed this behavior in a synthetic test environment. Intel has not observed this erratum with any commercially available system.
Workaround	It is possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL051	Performance Monitoring Event IDQ.MS_UOPS May Undercount
Problem	The performance monitoring events IDQ.MS_UOPS, IDQ.MS_SWITCHES, and IDQ.MS_CYCLES_ANY (Event 79h, UMask 30h) may undercount MS_UOPS that come from the Decode Stream Buffer (DSB).
Implication	Due to this erratum, performance monitoring counters may report counts lower than expected.
Workaround	None identified. Performance monitoring event UOPS_RETIRED.MS may be used instead.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL052	Performance Monitoring Events TOPDOWN.BACKEND_BOUND_SLOTS and IDQ_BUBBLES May be Inaccurate
Problem	The performance monitoring events TOPDOWN.BACKEND_BOUND_SLOTS (Event A4h, UMask 02h) and IDQ_BUBBLES.* (Event 9Ch, UMask 01h) may not count when the processor is in the C0.2 power sub-state, which is entered via the TPAUSE or UWAIT instructions. This erratum also impacts the accuracy of MSR_PERF_METRICS fields Frontend Bound, Backend Bound, and Fetch Latency (MSR 329h, Bits [23:16], [31:24] and [55:48]).
Implication	Due to this erratum, these performance monitoring events and the fields in MSR_PERF_METRICS may be inaccurate.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL053	Type-C Display May be Blank Following S3/S4/S5 Resume
Problem	When switching between Type-C Display Alt Mode and an Multi-Function Device (MFD) while the system is in S3/S4/S5, the Display may not enumerate.
Implication	When this erratum occurs the Display may be blank. A device unplug and re-plug may be necessary to recover the display.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL054	Performance Monitoring Event Branch Instruction Retired Will Not Count CALLs to Next Sequential Instruction
Problem	A CALL instruction whose target is the next sequential instruction (the same address pushed onto the stack) will not increment the performance monitoring event BR_INST_RETIRED (Event: C4H, UMask: 00H, F9H).
Implication	Due to this erratum, software monitoring Branch Instruction Retired events may undercount. Since the CALL is to the next instruction, control flow tracing with the Last Branch Retired (LBR) records should not be affected.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL055	Performance Monitoring Event Branch Instruction Retired Will Overcount on Certain Types of Branch and Complex Instructions
Problem	On certain types of branch and complex instructions the performance monitoring event BR_INST_RETIRED (Event: C4H, UMask: 00H / 7EH / BFH / C0H / DFH / EBH / FBH / F9H) will overcount by 1. Affected instructions include FAR CALL/JMP, RETF, IRET, VMENTRY/VMEXIT/VMPTRLD and complex SGX/SMX/CSTATE instructions/flows.
Implication	Due to this erratum, software monitoring Branch Instruction Retired events may overcount.
Workaround	None identified.

Status	For the steppings affected, refer to the Summary Table of Changes.

RPL056	**Unexpected System Behavior When Re-Enabling Intel® HT**
Problem	When performing a warm reset as part of enabling of Intel® Hyper-Threading, machine check banks may not be initialized correctly.
Implication	Due to this erratum, software that relies on initialized values in machine check banks may not behave as expected.
Workaround	None identified. Software or BIOS can avoid this erratum by performing cold reset when re-enabling Intel® HT.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL057	**Processor Trace May Generate PSB Packets Too Infrequently**
Problem	A Packet Stream Boundary (PSB) packet should be generated for every PSBFreq number of trace output bytes. Due to this erratum, PSB packets may be generated only after as many as four times that number of output bytes have been generated.
Implication	Due to this erratum, trace decoder software may see fewer PSB packets than expected. This may lead to the trace decoder software needing to search further to find a starting point to decode or, when used in circular mode, being unable to decode the trace due to lacking any PSB packets.
Workaround	None identified. Software can request more frequent PSB packets by programming PSBFreq (bits[27:24]) of IA32_RTIT_CTL MSR (570H) to a value 1/4 of the desired value.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL058	**Processor Trace May Not Generate a CYC Packet Before MODE.EXEC Packets**
Problem	When a Processor Trace MODE.EXEC packet is generated due to a change in RFLAGS.IF (interrupt flag) or the CS.L or CS.D bits, the processor may not generate a CYC packet before generating the MODE.EXEC packet.
Implication	Due to this erratum, trace decoder software may not be able to precisely determine when mode changes that involve changing the interrupt flag or the application's default operand size happened.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL059	**Disabling The APIC While an Interrupt is Being Delivered May Cause a System Hang**
Problem	If software disables the APIC by clearing APIC global enable flag (bit 11) in IA32_APIC_BASE (MSR 1Bh) while an interrupt is being delivered, the system may hang with a machine check exception reported in IA32_MCi_STATUS, with MCACOD (bits [15:0]) value of 0400H, and MSCOD (bits [31:16]) value of 0080H.

RPL059	**Disabling The APIC While an Interrupt is Being Delivered May Cause a System Hang**
Implication	Due to this erratum, the system may hang. Intel has not observed this erratum in any commercial available software.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL060	**Split Load May Return Incorrect Data**
Problem	Under complex microarchitectural conditions, a cache line split load may return incorrect data.
Implication	Due to this erratum, split loads may return incorrect data, which may lead to unpredictable system behavior. Intel has only observed this erratum in a synthetic test environment.
Workaround	It may be possible for BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL061	**PCONFIG Error Reporting May be Incorrect**
Problem	If invalid parameters are provided, the PCONFIG instruction should generate a #GP exception. Due to this erratum, the processor may instead set a ZF flag, with EAX reporting failure reasons.
Implication	Due to this erratum, incorrectly configured PCONFIG usage may lead to unexpected error reporting.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL062	**xHCI Out of Order ACK Due to LCRD1**
Problem	A delay in the availability of LCRD1 (Link Credit 1) from a USB 3.2 hub, with two or more downstream USB 3.2 bulk endpoint devices engaged in SuperSpeedPlus concurrent transfers, may lead to the connected xHCI controller sending the ACK and Status of a transfer packet out of order.
Implication	Due to this erratum, a USB 3.2 bulk endpoint device may not respond to subsequent transfers. It may be possible for a device driver to recover the USB 3.2 device.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL063	**Incorrect Internal Voltage Request May Lead to Unpredictable System Behavior**
Problem	The processor may request elevated voltages from the voltage regulator, resulting in an eventual increase to the minimum required operating voltage.
Implication	Due to this erratum, an increase to minimum operating voltage may lead to unpredictable system behavior.
Workaround	It may be possible for the BIOS to contain a mitigation for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL064	**PCIe REFCLK Inactive Prior to PERST#**
Problem	PCIe differential reference clocks may go inactive prior to the assertion of PERST#.
Implication	Due to this erratum, the PCI Express® Card Electromechanical Specification, Revision 5.0, Version 1.0 Power Section 2.2.2 "Management States (S0 to S3/S4 to S0)" requirement is not followed. Intel has not observed any functional implications due to this erratum.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL065	**Display Artifacts With YUV420 Format**
Problem	While in DP2.1 UHBR mode and using the YUV420 format with scaling, displays with a resolution higher than 5K @ 60Hz may show display artifacts.
Implication	Due to this erratum, display artifacts may be seen.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL066	**VM Exit Following MOV to CR8 Instruction May Lead to Unexpected IDT Vectoring-Information**
Problem	Under certain conditions, a VM exit following execution of the MOV to CR8 instruction may unexpectedly result in setting the Valid bit (bit 31) of the IDT-Vectoring Information Field in the Virtual Machine Control Structure (VMCS).
Implication	Depending on the operation of the virtual-machine monitor (VMM), this may result in unexpected VM behavior.
Workaround	It may be possible for the BIOS to contain a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

RPL067	Cache Level Wrongly Reported in Machine Check Banks
Problem	When reporting a machine check in the module level caches (IA32_MC1_STATUS, MSR 405H), a Compound Error Code of type Cache Hierarchy Error will be reported with a Level (LL) Sub-field of 0b10[L2] instead of 0b01[L1].
Implication	Due to this erratum, system software relying on this data, may wrongly categorize the cache level in which the error was reported. The severity of the error will be reported accurately.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

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5   *Specification Changes*

None.

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6 Specification Clarification

None.

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7 Document-Only Change

None.

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