Intel® 700 Series Chipset Family Platform Controller Hub (PCH)

Specification Update

Revision 005

July 2023

Document Number: 743621

Contents

Revision History

Document Number	Revision Number	Description	Revision Date
743621	001	Initial release	September 2022
	002	Added Errata: 014	January 2023
	003	Added Errata: 015 Added Workstation Intel® Chipset W790, Desktop Intel® Chipset H770 and B760, Mobile Intel® Chipset WM790 and HM770 identification.	May 2023
	004	Added Errata: 016	June 2023
	005	Added Errata: 017	July 2023

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1 Preface

This document is an update to the specifications contained in the documents listed in the following Affected Documents table. This document is a compilation of device and document errata and specification clarifications and changes. It is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into the specification update and are no longer published in other documents. This document may also contain information that has not been previously published.

1.1 Affected Documents

Document Title	Document Number
Intel® 700 Series Chipset Family Platform Controller Hub (PCH) Datasheet, Volume 1 of 2	743835
Intel® 700 Series Chipset Family Platform Controller Hub (PCH) Datasheet, Volume 2 of 2	743845

1.2 Nomenclature

Errata are design defects or errors. Errata may cause the behavior of the PCH to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present in all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

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2 Identification Information

2.1 Marking

Table 2-1. PCH Lines Component Identification

PCH Stepping	Top Marking (S-Spec)	Notes
B1	SRL02	Workstation Intel® Chipset W790
B1	SRM8V	Desktop Intel® Chipset B760
B1	SRM8T	Desktop Intel® Chipset H770
B1	SRM8P	Desktop Intel® Chipset Z790
B1	SRM8N	Mobile Intel® Chipset WM790
B1	SRM8M	Mobile Intel® Chipset HM770

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3 Summary Tables of Changes

The following tables indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes, which apply to the product. Intel may fix some of the errata in a future stepping of the component and account for the other outstanding issues through documentation or specification changes as noted. These tables use the following notations:

3.1 Codes Used in Summary Table

Status	Description
Doc	Document change or update that is implemented.
Planned Fix	This erratum may be fixed in a future stepping of the product.
Fixed	This erratum has been previously fixed in Intel® hardware, firmware, or software.
No Fix	There are no plans to fix this erratum.
N/A	This erratum is not applicable to the listed product/stepping or the Specification Change does not apply to the listed product/stepping.
X	Specification Changes applies to the listed product/stepping.

3.2 Errata Summary Table

Erratum ID	Stepping	Errata
	B1	
001	No Fix	SATA Enclosure Management LED Messaging
002	No Fix	eSPI SBLCL Register Bit Not Cleared by PLTRST#
003	No Fix	PCIe Clock and PCIe Reference Clock to Processor Maximum Rising/Falling Edge Rate and VCROSS
004	No Fix	USB Audio Offload Traffic with Full-Speed Device Behind Hub
005	No Fix	Integrated GbE Controller Reset on D3 Exit
006	No Fix	xHCI Link Protocol Field Value - USB 3.2 Gen 1x2 and 2x2
007	No Fix	xHCI Force Header Command Incorrect Return Code
008	No Fix	USB VTIO Device Capabilities Field Length
009	No Fix	SLP_A# Minimum Assertion Width Timer During G3 Exit
010	No Fix	xHCI Dropped ACK Packet after Upstream Truncated Packet with DPPABORT OS

Erratum ID	Stepping	Errata
	B1	
011	No Fix	Processor C-States with USB Full-speed or Low-speed Device Hotplug
012	No Fix	Timed GPIO Event May Have a Mismatched Time Stamp
013	No Fix	USB 3.2 Gen 1x1 Port Does Not Send 16 Polling LFPS Burst
014	No Fix	USB 2.0 Full-speed Device Enumeration With Certain Cables
015	No Fix	Precision Time Measurement (PTM) Interpretation Capability Bit Incorrect Register Offset
016	No Fix	ESPI_CS1#, ESPI_CS2#, and ESPI_CS3# Floating Following Initial eSPI Reset Deassertion
017	Fixed	USB Low-Speed or Full-Speed Device Enumeration Failures During Hot-Plug

3.3 Specification Changes

No.	Specification Changes
	No specification changes for this revision of the specification update.

3.4 Specification Clarifications

No.	Specification Clarifications
	No specification clarification for this revision of this specification update.

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4 Errata Details

001	SATA Enclosure Management LED Messaging
Problem	When sending a SATA enclosure LED message and all SATA ports are either idle or disabled, the PCH may not transmit the LED message due to an internal clock gating issue.
Implication	The LED status for SATA enclosure may be incorrect.
Workaround	None identified. Enclosure Management SW can poll the Enclosure Management (EM_CTL) - Offset 20h bit 8 register for a 0 value immediately before writing LED messages.
Status	For the steppings affected, refer to the Summary Table of Changes.

002	eSPI SBLCL Register Bit Not Cleared by PLTRST#
Problem	The IOSF-SB eSPI Link Configuration Lock (SBLCL) bit (offset 4000h, bit 27 in eSPI PCR space) is reset by RSMRST# assertion instead of PLTRST# assertion.
Implication	If the SBLCL bit is set to 1, software will not be able to access the eSPI device Capabilities and Configuration register in the reserved address range (0h - 7FFh) until RSMRST# asserts.
Workaround	If software needs to access the eSPI device reserved range 0h - 7FFh while SBLCL bit is set to 1, a RSMRST# assertion should be performed.
Status	For the steppings affected, refer to the Summary Table of Changes.

003	PCIe Clock and PCIe Reference Clock to Processor Maximum Rising/Falling Edge Rate and VCROSS
Problem	The PCIe Clock Output signals (CLKOUT_PCIE_P/N) and PCIe reference clock signals to processor (CLKOUT_CPUPCIBCLK_P/N) may not meet the maximum Rising/Falling Edge Rate and VCROSS specifications as defined in the PCI Express Card Electromechanical Specification Revision 3.0, section 2.1.3, REFCLK AC Specifications.
Implication	There are no known functional failures due to this erratum.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

004	USB Audio Offload Traffic with Full-Speed Device Behind Hub
Problem	If USB audio offload is enabled for a USB Full-Speed Isochronous audio device connected behind a USB 2.0 or later hub and there is an active concurrent bulk transfer to another device on any port of the xHCI controller or behind the hub, the controller may stall the offloaded audio traffic and a split transaction error may occur.
Implication	The USB audio offload playback may stop. Audio may be recovered if the audio stream is paused and restarted, the audio device is removed and reconnected, or the audio application is restarted.

Workaround	None identified. A mitigation for this erratum is available with Intel® Smart Sound Technology version 10.29.00.5574 or later for systems with Microsoft Windows* 11 OS Release or Intel Smart Sound Technology version 10.29.00.7767 or later for systems with Microsoft Windows 10 OS Release. This mitigation will disable audio offload functionality for USB audio devices connected behind a hub.
Status	For the steppings affected, refer to the Summary Table of Changes.

005	**Integrated GbE Controller Reset on D3 Exit**
Problem	Upon GbE controller D3 exit, the GbE host driver performs a controller reset. During this reset, software accesses to the GbE MMIO registers may not complete.
Implication	The system may hang. Note: This erratum has only been observed in a synthetic environment.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

006	**xHCI Link Protocol Field Value - USB 3.2 Gen 1x2 and 2x2**
Problem	The xHCI Host Controller reports the value of 0h for the Link Protocol (LP) bits [15:14] in register XECP_SUPP_USB3_6 (MMIO offset 8038h) and XECP_SUPP_USB3_7 (MMIO offset 803Ch), which does not meet the xHCI specification revision 1.2.
Implication	There are no known functional failures due to this erratum.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

007	**xHCI Force Header Command Incorrect Return Code**
Problem	The xHCI controller does not return the correct completion code for the Force Header Command as defined in the Section 4.6.16 of the eXtensible Host Controller Interface for Universal Serial Bus (xHCI) Requirements Specification Rev 1.2.
Implication	xHCI CV TD4.12 - Force Header Command Test may report an error. Intel has obtained a waiver for TD 4.12. The Force Header Command is only used by the USB-IF Command Verifier (xHCI CV) tool for device testing. There are no known functional failures due to this erratum.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

008	USB VTIO Device Capabilities Field Length
Problem	The xHCI spec version 1.2 defines the PCI Express Capability structure offset 04h Device Capabilities (DVSEC) field to be 8 bytes. The USB Virtualization Based Trusted IO (VTIO) Management controller implements the DVSEC field as 12 bytes.
Implication	An USB controller driver may not be able to enable the USB VTIO controller.
Workaround	None identified. To mitigate this erratum, an Independent Software Vendor could account for the field length in the USB controller driver.
Status	For the steppings affected, refer to the Summary Table of Changes.

009	SLP_A# Minimum Assertion Width Timer During G3 Exit
Problem	Setting the Disable SLP_X Stretching After SUS Well Power Up (DIS_SLP_X_STRCH_SUS_UP) bit (offset 1020h, bit 12 in PMC_MMIO space) to 1 does not disable the SLP_A# Minimum Assertion Width (SLP_A_MIN_ASST_WDTH) timer (offset 1020h, bit 17 and 16 in PMC_MMIO space).
Implication	G3 exit duration may be extended by the value programmed in the SLP_A_MIN_ASST_WDTH register.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

010	xHCI Dropped ACK Packet after Upstream Truncated Packet with DPPABORT OS
Problem	If a USB 3.2 Gen 1x1 hub sends an upstream truncated packet with DPPABORT OS (Data Packet Payload Abort Order Set) framing followed by an ACK packet for a previous OUT transfer from the xHCI controller, the ACK packet may be dropped by the xHCI controller.
Implication	A timeout may be observed for the OUT transfer packet. Per the xHCI spec, a xHCI controller driver will issue a warm port reset to the device causing a device re-enumeration.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

011	Processor C-States with USB Full-speed or Low-speed Device Hotplug
Problem	When doing a hotplug on a USB hub with two or more USB Full-speed or Low-speed devices each with a 1 ms service interval interrupt endpoint, a race condition may occur between the PMC and the xHCI controller.
Implication	The processor may fail to enter C3 or deeper package C-States. Note: This erratum has only been observed in a synthetic environment.
Workaround	None identified. This condition is recovered after the xHCI controller has successfully entered D3.
Status	For the steppings affected, refer to the Summary Table of Changes.

Errata Details

012	Timed GPIO Event May Have a Mismatched Time Stamp
Problem	When a Timed GPIO event is counted in the Event Counter Capture (TGPIOECCV) register (offset 1238h, bits 31 to 0 in PWRMBASE space), the Time Capture (TGPIOTCV) register (offset 1230h, bits 31 to 0 in PWRMBASE space) value is not immediately updated after that event is counted.
Implication	A Timed GPIO event may have a mismatched time stamp.
Workaround	None identified. A Timed GPIO driver can partially mitigate for this erratum by detecting that a TGPIOECCV register change has occurred without a TGPIOTCV register change and then repeatedly re-read the TGPIOTCV register until a change does occur.
Status	For the steppings affected, refer to the Summary Table of Changes.

013	USB 3.2 Gen 1x1 Port Does Not Send 16 Polling LFPS Burst
Problem	On USB 3.2 Gen 1x1 only capable ports, including ports configured as USB 3.2 Gen 1x1 by soft strap, the xHCI controller may send only 15 LFPS signals instead of a burst of 16 LFPS signals as specified by the USB 3.2 specification.
Implication	There are no known functional implications due to this erratum. LFPS handshake requires the receiver link partner to only detect 2 LFPS signals. This issue may impact the SuperSpeed compliance test case which checks for the 16 LFPS burst requirements: TD6.4, TD6.5, and TD7.31.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

014	USB 2.0 Full-speed Device Enumeration With Certain Cables
Problem	The xHCI controller may not complete the detection of the End of Packet Single Ended 0 (EOP SE0) when a USB Full-speed device is connected through a USB 2.0 cable that has a connector-to-connector propagation delay greater than 15.6 ns.
Implication	Due to this erratum, the USB 2.0 Full-speed device may fail to enumerate.
Workaround	None identified.
Status	For the steppings affected, refer to the Summary Table of Changes.

015	Precision Time Measurement (PTM) Interpretation Capability Bit Incorrect Register Offset
Problem	The PTM Propagation Delay Adaptation Interpretation B (PTMPDAIB) Bit is implemented at Configuration Space (CFG) Offset 158h instead of at 50h as documented in the PCI-SIG PTM Byte Ordering Adaptation Engineering Change Notice (ECN).
Implication	Due to this erratum, End Point Device (EPD) software that implements the PTM Byte Ordering Adaptation ECN will not be able to program their PTMPDAIB Bit correctly since it is located at a different register offset.
Workaround	None identified. To mitigate this issue, EPD software that implements the PTM Byte Ordering Adaptation ECN must access PTMPDAIB at CFG Offset 158h.
Status	For the steppings affected, refer to the Summary Table of Changes.

016	ESPI_CS1#, ESPI_CS2#, and ESPI_CS3# Floating Following Initial eSPI Reset Deassertion
Problem	During Deep Sx exit or booting from G3 state, ESPI_CS1#, ESPI_CS2#, and ESPI_CS3# are momentarily high impedance and may float low following the initial ESPI_RESET# deassertion.
Implication	Due to this erratum, unexpected system behavior may occur on systems with more than one eSPI device.
Workaround	Implement 10 kohm external pull-up resistors to the VCCPRIM_1P8 voltage rail on ESPI_CS1#, ESPI_CS2#, and ESPI_CS3#.
Status	For the steppings affected, refer to the Summary Table of Changes.

017	USB Low-Speed or Full-Speed Device Enumeration Failures During Hot-Plug
Problem	During the hot-plug of a USB 2.0 hub with Low-Speed or Full-Speed device connected behind the hub, a split transaction error may occur during the enumeration of the USB Low-Speed or Full-Speed device.
Implication	Due to this erratum, the USB Low-Speed or Full-Speed device may fail to enumerate when connected to the USB 2.0 hub. This condition is recovered after the xHCI controller has been reset (for example, software setting the xHCI Host Controller Reset (HCRST) bit or by performing a power button override).
Workaround	A BIOS code change has been identified and may be implemented as a workaround for this erratum.
Status	For the steppings affected, refer to the Summary Table of Changes.

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5 Specification Changes

There are no specification changes in this revision of the Specification Update.

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6 Specification Clarification

There are no specification clarifications in this revision of the Specification Update.

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