Agilex™ 5 FPGAs and SoCs E-Series Product Table

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Version 2024.01.09

Product Line		Device Group A FPGAs				
		A5E 013A	A5E 028A	A5E 043A	A5E 052A	A5E 065A
Resources	Logic elements (LEs)	138,060	282,256	434,240	523,920	656,080
	Adaptive logic modules (ALMs)	46,800	95,680	147,200	177,600	222,400
	ALM registers	187,200	382,720	588,800	710,400	889,600
	M20K memory blocks	358	716	1,050	1,288	1,611
	M20K memory size (Mb)	6.99	13.98	20.51	25.16	31.46
	MLAB memory count	2,340	4,784	6,720	8,440	11,120
	MLAB memory size (Mb)	1.43	2.92	4.10	5.15	6.79
	I/O PLL	4	4	8	8	8
	Fabric-feeding I/O PLL[1]	8	10	13	13	13
	Variable-precision digital signal processing (DSP) blocks	188	376	564	676	846
	18 x 19 multipliers	376	752	1,128	1,352	1,692
	Peak INT8 (TOPS)	5.78	11.55	17.33	20.78	25.99
Maximum Available Device Resources	LVDS pairs at 1.6 Gbps	96	96	192	192	192
	DDR4/5 and LPDDR4/5 interfaces (x32)	2	2	4	4	4
	MIPI D-PHY interface	14	14	28	28	28
	Differential (RX or TX) pairs at 28 Gbps	4	12	16	24	24
	PCIe 4.0 x4 instance	1	3	4	6	6
	High-speed I/O (HSIO)	192	192	384	384	384
	High-voltage I/O (HVIO)	200	200	120	120	120
	Secure device manager (SDM)	Provides SHA-384 bitstream integrity, ECDSA 256/384 bitstream authentication, AES-256 bitstream encryption, physically unclonable function (PUF) protected key storage, side-channel attack resistance, SPDM attestation, cryptographic services, physical anti-tamper support				
	Hard processor system	Multi-core with 32-bit/64-bit dual-core Arm Cortex*-A55 up to 1.5 GHz with 32 KB I/D cache and 128 KB L2 cache, and dual-core Arm Cortex-A76 up to 1.8 GHz with 64 KB I/D cache and 256 KB L2 cache, and up to 2 MB L3 shared cache, multi-channels direct memory access (DMA), 512 KB on-chip RAM, USB 3.1 x1, USB 2.0 OTG x2, TSN MAC x3, UART x2, SPI M x2, SPI S x2, I3C x2, I2C x5, NAND x1, SDMMC x1, Osc timer x2, SP timer x2, watchdog x5, GPIO x2.				
	Transceiver	PCI Express* (PCIe*) hard IP up to PCIe 4.0 x4 EP and RP Transceiver channel count: up to 24 channels at 28 Gbps (NRZ) Ethernet IP: up to 6 x10/25 GbE hard IP (MAC, PCS, and FEC)				

Package Options[2] and I/O Pins

Package code (Package size, minimum ball pitch, grid array pattern)	HVIO/ HSIO/Transceivers				
B23A (23 mm x 23 mm, 0.65 mm[3], Variable Pitch BGA)	120/96/4	120/96/12	120/96/12	120/96/12	120/96/12
B32A (32 mm x 32 mm, 0.65 mm[3], Variable Pitch BGA)	200/192/4	200/192/12	120/384/16	120/384/24	120/384/24

Notes:
1. The fabric-feeding IOPLL count inclusive of system PLL at transceiver bank, the System PLL can be repurposed for core fabric usage if not used for transceiver.
2. For more information about the device migration path, please refer to the AN 979: Intel Agilex® 5 FPGAs and SoCs Device Migration Guidelines: E-Series Application Note.
3. 0.65 mm is the minimum ball pitch, and this is not meant for signal trace routing. This VPBGA meets the 0.8 mm design rules and the use of standard plated through hole (PTH) via.
4, All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit www.intel.com/fpga.

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Product Line		Device Group B FPGAs							
		A5E 005B	A5E 007B	A5E 008B	A5E 013B	A5E 028B	A5E 043B	A5E 052B	A5E 065B
Resources	Logic elements (LEs)	50,445	69,030	85,196	138,060	282,256	434,240	523,920	656,080
	Adaptive logic modules (ALMs)	17,100	23,400	28,880	46,800	95,680	147,200	177,600	222,400
	ALM registers	68,400	93,600	115,520	187,200	382,720	588,800	710,400	889,600
	M20K memory blocks	130	179	229	358	716	1,050	1,288	1,611
	M20K memory size (Mb)	2.54	3.50	4.47	6.99	13.98	20.51	25.16	31.46
	MLAB memory count	850	1,170	1,780	2,340	4,784	6,720	8,440	11,120
	MLAB memory size (Mb)	0.52	0.71	1.09	1.43	2.92	4.10	5.13	6.79
	I/O PLL	2	2	4	4	4	8	8	8
	Fabric-feeding I/O PLL[1]	5	5	8	8	10	13	13	13
	Variable-precision digital signal processing (DSP) blocks	65	94	116	188	376	564	676	846
	18 x 19 multipliers	130	188	232	376	752	1,128	1,352	1,692
	Peak INT8 (TOPS)	1.7	2.46	3.05	4.93	9.85	14.78	17.72	22.17
Maximum Available Device Resources	LVDS pairs at 1.6 Gbps	48	48	96	96	96	192	192	192
	DDR4 and LPDDR4/5 interfaces (x32)	1	1	2	2	2	4	4	4
	MIPI D-PHY interface	7	7	14	14	14	28	28	28
	Differential (RX or TX) pairs at 17 Gbps	0	0	4	4	12	16	24	24
	PCIe 4.0 x4 instance	0	0	1	1	3	4	6	6
	High-speed I/O (HSIO)	96	96	192	192	192	384	384	384
	High-voltage I/O (HVIO)	160	160	200	200	200	120	120	120
	Secure device manager (SDM)	Provides SHA-384 bitstream integrity, ECDSA 256/384 bitstream authentication, AES-256 bitstream encryption, physically unclonable function (PUF) protected key storage, side-channel attack resistance, SPDM attestation, cryptographic services, physical anti-tamper support							
	Hard processor system	NA		Multi-core with 32-bit/64-bit dual-core Arm Cortex-A55 up to 1.25 GHz with 32 KB I/D cache and 128 KB L2 cache, and dual-core Arm Cortex-A76 up to 1.4 GHz with 64 KB I/D cache and 256 KB L2 cache, and up to 2 MB L3 shared cache, multi-channels direct memory access (DMA), 512 KB on-chip RAM, USB 3.1 x1, USB 2.0 OTG x2, TSN MAC x3, UART x2, SPI M x2, SPI S x2, I3C x2, I2C x5, NAND x1, SDMMC x1, Osc timer x2, SP timer x2, watchdog x5, GPIO x2.					
	Transceiver	NA		PCIe hard IP up to PCIe 4.0 x4 EP and RP Transceiver channel count: up to 24 channels at 17 Gbps (NRZ) Ethernet IP: up to 6 x10 GbE hard IP (MAC, PCS, and FEC)					

Package Options[2] and I/O Pins

Package code (Package size, minimum ball pitch, grid array pattern)	HVIO/ HSIO/Transceivers							
B15A (15 mm x 15 mm, 0.65 mm[3], Variable Pitch BGA)	80/62	80/62						
M16A (16 mm x 16 mm, 0.5 mm, Standard BGA)			40/192/4	40/192/4	40/192/8			
B18A (18mm x 18mm, 0.65 mm[3], Variable Pitch BGA)	160/52	160/52						
B23B (23 mm x 23 mm, 0.65 mm[3], Variable Pitch BGA)	160/96	160/96	160/192	160/192	160/192			
B23A (23 mm x 23 mm, 0.65 mm[3], Variable Pitch BGA)			120/96/4	120/96/4	120/96/12	120/96/12	120/96/12	120/96/12
B32A (32 mm x 32 mm, 0.65 mm[3], Variable Pitch BGA)			200/192/4	200/192/4	200/192/12	120/384/16	120/384/24	120/384/24

Notes:
1. The fabric-feeding IOPLL count inclusive of system PLL at transceiver bank, the System PLL can be repurposed for core fabric usage if not used for transceiver.
2. For more information about the device migration path, please refer to the AN 979: Intel Agilex® 5 FPGAs and SoCs Device Migration Guidelines: E-Series Application Note.
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