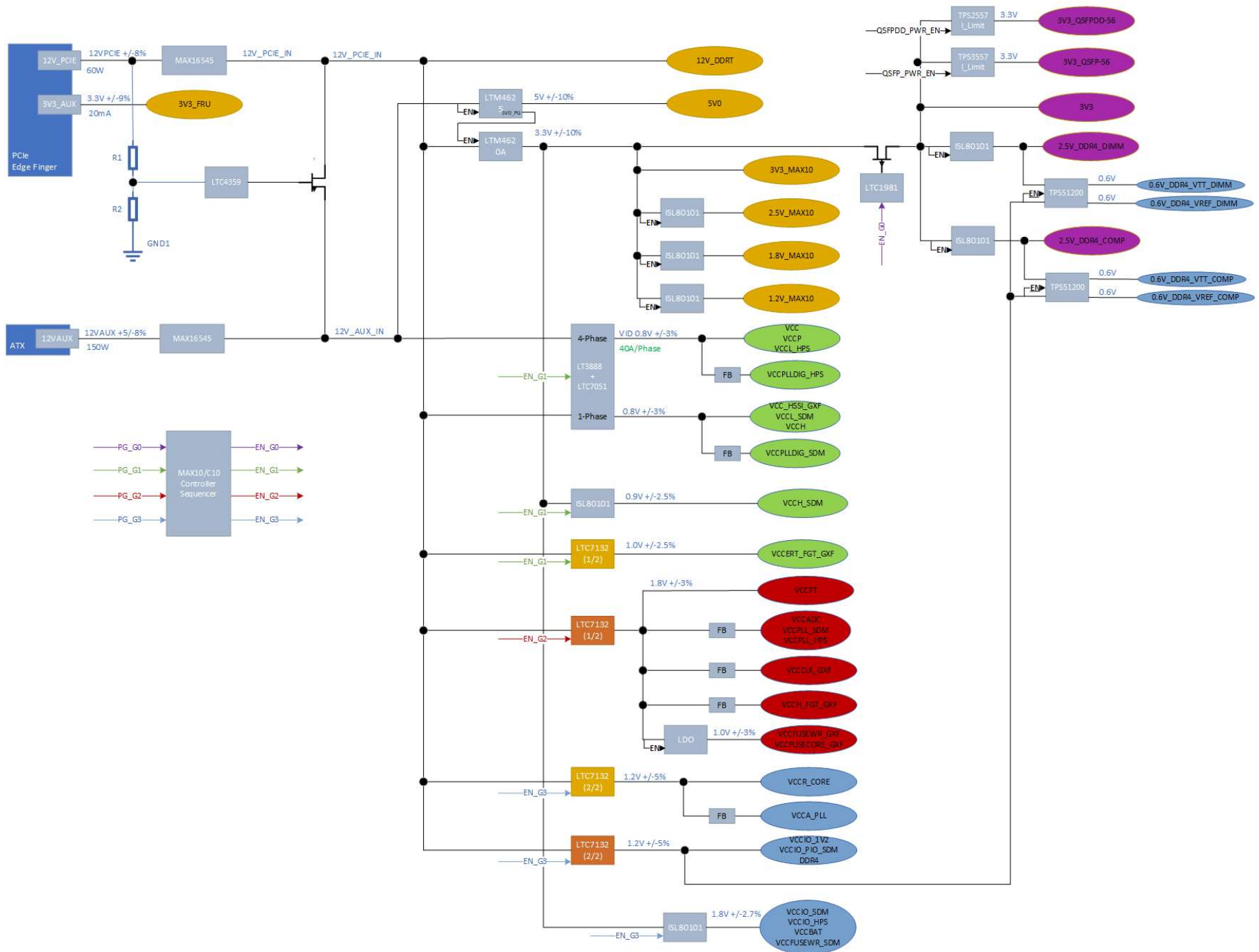


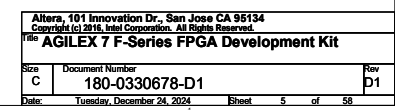


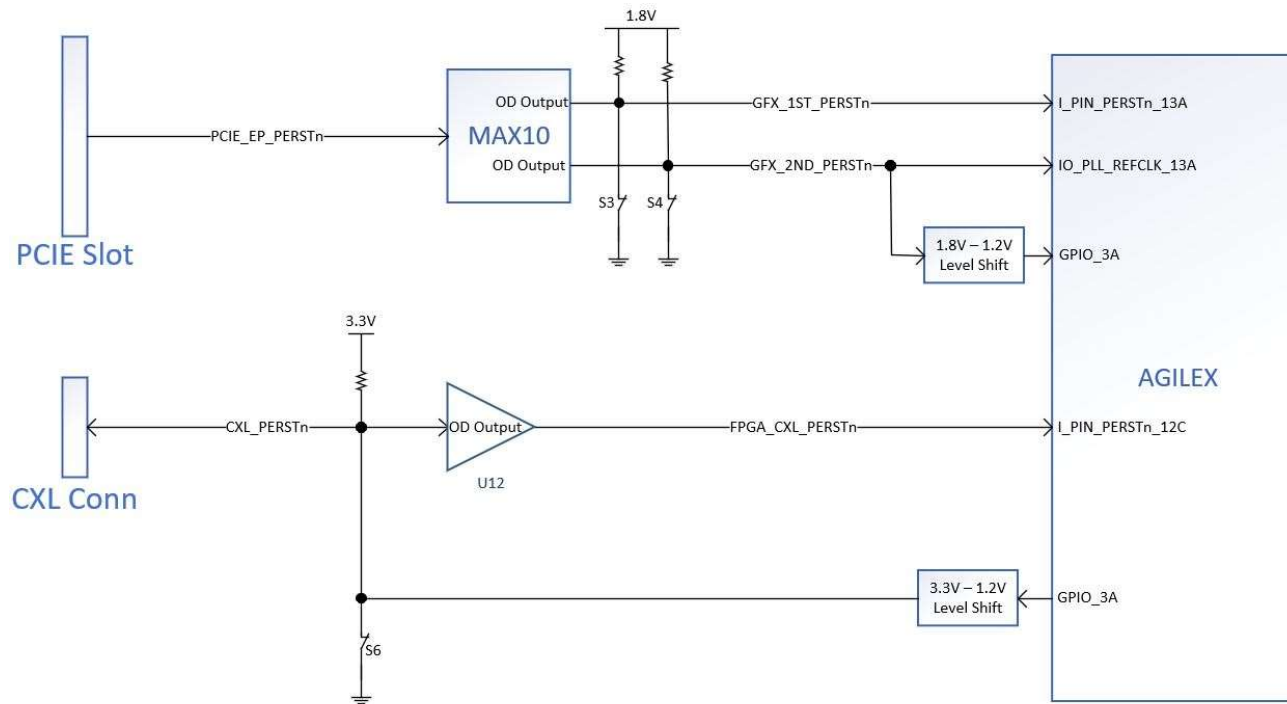
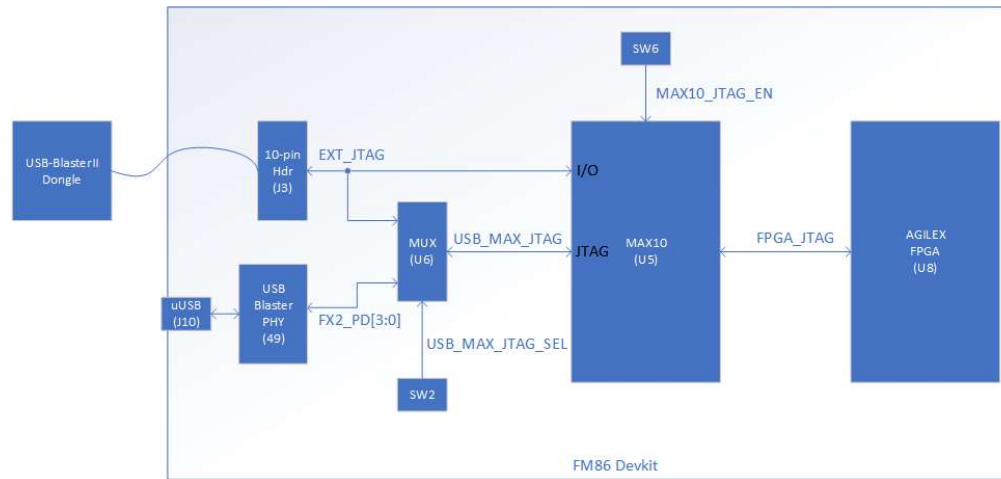


# Power Tree

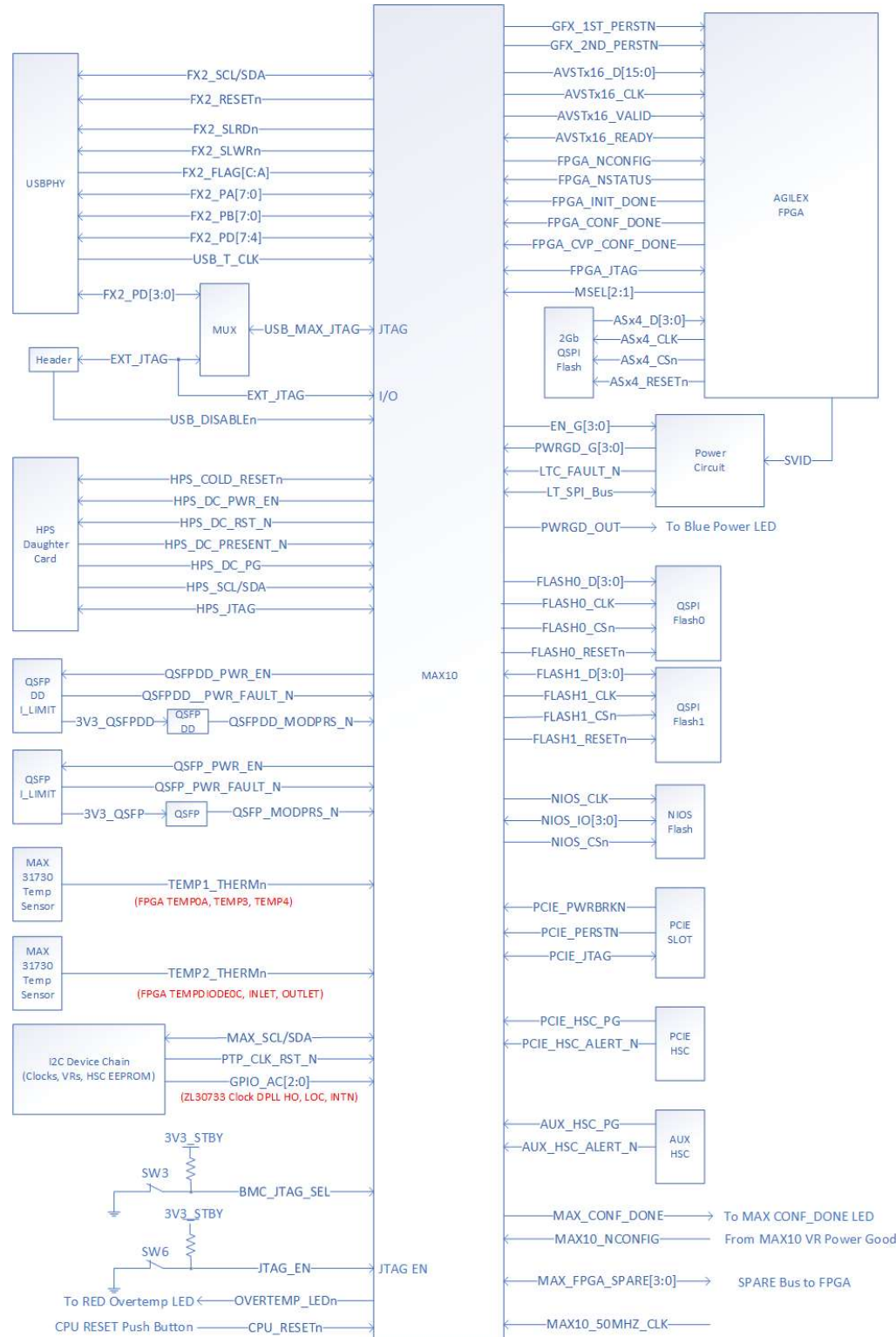




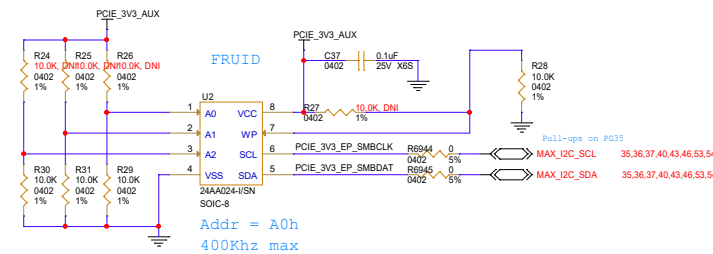
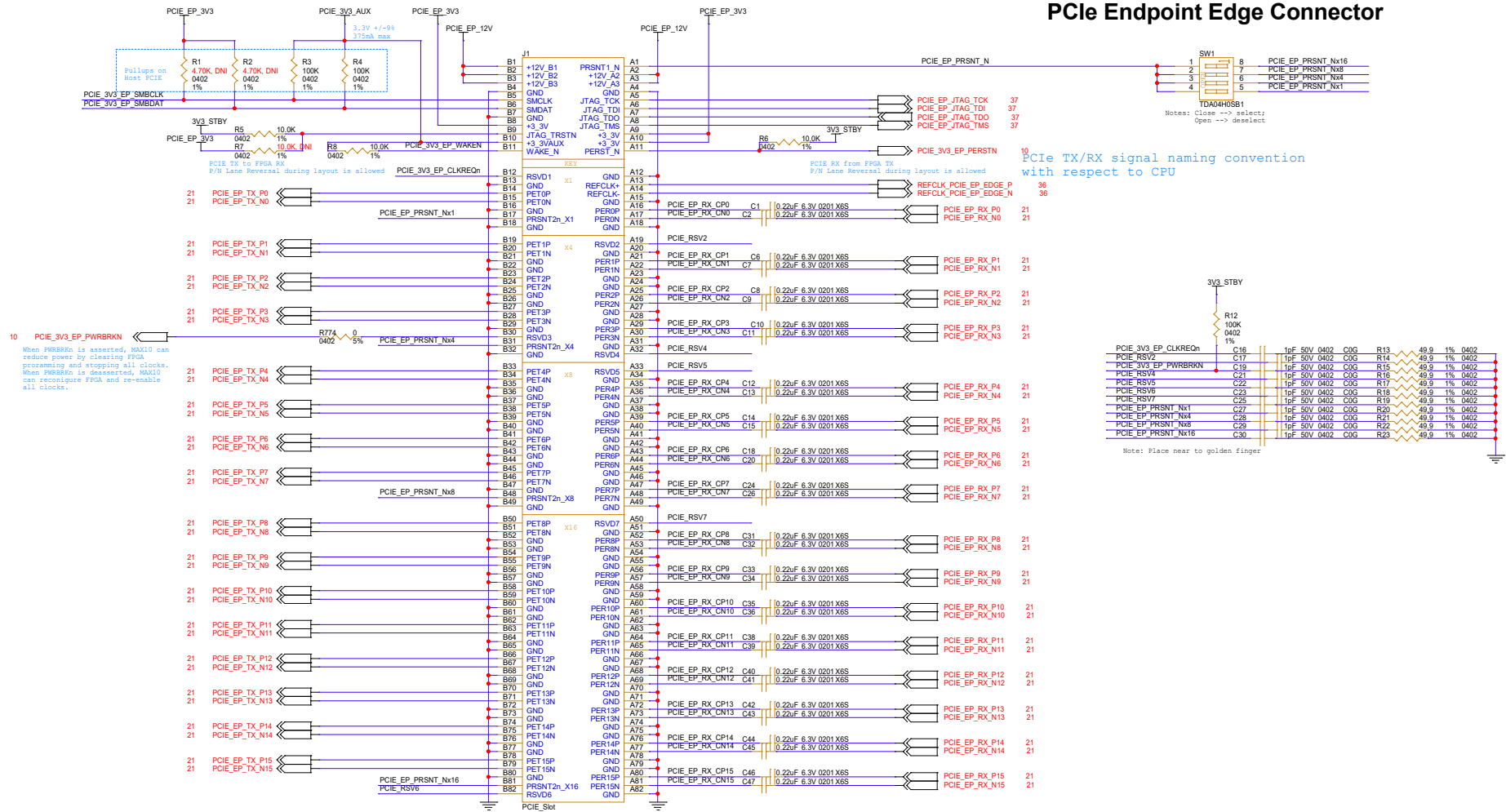








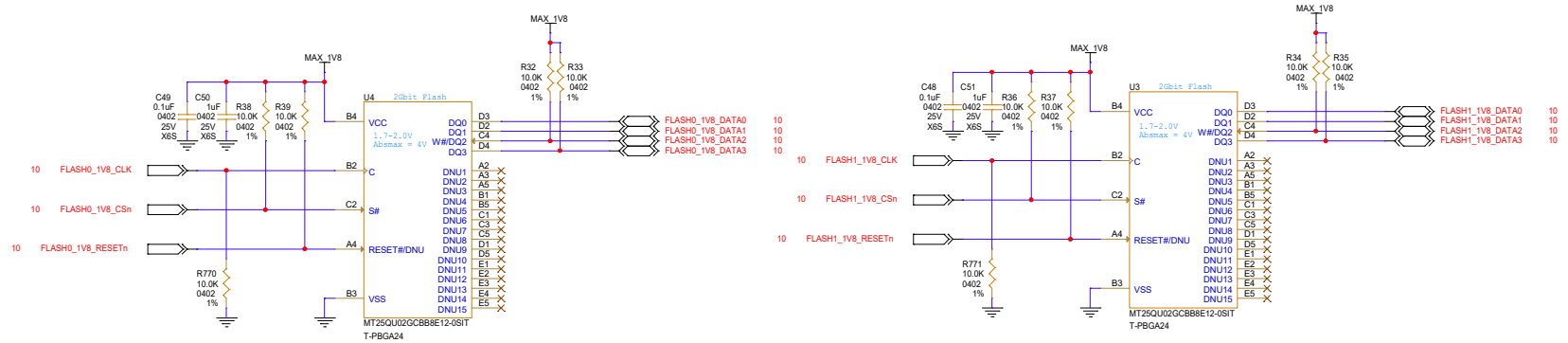
# PCIe Endpoint Edge Connector



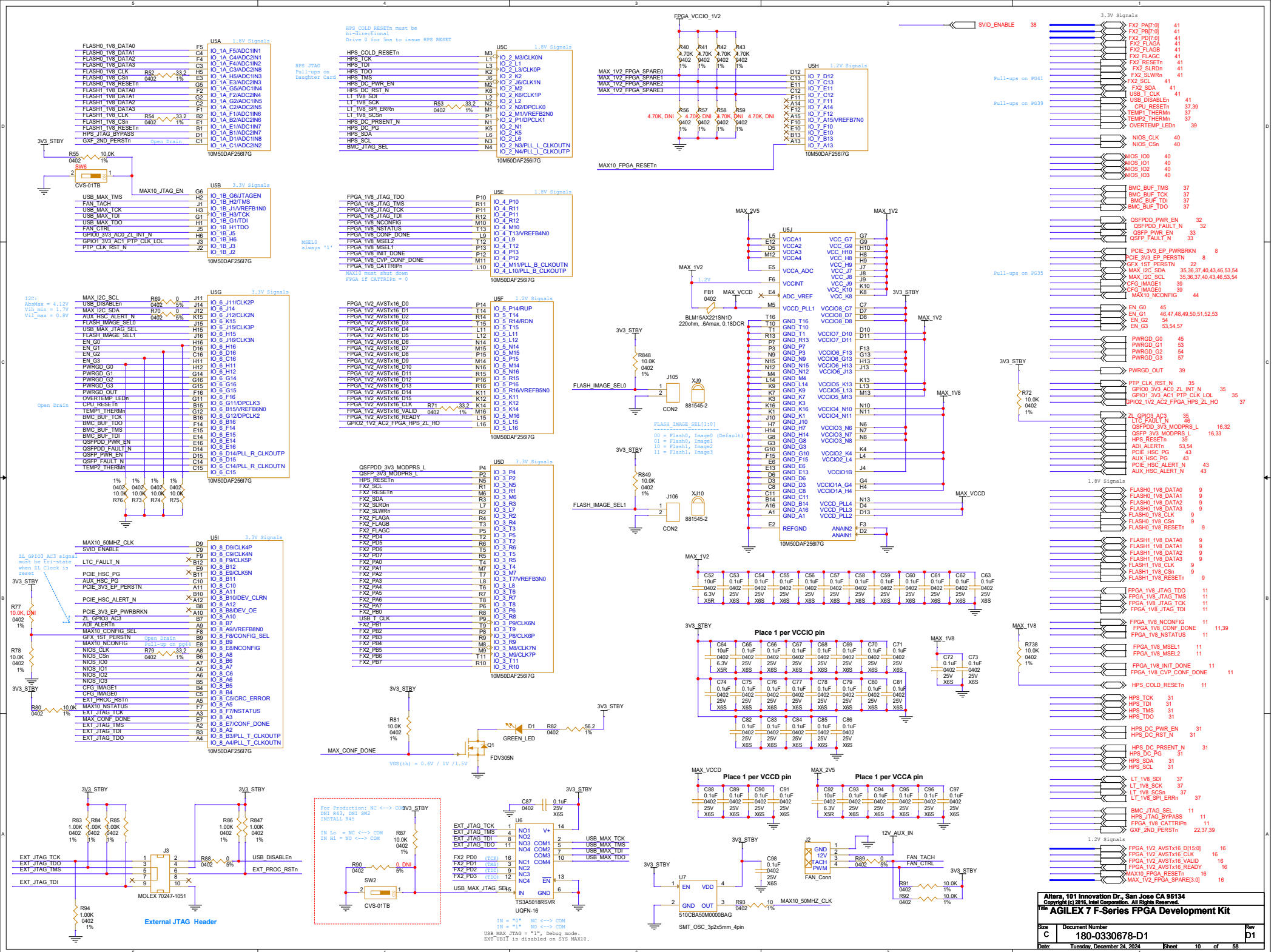


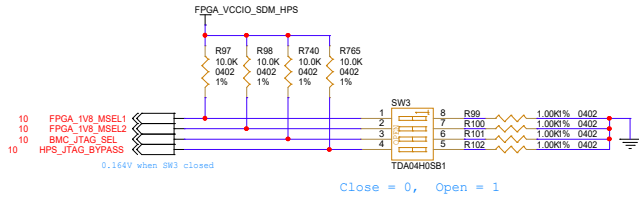
# QSPI Flash for FPGA Image

AGILEX AGF027 Bit Stream size = 833.4Mbits  
total FPGA image support = 4



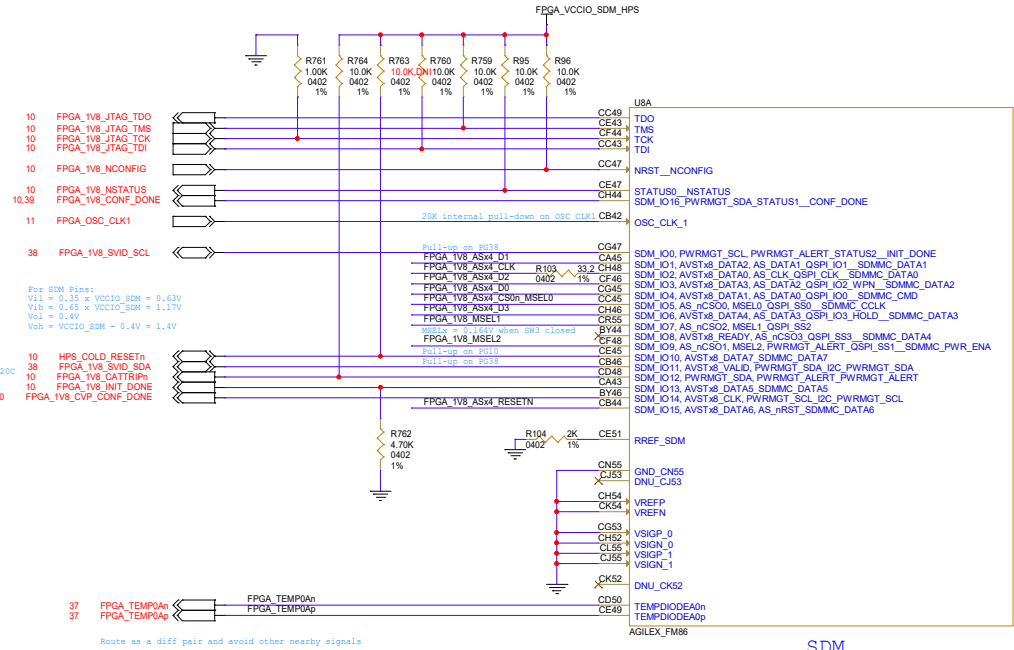
These are dual-die flash so each device is 2 loads on MAX10 IOs



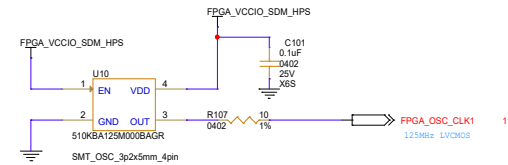
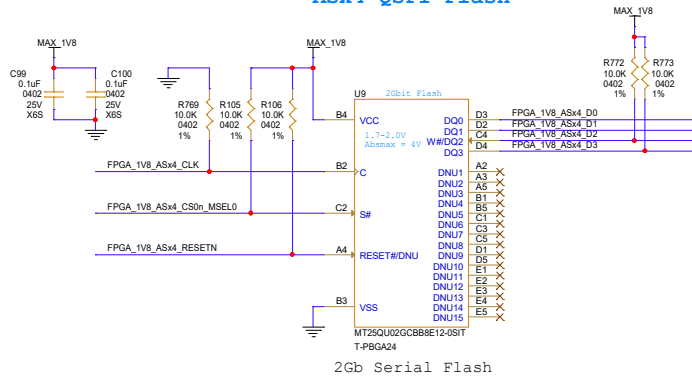


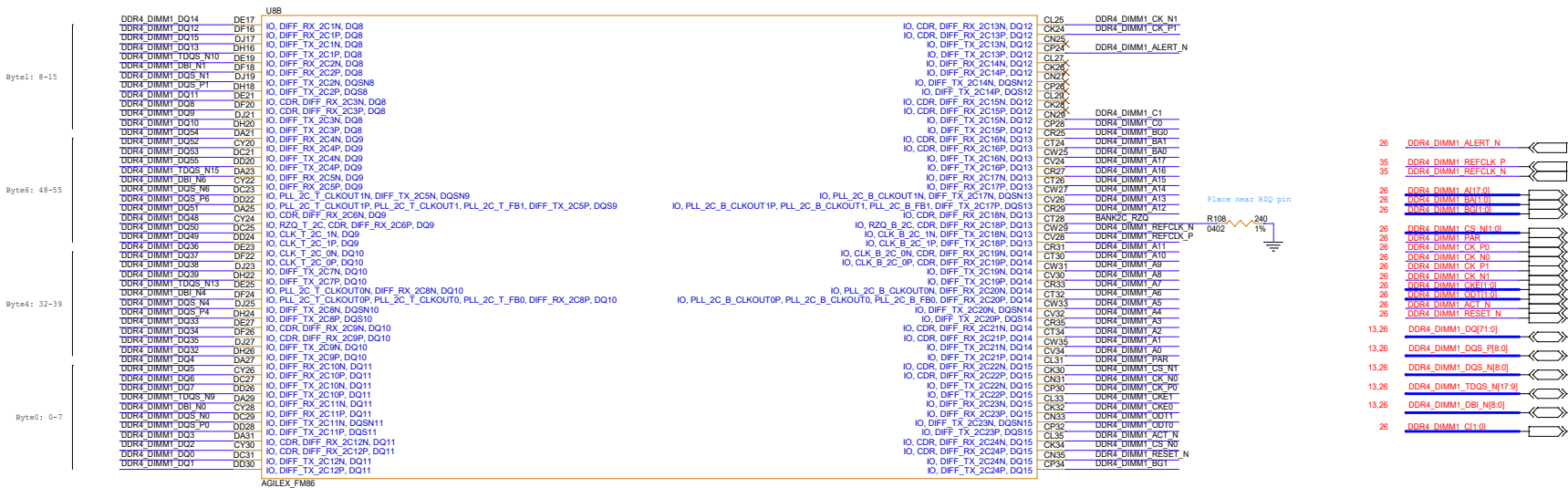
Config Mode	MSEL2	MSEL1	MSEL0
JTAG	1	1	1
AVST x16	1	0	1
AS x4 Fast (CVP)	0	0	1
AS x4 Norm	0	1	1

CATREF = 0 if FPGA Die Temp >= 120C



## ASx4 QSPI Flash







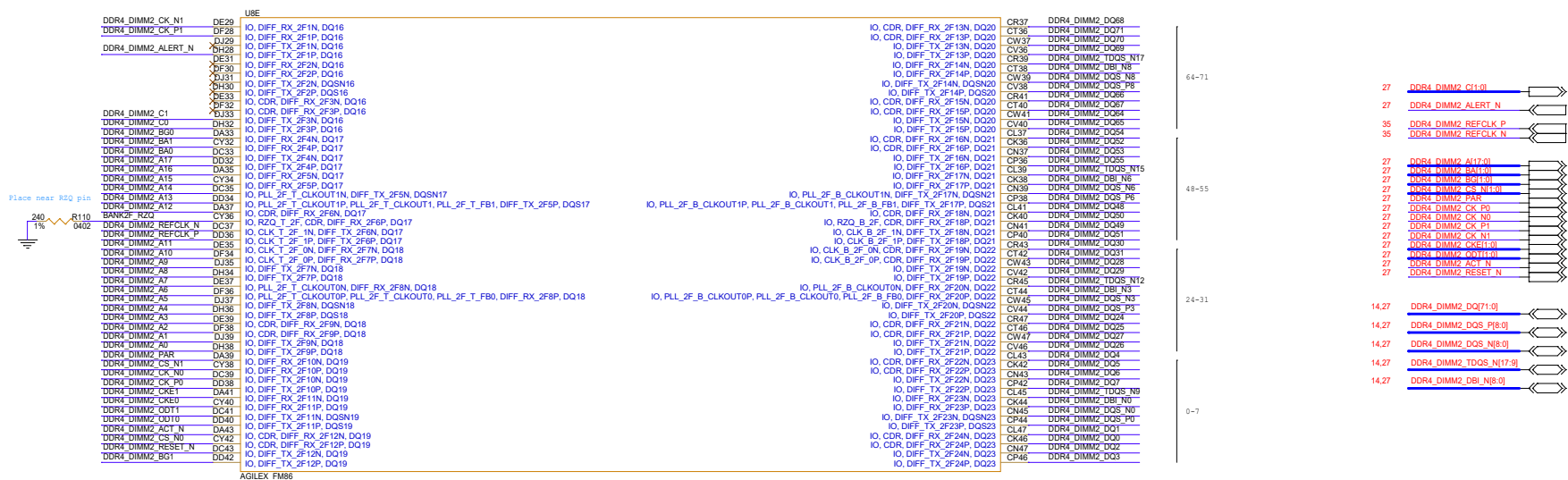
DIMM2 not available in FM76 Devkit version since Bank2E does not migrate from FM86 --> FM76

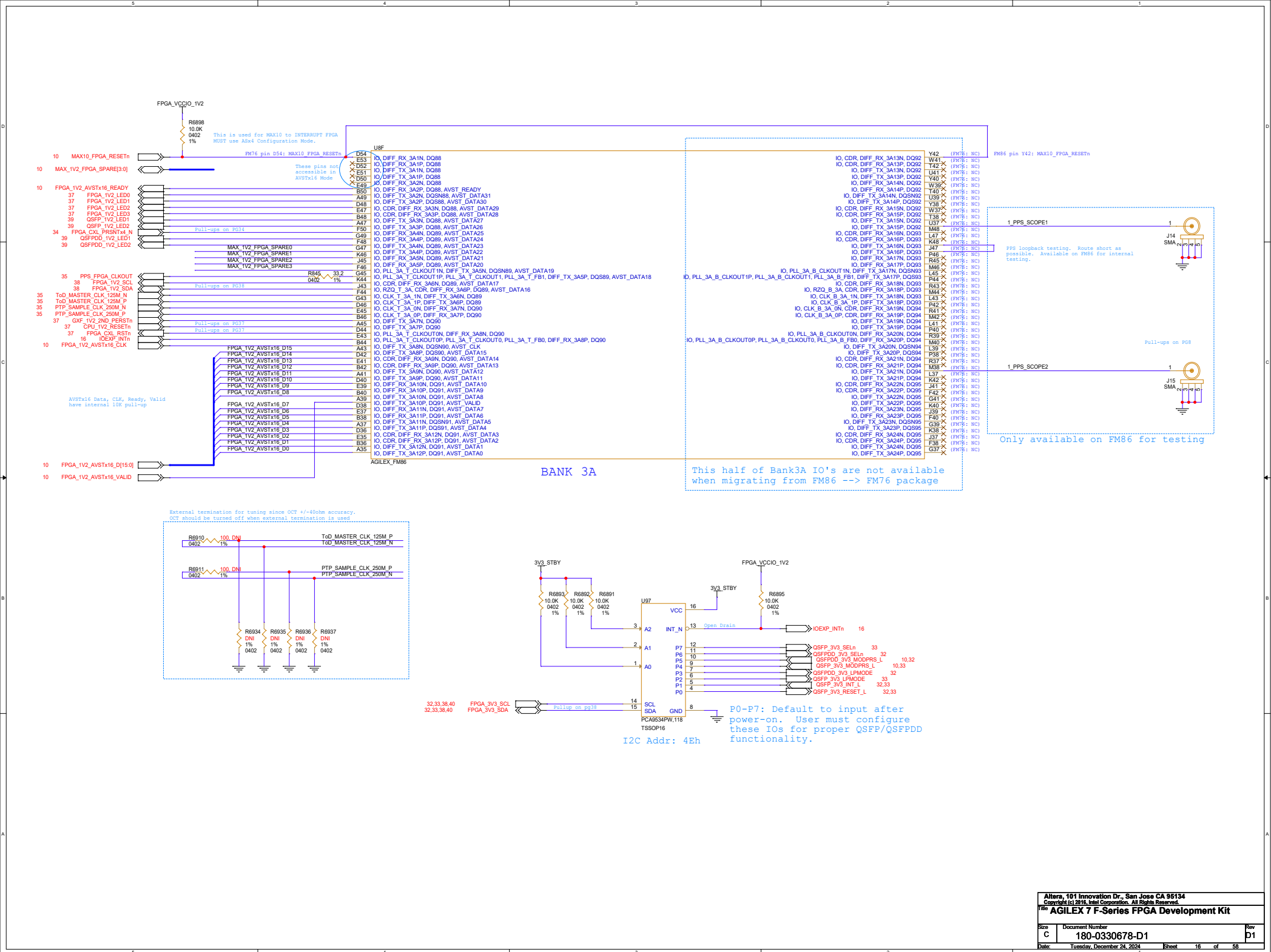
[illegible]

BANK 2E available only in FM86, not FM76



DIMM2 not available in FM76 Devkit version





Bank3B is not available in Agilex FM76.  
So no IO's will be used to support Migration from FM86 --> FM76.

U8G		
(FM76: NC)	X K36	IO, DIFF_RX_3B1N, DQ80
(FM76: NC)	X J35	IO, DIFF_RX_3B1P, DQ80
(FM76: NC)	X F36	IO, DIFF_TX_3B1N, DQ80
(FM76: NC)	X G35	IO, DIFF_TX_3B1P, DQ80
(FM76: NC)	X K34	IO, DIFF_RX_3B2N, DQ80
(FM76: NC)	X J33	IO, DIFF_RX_3B2P, DQ80
(FM76: NC)	X F34	IO, DIFF_TX_3B2N, DQSN80
(FM76: NC)	X G33	IO, DIFF_TX_3B2P, DQSN80
(FM76: NC)	X K32	IO, CDR, DIFF_RX_3B3N, DQ80
(FM76: NC)	X J31	IO, CDR, DIFF_RX_3B3P, DQ80
(FM76: NC)	X F32	IO, DIFF_TX_3B3N, DQ80
(FM76: NC)	X G31	IO, DIFF_TX_3B3P, DQ80
(FM76: NC)	X D34	IO, DIFF_RX_3B4N, DQ81
(FM76: NC)	X E33	IO, DIFF_RX_3B4P, DQ81
(FM76: NC)	X R34	IO, DIFF_TX_3B4N, DQ81
(FM76: NC)	X A33	IO, DIFF_TX_3B4P, DQ81
(FM76: NC)	X D32	IO, DIFF_RX_3B5N, DQ81
(FM76: NC)	X E31	IO, DIFF_RX_3B5P, DQ81
(FM76: NC)	X B32	IO, PLL_3B_T_CLKOUT1N, DIFF_TX_3B5N, DQSN81
(FM76: NC)	X A31	IO, PLL_3B_T_CLKOUT1P, PLL_3B_T_CLKOUT1, PLL_3B_T_FB1, DIFF_TX_3B5P, DQSN81
(FM76: NC)	X D30	IO, CDR, DIFF_RX_3B6N, DQ81
(FM76: NC)	X E29	IO, RZQ, T_3B, CDR, DIFF_RX_3B6P, DQ81
(FM76: NC)	X B30	IO, CLK, T_3B_1N, DIFF_TX_3B6N, DQ81
(FM76: NC)	X A29	IO, CLK, T_3B_1P, DIFF_TX_3B6P, DQ81
(FM76: NC)	X K30	IO, CLK, T_3B_0N, CDR, DIFF_RX_3B7N, DQ82
(FM76: NC)	X J29	IO, CLK, T_3B_0P, CDR, DIFF_RX_3B7P, DQ82
(FM76: NC)	X F30	IO, DIFF_TX_3B7N, DQ82
(FM76: NC)	X G29	IO, DIFF_TX_3B7P, DQ82
(FM76: NC)	X K28	IO, PLL_3B_T_CLKOUT0N, DIFF_RX_3B8N, DQ82
(FM76: NC)	X J27	IO, PLL_3B_T_CLKOUT0P, PLL_3B_T_CLKOUT0, PLL_3B_T_FB0, DIFF_RX_3B8P, DQ82
(FM76: NC)	X F28	IO, DIFF_TX_3B8N, DQSN82
(FM76: NC)	X G27	IO, DIFF_TX_3B8P, DQSN82
(FM76: NC)	X K26	IO, CDR, DIFF_RX_3B9N, DQ82
(FM76: NC)	X J25	IO, CDR, DIFF_RX_3B9P, DQ82
(FM76: NC)	X F26	IO, DIFF_TX_3B9N, DQ82
(FM76: NC)	X G25	IO, DIFF_TX_3B9P, DQ82
(FM76: NC)	X D28	IO, DIFF_RX_3B10N, DQ83
(FM76: NC)	X E27	IO, DIFF_RX_3B10P, DQ83
(FM76: NC)	X B28	IO, DIFF_TX_3B10N, DQ83
(FM76: NC)	X A27	IO, DIFF_TX_3B10P, DQ83
(FM76: NC)	X D26	IO, DIFF_RX_3B11N, DQ83
(FM76: NC)	X E25	IO, DIFF_RX_3B11P, DQ83
(FM76: NC)	X B26	IO, DIFF_TX_3B11N, DQSN83
(FM76: NC)	X A25	IO, DIFF_TX_3B11P, DQSN83
(FM76: NC)	X D24	IO, CDR, DIFF_RX_3B12N, DQ83
(FM76: NC)	X E23	IO, CDR, DIFF_RX_3B12P, DQ83
(FM76: NC)	X B24	IO, DIFF_TX_3B12N, DQ83
(FM76: NC)	X A23	IO, DIFF_TX_3B12P, DQ83
AGILEX_FM86		
(FM76: NC)	X K36	IO, CDR, DIFF_RX_3B13N, DQ84
(FM76: NC)	X J35	IO, CDR, DIFF_RX_3B13P, DQ84
(FM76: NC)	X F36	IO, DIFF_TX_3B13N, DQ84
(FM76: NC)	X G35	IO, DIFF_TX_3B13P, DQ84
(FM76: NC)	X K34	IO, DIFF_RX_3B14N, DQ84
(FM76: NC)	X J33	IO, DIFF_RX_3B14P, DQ84
(FM76: NC)	X F34	IO, DIFF_TX_3B14N, DQSN84
(FM76: NC)	X G33	IO, DIFF_TX_3B14P, DQSN84
(FM76: NC)	X K32	IO, CDR, DIFF_RX_3B15N, DQ84
(FM76: NC)	X J31	IO, CDR, DIFF_RX_3B15P, DQ84
(FM76: NC)	X F32	IO, DIFF_TX_3B15N, DQ84
(FM76: NC)	X G31	IO, DIFF_TX_3B15P, DQ84
(FM76: NC)	X D34	IO, CDR, DIFF_RX_3B16N, DQ85
(FM76: NC)	X E33	IO, CDR, DIFF_RX_3B16P, DQ85
(FM76: NC)	X R34	IO, DIFF_TX_3B16N, DQ85
(FM76: NC)	X A33	IO, DIFF_TX_3B16P, DQ85
(FM76: NC)	X D32	IO, DIFF_RX_3B17N, DQ85
(FM76: NC)	X E31	IO, DIFF_RX_3B17P, DQ85
(FM76: NC)	X B32	IO, PLL_3B_B_CLKOUT1N, DIFF_TX_3B17N, DQSN85
(FM76: NC)	X A31	IO, PLL_3B_B_CLKOUT1P, PLL_3B_B_FB1, DIFF_TX_3B17P, DQSN85
(FM76: NC)	X D30	IO, CDR, DIFF_RX_3B18N, DQ85
(FM76: NC)	X E29	IO, RZQ, T_3B, CDR, DIFF_RX_3B18P, DQ85
(FM76: NC)	X B30	IO, CLK, B_3B_1N, DIFF_TX_3B18N, DQ85
(FM76: NC)	X A29	IO, CLK, B_3B_1P, DIFF_TX_3B18P, DQ85
(FM76: NC)	X K30	IO, CLK, B_3B_0N, CDR, DIFF_RX_3B19N, DQ86
(FM76: NC)	X J29	IO, CLK, B_3B_0P, CDR, DIFF_RX_3B19P, DQ86
(FM76: NC)	X F30	IO, DIFF_TX_3B19N, DQ86
(FM76: NC)	X G29	IO, DIFF_TX_3B19P, DQ86
(FM76: NC)	X K28	IO, PLL_3B_B_CLKOUT0N, DIFF_RX_3B20N, DQ86
(FM76: NC)	X J27	IO, PLL_3B_B_CLKOUT0P, PLL_3B_B_FB0, DIFF_RX_3B20P, DQ86
(FM76: NC)	X F28	IO, DIFF_TX_3B20N, DQSN86
(FM76: NC)	X G27	IO, DIFF_TX_3B20P, DQSN86
(FM76: NC)	X K26	IO, CDR, DIFF_RX_3B21N, DQ86
(FM76: NC)	X J25	IO, CDR, DIFF_RX_3B21P, DQ86
(FM76: NC)	X F26	IO, DIFF_TX_3B21N, DQ86
(FM76: NC)	X G25	IO, DIFF_TX_3B21P, DQ86
(FM76: NC)	X D28	IO, CDR, DIFF_RX_3B22N, DQ87
(FM76: NC)	X E27	IO, CDR, DIFF_RX_3B22P, DQ87
(FM76: NC)	X B28	IO, DIFF_TX_3B22N, DQ87
(FM76: NC)	X A27	IO, DIFF_TX_3B22P, DQ87
(FM76: NC)	X D26	IO, DIFF_RX_3B23N, DQ87
(FM76: NC)	X E25	IO, DIFF_RX_3B23P, DQ87
(FM76: NC)	X B26	IO, DIFF_TX_3B23N, DQSN87
(FM76: NC)	X A25	IO, DIFF_TX_3B23P, DQSN87
(FM76: NC)	X D24	IO, CDR, DIFF_RX_3B24N, DQ87
(FM76: NC)	X E23	IO, CDR, DIFF_RX_3B24P, DQ87
(FM76: NC)	X B24	IO, DIFF_TX_3B24N, DQ87
(FM76: NC)	X A23	IO, DIFF_TX_3B24P, DQ87

BANK 3B available only in FM86, not FM76

Bank3C is not available in Agilex FM76.  
So no IO's will be used to support Migration from FM86 --> FM76.

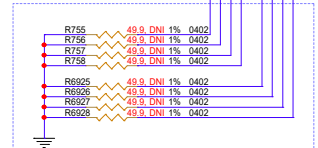
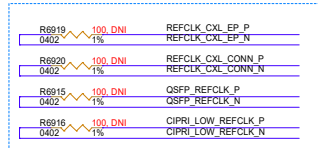
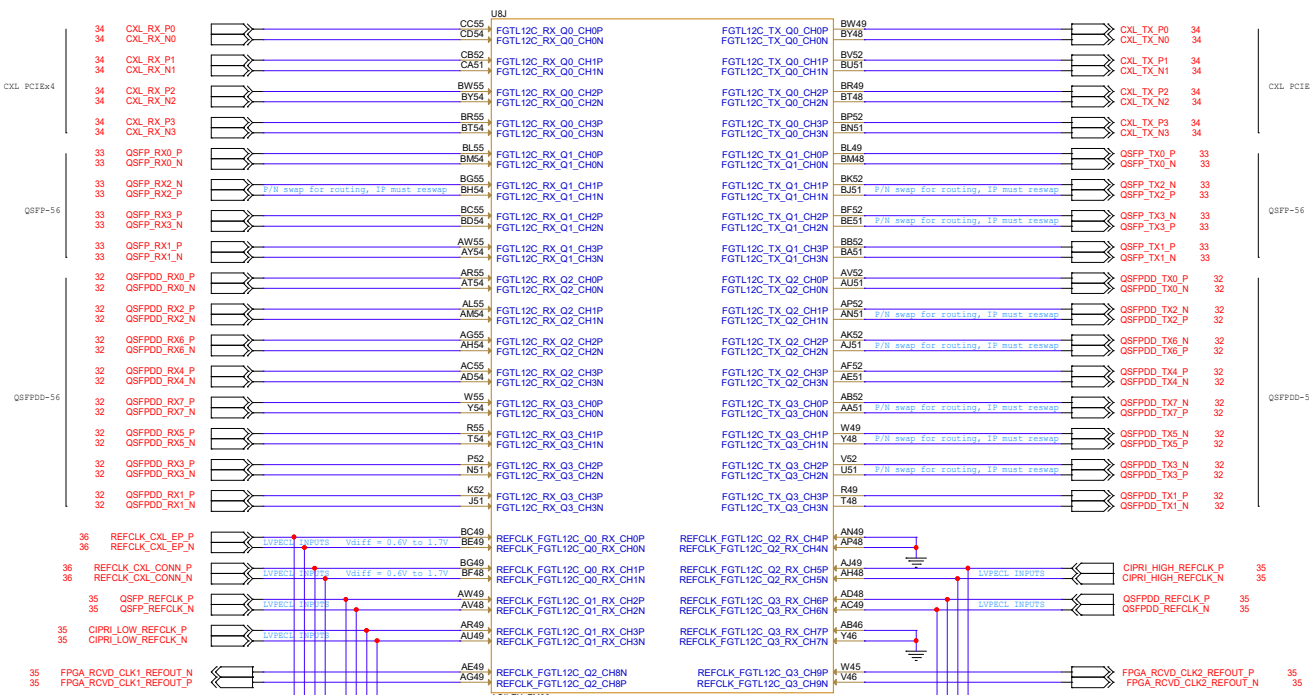
Only half of Bank3C migrates from FM86 --> FM76

USH			
(FM76: NC)	<del>X</del> D12	IO, DIFF_RX_3C1N, DQ56	IO, CDR, DIFF_RX_3C13N, DQ80
(FM76: NC)	<del>X</del> E11	IO, DIFF_RX_3C1P, DQ56	IO, CDR, DIFF_RX_3C13P, DQ80
(FM76: NC)	<del>X</del> B12	IO, DIFF_TX_3C1N, DQ56	IO, DIFF_TX_3C13N, DQ80
(FM76: NC)	<del>X</del> A11	IO, DIFF_TX_3C1P, DQ56	IO, DIFF_TX_3C13P, DQ80
(FM76: NC)	<del>X</del> D14	IO, DIFF_TX_3C1P, DQ56	IO, DIFF_TX_3C13P, DQ80
(FM76: NC)	<del>X</del> E13	IO, DIFF_RX_3C2N, DQ56	IO, DIFF_RX_3C14N, DQ80
(FM76: NC)	<del>X</del> B14	IO, DIFF_RX_3C2P, DQ56	IO, DIFF_RX_3C14P, DQ80
(FM76: NC)	<del>X</del> A13	IO, DIFF_TX_3C2N, DQ56	IO, DIFF_TX_3C14N, DQ80
(FM76: NC)	<del>X</del> D16	IO, DIFF_TX_3C2P, DQ56	IO, DIFF_TX_3C14P, DQ80
(FM76: NC)	<del>X</del> E15	IO, CDR, DIFF_RX_3C3N, DQ56	IO, CDR, DIFF_RX_3C15N, DQ80
(FM76: NC)	<del>X</del> B16	IO, CDR, DIFF_RX_3C3P, DQ56	IO, CDR, DIFF_RX_3C15P, DQ80
(FM76: NC)	<del>X</del> A15	IO, DIFF_TX_3C3N, DQ56	IO, DIFF_TX_3C15N, DQ80
(FM76: NC)	<del>X</del> D14	IO, DIFF_TX_3C3P, DQ56	IO, DIFF_TX_3C15P, DQ80
(FM76: NC)	<del>X</del> J13	IO, DIFF_RX_3C4N, DQ57	IO, CDR, DIFF_RX_3C16N, DQ81
(FM76: NC)	<del>X</del> E14	IO, DIFF_RX_3C4P, DQ57	IO, CDR, DIFF_RX_3C16P, DQ81
(FM76: NC)	<del>X</del> C14	IO, DIFF_TX_3C4N, DQ57	IO, DIFF_TX_3C16N, DQ81
(FM76: NC)	<del>X</del> K16	IO, DIFF_TX_3C4P, DQ57	IO, DIFF_TX_3C16P, DQ81
(FM76: NC)	<del>X</del> J15	IO, DIFF_RX_3C5N, DQ57	IO, DIFF_RX_3C17N, DQ81
(FM76: NC)	<del>X</del> F16	IO, DIFF_RX_3C5P, DQ57	IO, DIFF_RX_3C17P, DQ81
(FM76: NC)	<del>X</del> G15	IO, PLL_3C_T_CLKOUT1N, DIFF_TX_3C5N, DQ56	IO, PLL_3C_B_CLKOUT1P, PLL_3C_B_CLKOUT1, PLL_3C_T_FB1, DIFF_TX_3C5P, DQ57
(FM76: NC)	<del>X</del> K16	IO, PLL_3C_T_CLKOUT1P, PLL_3C_T_CLKOUT1, PLL_3C_T_FB1, DIFF_TX_3C5P, DQ57	IO, PLL_3C_B_CLKOUT1P, PLL_3C_B_CLKOUT1, PLL_3C_T_FB1, DIFF_TX_3C5P, DQ57
(FM76: NC)	<del>X</del> J17	IO, CDR, DIFF_RX_3C6N, DQ57	IO, CDR, DIFF_RX_3C18N, DQ81
(FM76: NC)	<del>X</del> F18	IO, R2Q_T_3C, CDR, DIFF_RX_3C6P, DQ57	IO, R2Q_B_3C, CDR, DIFF_RX_3C18P, DQ81
(FM76: NC)	<del>X</del> G17	IO, CLK_T_3C, IN, DIFF_TX_3C6N, DQ57	IO, CLK_B_3C, IN, DIFF_TX_3C18N, DQ81
(FM76: NC)	<del>X</del> D16	IO, CLK_T_3C-1P, DIFF_TX_3C6P, DQ57	IO, CLK_B_3C-1P, DIFF_TX_3C18P, DQ81
(FM76: NC)	<del>X</del> E17	IO, CLK_T_3C-0N, DIFF_RX_3C7N, DQ58	IO, CLK_B_3C-0N, DIFF_RX_3C19N, DQ82
(FM76: NC)	<del>X</del> B18	IO, CLK_T_3C-0P, DIFF_RX_3C7P, DQ58	IO, CLK_B_3C-0P, CDR, DIFF_RX_3C19P, DQ82
(FM76: NC)	<del>X</del> A17	IO, DIFF_TX_3C7N, DQ58	IO, DIFF_TX_3C19N, DQ82
(FM76: NC)	<del>X</del> D20	IO, DIFF_TX_3C7P, DQ58	IO, DIFF_TX_3C19P, DQ82
(FM76: NC)	<del>X</del> E19	IO, PLL_3C_T_CLKOUT0N, DIFF_RX_3C8N, DQ58	IO, PLL_3C_B_CLKOUT0N, DIFF_RX_3C20N, DQ82
(FM76: NC)	<del>X</del> B20	IO, PLL_3C_T_CLKOUT0P, PLL_3C_T_CLKOUT0, PLL_3C_T_FB0, DIFF_RX_3C8P, DQ58	IO, PLL_3C_B_CLKOUT0P, PLL_3C_B_CLKOUT0, PLL_3C_T_FB0, DIFF_RX_3C20P, DQ82
(FM76: NC)	<del>X</del> A19	IO, DIFF_TX_3C8N, DQ58	IO, DIFF_TX_3C20N, DQ82
(FM76: NC)	<del>X</del> D22	IO, DIFF_TX_3C8P, DQ58	IO, DIFF_TX_3C20P, DQ82
(FM76: NC)	<del>X</del> E21	IO, CDR, DIFF_RX_3C9N, DQ58	IO, CDR, DIFF_RX_3C21N, DQ82
(FM76: NC)	<del>X</del> B22	IO, CDR, DIFF_RX_3C9P, DQ58	IO, CDR, DIFF_RX_3C21P, DQ82
(FM76: NC)	<del>X</del> A21	IO, DIFF_TX_3C9N, DQ58	IO, DIFF_TX_3C21N, DQ82
(FM76: NC)	<del>X</del> K20	IO, DIFF_TX_3C9P, DQ58	IO, DIFF_TX_3C21P, DQ82
(FM76: NC)	<del>X</del> F19	IO, DIFF_RX_3C10N, DQ59	IO, CDR, DIFF_RX_3C22N, DQ83
(FM76: NC)	<del>X</del> F20	IO, DIFF_RX_3C10P, DQ59	IO, CDR, DIFF_RX_3C22P, DQ83
(FM76: NC)	<del>X</del> G19	IO, DIFF_TX_3C10N, DQ59	IO, DIFF_TX_3C22N, DQ83
(FM76: NC)	<del>X</del> D22	IO, DIFF_TX_3C10P, DQ59	IO, DIFF_TX_3C22P, DQ83
(FM76: NC)	<del>X</del> J21	IO, DIFF_RX_3C11N, DQ59	IO, DIFF_RX_3C23N, DQ83
(FM76: NC)	<del>X</del> F22	IO, DIFF_RX_3C11P, DQ59	IO, DIFF_RX_3C23P, DQ83
(FM76: NC)	<del>X</del> G21	IO, DIFF_TX_3C11N, DQ59	IO, DIFF_TX_3C23N, DQ83
(FM76: NC)	<del>X</del> K24	IO, DIFF_TX_3C11P, DQ59	IO, DIFF_TX_3C23P, DQ83
(FM76: NC)	<del>X</del> J23	IO, CDR, DIFF_RX_3C12N, DQ59	IO, CDR, DIFF_RX_3C24N, DQ83
(FM76: NC)	<del>X</del> F24	IO, CDR, DIFF_RX_3C12P, DQ59	IO, CDR, DIFF_RX_3C24P, DQ83
(FM76: NC)	<del>X</del> G23	IO, DIFF_TX_3C12N, DQ59	IO, DIFF_TX_3C24N, DQ83
(FM76: NC)	<del>X</del> K23	IO, DIFF_TX_3C12P, DQ59	IO, DIFF_TX_3C24P, DQ83
AGILEX_FM86			

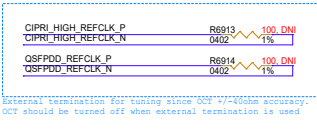
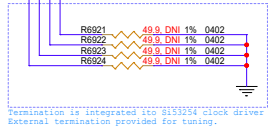
Not available in FM76

Available in FM86 and FM76

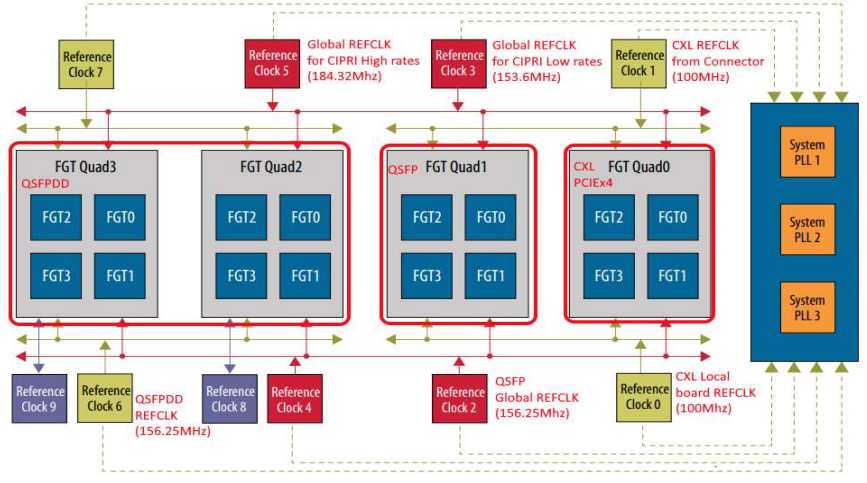




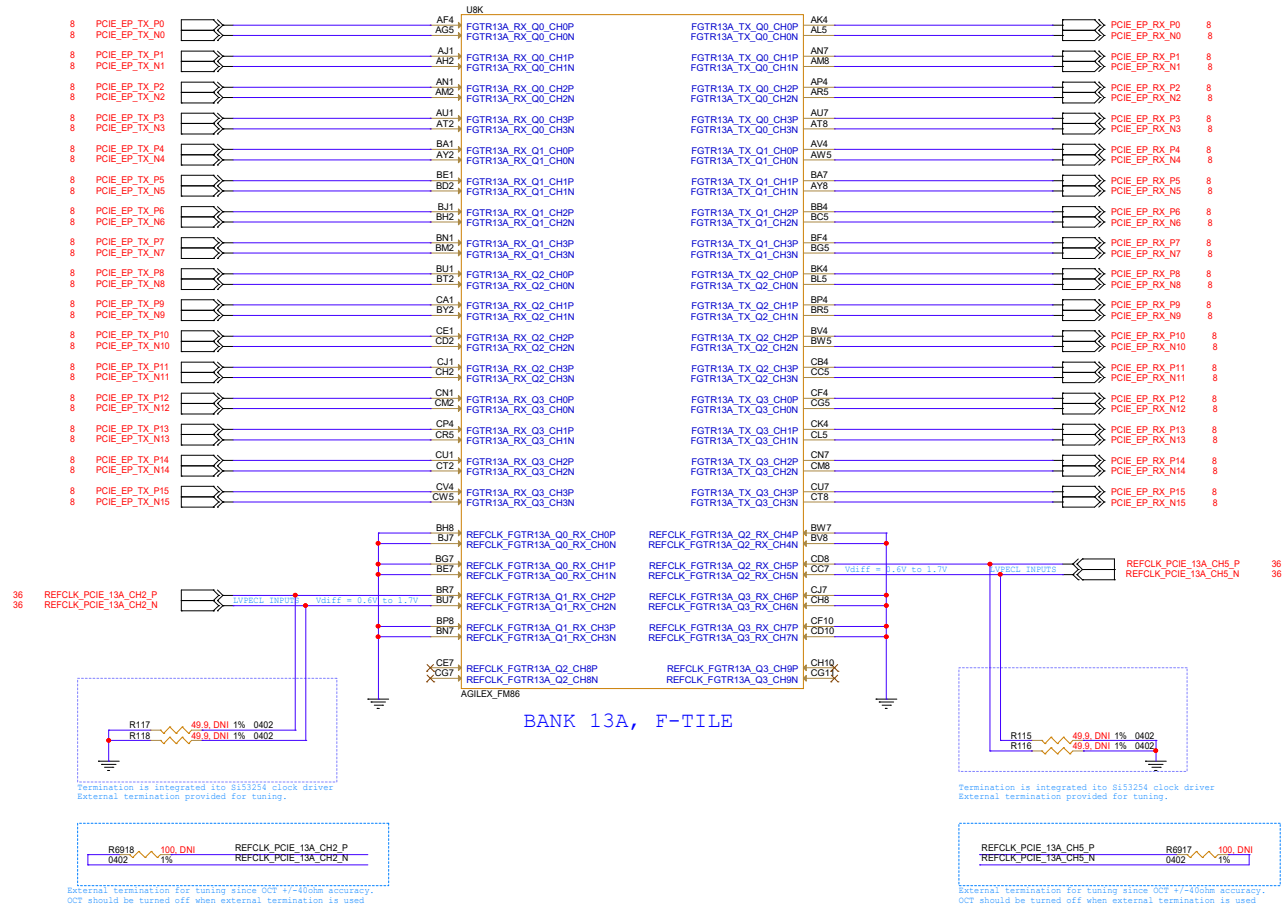
BANK 12C, F-TILE

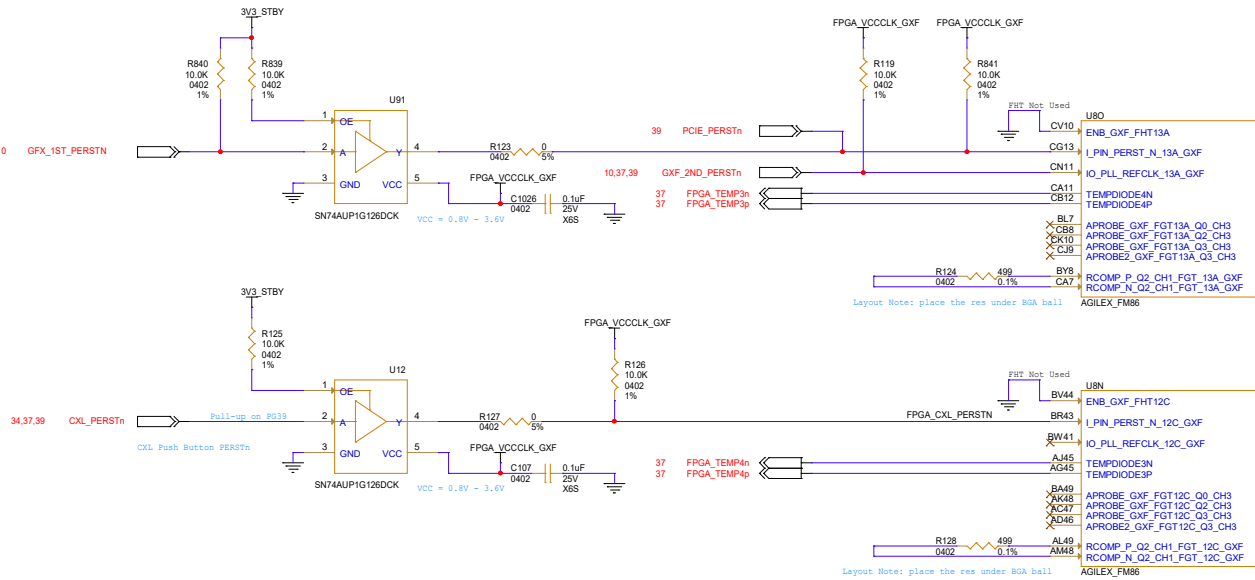
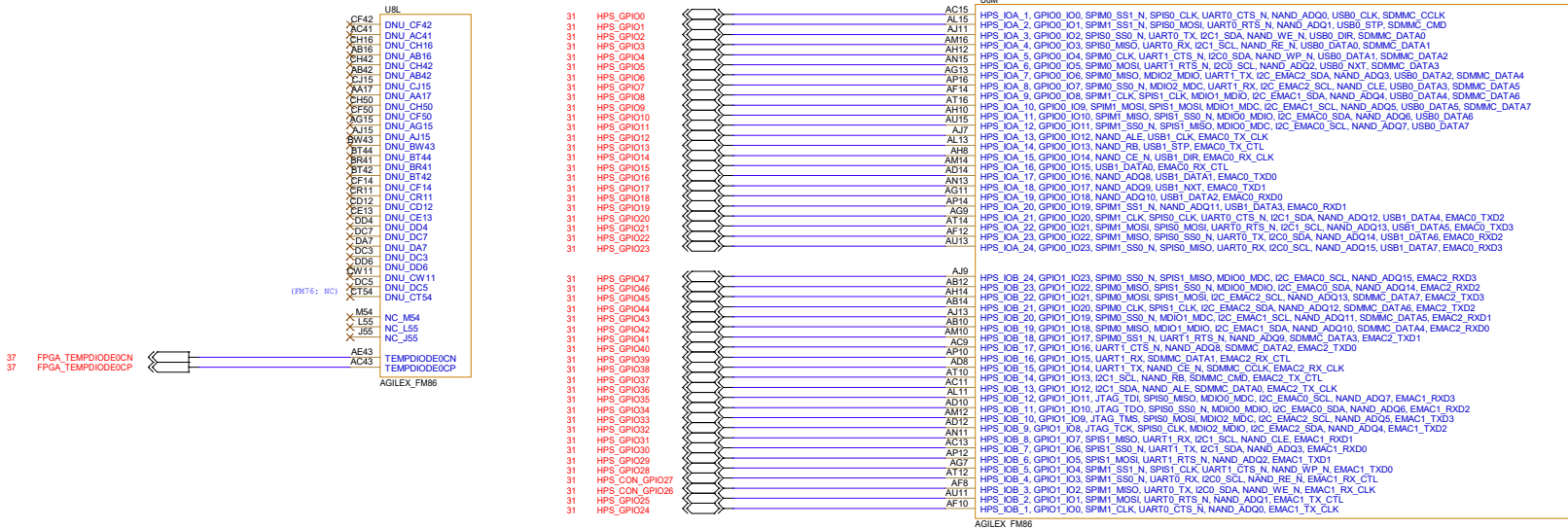


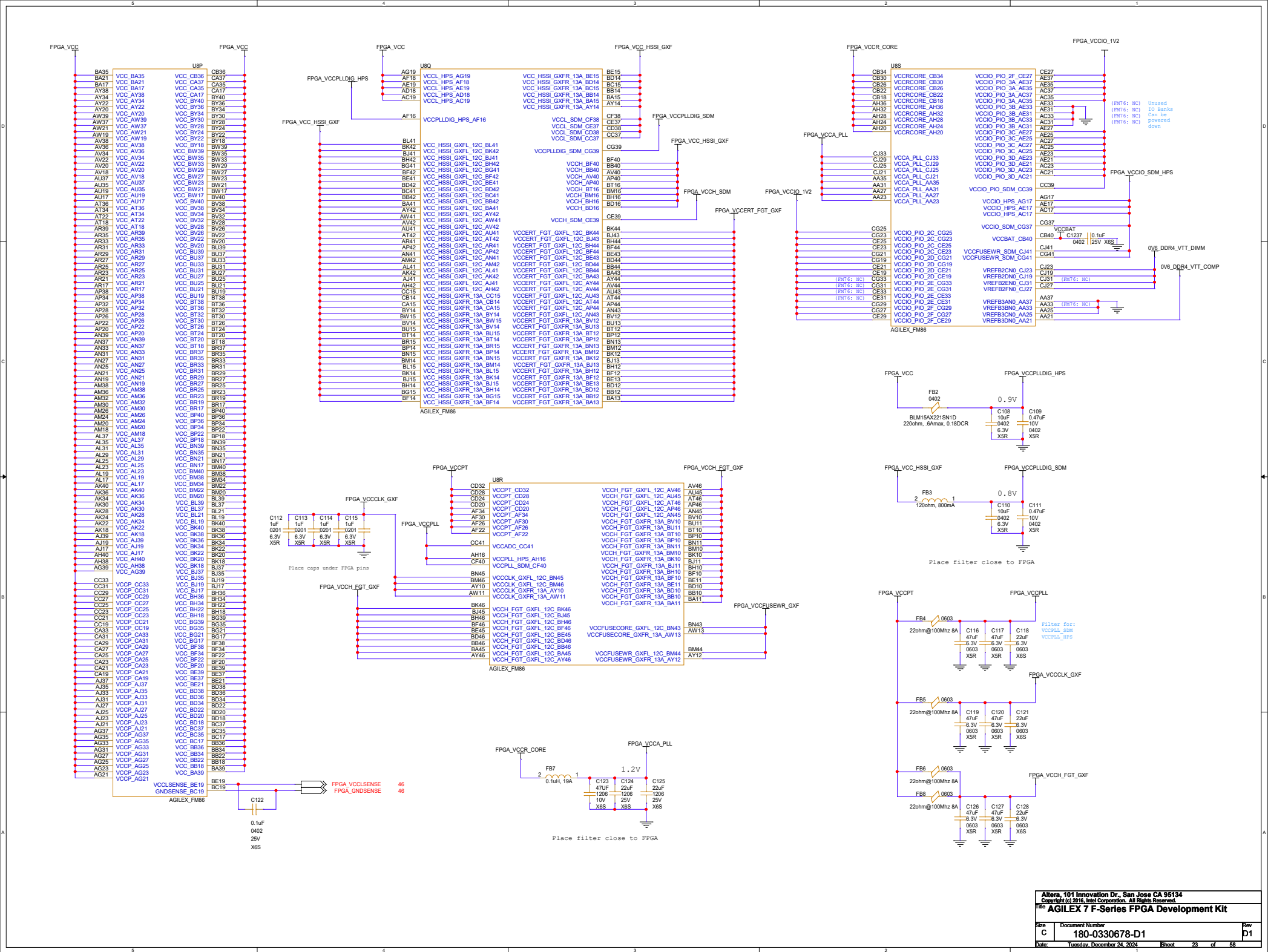
FGT and System PLL Reference Clock Network

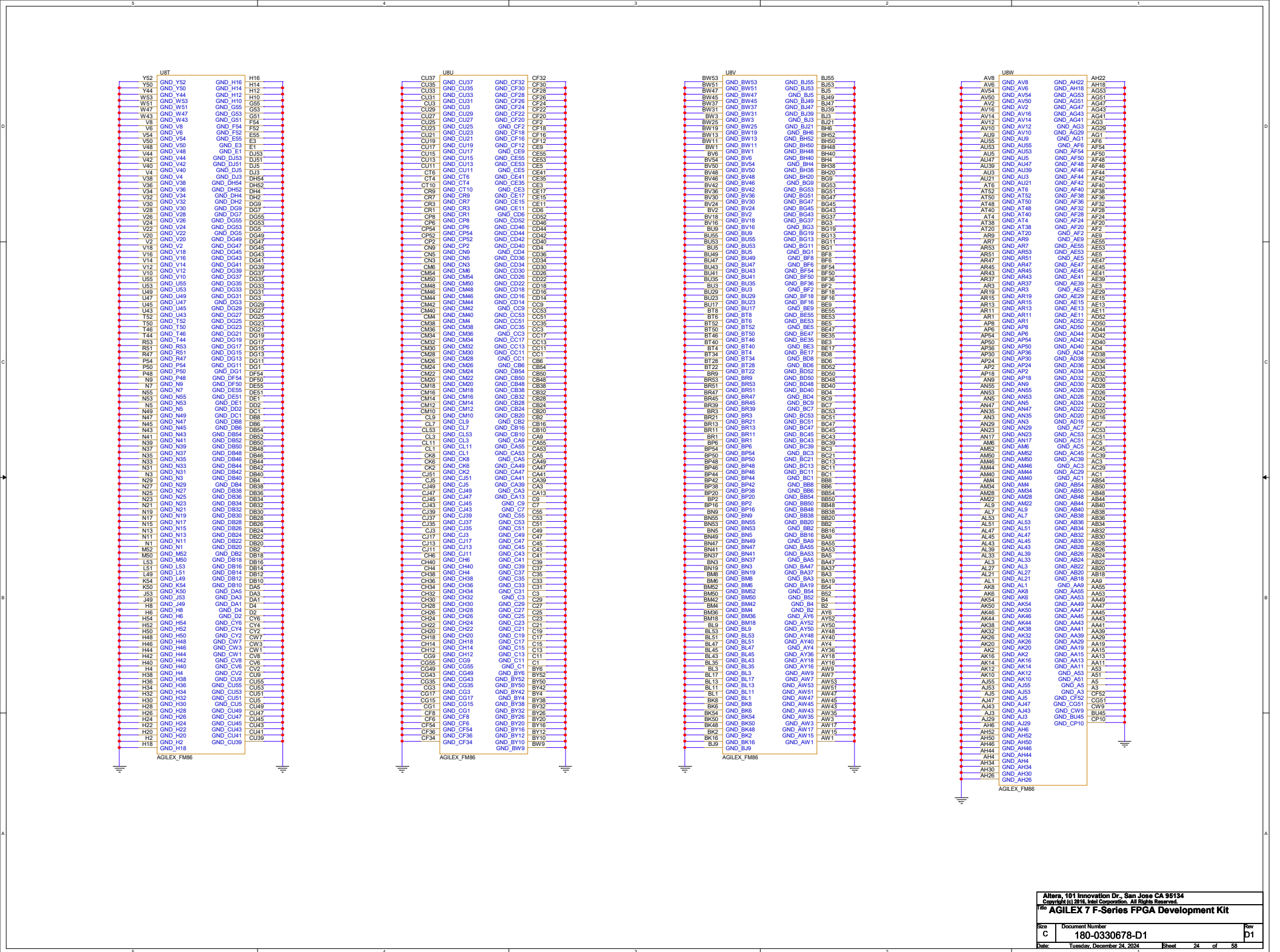












# DDR4/DDR-T DIMM Pin Map

Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side
1	VDD	145	VDD	38	DQ24	182	VSS	75	CLK0#	219	CLK1#	108	DQ40	252	VSS
2	VSS	146	VREFCA	39	VSS	183	DQ25	76	VDD	220	VDD	109	VSS	253	DQ41
3	DQ4	147	VSS	40	DQS12	184	VSS	77	VTT	221	VTT	110	DQS14	254	VSS
4	VSS	148	DQ5	41	DQS12#	185	DQS13#					111	DQS14#	255	DQS5#
5	DQ0	149	VSS	42	VSS	186	DQS3					112	VSS	256	DQS5
6	VSS	150	DQ1	43	DQ30	187	VSS					113	DQ46	257	VSS
7	DQS0	151	VSS	44	VSS	188	DQ31					114	VSS	258	DQ47
8	DQS0#	152	DQS0#	45	DQ26	189	VSS	78	EVENT	222	PARITY	115	DQ42	259	VSS
9	VSS	153	DQS0	46	VSS	190	DQ27	79	A0	223	VDD	116	VSS	260	DQ43
10	DQ6	154	VSS	47	CB4	191	VSS	80	VDD	224	BA1	117	DQ52	261	VSS
11	VSS	155	DQ7	48	VSS	192	CB5	81	BA0	225	A10	118	VSS	262	DQ53
12	DQ2	156	VSS	49	CB0	193	VSS	82	RASH/A16	226	VDD	119	DQ49	263	VSS
13	VSS	157	DQ3	50	VSS	194	CB1	83	VDD	227	RFU	120	VSS	264	DQ49
14	DQ12	158	VSS	51	DQS17	195	VSS	84	CS0#	228	WE#/A14	121	DQS15	265	VSS
15	VSS	159	DQ13	52	DQS17#	196	DQS8#	85	VDD	229	VDD	122	DQS15#	266	DQS6#
16	DQ8	160	VSS	53	VSS	197	DQS8	86	CASH/A15	230	SAVE#	123	VSS	267	DQS6
17	VSS	161	DQ9	54	CB6	198	VSS	87	ODT0	231	VDD	124	DQ54	268	VSS
18	DQS10	162	VSS	55	VSS	199	CB7	88	VDD	232	A13	125	VSS	269	DQS5
19	DQS10#	163	DQS1#	56	CB2	200	VSS	89	CS1#	233	VDD	126	DQ50	270	VSS
20	VSS	164	DQS1	57	VSS	201	CB3	90	VDD	234	A17	127	VSS	271	DQS1
21	DQ14	165	VSS	58	RESET#	202	VSS	91	ODT1	235	C2	128	DQ60	272	VSS
22	VSS	166	DQ15	59	VDD	203	CKE1	92	VDD	236	VDD	129	VSS	273	DQ51
23	DQ10	167	VSS	60	CKE0	204	VDD	93	C0	237	C1	130	DQ36	274	VSS
24	VSS	168	DQ11	61	VDD	205	RFU	94	VSS	238	SA2	131	VSS	275	DQ57
25	DQ20	169	VSS	62	ACT#	206	VDD	95	DQ36	239	VSS	132	DQS16	276	VSS
26	VSS	170	DQ21	63	BG0	207	BG1	96	VSS	240	DQ37	133	DQS16#	277	DQS7#
27	DQ16	171	VSS	64	VDD	208	ALERT#	97	DQ32	241	VSS	134	VSS	278	DQS7
28	VSS	172	DQ17	65	A12	209	VDD	98	VSS	242	DQ33	135	DQ52	279	VSS
29	DQS11	173	VSS	66	A9	210	A11	99	DQS13	243	VSS	136	VSS	280	DQ63
30	DQS11#	174	DQS2#	67	VDD	211	A7	100	DQS13#	244	DQS4#	137	DQ58	281	VSS
31	VSS	175	DQS2	68	A8	212	VDD	101	VSS	245	DC154	138	VSS	282	DQ59
32	DQ22	176	VSS	69	A6	213	A5	102	DQ38	246	VSS	139	SA0	283	VSS
33	VSS	177	DQ23	70	VDD	214	A4	103	VSS	247	DQ39	140	SA1	284	VDDSPD
34	DQ18	178	VSS	71	A3	215	VDD	104	DQ34	248	VSS	141	SCL	285	SDA
35	VSS	179	DQ19	72	A1	216	A2	105	VSS	249	DQ35	142	VPP	286	VPP
36	DQ28	180	VSS	73	VDD	217	VDD	106	DQ44	250	VSS	143	VPP	287	VPP
37	VSS	181	DQ29	74	CLK0	218	CLK1	107	VSS	251	DQ45	144	RFU	288	VPP

DDR-T DIMM Pin Map is Identical to standard DDR4 DIMM Pin Map except the DDR-T protocol repurposes five of these pins:

CS1# (pin 89) : Grant, GNT# <0> Input

CKE1 (pin 203) : Request, REQ# <0> Output

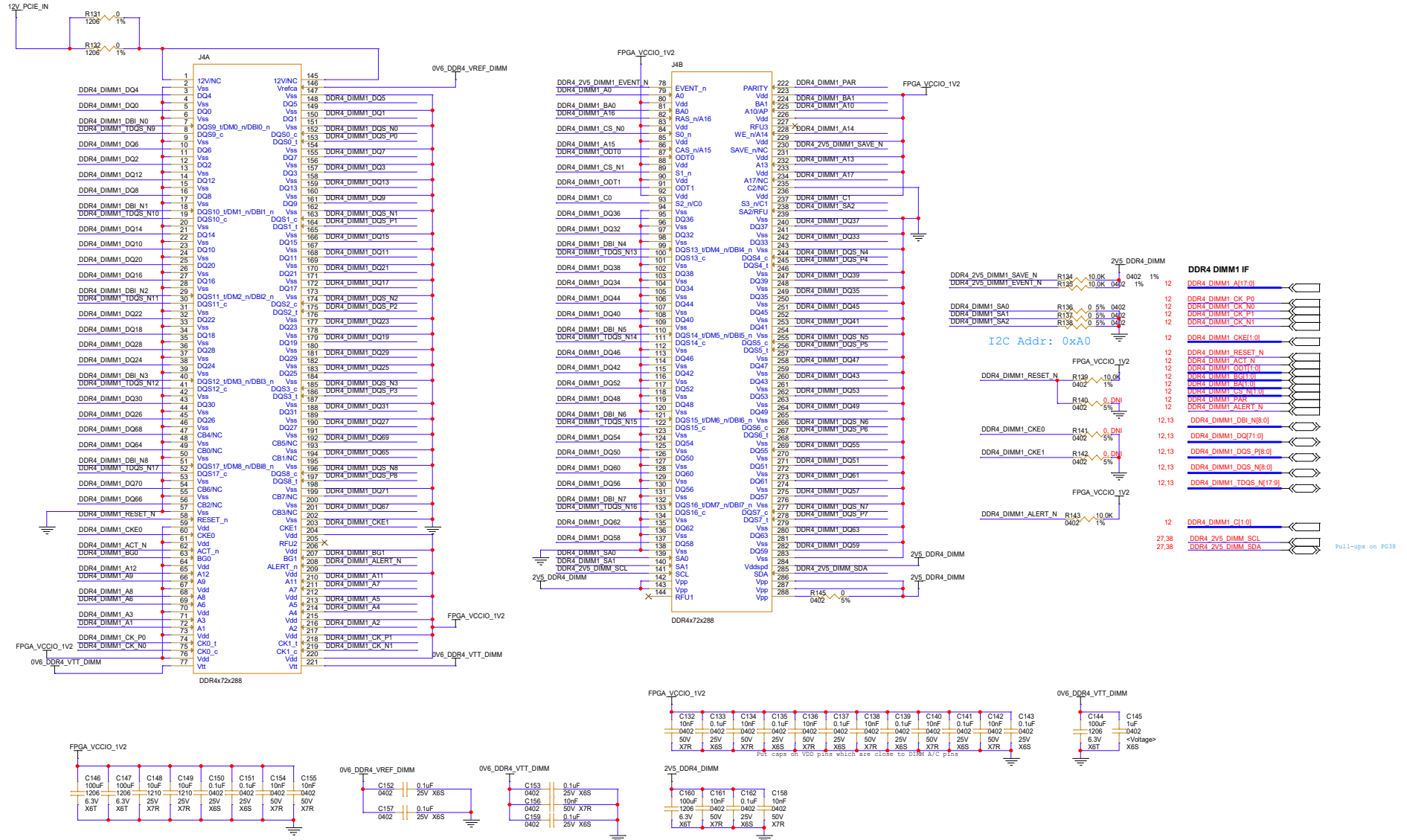
ODT1 (pin 91) : Error, ERR# Output

CLK1 (pin 218):Early Read ID, ERID<0> Output

CLK1# (pin 219):Early Read ID, ERID<1> Output



### DDR4/DDR-T DIMM 1

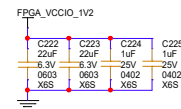
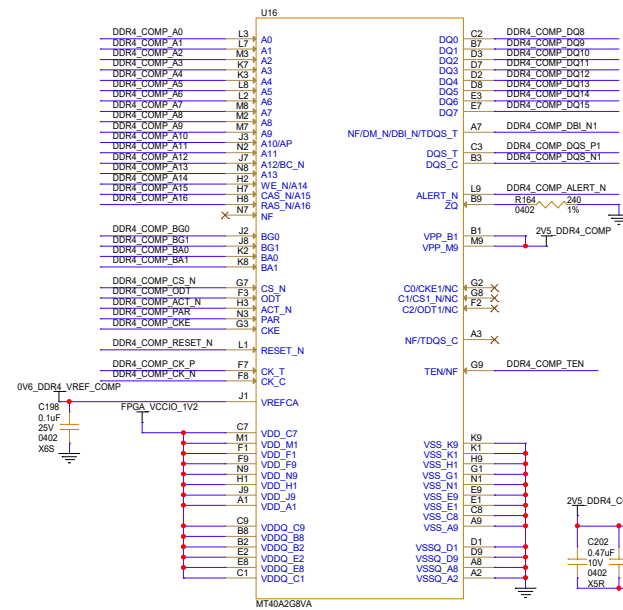
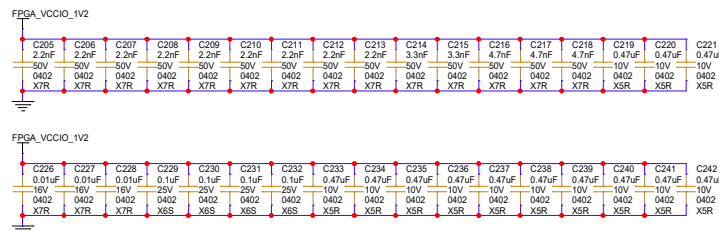
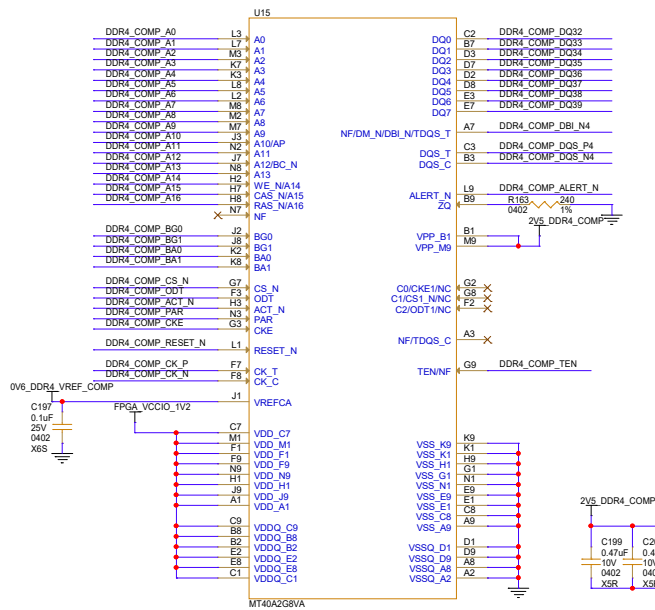




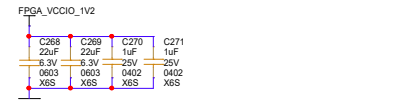
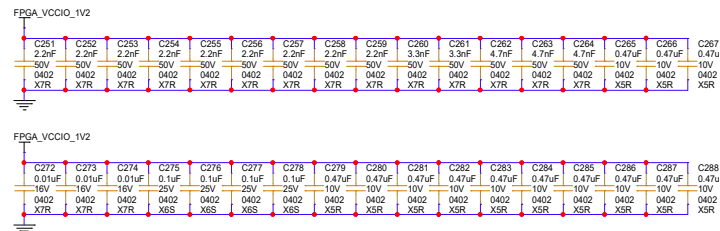
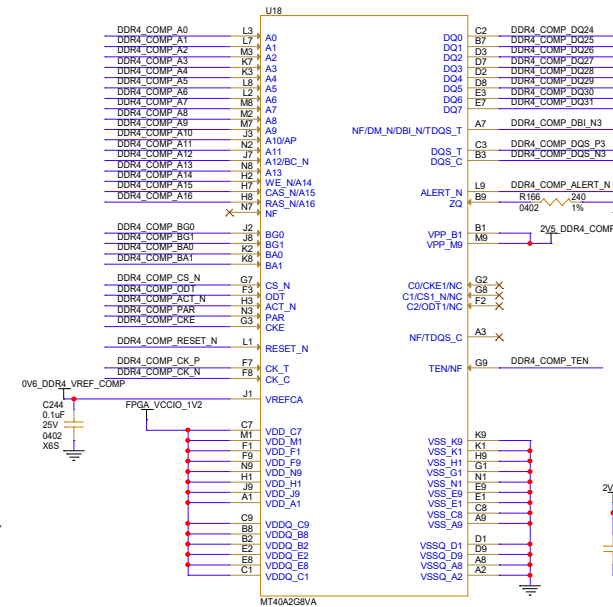
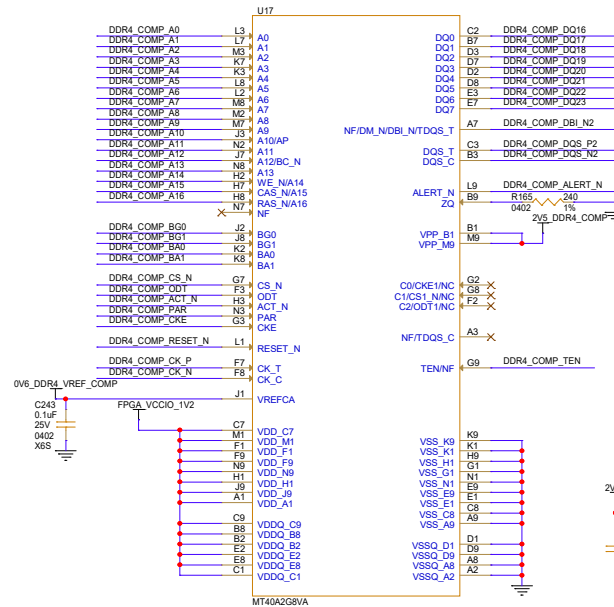
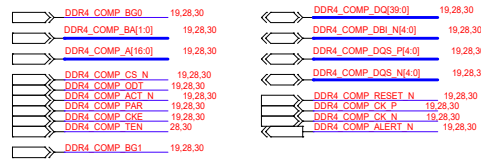


# DDR4 COMPONENT #1/#2

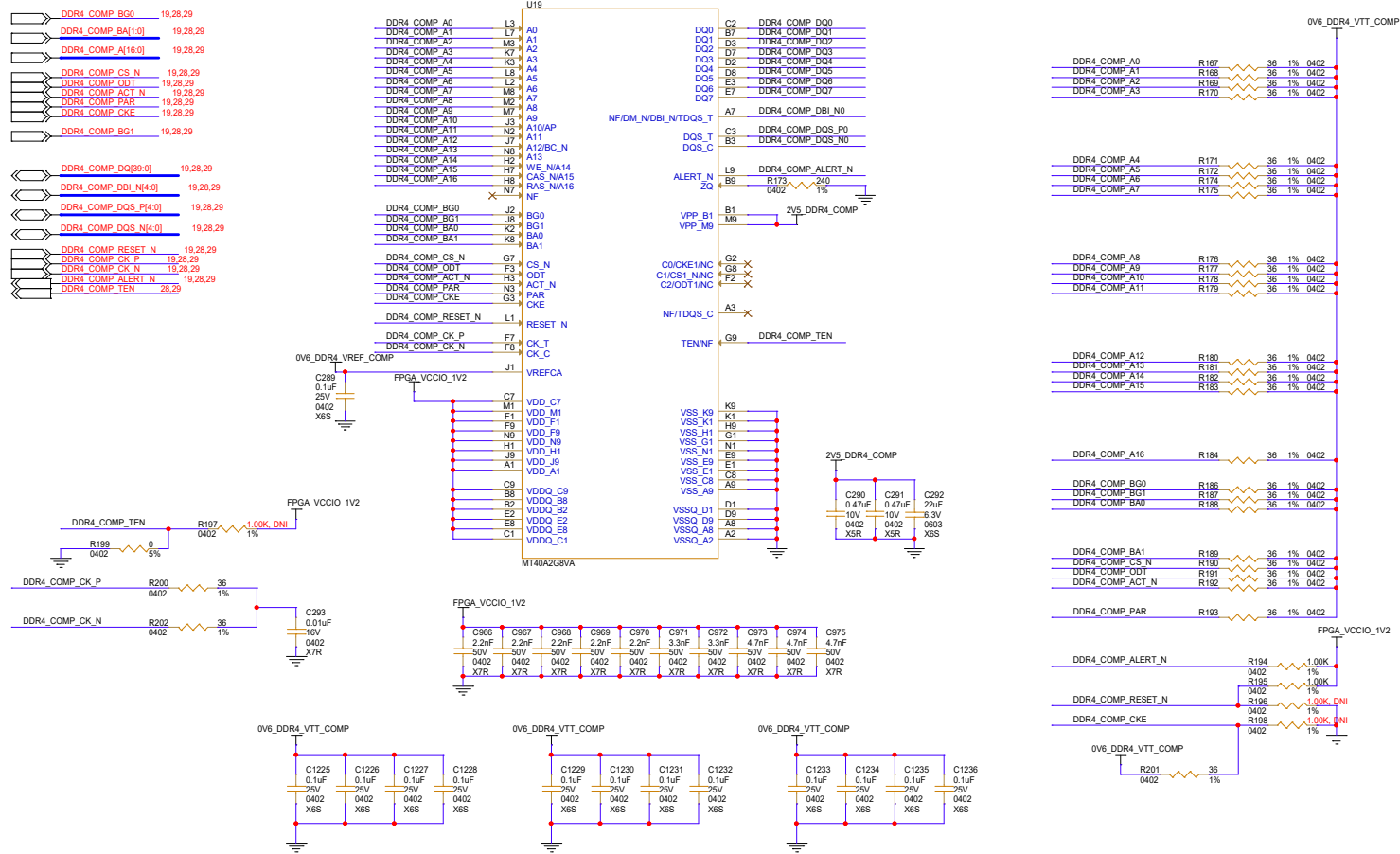
DDR4_COMP_BG0	19,29,30	DDR4_COMP_DQ[39:0]	19,29,30
DDR4_COMP_BA[1:0]	19,29,30	DDR4_COMP_DBI_N[4:0]	19,29,30
DDR4_COMP_A[16:0]	19,29,30	DDR4_COMP_DQS_P[4:0]	19,29,30
DDR4_COMP_CS_N	19,29,30	DDR4_COMP_DQS_N[4:0]	19,29,30
DDR4_COMP_ODT	19,29,30	DDR4_COMP_RESET_N	19,29,30
DDR4_COMP_ACT_N	19,29,30	DDR4_COMP_CK_P	19,29,30
DDR4_COMP_PAR	19,29,30	DDR4_COMP_CK_N	19,29,30
DDR4_COMP_CKE	19,29,30	DDR4_COMP_ALERT_N	19,29,30
DDR4_COMP_TEN	29,30		
DDR4_COMP_BG1	19,29,30		



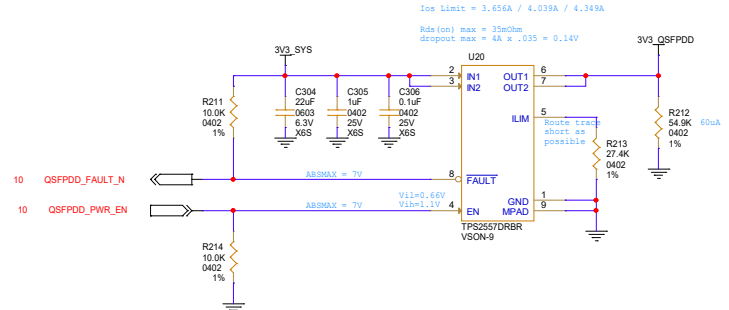
# DDR4 COMPONENT #3/#4



# DDR4 COMPONENT #5 & Termination







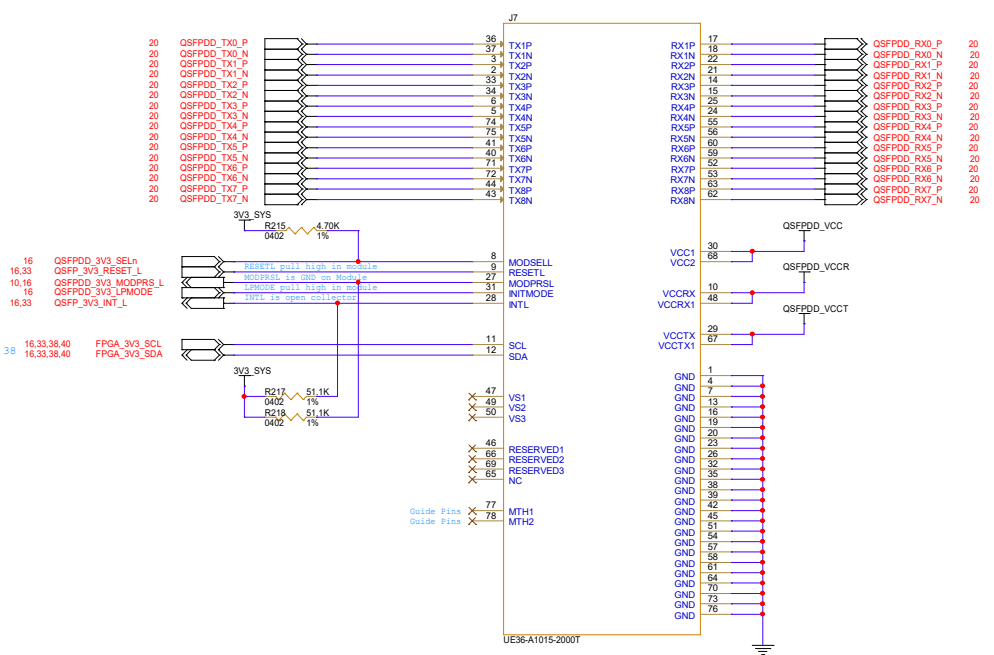
$$I_{OSmax}(mA) = \frac{99038V}{R_{ILIM} \cdot 0.947k\Omega}$$

$$I_{OSnom}(mA) = \frac{111704V}{R_{ILIM} \cdot 1.0026k\Omega}$$

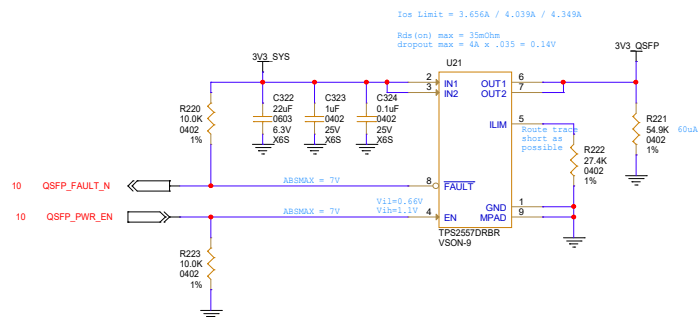
$$I_{OSmin}(mA) = \frac{127981V}{R_{ILIM} \cdot 1.0708k\Omega}$$

## QSFPDD-56

- NOTE 1: Bypass Capacitors should be placed as close to the associated 20-pin connector as possible.
- NOTE 2: zQSFP 100-ohm termination is implemented via the FPGA on-chip termination.
- NOTE 3: DC blocking capacitors are in the module for RX and TX.
- NOTE 4: 1uH inductors should have a DC Resistance of less than 0.1-ohm.







$$I_{OSmax}(mA) = \frac{99038V}{R_{ILIM} \cdot 0.947k\Omega}$$

$$I_{OSnom}(mA) = \frac{111704V}{R_{ILIM} \cdot 1.0028k\Omega}$$

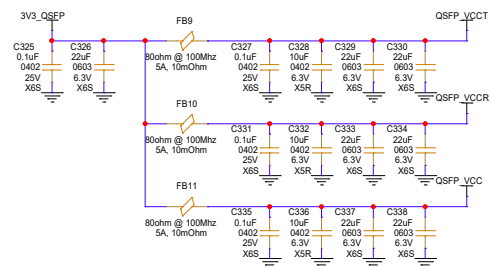
$$I_{OSmin}(mA) = \frac{127981V}{R_{ILIM} \cdot 1.0708k\Omega}$$

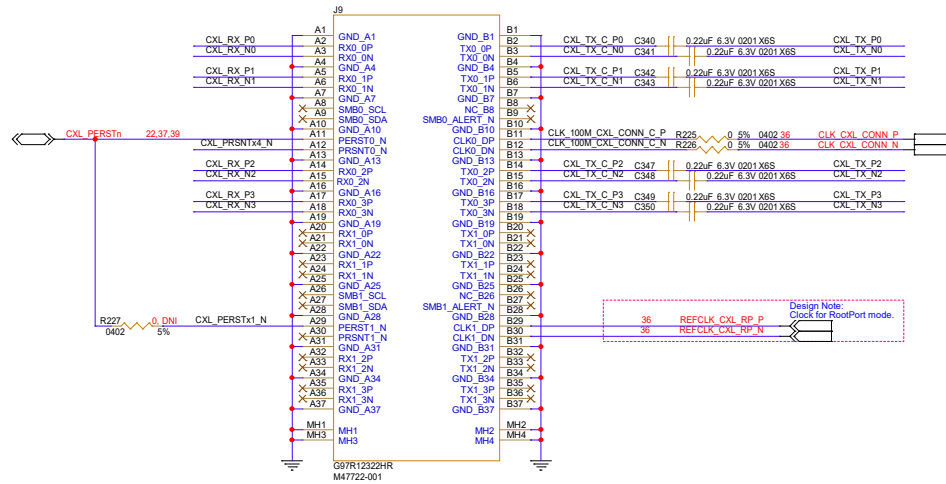
NOTE 1: Bypass Capacitors should be placed as close to the associated 20-pin connector as possible.

NOTE 2: zQSFP 100-ohm termination is implemented via the FPGA on-chip termination.

NOTE 3: DC blocking capacitors are in the module for RX and TX.

NOTE 4: 1uH inductors should have a DC Resistance of less than 0.1-ohm.



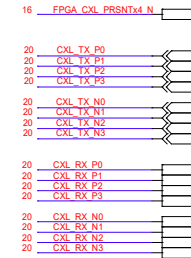
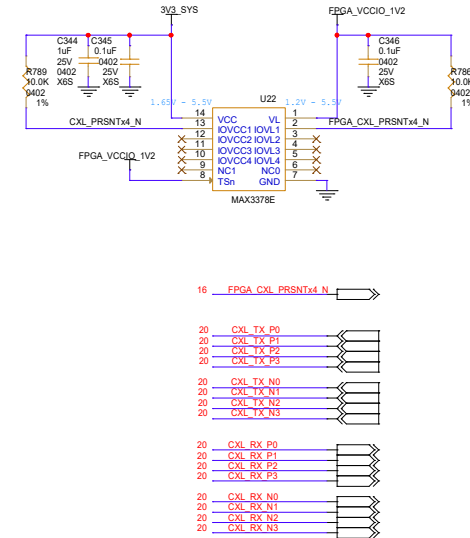


CXL Interface is designed to support the FM85 Devkit M.2 Daughter Card (M-Key for PCIe4 and SATA). When connecting to this card, FM86 Devkit CXL channels will be connected to M.2 channels 8-11 (J5) on the daughter card. PCIe\_100M\_ROOT0\_P/N clock must be selected as the default PCIe clock on the M.2 Daughter Card.

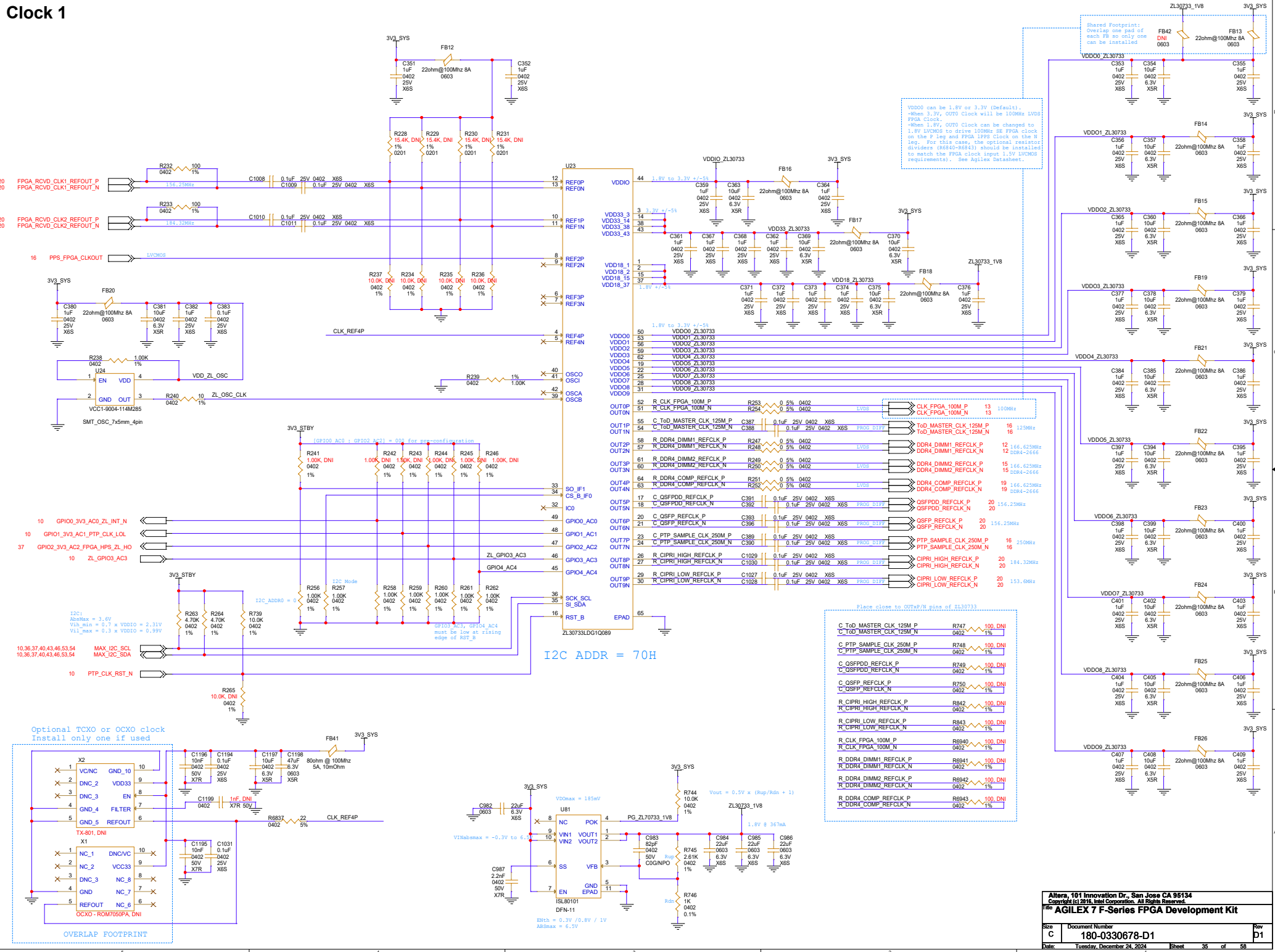
For FM86 Devkit to FM86 Devkit communication using PCIe4 over CXL with one devkit configured as the RP and the other as the EP, you must use the local PCIe CLK from U25 (REFCLK\_CXL\_RP\_P/N) for each board

I2C is not supported.

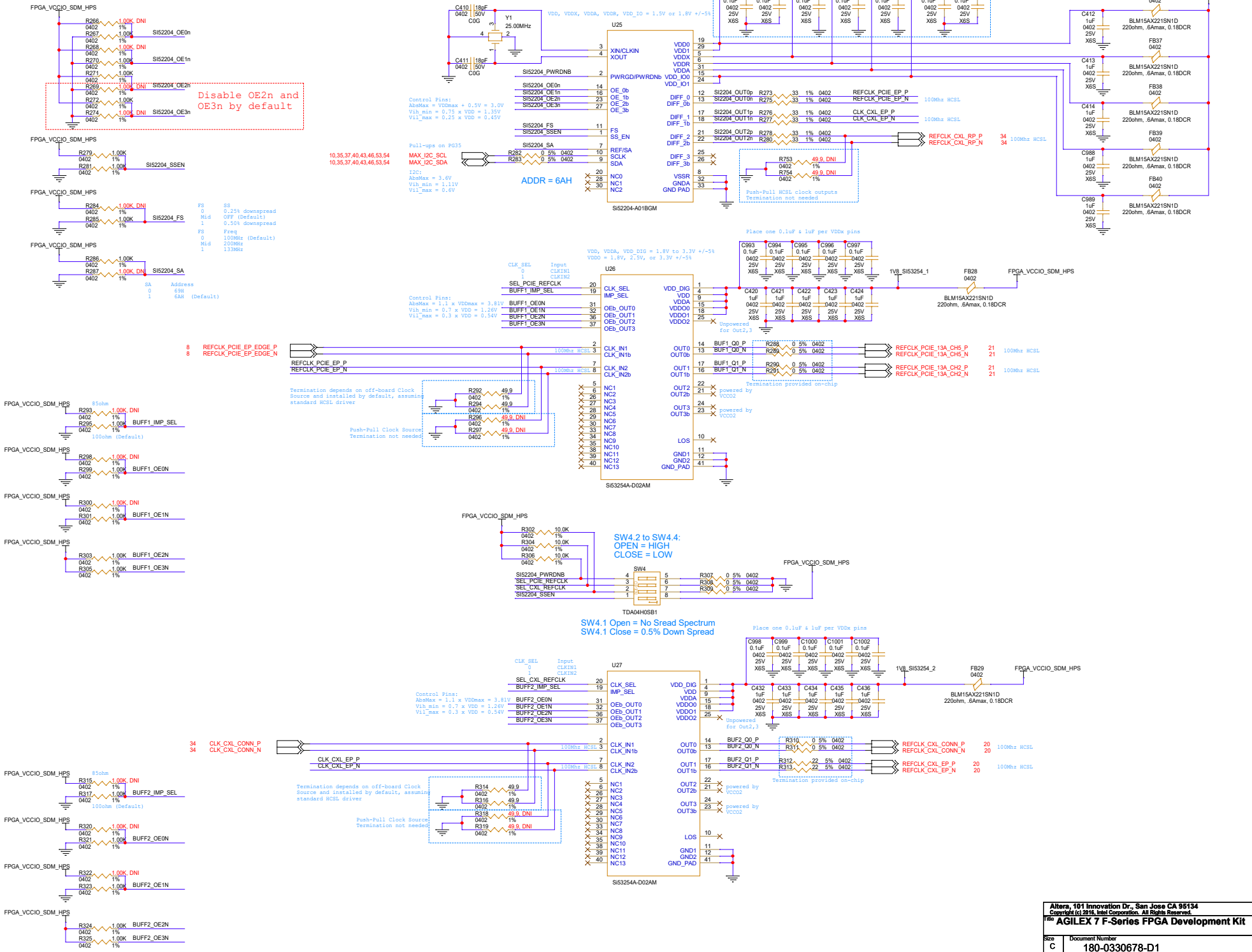
## CXL Connector

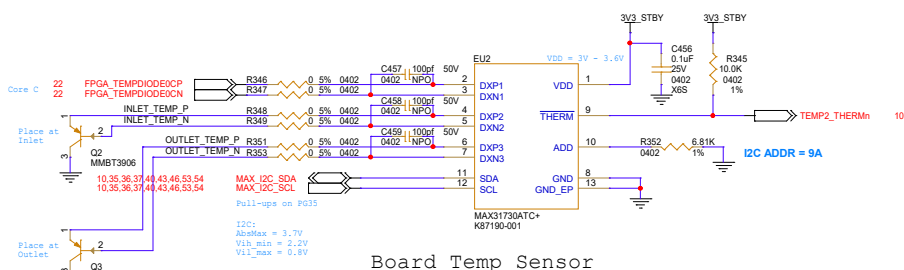
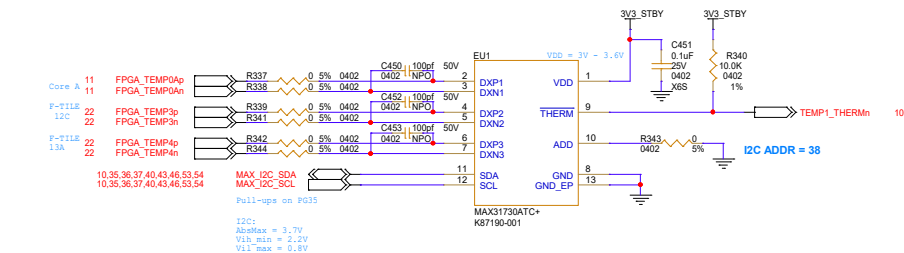
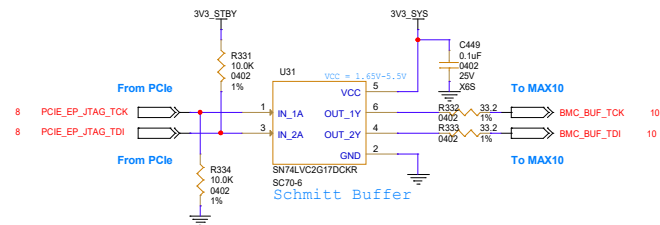
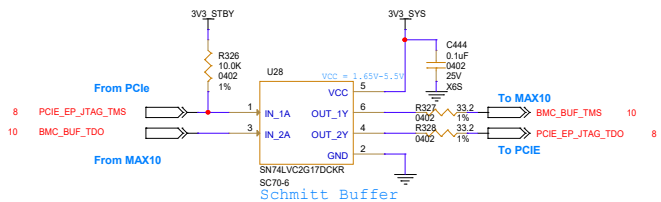


## Clock 1

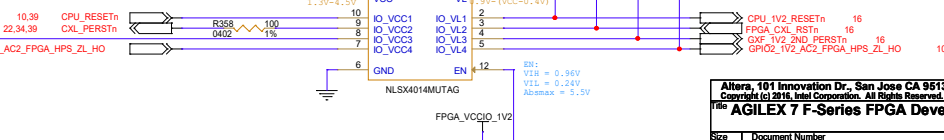
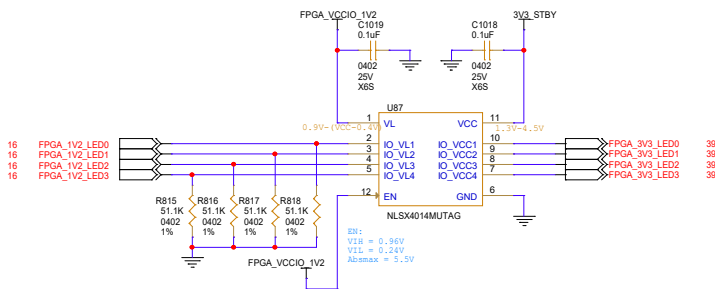
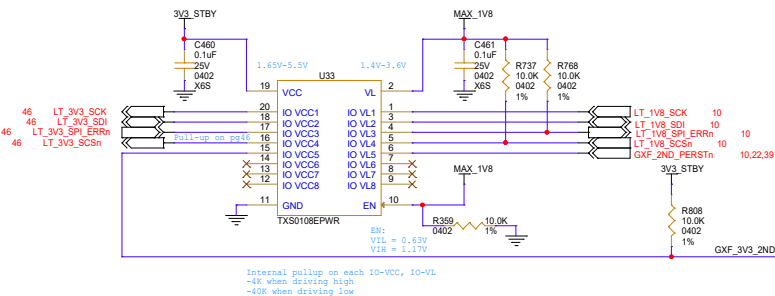


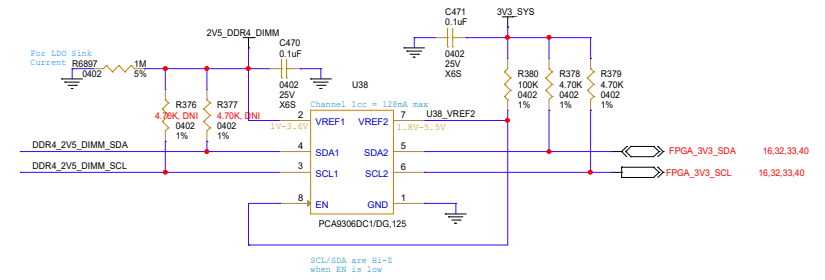
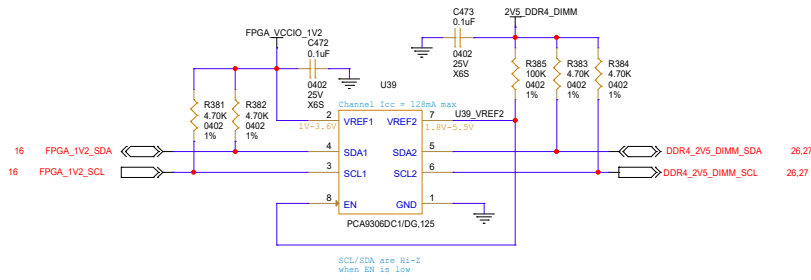
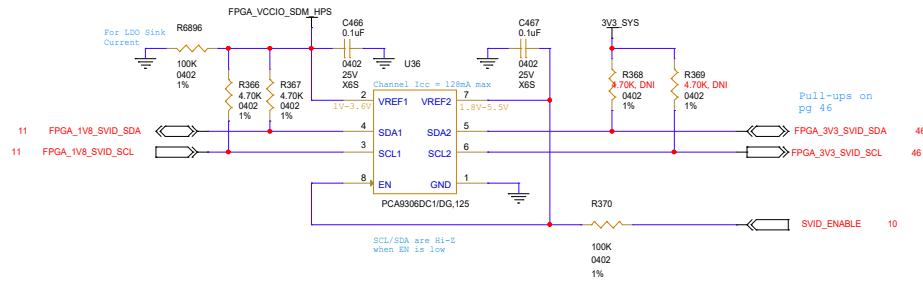
# Clock 2





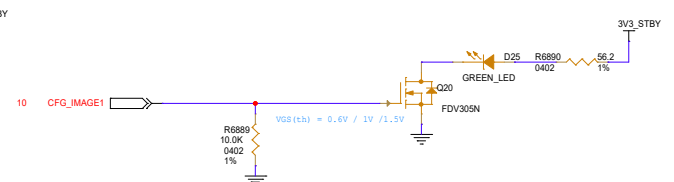
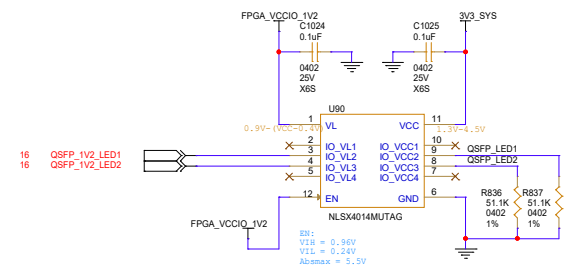
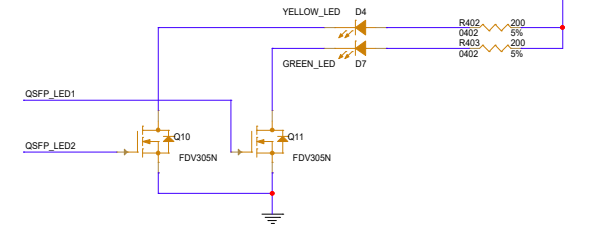
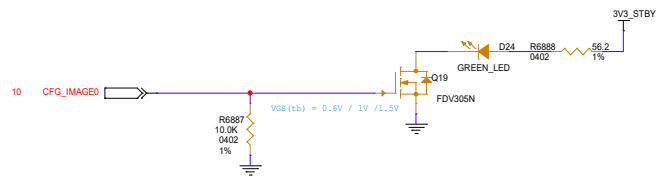
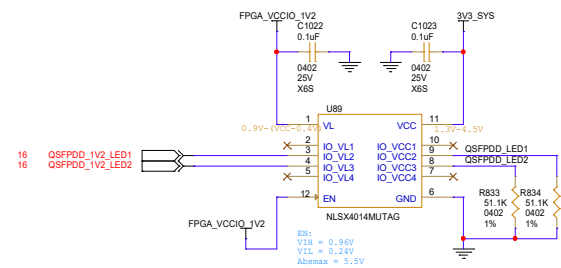
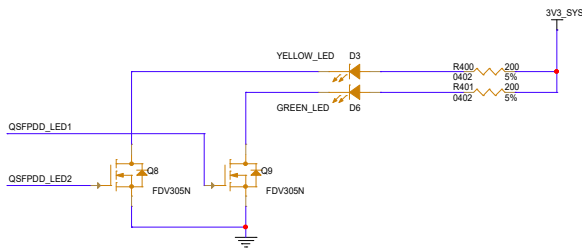
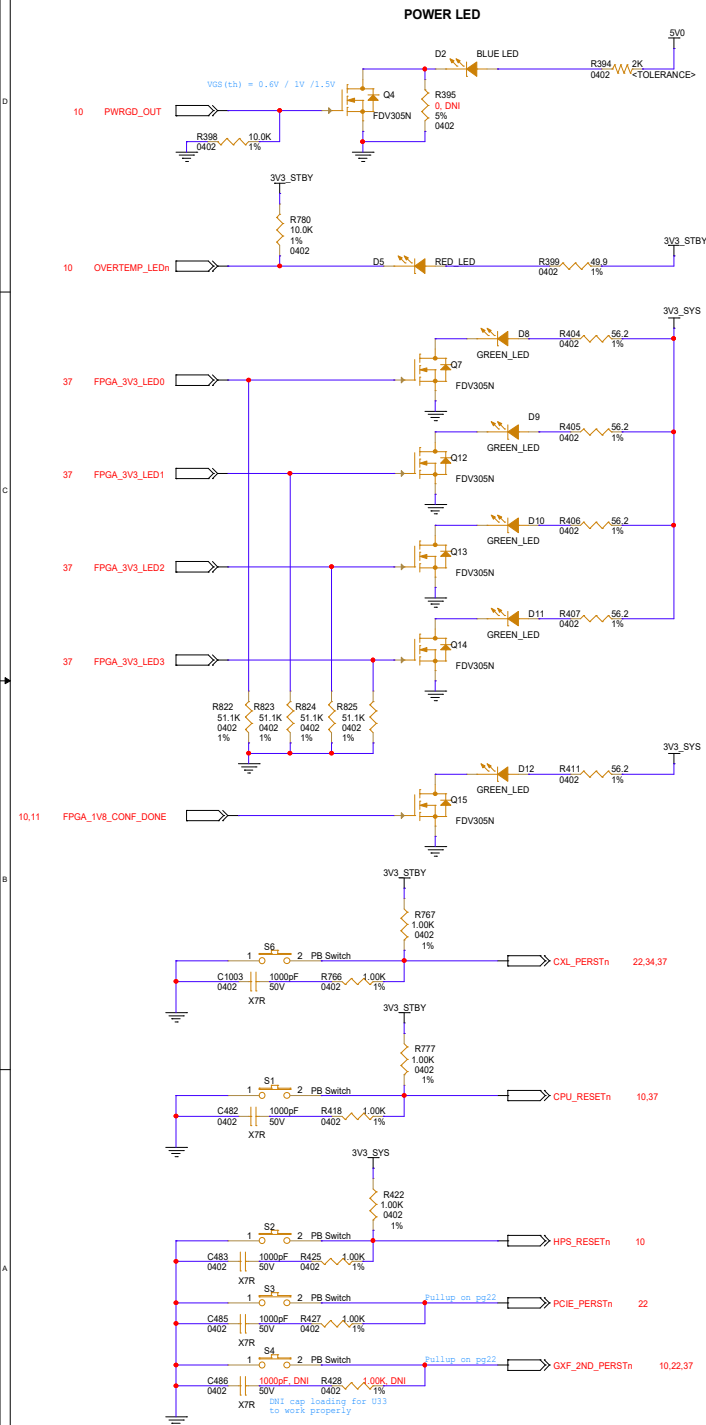
Board Temp Sensor



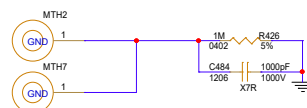




## LEDs And PushButtons



Large Mounting holes on the rear of board



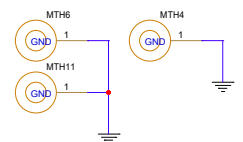
Large Mounting holes on the front of board

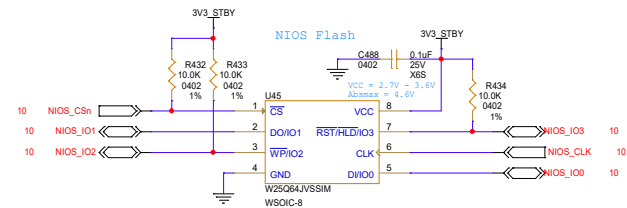
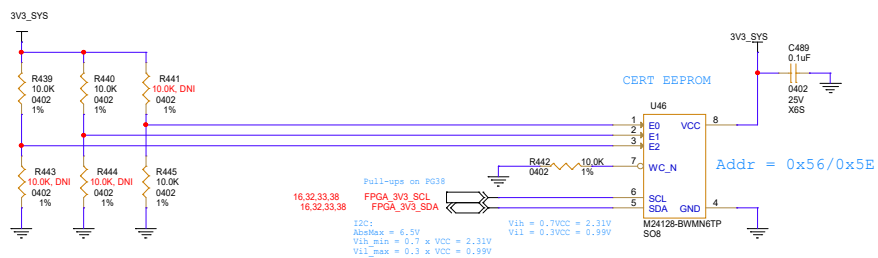
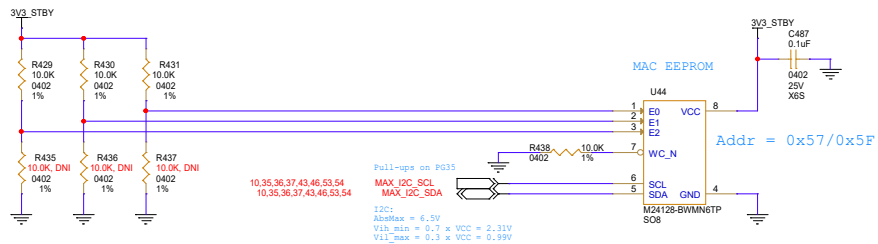


Large Mounting holes for heatsink

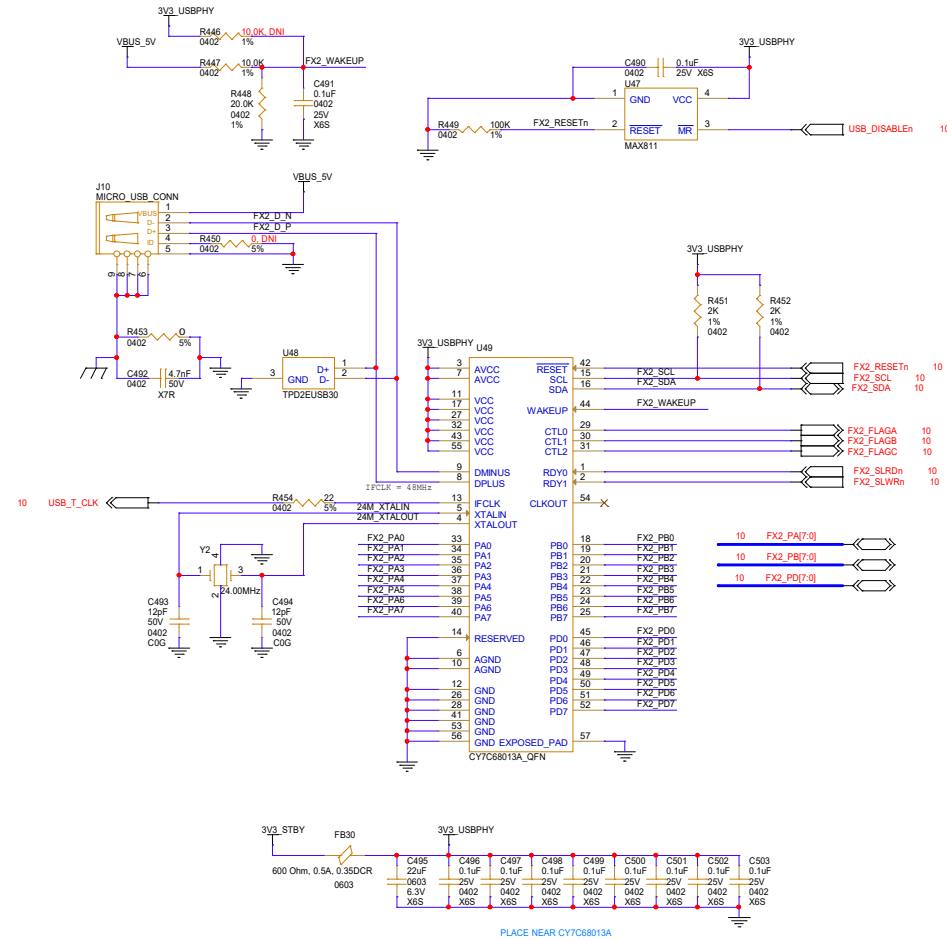


Large Mounting holes for IO48 Daughter Card





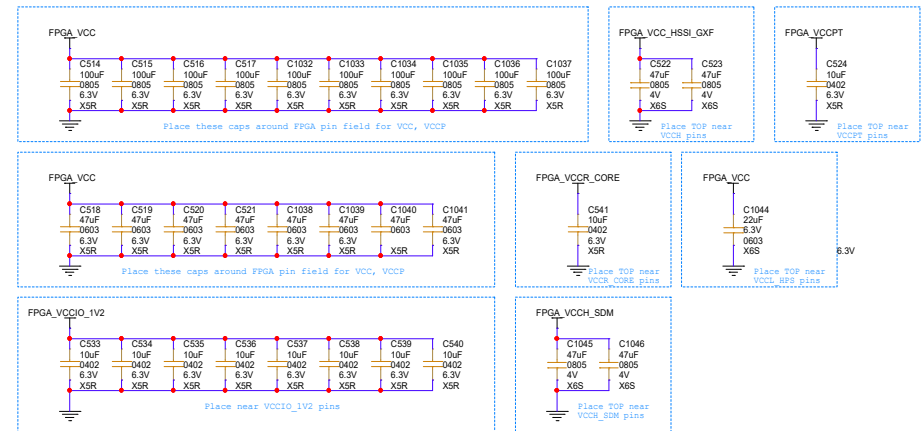
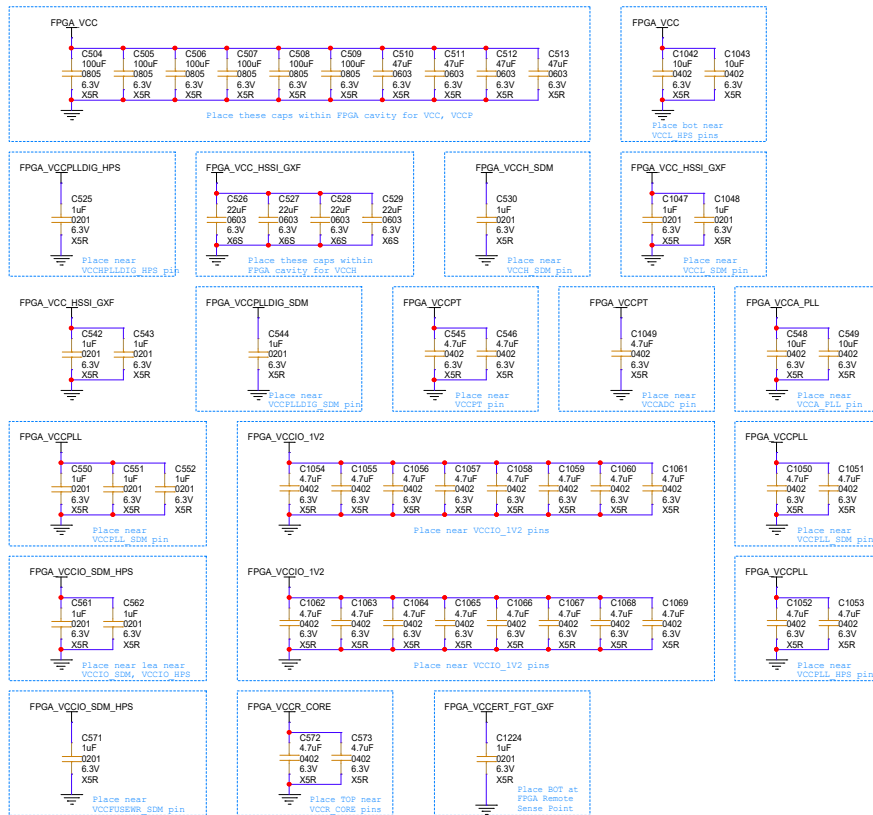
## USB-BlasterII Phy



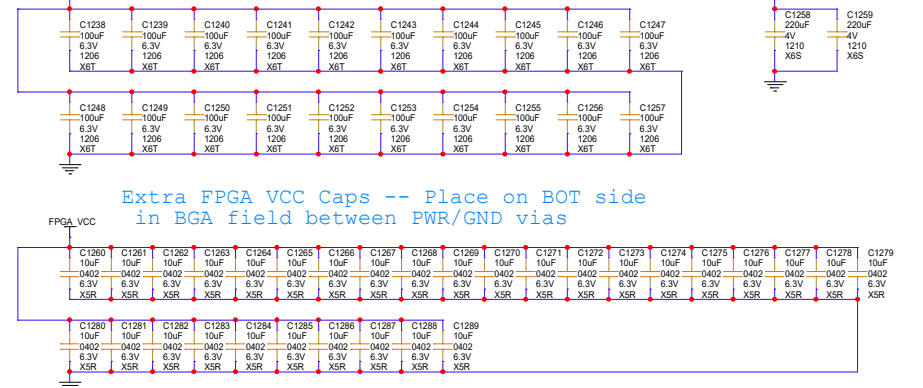
## FPGA Core Decoupling

Place on TOP Side

Place on BOT Side



Extra FPGA VCC Caps -- Place on BOT side  
periphery, 2-GND vias each cap gnd pad minimum

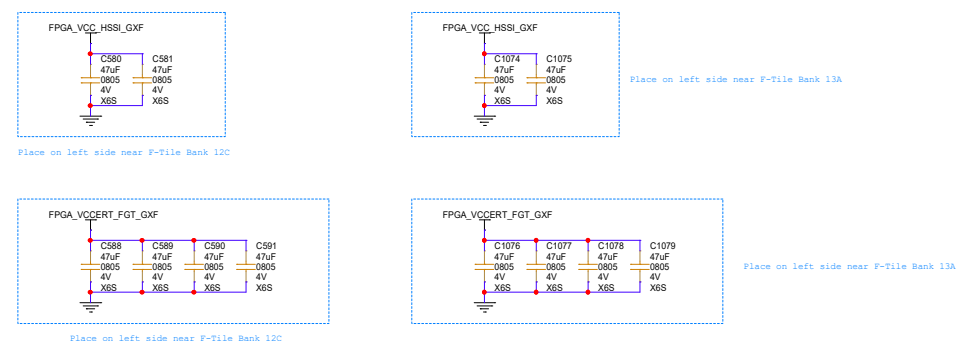
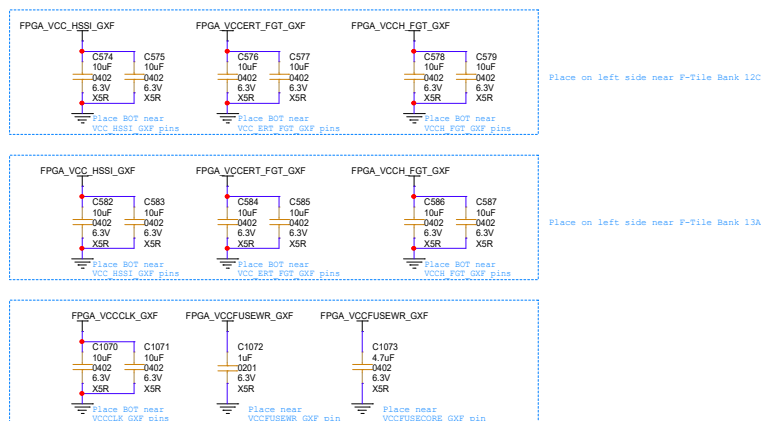


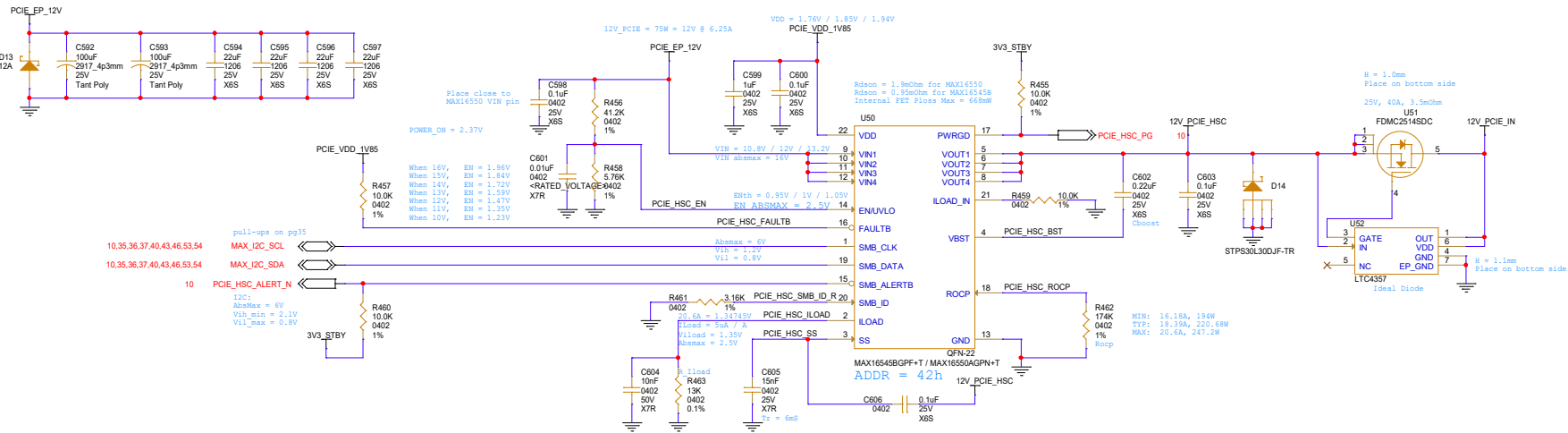
Extra FPGA VCC Caps -- Place on BOT side  
in BGA field between PWR/GND vias

## FPGA F-Tile Decoupling

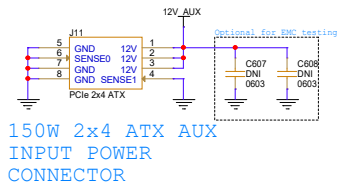
Place on TOP Side

Place on BOT Side



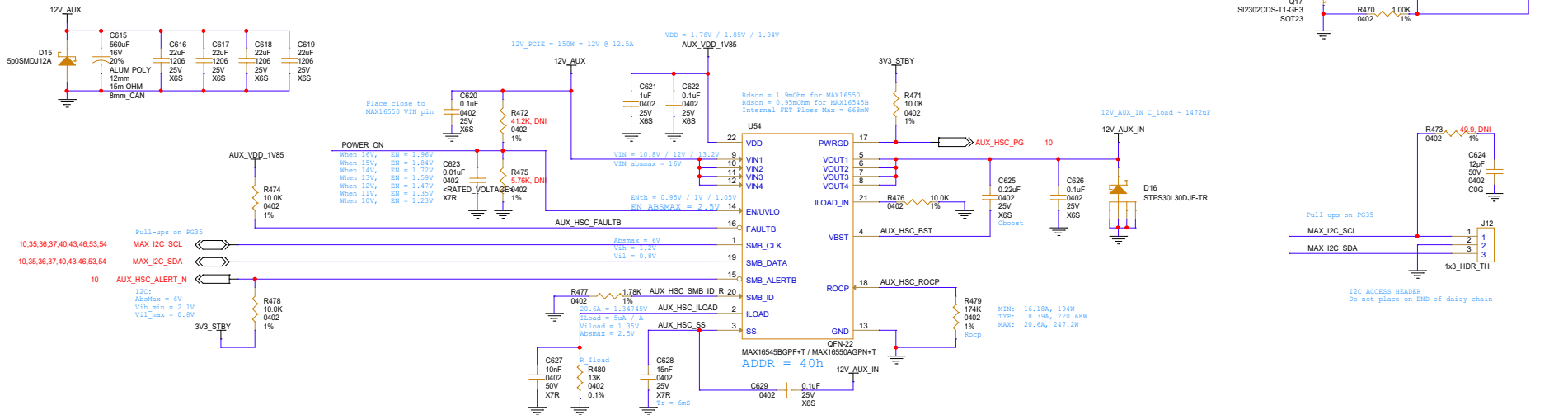


## Power On Switch



-When 12V PCIe slot power and 12V AUX power is provided (Add-in Card Mode), ON switch has no function.

-When No 12V PCIe slot power is available (Bench Mode), ON switch is used to power the board on/off.



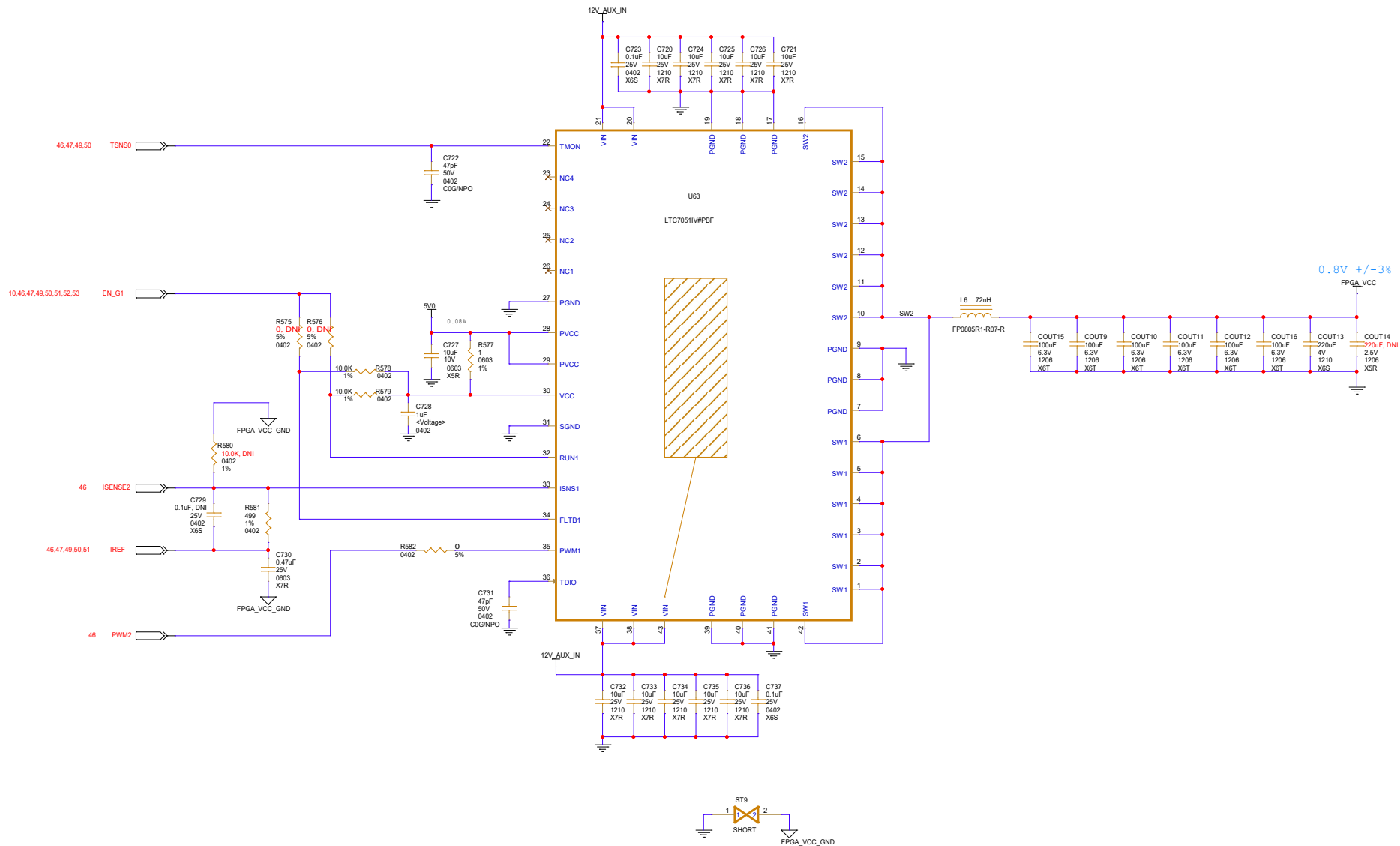


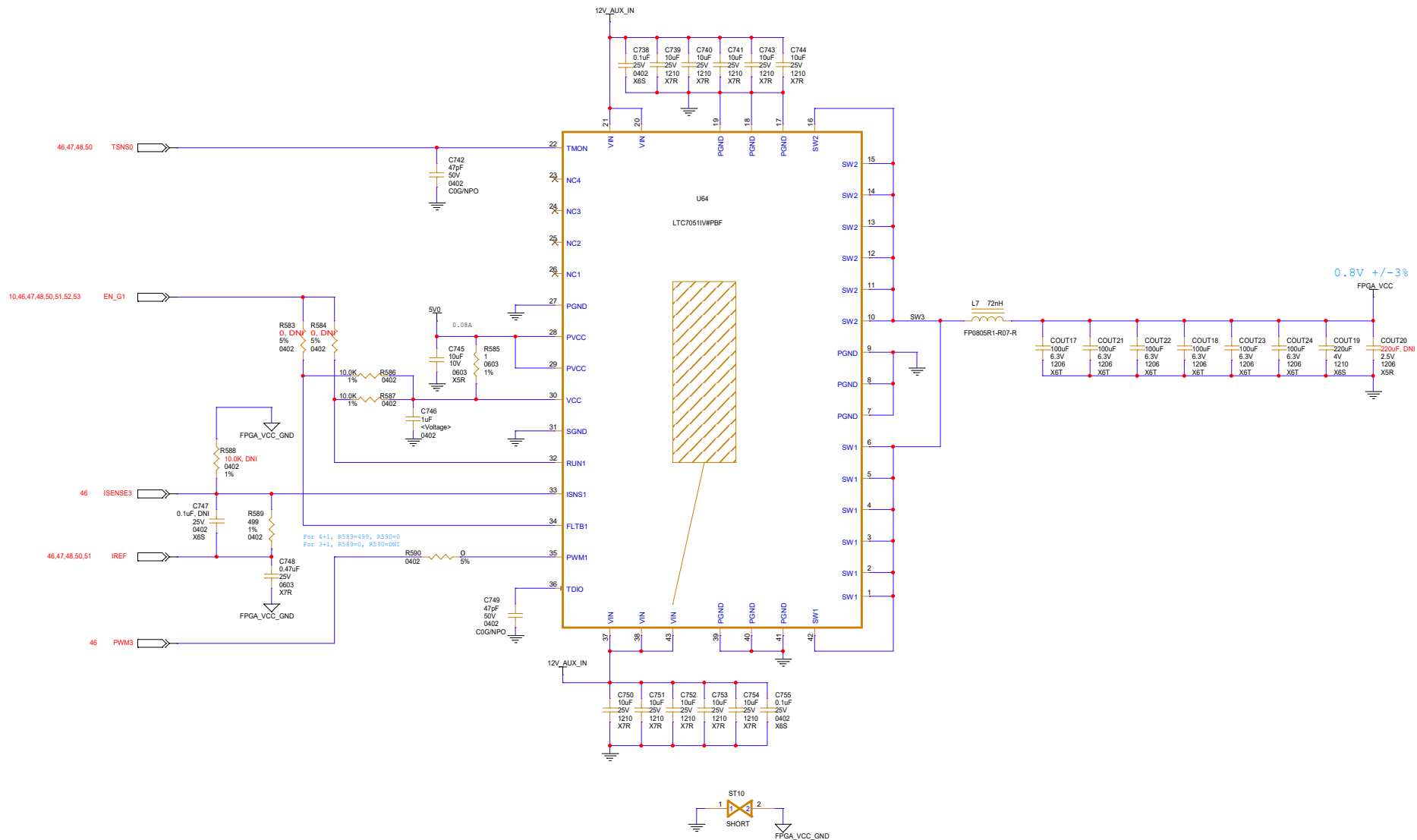


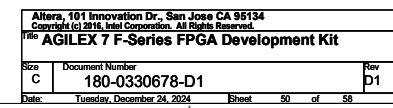




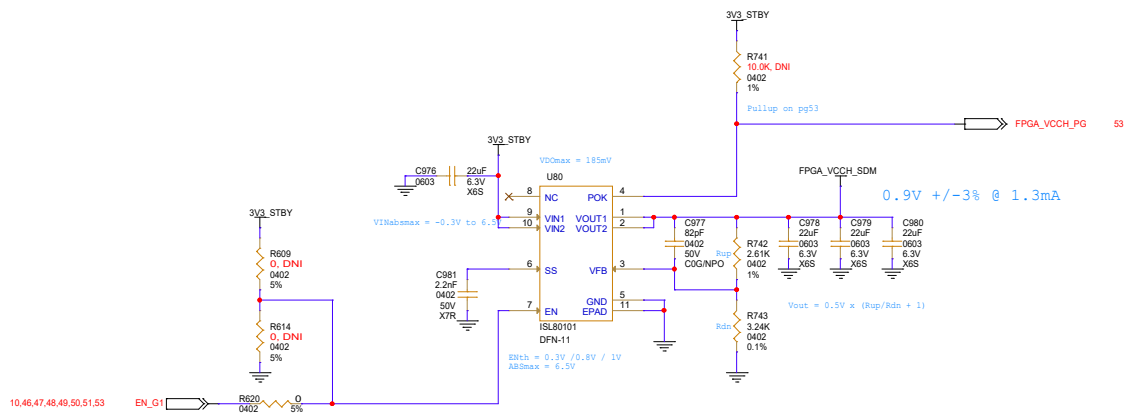




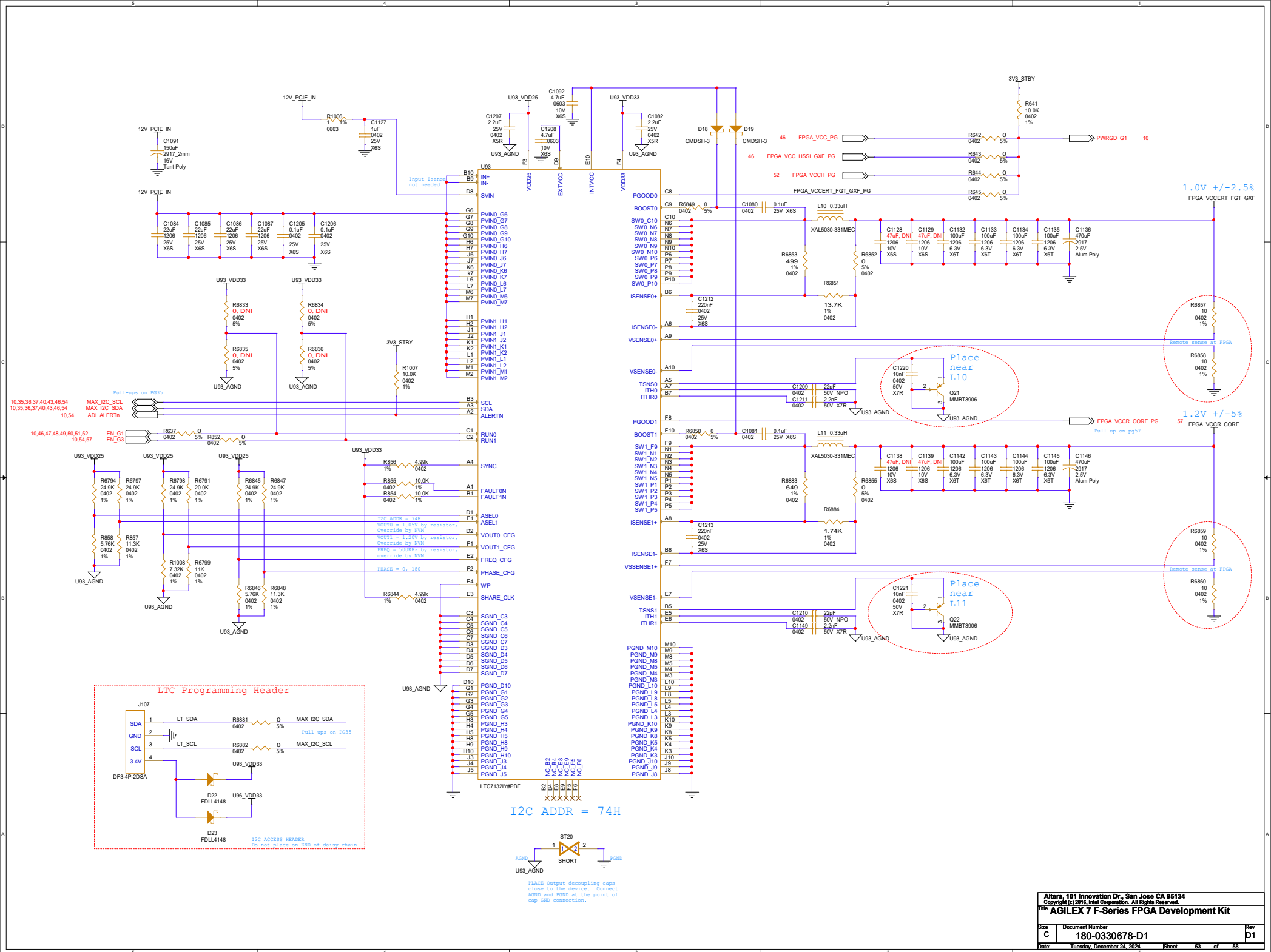


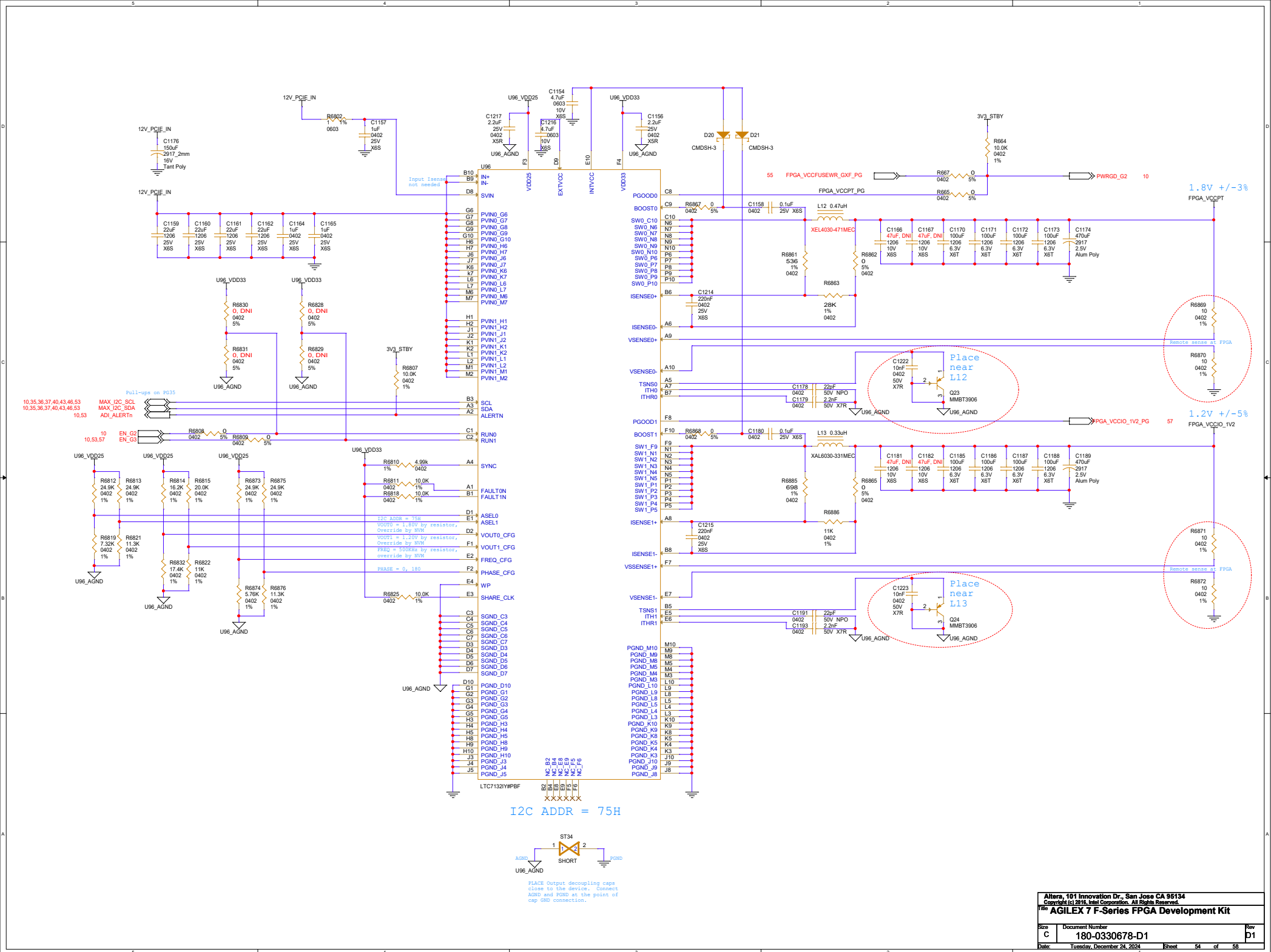


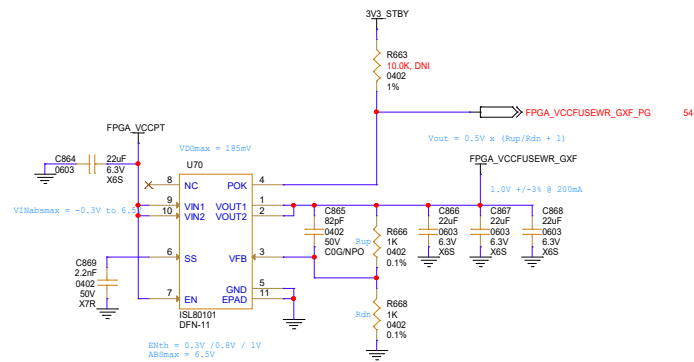












# VCCBAT Circuit intended for FM76 Device with Crypto Support

