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DWG NO. 100-0330678-C1 | REV C1

NOTES:(UNLESS OTHERWISE SPECIFIED)

1. MATERIALS: MEG*6.
2. THIS DRAWING ALSO EXISTS ON ELECTRONIC MEDIA.
3. FABRICATE PWB PER IPC-6012 CLASS 2 (LATEST REVISION).
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M.
5. BOARD MUST BE UL 94V-0 APPROVED.
6. BREAKOUT IN THE REGION OF THE TRACE/PAD JUNCTION SHALL NOT REDUCE THE TRACE WIDTH BY MORE THAN 25% UNLESS OTHERWISE SPECIFIED.
7. COPPER IN HOLES SHALL BE PER I PC - 6012(LATEST REVISION), CLASS 2.
8. MAXIMUM BOARD WARPAGE IN ANY DIRECTION TO BE .0075'/INCH, AS MEASURED BY IPC-TM-650 TEST METHOD 2.4.22.
9. VENDOR MARKING: VENDOR LOGO, UL MARKING AND DATECODE (4DIGIT WWYY)TO BE IN ETCH ON SECONDARY (BOTTOM) SIDE AWAY FROM ALL BOARD FEATURES.
10. FEATURE SIZE TOLERANCE: PLATED THRU HOLE PADS, INTERNAL PLANE CLEARANCES (ANTIPADS) AND SURFACE MOUNT LAND PATTERNS SHALL BE +/- 10% OF THEIR CAD DIMENSION WITH THE FOLLOWING EXCEPTION. ANY SMT LAND PATTERNS THAT HAVE A FINISHED PAD WIDTH OR DIAMETER LESS THAN OR EQUAL TO .012' MUST USE THE FOLLOWING TOLERANCE, +/-.001'. PCB VENDOR TO ADJUST ARTWORK TO COMPENSATE FOR ETCH PROCESS. NOTE: THIS APPLIES TO ETCH SIZES BEFORE SOLDERMASK. FURTHERMORE, FOR ETCH COMPENSATION, ONLY MINIMAL AMOUNT IS ALLOWED. NO GEOMETRIES MAY BE ENLARGED FOR YIELD PURPOSES. FINISHED PRODUCT MUST MATCH INTEL CAD DATA AS CLOSE AS POSSIBLE.
11. FEATURE LOCATION TOLERANCE: ALL CONDUCTIVE FEATURES SHALL BE WITHIN .008' DIAMETER TRUE POSITION REGARDLESS OF FEATURE SIZE (RFS).
12. HOLE LOCATION TOLERANCE: PLATED THRU HOLES SHALL BE WITHIN .003' DIAMETER TRUE POSITION AT MAXIMUM MATERIAL CONDITION (MMC). NON-PLATED HOLES <.200" SHALL BE WITHIN .003' DIAMETER TRUE POSITION WITH RESPECT TO 0,0 DATUM. NON-PLATED HOLES >.200 SHALL BE WITHIN .003' DIAMETER TRUE POSITION WITH RESPECT TO DATUM.
13. SILKSCREEN BOTH SIDES USING NON - CONDUCTIVE INK. COLOR: WHITE. NO SILKSCREEN SHALL BE ON ANY EXPOSED COPPER PAD. TRIMMING ALLOWED EVEN IF IMPACT TO LEGIBILITY.
14. REMOVE ALL UNUSED PADS FROM INNER LAYERS.
15. IMPEDANCE TO BE VERIFIED PER TABLE. IMPEDANCE COUPONS MUST REFLECT EACH CONTROLLED IMPEDANCE FOR EACH LAYER. MEASUREMENTS MUST BE PERFORMED BY TDR. IMPEDANCE REPORTING MUST SPECIFY EACH CONTROLLED IMPEDANCE GEOMETRY BY LAYER. FULL AND ACCURATE REPORTING AND COUPONS MUST BE PROVIDED WITH BOARDS. RECORDS MUST BE MAINTAINED BY SUPPLIER FOR REFERENCE BY DESIGN TEAM AS REQUIRED. REPORTS PER LOT INFORMATION PER DATE CODE MUST BE AVAILABLE UPON REQUEST.
16. SURFACE FINISH: ENIG (ENTHONE HT PLUS,FORMOCHEM F35,SHIKOKU F2 (LX) PLUX THICKNESS SHALL BE 0.25 TO 0.50 MICRON).
17. VIAS THAT ARE MASKED OVER BY DESIGN ARE PLUGGED, 30% TO 90%. VIAS WITH SOLDERMASK OPENINGS ON TOP SIDE ARE BY DESIGN AND REMAIN OPEN. EXCEPTION IS NOTE 23
18. SOLDERMASK BOTH SIDES, USING GREEN MATTE OR GLOSS SOLDERMASK PER I PC-SM-840. SOLDERMASK PADS SHALL BE ENLARGED BY .004" OVERALL OR .002' PER SIDE INCLUDING SOLDERMASK DEFINED PADS. SOLDERMASK DEFINED PADS SHALL STRICTLY FOLLOW .002' OVERSIZE PER SIDE. NOTE 22 IS THE EXCEPTION. NO CHANGE ALLOWED WITHOUT INTEL APPROVAL.

(USE FOR OSP ONLY)

19. VIA PLUGGING REQUIREMENTS FOR TEST PAD VIA (EXCEPTION IS NOTE 23):
    THE VIAS THAT ARE USED AS TEST PADS ARE REQUIRED TO BE PLUGGED ON THE SIDE THAT IS OPPOSITE TO THE TEST PADS. THE PLUGGED MATERIAL HAS TO BE FILLED AT LEAST 40% AND NO MORE THAN 90% OF THE VIA HEIGHT MEASURED FROM THE SIDE OPPOSITE TO THE TEST PADS. IT IS REQUIRED THAT AIR SHALL NOT FLOW THROUGH FROM ONE END OF THE TEST PAD VIA TO THE OTHER. THERE IS NO CONTINUOUS AIR GAP FROM ONE END TO THE OTHER END OF THE VIA. THEY ARE REQUIRED TO BE STUFFED 3 TIMES AS FOLLOWS:
    a. STUFF SOLDERMASK INTO THE VIAS FROM THE SIDE OPPOSITE THE TEST PADS.
    b. SEAL THE VIAS USING SOLDERMASK ON THE SIDE OPPOSITE OF THE TEST PADS.
    c. SEAL THE VIAS USING SOLDERMASK ON THE TEST PAD SIDE.
    d. MAKE SURE THE SOLDERMASK IS TOTALLY CLEANED FROM ALL TEST PADS DURING THE SOLDERMASK CLEANING PROCESS.

(IMPEDANCES SUBJECT TO CHANGE PER PROJECT REQUIREMENTS)

20. REQUIRED REPORT OF PRODUCTION BOARDS:
    EVERY 3 OR LESS LOTS AND 5000 OR LESS BOARDS, THE FOLLOWING TESTS ARE REQUIRED BEFORE THE BOARDS ARE SHIPPED OUT. A COPY OF THE REPORT AND IMPEDANCE COUPON TO BE SENT TO THE ENGINEER INVOLVED.
    a. MEASURE THE FOLLOWING IMPEDANCES OF 30 RANDOMLY PICKED BOARDS:
       i. SEE IMEPACNE TABLE FOR REQUIRED IMPEDANCES AND LAYERS TO BE MEASURED.
    b. MEASURE THE Tg OF A PIECE OF MATERIAL FROM THE BOARD PANEL. THE Tg VALUE HAS TO BE GREATER THAN .145.
    c. CROSS SECTION A TEST PAD VIA FROM EACH CORNER OF ONE PCB (4 TEST PADS VIAS TOTAL). THEY HAVE TO BE PICKED FROM TEST PAD VIAS THAT ARE CLOSE TO EACH CORNER. PICTURES OF THE CROSS SECTION SHOWING THE STUFFING ARE REQUIRED IN THE REPORT. MEASURE THE PERCENTAGE OF THE STUFFING IN THE PLUGGED VIAS, COPPER FOIL + PLATING THICKNESS (TOP TO BOTTOM), COPPER PLATING THICKNESS IN HOLE (6 LOCATIONS - 2 TOPS, 2 MIDDLES AND 2 BOTTOMS), DIELECTRIC THICKNESS (CENTER AND CORNER), TRACE PROPERTY (TOP WIDTH, BANDWIDTH AND THICKNESS), AND BOARD THICKNESS (WITHOUT SOLDERMASK).
    d. MEASURE ALSO THE FOLLOWING ITEMS FROM ONE BOARD:
       i. OSP THICKNESS
       ii. BOW AND TWIST (MAX AND MIN)
       iii PEEL STRENGTH
       iv. CLEANLINESS TEST
       v. SOLDERABILITY
       vi. THERMAL STRESS
       vii. THE DIMENSIONS OF ONE OF EVERY KIND OF HOLE
       viii. THE OUTER DIMENSIONS OF THE BOARD

21. EDGE CONNECTOR FINGERS:REQUIRE 30 MICRO INCHES HARD GOLD OVER 150-200 MICRO INCHES OF NICKEL.
22. ~~FOR BGA "U2", ALL EXPOSED COPPER PADS, WHETHER SMD OR NSMD, MUST HAVE A 20 MILS PAD DIAMETER, THEY ALL MUST BE EQUAL.~~
23. FILL ALL 8MIL, 10MIL AND 12MIL DRILL HOLES USING NON - CONDUCTIVE EPOXY AND OVERPLATE WITH COPPER (VIPPO).
24. PLEASE ADD TEAR DROPS TO OUTER AND INNER LAYERS.
25. ADD COPPER THIEVING WHERE NECESSARY, AND MAINTAIN A CLEARANCES OF 35 MILS TO ALL NETS.
26. ~~REMOVE THE THROUGH HOLE VIA PAD ON BOTTOM LAYER FOR THE PCIE GEN5 TO EDGE FINGER, CXL TO MCIO CONNECTOR AND QSFP-DD SIGNALS ROUTED ON LAYER16.~~
27. IN EDGE FINGER REGION, SOME RESIDUAL METAL FROM THE PLATING TIE BAR IS PERMITTED TO EXTEND NO MORE THAN 0.13 MM BEYOND THE BOTTOM OF THE EDGE FINGERS, INTO THE METAL EXCLUSION REGION (BETWEEN THE EDGE FINGER AND CHAMFER REGION). "ETCH BACK" PROCESS MAYBE REQUIRED TO DO THIS.

DRILL CHART: TOP to L02_GND1 (ALL UNITS ARE IN MILS)

FIGURE	FINISHED_SIZE	TOLERANCE_DRILL	PLATED	QTY
•	10.0	+0.0/-10.0	PLATED	17

DRILL CHART: TOP to L03_SIG1 (ALL UNITS ARE IN MILS)

FIGURE	FINISHED_SIZE	TOLERANCE_DRILL	PLATED	QTY
•	10.0	+0.0/-10.0	PLATED	210

IMPEDANCE TABLE (SEE SPECIAL NOTE)

Impedance / Layer	42.5 OHM (MILS)	45 OHM (MILS)	85 OHMS Width/SP (MILS)	85 OHMS Width/SP (MILS)	90 OHMS Width/SP (MILS)	85 OHMS NECKDOWN Width/SP	90 OHMS NECKDOWN Width/SP
1	6.70	5.85	4.55/4.95		4.00/5.00		
3	~~3.60~~	3.20	3.35/4.65	3.20/4.00	3.10/5.90	3.00/4.00	3.20/4.50
5	~~3.60~~	3.20	~~3.35/4.65~~	3.20/4.00	3.10/5.90	3.00/4.00	3.20/4.50
7	~~3.80~~	3.50	~~3.55/4.45~~	3.50/4.00	3.35/5.65	3.00/4.00	3.20/4.50
12	~~3.80~~	3.50	~~3.55/4.45~~	3.50/4.00	~~3.35/5.65~~	3.00/4.00	~~3.20/4.50~~
14	~~3.60~~	3.20	~~3.35/4.65~~	3.20/4.00	3.10/5.90	3.00/4.00	3.20/4.50
16	~~3.60~~	3.20	3.35/4.65	3.20/4.00	3.10/5.90	3.00/4.00	3.20/4.50
18	6.70	5.85	4.55/4.95		4.00/5.00		

*** SPECIAL NOTES***
1. INNER LAYER IMPEDANCE IS +/-7% (BOTH FOR MASS AND SAMPLE PRODUCTION)
2. OUYER LAYER IMPEDANCE IS +/-10% (BOTH FOR MASS AND SAMPLE PRODUCTION)
3. THROUGH HOLE VIA 8MILS DRILL : FINISHED HOLE WITH EPOXY AND PLATED SHUT ALMOST 6MIL
4. MICRO VIA 1-2, VIA 1-3, & 16-18, 17-18 : 10 MIL DRILL; FILLED MICRO-VIA WITH EPOXY.

DRILL CHART: L16_SIG6 to BOTTOM (ALL UNITS ARE IN MILS)

FIGURE	FINISHED_SIZE	TOLERANCE_DRILL	PLATED	QTY
•	10.0	+0.0/-10.0	PLATED	33

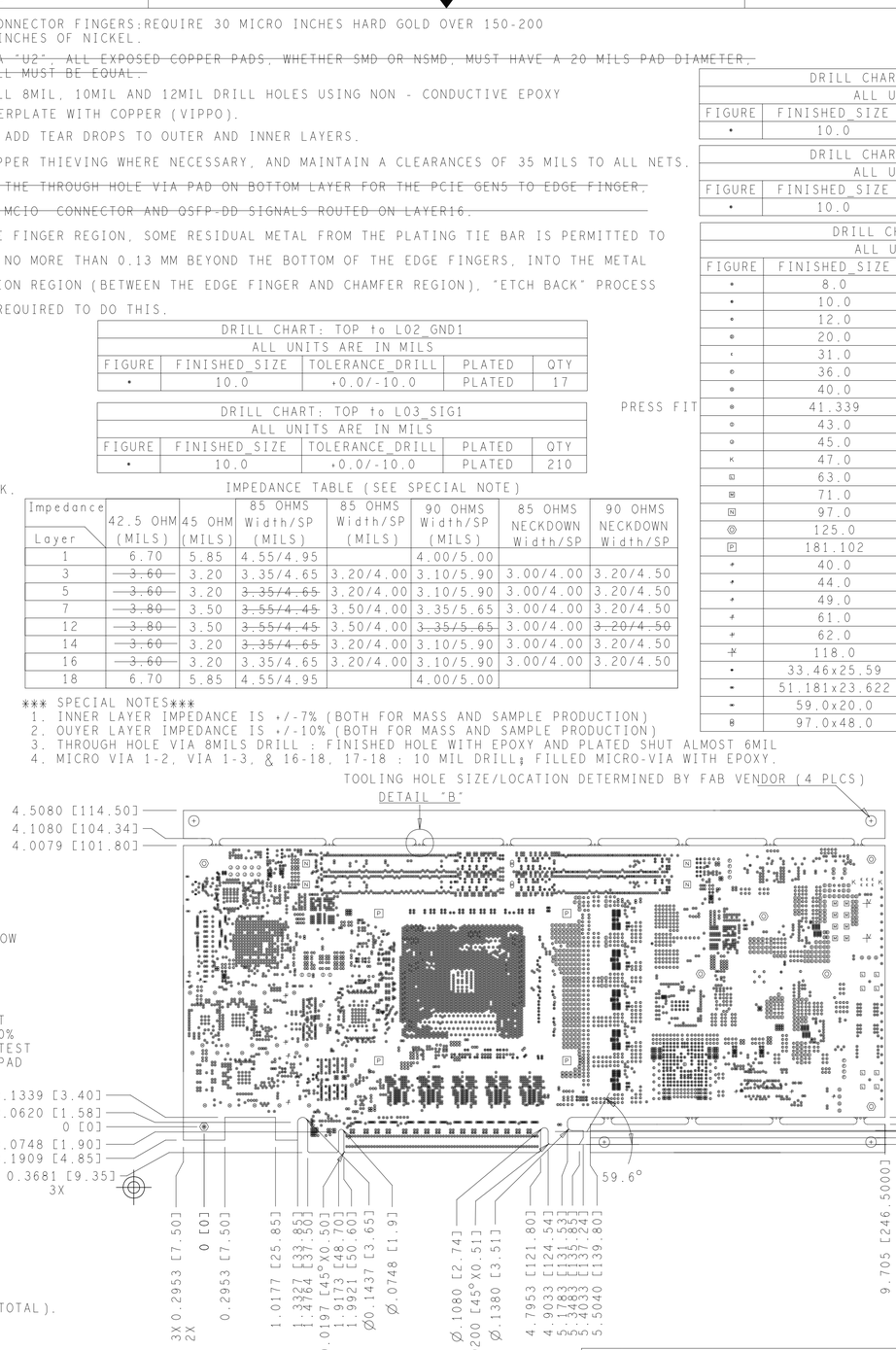
DRILL CHART: L17_GND8 to BOTTOM (ALL UNITS ARE IN MILS)

FIGURE	FINISHED_SIZE	TOLERANCE_DRILL	PLATED	QTY
•	10.0	+0.0/-10.0	PLATED	28

DRILL CHART: TOP to BOTTOM (ALL UNITS ARE IN MILS)

FIGURE	FINISHED_SIZE	TOLERANCE_DRILL	PLATED	QTY
•	8.0	+0.0/-8.0	PLATED	5823
•	10.0	+0.0/-10.0	PLATED	674
•	12.0	+0.0/-12.0	PLATED	1317
⊕	20.0	+3.0/-3.0	PLATED	375
‘	31.0	+3.0/-3.0	PLATED	6
⊕	36.0	+3.0/-3.0	PLATED	8
⊕	40.0	+3.0/-3.0	PLATED	7
⊕	41.339	+1.969/-1.969	PLATED	24
⊕	43.0	+3.0/-3.0	PLATED	4
⊕	45.0	+3.0/-3.0	PLATED	10
K	47.0	+3.0/-3.0	PLATED	2
⊡	63.0	+3.0/-3.0	PLATED	8
⊠	71.0	+3.0/-3.0	PLATED	8
N	97.0	+3.0/-3.0	PLATED	4
◎	125.0	+3.0/-3.0	PLATED	7
P	181.102	+5.0/-0.0	PLATED	4
*	40.0	+2.0/-2.0	NON-PLATED	2
*	44.0	+2.0/-2.0	NON-PLATED	2
*	49.0	+2.0/-2.0	NON-PLATED	1
*	61.0	+2.0/-2.0	NON-PLATED	2
*	62.0	+2.0/-2.0	NON-PLATED	2
X	118.0	+2.0/-2.0	NON-PLATED	2
▪	33.46x25.59	+3.0/-3.0	PLATED	2
▪	51.181x23.622	+3.0/-3.0	PLATED	2
▪	59.0x20.0	+3.0/-3.0	PLATED	4
▪	97.0x48.0	+3.0/-3.0	PLATED	2

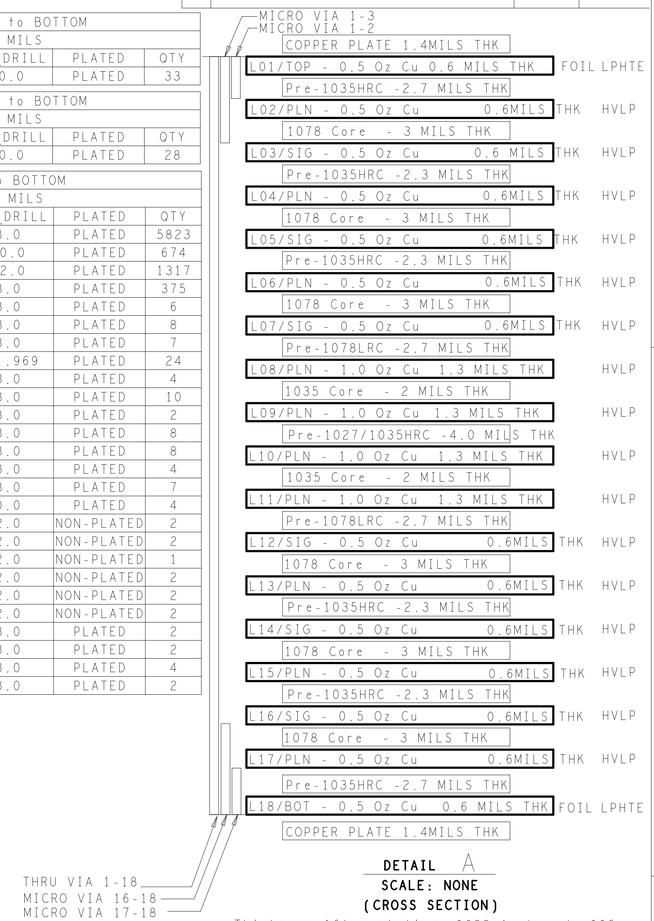
TOOLING HOLE SIZE/LOCATION DETERMINED BY FAB VENDOR (4 PLCS)



PRIMARY SIDE SHOWN

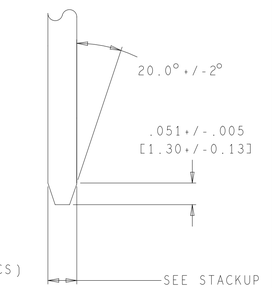
REVISIONS

REV	DESCRIPTION	DATE	APPROVED



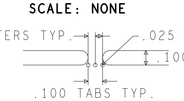
DETAIL A
SCALE: NONE
(CROSS SECTION)

Thickness After plating .0622 inch +/-.005
(not including solder mask)



CHAMFER EDGE CONNECTOR
SCALE: NONE

DETAIL B
SCALE: NONE



REV C1 DWG NO. 100-0330678-C1

			MATL	
			SPEC	
.	XX-XXX-XXXX			
DASH	NEXT ASSY	USED ON	FNSH	
APPLICATION				

THIRD ANGLE PROJECTION

TOLERANCES: DEC .X ± / DEC .XX ± .01 / DEC .XXX ± .005 / DEC .XXXX ± .002 / FRACTIONS ± / ANGLES ± 1°

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES IN ACCORDANCE WITH ANSI Y14.5. DRILL TOLERANCES ARE PER 10387

DWN	ACRONICS 04-NOV-24
CHKR	
DSGN ENGR	
RELEASE	
CONTRACT NO.	XXXXXXXX

INTEL CONFIDENTIAL

3065 BOWERS AVE
SANTA CLARA
CALIF. 95051

TITLE: PCB FABRICATION

AGILEX F-SERIES FPGA DEVKIT

SIZE	CAGE CODE	DWG NO.	REV
D	N/A	100-0330678-C1	C1

SCALE: 1/1 | SHEET 1 OF 2