# Intel Agilex® 7 F-Series FPGA (Two F-Tiles) Development Kit User Guide


Online Version


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739942

2023.08.07

# Contents

**1. Overview ..... 4**
1.1. Block Diagram ..... 4
1.2. Feature Summary ..... 5
1.3. Box Contents ..... 6
1.4. Recommended Operating Conditions ..... 6

**2. Getting Started ..... 7**
2.1. Intel Quartus® Prime Software and Driver Installation ..... 7
2.2. Design Examples ..... 7

**3. Power Up the Development Kit ..... 9**
3.1. Default Settings ..... 9
3.2. Applying Power to the Development Board ..... 10

**4. Board Test System ..... 12**
4.1. Set Up BTS GUI Running Environment ..... 13
4.1.1. Download OpenJDK ..... 13
4.1.2. Download OpenJFX ..... 13
4.1.3. Install OpenJDK and OpenJFX ..... 14
4.1.4. Install the Intel Quartus Prime Software ..... 14
4.1.5. Run BTS GUI ..... 14
4.2. Test the Functionality of the Development Kit ..... 16
4.2.1. The Bottom Info Bar ..... 16
4.2.2. The Configure Menu ..... 16
4.2.3. The Sys Info Tab ..... 17
4.2.4. The GPIO Tab ..... 18
4.2.5. The XCVR Tab ..... 19
4.2.6. The Memory Tab ..... 25
4.3. Control On-Board Clock through Clock Controller GUI ..... 28
4.4. Monitor On-Board Power Regulator through Power Monitor GUI ..... 29
4.5. BTS Test Areas ..... 30
4.6. Identify Test Pass- or Fail-based on BTS GUI Test Status ..... 30

**5. Development Kits Hardware and Configuration ..... 31**
5.1. JTAG Configuration Mode ..... 31
5.2. Active Serial (AS) x4 Configuration Mode ..... 31
5.3. Avalon-ST x16 Configuration Mode ..... 31

**6. Custom Projects for the Development Kit ..... 33**
6.1. Add SmartVID Settings in the Intel Quartus Prime QSF File ..... 33
6.2. Golden Top ..... 33

**7. Revision History ..... 34**

**A. Development Kit Components ..... 35**
A.1. Board Overview and Components ..... 35
A.1.1. Board Overview ..... 35
A.1.2. Board Components ..... 35
A.1.3. Intel MAX 10 CPLD System Controller ..... 39

A.2. FPGA Configuration....39
A.2.1. Programming the FPGA over On-Board Intel FPGA Download Cable II....40
A.2.2. Programming the FPGA over an External Intel FPGA Download Cable II....40
A.3. Default Switch and Jumper Settings....40
A.3.1. Switch Description....41
A.3.2. Jumper Description....42
A.4. Input and Output Components....43
A.4.1. Push Buttons....43
A.4.2. Switches....43
A.4.3. LEDs....44
A.5. Components and Interfaces....44
A.5.1. PCI Express (PCIe) Interface....44
A.5.2. QSFP-DD Interface....47
A.5.3. QSFP Interface....49
A.5.4. CXL Interface....50
A.5.5. DDR4 DIMM1 Interface....51
A.5.6. DDR4 DIMM2 Interface....55
A.5.7. DDR4 Component Interface....60
A.5.8. HPS I/O48 Interface....63
A.6. $I^2C$....64
A.7. Intel MAX 10 SPI Bus....66
A.8. Clock Circuits....66
A.9. HPS Daughter Card....67
A.10. System Power....69
A.11. Power Guidelines....70
A.11.1. In a Standard PCIe-Compliant System....70
A.11.2. As a Standalone Evaluation Board Powered by Included Power Supply....70
A.12. Power Distribution System....71
A.13. Power Measurement....72
A.14. Thermal Limitations and Protection....72

**B. Additional Information....73**
B.1. Safety and Regulatory Information....73
B.1.1. Safety Warnings....74
B.1.2. Safety Cautions....75
B.2. Compliance Information....78

# 1. Overview

The Intel Agilex® 7 FPGA Development Kit provides a hardware development platform for evaluating the performance and features of the Intel Agilex 7 F-Series FPGA with two F-tiles.

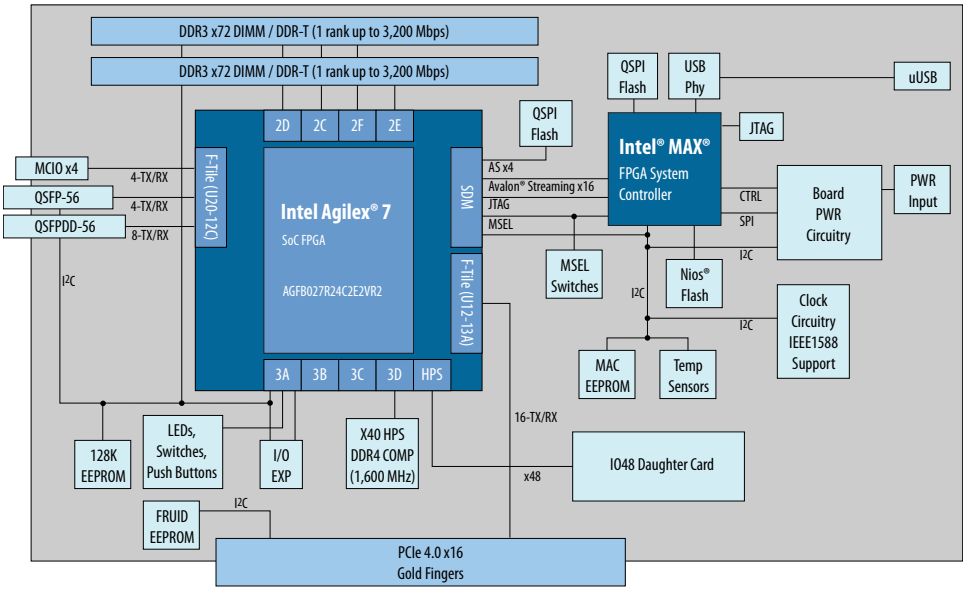
**Table 1. Ordering Information**

| Development Kit Version | Ordering Code | Device Part Number |
|---|---|---|
| Intel Agilex 7 F-Series FPGA (Two F-Tiles Edition) Development Kit (ES) | DK-DEV-AGF027F1ES | AGFB027R24C2E2VR2(1) |

For more information about the *Intel Agilex 7 ES Device Errata Sheet and User Guidelines (ES-1069)*, contact Intel® Premier Support and quote ID #15011992053.

## 1.1. Block Diagram

**Figure 1. Intel Agilex 7 F-Series FPGA (Two F-Tiles) Development Kit Block Diagram**




(1) AGFB027R24C2E2VR2 supports PCIe* x8 interface and not PCIe x16 interface.

## 1.2. Feature Summary

- Intel Agilex 7 F-Series (AGFB027) device in 2340A BGA package
  - Quad-core 64-bit Arm Cortex-A53 hard processor (HPS)
  - 0.8 V VID-adjustable VCC core
  - Dual F-tile transceivers supporting 56 Gbps (PAM4) and 32 Gbps (NRZ) data rates
  - 2.69M logic elements (LE)
  - 3.65M adaptive logic modules (ALM)
  - 8.5K digital signal processing (DSP) blocks
- FPGA configuration
  - Avalon®-ST x16 and active serial (AS) x4 configuration modes support
  - 2 Gb flash for AS x4
  - Dual 2 Gb flash for Avalon-ST x16
  - JTAG header for device programming
  - Built-in Intel FPGA Download Cable II for device programming
- Programmable clock sources
- Transceiver interfaces
  - PCI Express* (PCIe) x16 interface supporting Gen 4 end-point connected to a PCIe x16 edge connector (gold edge fingers)
  - 1x QSFP optical module interface connected to F-tile transceiver
  - 1x QSFPDD optical module interface connected to F-tile transceiver
  - 1x PCIe/CXL interface supporting x4 interface connected to MCIO connector
- Memory interfaces
  - Two x72 DIMM sockets supporting DDR4-2666 or DDR-T Intel Optane™ persistent memory module
  - Single x40 DDR4 component interface for HPS processor memory
- Communication ports
  - JTAG header
  - Micro USB on-board Intel FPGA Download Cable II
  - System I2C header
- Buttons, switches, and LEDs
  - CPU reset push button
  - PCIe reset push button
  - CXL reset push button
  - HPS reset push button
  - Four dedicated user LEDs
  - Board power good LED
  - FPGA configuration done LED

- Heatsink and fan
  - Air-cooled heatsink assembly
  - Red over-temperature warning LED
- Power
  - PCIe input power including required 2x4 auxiliary power connector
  - Blue power-good status LED
  - On/off slide power switch for benchtop operation
  - On-board power and temperature measurement circuitry
- Mechanical
  - PCIe standard height form-factor (full height, ¾ length, dual-width)
  - 4.375” x 10.0” board size
  - Two slots height with heatsink/fan assembly
- Operating environment
  - Maximum ambient temperature of 0-35°C

## 1.3. Box Contents

- Intel Agilex 7 F-Series (Two F-Tiles)FPGA Development Kit
- 1x DDR4 DIMM module
- 1x IO48 HPS daughter board
- USB 2.0 MicroUSB cable
- 240W power adapter and NA/EU/JP/UK cords

## 1.4. Recommended Operating Conditions

**Table 2. Recommended Operating Conditions**

| Operating Condition | Range of Values |
|---|---|
| Ambient operating temperature range | 0°C to 35°C |
| Maximum ICC load current | 150 A |
| Maximum ICC load transient percentage | 30% |
| FPGA maximum power supported by active heatsink/fan | 150 W |

When handling the board, it is important to observe static discharge precautions.

***Caution:*** Without proper anti-static handling, the board can be damaged. Therefore, use anti-static handling precautions when touching the development kit.

***Caution:*** This development kit should not be operated in a vibration environment.

# 2. Getting Started

## 2.1. Intel Quartus® Prime Software and Driver Installation

Intel Quartus® Prime design software is a multiplatform design environment that easily adapts to your specific needs in all phases of FPGA, CPLD and SoC designs. The Intel Quartus Prime software delivers the highest performance and productivity for Intel FPGAs, CPLDs, and SoCs. Intel Quartus Prime Pro Edition software is optimized to support the advanced features in next-generation FPGAs and SoCs with the Intel Agilex 7, Intel Stratix® 10, Intel Arria® 10, and Intel Cyclone® 10 GX device families.

Intel Agilex 7 F-Series (Two F-Tiles) Development Kit includes on-board Intel FPGA Download Cable II circuits for FPGA and system Intel MAX® 10 programming. However, for the host computer and board to communicate, you must install the Intel FPGA Download Cable II driver on the host computer. Installation instructions for the Intel FPGA Download Cable II driver for your operating system are available on the Intel website.

On the Intel website, navigate to the Cable and Adapter Drivers Information link to locate the table entry for your configuration and click the link to access the instructions.

### Related Information

- Quick-Start for Intel Quartus Prime Pro Edition Software
- Intel Quartus Prime Pro Edition User Guide: Getting Started

## 2.2. Design Examples

Unzip the install package which includes board design files, documents and examples directories. The table below lists the file directory names and a description of their contents.

**Table 3. Installed Development Kit Directory Structure**

| Directory Name | Description of Directory Contents |
|---|---|
| `board_design_files` | Contains schematics, layout, assembly, and bill of material board design files. Use these files as a starting point for a new prototype board design. |
| `demos` | Contains demonstration applications when available. |
| `documents` | Contains the development kit documentation. |
| `examples` | Contains: |

*continued...*

| Directory Name | Description of Directory Contents |
|---|---|
| | • Board Test System: BTS GUI, Power GUI, and Clock GUI<br>• Golden Top project for pinout assignments management<br>• Design Examples: Memory, XCVR, GPIO, PCIe Gen 4 |
| `factory_recovery` | Contains the original data programmed onto the board before shipment. Use this data to restore the board with its original factory content. |

# 3. Power Up the Development Kit

This chapter describes how to apply power to the development board and provides default switch and jumper settings.

## 3.1. Default Settings

The Intel Agilex 7 F-Series FPGA (Two F-Tiles) Development Kit ships with its board switches preconfigured to support the design examples in the kit. If you suspect your board might not be correctly configured with the default settings, follow the instructions in the table below to return to its factory settings before proceeding.

**Table 4. Factory Default Switch Settings**

<table>
<tr><th>Switch</th><th>Default Position</th><th>Function</th></tr>
<tr><td>SW1[1:4]</td><td>ON/OFF/OFF/OFF</td><td>PCIe PRSNT x1/x4/x8/x16 settings switches. Default = x16.
<table>
<tr><th>PRSNT x16</th><th>PRSNT x8</th><th>PRSNT x4</th><th>PRSNT x1</th></tr>
<tr><td>ON</td><td>OFF</td><td>OFF</td><td>OFF</td></tr>
</table></td></tr>
<tr><td>SW2</td><td>ON</td><td>Intel FPGA Download Cable II JTAG Selection switch. Default ON selects the micro-USB port on-board blaster for FPGA programming.</td></tr>
<tr><td>SW3[1:4]</td><td>ON/ON/ON/OFF</td><td>Configuration mode selection, BMC JTAG selection, and HPS JTAG Bypass switches.<br>SW3[1:2]—Configuration mode selection. MSEL0 is pulled high. Default mode is AS x4.
<table>
<tr><th>Mode</th><th>SW3[1] - MSEL1</th><th>SW3[2] - MSEL2</th></tr>
<tr><td>JTAG</td><td>OFF</td><td>OFF</td></tr>
<tr><td>Avalon-ST x16</td><td>ON</td><td>OFF</td></tr>
<tr><td>AS x4 (Fast)</td><td>ON</td><td>ON</td></tr>
</table>
SW3[3]—BMC JTAG selection.<br>• ON selects the on-board blaster as JTAG master when no external blaster is plugged<br>• OFF selects the PCIe RP as JTAG master when no external blaster is plugged<br>• Default JTAG chain selects the FPGA<br>SW4[4]—HPS JTAG Enable.<br>• ON enables the HPS as part of the JTAG chain<br>• OFF bypasses the HPS from the JTAG chain<br>• The HPS is set to bypass by default</td></tr>
<tr><td>SW4[1:4]</td><td>OFF/OFF/OFF/OFF</td><td>Clock features selection switches.</td></tr>
</table>

*continued...*

| Switch | Default Position | Function |
|---|---|---|
| | | SW4[4]—SI52204 (U25) PCIe clock power down.<br>• ON powers down the PCIe clocks<br>• OFF powers on the PCIe clocks (Default)<br>SW4[3]—PCIe refclk source selection.<br>• ON selects the local 100 Mhz clock source for PCIe<br>• OFF selects 100 Mhz clock source from the PCIe edge fingers (Default)<br>SW4[2]—CXL refclk source selection.<br>• ON selects local 100 Mhz clock source for CXL refclk<br>• OFF select 100 Mhz clock source from CXL connector (Default)<br>SW4[1]—PCIe clock spread spectrum enable.<br>• ON—Enable 0.5% down-spread<br>• OFF—Spread spectrum disable (Default) |
| SW5 | OFF | Power switch. Slide to ON position to turn on the board. Default is OFF. |
| SW6 | OFF | Intel MAX 10 JTAG_EN switch.<br>• ON sets the JTAG pins to function as dual-purpose I/O pins and JTAG function if the JTAG pin sharing option bit is enabled by the Intel Quartus Prime software.<br>• OFF sets the JTAG pins to function as JTAG dedicated pins if the JTAG pin sharing option bit is enabled by the Intel Quartus Prime software (Default). |

## 3.2. Applying Power to the Development Board

This development kit is designed to operate in two modes:

### As a PCIe Add-In Card

When operating the card as a PCIe system, insert the card into an available PCIe slot and connect a 2x4 pin PCIe power cable from the system to power connectors at **J11** of the board.

*Note:* When operating as a PCIe add-in card, the board does not power on unless power is supplied to **J11**.

### In Bench-Top Mode

In bench-top mode, you must supply the board with the provided power 240 W power supply connected to the power connector **J11**. The following describes the operation in bench-top mode.

This development board ships with its switches preconfigured to support the design examples in the kit.

If you suspect that your board may not be correctly configured with the default settings, follow the instructions in the *Default Switch and Jumper Settings* section.

1. The development board ships with design examples stored in the flash memory device for Avalon-ST x16. Ensure SW3[1] is ON and SW3[2] is OFF before powering up the board.
2. Connect the supplied power supply to an outlet and the DC Power Jack to **J11** on the FPGA board.

*Note:* Use only the supplied power supply. Power regulation circuits on the board can be damaged by power supplies with greater voltage.

3. Set the power switch (**SW5**) to the **ON** position.

   When the board powers up, the blue power-on LED (**D2**) illuminates signaling the board is ready for use. Since the default configuration mode is Avalon-ST x4, the FPGA automatically downloads its configuration image from the QSPI flash device connected to the FPGA's SDM interface. When the configuration is complete, green LED (**D12**) illuminates signaling the device configured successfully. If the configuration fails, **D12** will not illuminate.

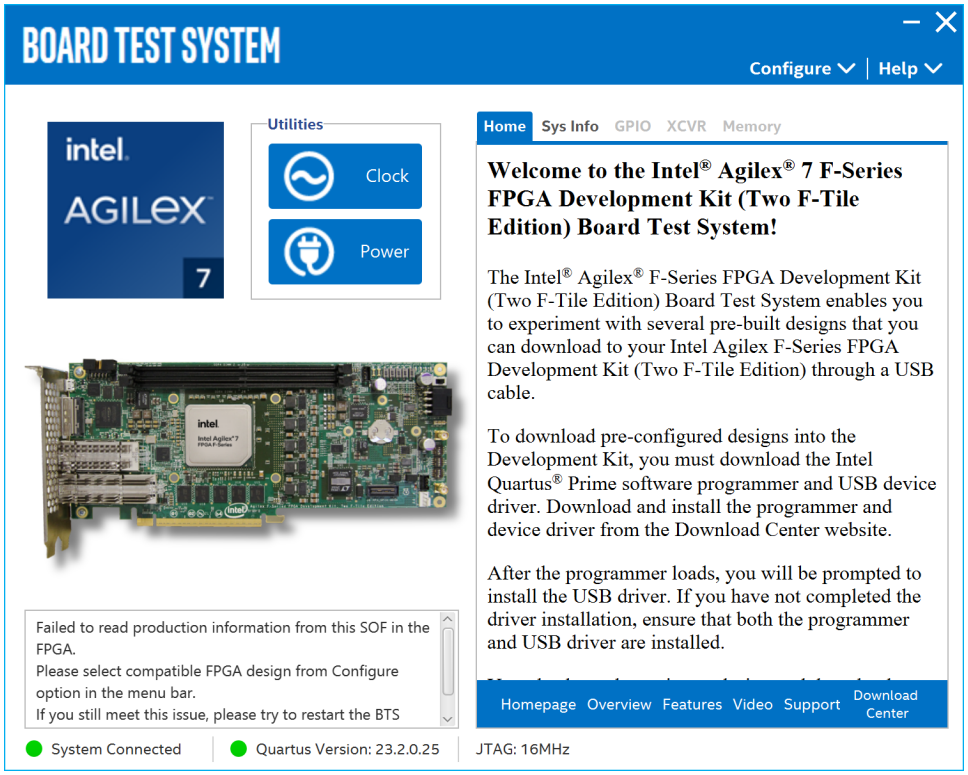
# 4. Board Test System

The Intel Agilex 7 F-Series FPGA (Two F-Tiles) Development Kit includes design examples and the board test system (BTS) GUI to test the functionality of this board. The BTS provides an easy-to-use interface to alter functional settings and observe results. You can use the BTS to test board components, modify functional parameters, observe performance, and measure power usage.

While using the BTS, you reconfigure the FPGA several times with test designs specific to the functionality that you are testing. The BTS is also useful as a reference for designing systems. The BTS communicates over the JTAG bus to a test design running in the Intel Agilex 7 F-Series FPGA device.

The following figure shows the graphical user interface (GUI) of a board that is in factory configuration.

**Figure 2. BTS GUI**



## 4.1. Set Up BTS GUI Running Environment

To run BTS GUI, including Power Monitor and Clock Controller GUI, you need to download and install Java runtime including OpenJDK and OpenJFX on your systems and set up the running environment. This is a one-time procedure, so if you have already completed it before, you do not need to do it again unless the Java version upgrade is needed.

### 4.1.1. Download OpenJDK

To download the Temurin OpenJDK, follow these steps:

1. Download the Temurin OpenJDK using this link: https://adoptium.net/releases.html.
2. Select Architecture x64, Package Type JRE, and Version 11.
3. On **Windows** system, choose the JRE zip format file.
4. On **Linux** system, choose the JRE tar.gz format file.

**Figure 3. OpenJDK Version**


*Note:* The JDK version can be updated, download the latest version.

### 4.1.2. Download OpenJFX

To download the OpenJFX, follow these steps:

1. Download the OpenJFX using this link: https://gluonhq.com/products/javafx/.
2. Select JavaFX version 17.0.2.
3. For the **Windows** system, download the JavaFX Windows x64 SDK.
4. For **Linux** system, download the JavaFX Linux x64 SDK.

**Figure 4. JavaFX Version**

### 4.1.3. Install OpenJDK and OpenJFX

You have two downloaded zip files, follow these steps to install them.

1. On **Windows** system, Intel recommends you to unzip the files and put them in the following directory:
   - C:\Program Files\Java\jre
   - C:\Program Files\Java\jfx

   *Note:* The unzipped folder name of JRE is `jdk-11.0.xx+x-jre` (for example, `jdk-11.0.15+10-jre`), you need to rename it to `jre`. The unzipped folder name of JFX is `javafx-sdk-17.0.2`, you need to rename it to `jfx`.
2. On **Linux** system, Intel recommends you to unzip the files and rename the folders using the following commands:

```
# unzip openjfx-17.0.2_linux-x64_bin-sdk.zip -d /opt/Java/
# tar zxvf OpenJDK11U-jre_x64_linux_hotspot_11.0.15_10.tar.gz -C /opt/Java/
# cd /opt/Java
# mv javafx-sdk-17.0.2 jfx
# mv jdk-11.0.15+10-jre jre
```

   You have the following two directories on your **Linux** system:
   - /opt/Java/jre
   - /opt/Java/jfx

### 4.1.4. Install the Intel Quartus Prime Software

You need to install the Intel Quartus Prime software that can support the silicon on the development kit. The recommended version can be found in the `README.txt` file under `examples\board_test_system` directory. If you choose to install individual files, you must install the Intel Agilex 7 device support.

The BTS communicates over JTAG to a test design running in the FPGA. The BTS and Power Monitor share the JTAG with other applications like the Nios® II Gen 2 JTAG Debug Module and the Signal Tap Logic Analyzer. Ensure closing other applications before you use the BTS, because the BTS is designed based on the Intel Quartus Prime software.

The BTS relies on the Intel Quartus Prime software's specific library. Before running the BTS, open the Intel Quartus Prime software to automatically set the environment variable QUARTUS_ROOTDIR. Otherwise, you can change it through the Environment Variables in System Properties on Windows. The BTS uses this environment variable to locate the Intel Quartus Prime library.

### 4.1.5. Run BTS GUI

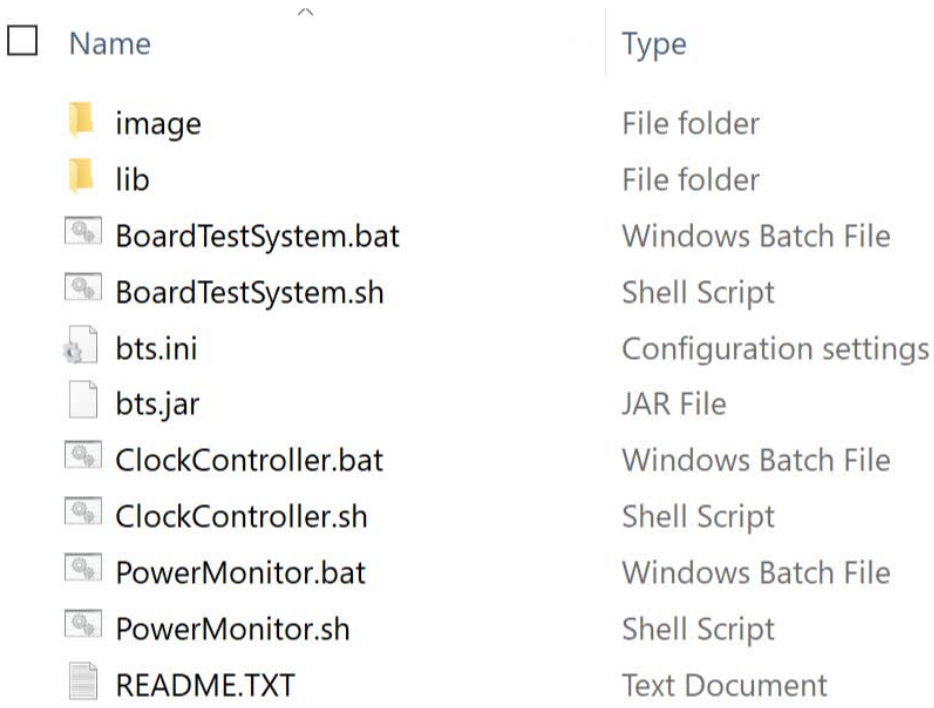
With the power to the board off, follow these steps:

1. Connect the USB cable to your PC and the board.
2. Ensure the development board switches and jumpers are set according to your preferences. For more information, refer to the *Factory Default Switch Settings* section.
3. Check the external modules' status: QSFP/QSFPDD/DDR4 DIMM.
4. Turn on the board power switch.

*Note:* To ensure operating stability, keep the USB cable connected and the board powered on when running the demonstration application. The BTS cannot run correctly unless the USB cable is attached and the board is powered on.

Navigate to the `<package dir>\examples\board_test_system` directory. The BTS release folder includes the following files.

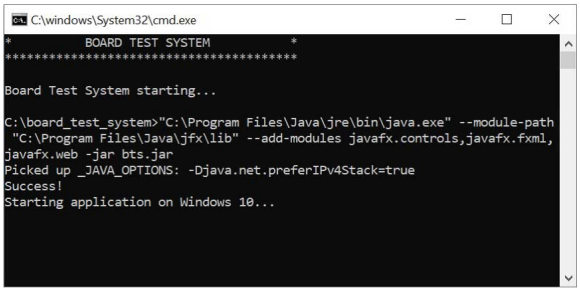
**Figure 5. BTS Folder**




You can run BTS GUI easily with the following scripts.

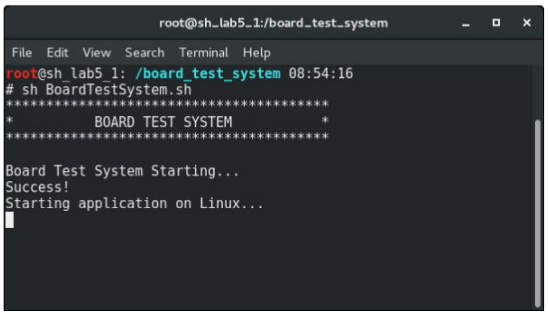
1. On **Windows** system, double click the .bat files to run BTS, Clock Controller, or Power Monitor GUI.

**Figure 6. Windows Console**




2. On **Linux** system, you need to run the shell script with root privilege.

**Figure 7. Linux Console**




*Note:* The .bat or shell script checks the Java environment settings, copy necessary files, and give some prompts if the environment is not set up correctly.

The GUI displays the application tab corresponding to the design running in the FPGA. If the design loaded in the FPGA is not supported by the BTS GUI, you receive a message prompting you to configure your board with a valid BTS design. For more information, refer to the *Configure Menu* section.

## 4.2. Test the Functionality of the Development Kit

This section describes each control in the BTS.

### 4.2.1. The Bottom Info Bar

The bottom information bar shows the status of the system connection, the Intel Quartus Prime version and the JTAG clock.

- **System Connected/Disconnected**: Shows if the board is connected to the system. The green sign turns gray if the board becomes disconnected.
- **Intel Quartus Prime Version**: Displays the current Intel Quartus Prime version installed and active on your system. The text turns red if your version is older than the required version. Change the QUARTUS_ROOTDIR environment variable if you have installed the right version but the active version doesn't meet the requirement.
- **JTAG**: Displays the JTAG clock frequency.

### 4.2.2. The Configure Menu

Use the Configure Menu to select the design you want to use. Each design example tests different functionality that corresponds to one or more application tabs.

**Figure 8. The Configure Menu**

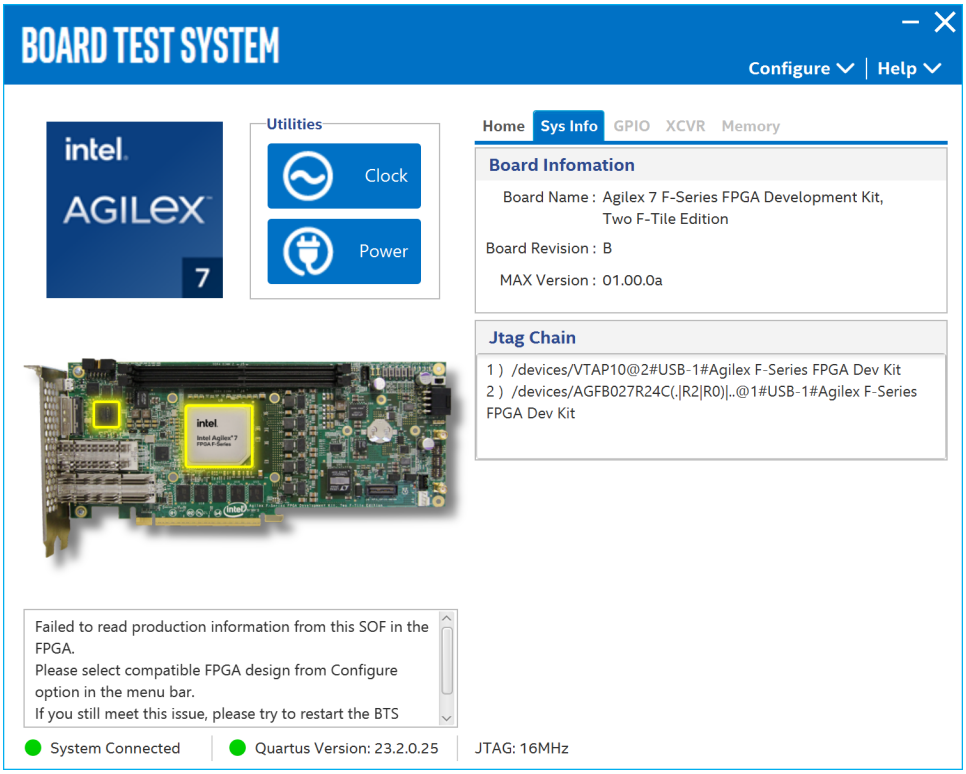

To configure the FPGA with a test system design, follow these steps:

1. On the **Configure** menu, click the **Configure** command that corresponds to the functionality you want to test.
2. In the dialog box that appears, click **Configure** to download the corresponding design's SRAM Object File (.sof) to the FPGA. The download process usually takes less than a minute.
3. When configuration finishes, the design begins running in the FPGA. The corresponding GUI application tabs that interface with the design are now enabled. If you use the Intel Quartus Prime Programmer for configuration, instead of the BTS GUI, you need to restart the GUI.

## 4.2.3. The Sys Info Tab

The **Sys Info** tab shows information about the board's current configuration. The tab displays the board information, JTAG Chain devices and other details stored on the board.

**Figure 9. The Sys Info Tab**




The following sections describe the controls on the System Info tab.

### Board Information

The board information control displays static information about your board.

- **Board Name**: Indicates the official name of the board given by the BTS.
- **Board Revision**: Indicates the revision of the board.
- **MAX Version**: Indicates the version of the system Intel MAX 10.

### JTAG Chain

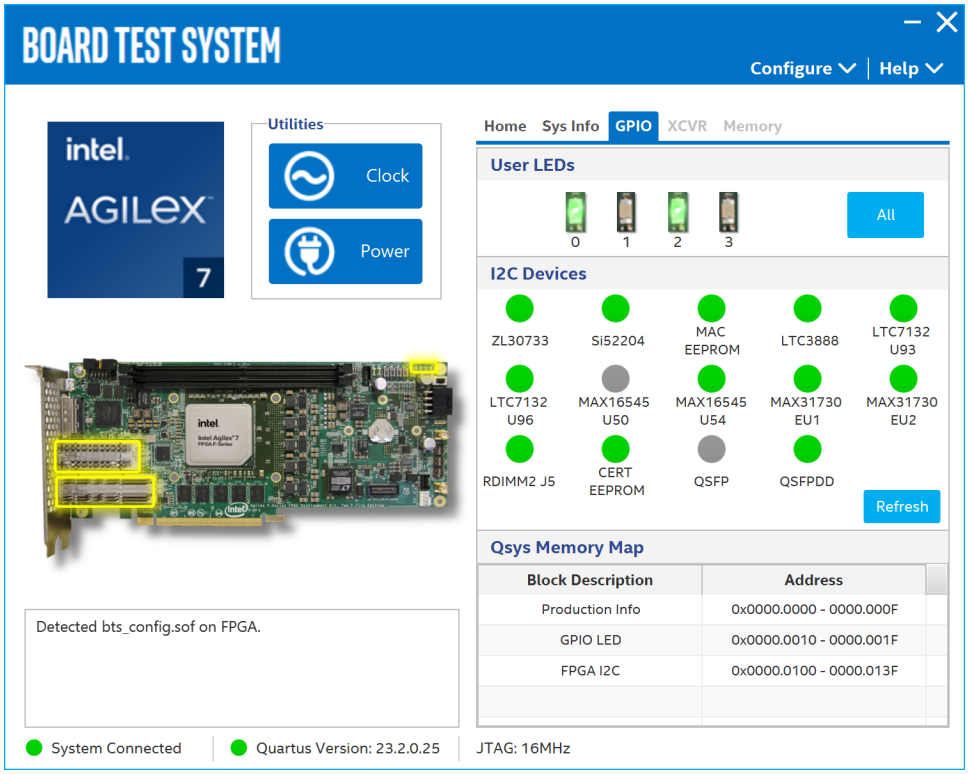
The JTAG chain control shows all the devices currently in the JTAG chain.

*Note:* Both System Intel MAX 10 and FPGA must be in the JTAG chain when running the BTS GUI.

## 4.2.4. The GPIO Tab

The **GPIO** tab allows you to interact with all the general-purpose user I/O components on your board. You can turn LEDs on or off and detect $I^2C$ target devices connection status.

**Figure 10. The GPIO Tab**




The following sections describe the controls on the GPIO tab.

### User LEDs

The User LEDs control displays the current state of the user LEDs. Toggle the LED buttons to turn the board LEDs on and off. Click the All button to reverse the state of all the LEDs.

### I²C

The read-only I²C target device control displays the connection status of some devices, which can be accessed by I²C bus. The status of QSFP and QSFPDD modules can be updated in real time.

### Platform Designer Memory Map

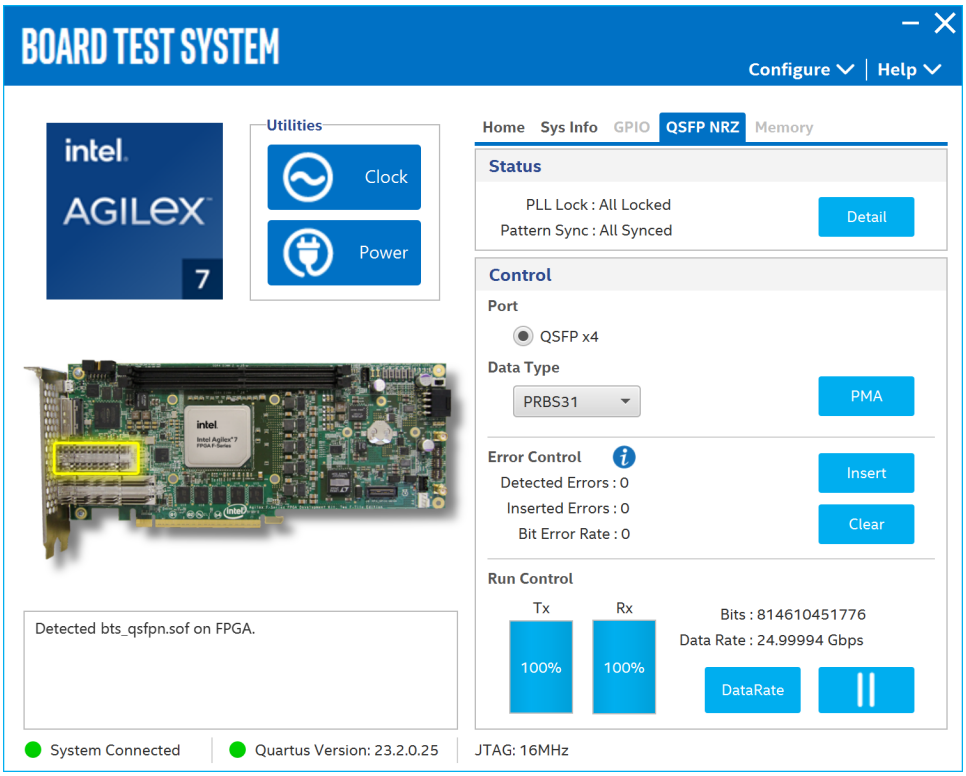
The Platform Designer Memory Map control shows the memory map of **bts_config.sof** design running on your board.

## 4.2.5. The XCVR Tab

The **XCVR** tab allows you to run transceiver tests on your board. You can run the test using either electrical loopback modules or optical fiber modules.

### 4.2.5.1. The QSFP NRZ Tab

**Figure 11. The QSFP NRZ Tab**




The following sections describe controls in the QSFP NRZ tab.

#### Status

The Status control displays the following status information during the loopback test:

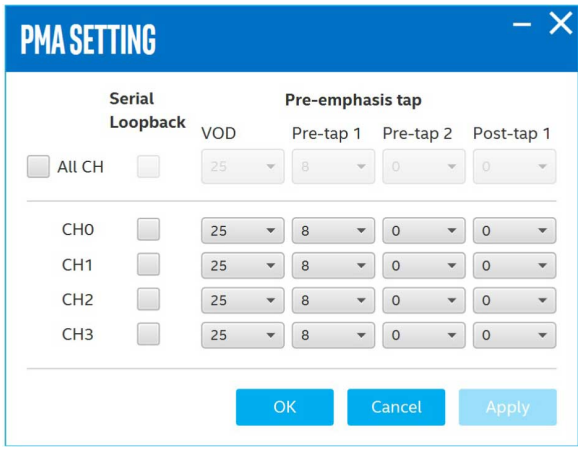
- **PLL Lock:** Shows the PLL locked or unlocked state.
- **Pattern Sync:** Shows the pattern synced or not state. The pattern is considered synced when the start of the data sequence is detected.
- **Detail:** Shows the PLL lock and pattern sync status of each channel. The number of the error bits of each channel can be found here.

### PMA Setting

Allows you to make changes to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis:

- **Serial Loopback:** Displays the signal status between the transmitter and the receiver.
- **VOD:** Specifies the voltage output differential of the transmitter buffer.
- **Pre-emphasis tap:**
  - Pre-tap 1: Specifies the amount of pre-emphasis on the first pre-tap of the transmitter buffer.
  - Pre-tap 2: Specifies the amount of pre-emphasis on the second pre-tap of the transmitter buffer.
  - Post-tap 1: Specifies the amount of pre-emphasis on the post-tap of the transmitter buffer.

**Figure 12. QSFP NRZ-PMA Setting**




### Data Type

The Data Type control specifies the type of data pattern contained in the transactions. Select the following available data types for analysis:

- **PRBS7:** pseudo-random 7-bit binary sequences
- **PRBS15:** pseudo-random 15-bit binary sequences
- **PRBS23:** pseudo-random 23-bit binary sequences
- **PRBS31:** pseudo-random 31-bit binary sequences (default)

### Error Control

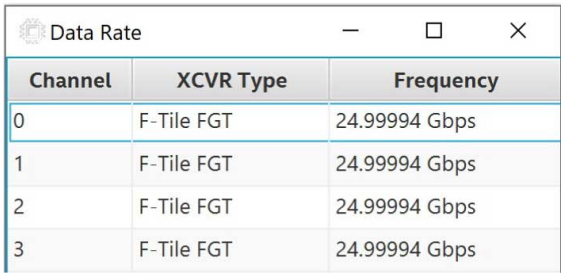
This control displays data errors detected during analysis and allows you to insert errors:

- **Detected Errors:** Displays the number of data errors detected in the received bit stream.
- **Inserted Errors:** Displays the number of errors inserted into the transmit data stream.
- **Bit Error Rate:** Calculates the bit error rate of the transmit data stream.
- **Insert:** Insert a one-word error into the transmit data stream each time you click the button. Insert Error is only enabled during transaction performance analysis.
- **Clear:** Resets the Detected Errors counter and Inserted Errors counter to zeros.

### Run Control

- **TX and RX performance bars:** Show the percentage of maximum theoretical data rate that the requested transactions can achieve.
- **Start:** This control initiates the loopback tests.
- **Data Rate:** Displays the XCVR type and data rate of each channel.

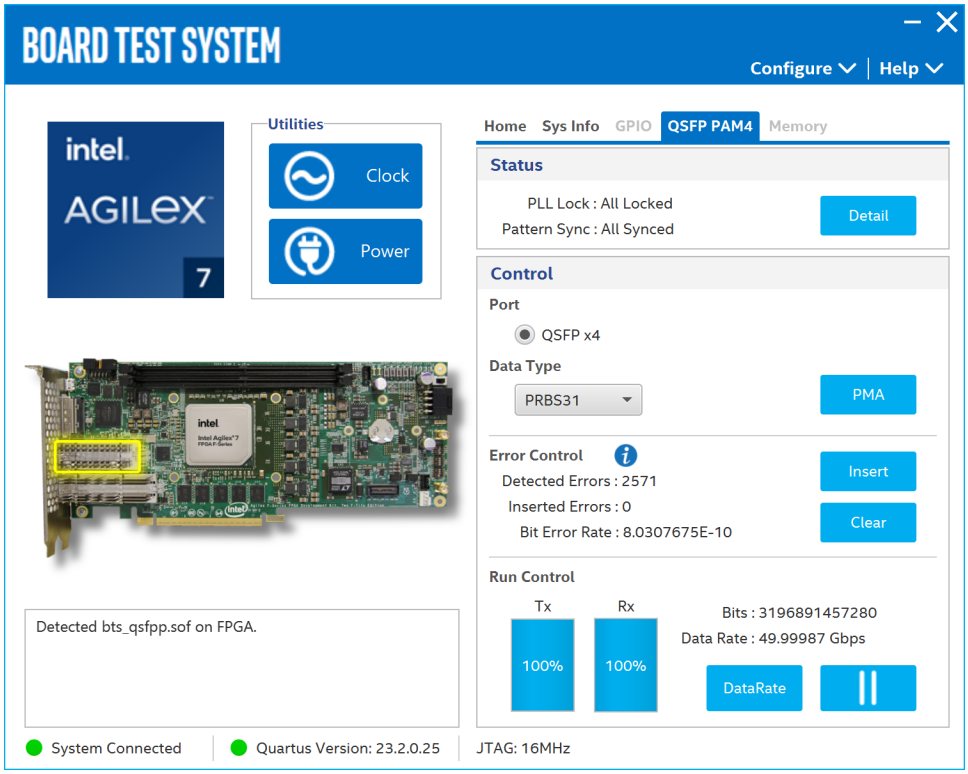
**Figure 13. QSFP NRZ - Data Rate**




## 4.2.5.2. The QSFP PAM4 Tab

Similar control functions with the QSFP NRZ tab.

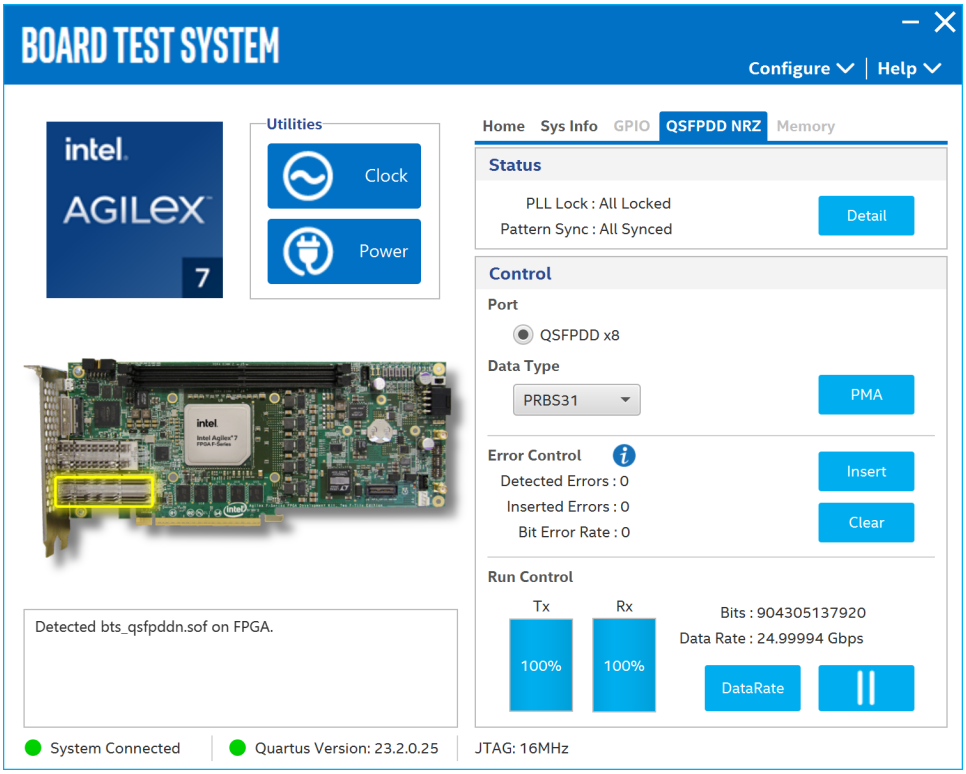
**Figure 14. The QSFP PAM4 Tab**




### 4.2.5.3. The QSFPDD NRZ Tab

Similar control functions with the QSFP NRZ tab.

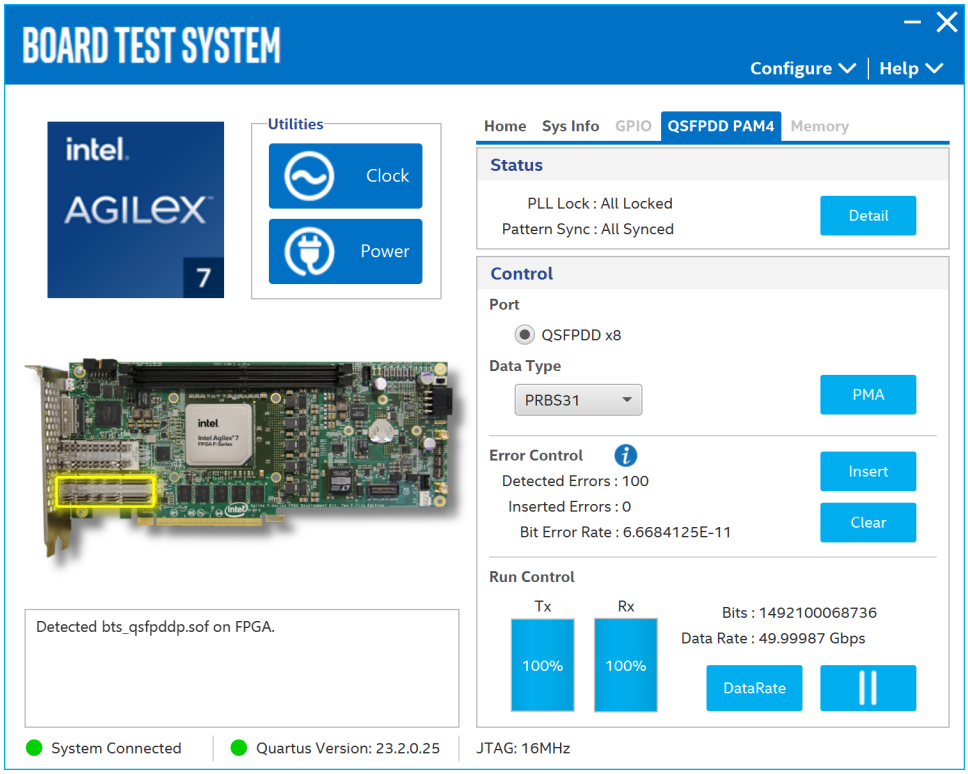
**Figure 15. The QSFPDD NRZ Tab**




### 4.2.5.4. The QSFPDD PAM4 Tab

Similar control functions with the QSFP NRZ tab.

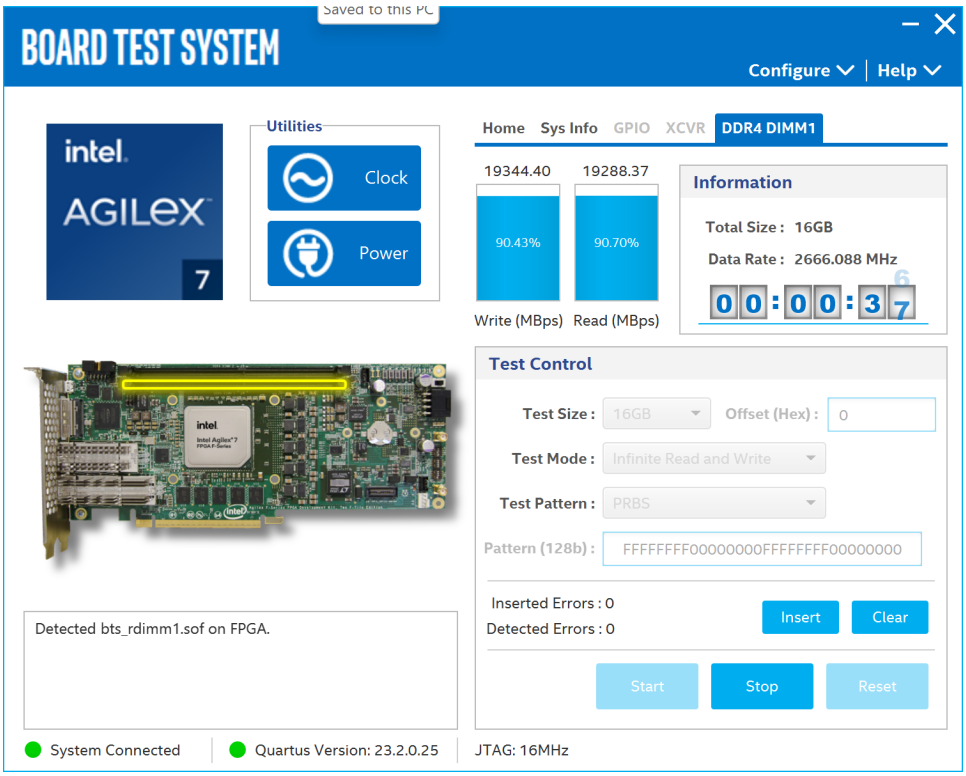
**Figure 16. The QSFPDD PAM4 Tab**




## 4.2.6. The Memory Tab

This tab allows you to read and write DDR4 DIMM1 and DDR4 DIMM2 memory on your board. Download the design through BTS Configure.

**Figure 17. The RDIMM1 Tab**




The following sections describe controls on this tab.

### Start

Initiates DDR4 memory transaction performance analysis.

### Stop

Terminates transaction performance analysis.

### Performance Indicators

These controls display current transaction performance analysis information collected since you last clicked **Start**:

- **Write and Read performance bars**: Show the percentage of maximum theoretical data rate that the requested transactions can achieve.
- **Write (MBps) and Read (MBps)**: Show the number of bytes analyzed per second.
- **Data Bus**: 72 bits (8 bits ECC) wide, reference clock is 166.666 MHz, and the frequency is 1333.33 MHz double data rate 2666.66 MT/s.

### Test Control

- **Test Size**: You can choose the size of the memory to test. The available options are 64 KB, 256 KB, 1 MB, 4 MB, 16 MB, 64 MB, 256 MB, 1 GB, 4 GB, 8 GB, and 16GB (default).
- **Offset (Hex)**: You can define the memory start address to test.
- **Test Mode**: Infinite Read and Write (default), Single Read and Write.
- **Test Pattern**: PRBS (default), User Defined Constant, Walking '0', Walking '1'.

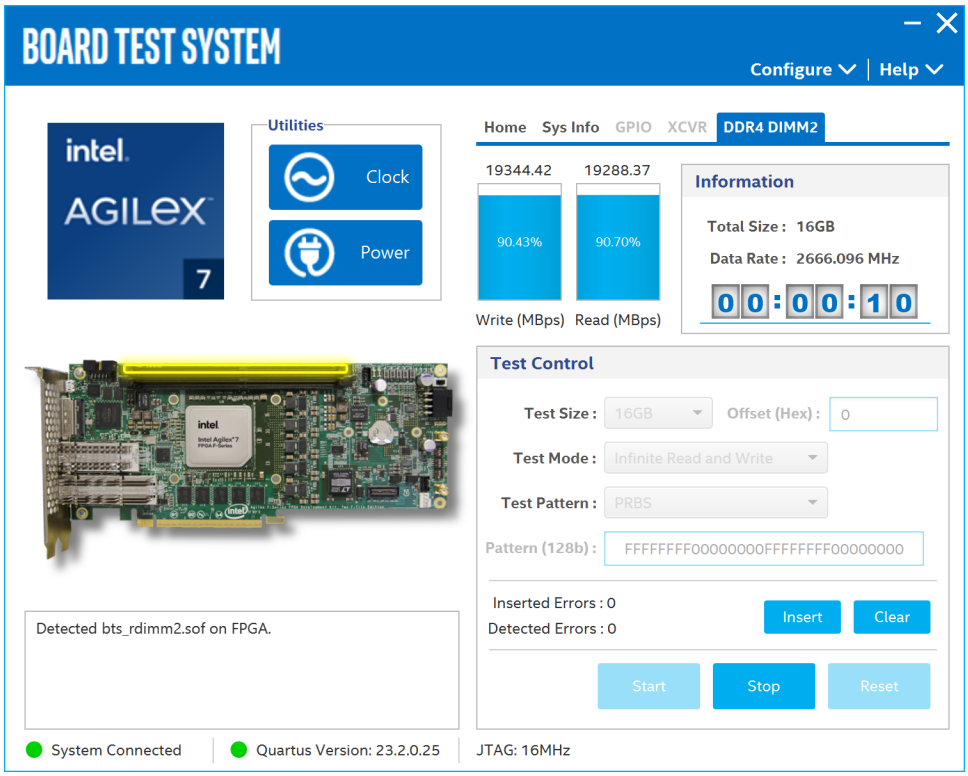
### Error Control

This control displays data errors detected during analysis and allows you to insert errors:

- **Detected Errors**: Displays the number of data errors detected in the hardware.
- **Inserted Errors**: Displays the number of errors inserted into the transaction stream.
- **Bit Error Rate**: Calculates the bit error rate of the transmit data stream.
- **Insert**: Insert a one-word error into the transaction stream each time you click the button. Insert error is only enabled during transaction performance analysis.
- **Clear**: Resets the Detected Errors counter and Inserted Errors counter to zeros.

**Figure 18. The RDIMM2 Tab**

Similar with RDIMM1.



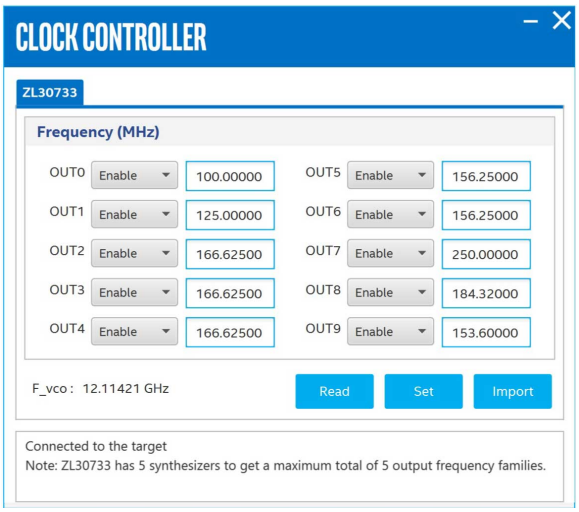
## 4.3. Control On-Board Clock through Clock Controller GUI

The Clock Controller GUI can change the on-board programmable PLLs to a large range of customized frequency. The instructions to run Clock Controller GUI are stated in the *Run BTS GUI* section. You can also start it using the BTS GUI icon "Clock".

The clock controller communicates with the system Intel MAX 10 device through a 10-pin JTAG header **J3** or Micro-USB connector **J10**. Then, system Intel MAX 10 controls these programmable clock parts through a 2-wire $I^2C$ bus.

*Note:* You cannot run the stand-alone Clock Controller GUI application when the BTS or Power Monitor GUI is running at the same time.

**Figure 19. ZL30733**




The output frequency of ZL30733 is from 0.5 Hz to 750 MHz. It can generate up to 10 differential outputs with a total of 5 output frequency families. The following sections describe the Clock Controller buttons.

### Read

Reads the current frequency setting for the oscillator associated with the active tab.

### Set

Sets the programmable oscillator frequency for the selected clock to the value in the 0UTx output controls for ZL30733. Frequency changes might take several milliseconds to take effect. You might see glitches on the clock during this time. Intel recommends resetting the FPGA logic after changing frequencies.

### Import

ZL30733 has a multiple time writable non-volatile memory (NVM). You can generate the register list with the following format:

- **Register Write Command Line**: X ,<register_address> , <data_bytes>—<register_address> and <data_bytes>, whose prefix must be "0x" are in hexadecimal
- **Wait Command Line**: W , <time_microseconds>

Import it into ZL30733 to update the settings of the RAM. Register changes are volatile after power cycling. For more details, refer to ZL30733 on the Microchip website.

## 4.4. Monitor On-Board Power Regulator through Power Monitor GUI

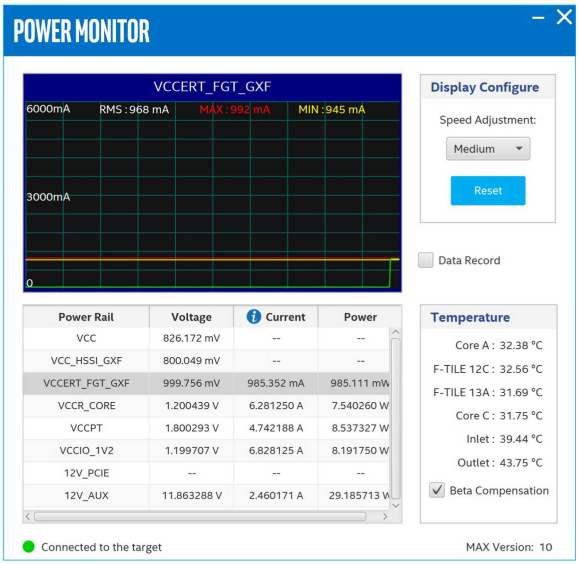
The Power Monitor GUI reports most power rails' voltage, current, and power information on the board. It also collects temperature from FPGA die, power modules, and diodes assembled on PCB.

The Power Monitor GUI communicates with system Intel MAX 10 through a 10-pin JTAG header **J3** or USB port **J10**. System Intel MAX 10 monitors and controls power regulator, temperature/voltage/current sensing chips through a 2-wire $I^2C$ bus.

The instructions to run Power Monitor GUI are stated in the *Run BTS GUI* section. It can also be started with the BTS GUI icon "Power".

*Note:* You cannot run the stand-alone Power Monitor GUI when the BTS or the Clock Controller GUI is running at the same time.

**Figure 20. Power Monitor GUI**




The following sections describe the details of the Power Monitor GUI.

### Display Configure

- **Speed Adjustment**: Adjusts the update rate of the current curve
- **Reset**: Regenerates the graph

### Data Record

When the box is checked, the telemetry data of the selected power rail can be recorded. The data will be saved into a .csv file in the `board_test_system/log` directory.

### Temperature

Reads the temperature data from FPGA die internal temperature sense diodes.

- **Beta Compensation**: Corrects the temperature-measurement errors due to low-beta sensing transistors

## 4.5. BTS Test Areas

BTS checks for hardware fault before you can use the board. If one or more BTS test items fail, it implies either a wrong hardware setting or hardware fault on specific interface.

## 4.6. Identify Test Pass- or Fail-based on BTS GUI Test Status

### QSFP

Plug QSFP loopback module in **J8** before you configure QSFP NRZ/PAM4 example build through BTS GUI.

### QSFPDD

Plug QSFPDD loopback module in **J7** before you configure QSFPDD NRZ/PAM4 example build through BTS GUI.

### DDR4 DIMM

Plug the DDR4 DIMM module which is shipped alone with this development kit in **J4**/**J5**. BTS GUI only supports fabric memory interfaces, namely DDR4 DIMM1 and DDR4 DIMM2.

# 5. Development Kits Hardware and Configuration

The development board supports multiple configuration modes as listed in the following table. The default configuration is AS x4 (Fast) using a 2 Gb QSPI flash device.

**Table 5. Supported Configuration Modes**

| Configuration Mode | MSEL2 SW3.2 | MSEL1 SW3.2 | MSEL0 (Pulled high) |
|---|---|---|---|
| JTAG | 1 | 1 | 1 |
| Avalon-ST x16 | 1 | 0 | 1 |
| AS x4 (Fast) (Default) | 0 | 0 | 1 |
| AS x4 (Normal) | 0 | 1 | 1 |

## 5.1. JTAG Configuration Mode

When MSEL[2:1] are both set to logic high by DIP switch SW3[2:1] = [OFF:OFF], the configuration mode defaults to JTAG.

## 5.2. Active Serial (AS) x4 Configuration Mode

The AS x4 configuration mode can be set to either fast or normal mode. When the AS x4 mode is enabled, the FPGA configures itself after power-on with the programming file stored within the QSPI flash (**U9**) connected directly to the FPGA SDM interface. In this mode, the FPGA downloads its programming bitstream directly from the QSPI flash device. This is the default configuration mode for the board shipped from the factory.

## 5.3. Avalon-ST x16 Configuration Mode

When set to the Avalon-ST x16 mode, the Intel MAX 10 System Controller (**U5**) acts as the configuration host to manage configuration download. After power on, the Intel MAX 10 reads the configuration bitstream programmed into the QSPI flash (**U4**) and sends this data to FPGA SDM interface to program the FPGA. The **U4** is a 2 Gb QSPI flash device, allowing for four FPGA images to be stored. Image download selection is controlled by jumpers **J105** and **J106** as listed in the following table. The default image to be programmed is image 0.

*Note:* Do not use **U3**, it is just hardware backup for future use.

**Table 6. Image Download Selection**

| Image Selection | J106 | J105 | Notes |
|---|---|---|---|
| Image 0 | Installed | Installed | Image 0—Default |
| Image 1 | Open | Installed | Image 1 |
| Image 2 | Installed | Open | Image 2 |
| Image 3 | Open | Open | Image 3 |

# 6. Custom Projects for the Development Kit

## 6.1. Add SmartVID Settings in the Intel Quartus Prime QSF File

By default, the Intel Agilex 7 silicon assembled on this development kit enables the SmartVID feature. To avoid the Intel Quartus Prime software from generating an error due to incomplete SmartVID settings, you must put constraints outlined below into the Intel Quartus Prime project QSF file.

Open your Intel Quartus Prime project QSF file, copy and paste the following constraint scripts into the file. Ensure there are no other similar settings with different values.

```
set_global_assignment -name PWRMGT_SLAVE_DEVICE_TYPE LTC3888
set_global_assignment -name PWRMGT_SLAVE_DEVICE0_ADDRESS 55
set_global_assignment -name PWRMGT_VOLTAGE_OUTPUT_FORMAT "LINEAR FORMAT"
set_global_assignment -name PWRMGT_LINEAR_FORMAT_N "-12"
set_global_assignment -name PWRMGT_PAGE_COMMAND_ENABLE ON
set_global_assignment -name PWRMGT_PAGE_COMMAND_PAYLOAD 0
set_global_assignment -name USE_PWRMGT_SCL SDM_IO0
set_global_assignment -name USE_PWRMGT_SDA SDM_IO11
set_global_assignment -name USE_CONF_DONE SDM_IO16
set_global_assignment -name USE_INIT_DONE SDM_IO13
set_global_assignment -name USE_CVP_CONFDONE SDM_IO14
set_global_assignment -name USE_NCATTRIP SDM_IO12
set_global_assignment -name USE_HPS_COLD_RESET SDM_IO10
```

## 6.2. Golden Top

You can use the Golden Top project as the starting point for your designs. It comes loaded with constraints, pin locations, defined I/O standard, direction, and general termination.

# 7. Revision History

**Table 7. Revision History for the Intel Agilex 7 F-Series FPGA (Two F-Tiles) Development Kit User Guide**

| Document Version | Changes |
|---|---|
| 2023.08.07 | Updated the *Block Diagram* figure to conform to Intel standards. |
| 2023.06.26 | • Updated product family name to "Intel Agilex® 7."<br>• Updated development kit name to "Intel Agilex 7 FPGA F-Series Development Kit."<br>• Retitled the document from *Intel Agilex F-Series FPGA (Two F-Tiles) Development Kit User Guide* to *Intel Agilex 7 F-Series FPGA (Two F-Tiles) Development Kit User Guide*. |
| 2022.09.21 | Initial release. |

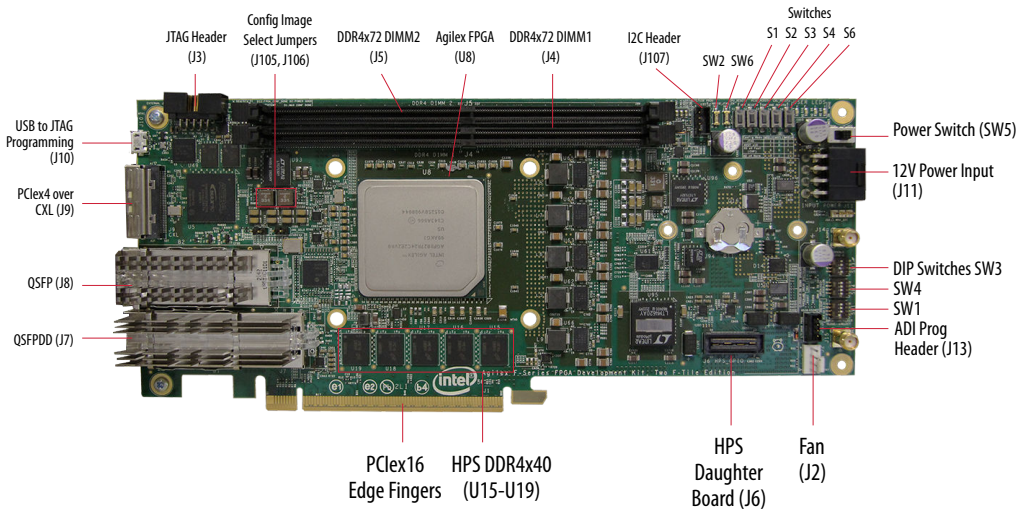
# A. Development Kit Components

## A.1. Board Overview and Components

This section describes all the important components on the development board. A complete set of schematics, a physical layout database, and GERBER files for the development board reside in the development kit documents directory.

### A.1.1. Board Overview

**Figure 21. Intel Agilex 7 FPGA Development Kit, 2 F-tile Edition (Top View)**




### A.1.2. Board Components

**Table 8. Featured Devices**

| Board Reference | Type | Description |
|---|---|---|
| U8 | FPGA | Intel Agilex 7 FPGA, AGFB027R24C2E2V<br>• 2,692,760 Logic Elements (LE)<br>• 912,800 Adaptive Logic Elements (ALM)<br>• 13,272 M20K Blocks<br>• 45,640 MLABs<br>• 8,528 DSP Blocks<br>• 17,056 18x19 Multipliers<br>• 744 GPIOs<br>• 372 LVDS |

*continued...*

| Board Reference | Type | Description |
|---|---|---|
| | | • 32 x 32 Gbps Transceivers<br>• 24 x 58Gbps Transceivers<br>• 2340 pin BGA Package |
| U5 | CPLD | Intel MAX 10 CPLD, 10M50DAF256I7G |

## Table 9. Configuration and Setup Elements

| Board Reference | Type | Description |
|---|---|---|
| J10 | On-board Intel FPGA Download Cable II | Micro-USB 2.0 connector for programming and debugging the FPGA. |
| SW1 | PCIe control DIP switch | Enables PCIe link widths x1, x4, x8, and x16. |
| SW2 | Intel FPGA Download Cable II selection switch | Selects between the on-board Intel FPGA Download Cable II or external Intel FPGA Download Cable II connected to J3 header. |
| SW3<br>Position 1-2 | JTAG bypass DIP switch | Enables and disables devices in the JTAG chain. |
| SW3 Position 3-4 | MSEL configuration DIP switch | Sets the Intel Agilex 7 MSEL configuration modes |
| SW4 | PCIe clock control DIP switch | Provides control for PCIe clock controls such as Spread Spectrum enable/disable, local or external PCIe clock source, and PCIe REFCLK power down. |
| SW5 | Power-on slide switch | Main switch for powering on the Board when used in bench-top mode. This switch is ignored when the board is used in a PCIe system. |
| SW6 | Intel MAX 10 JTAGEN switch | Enables Intel MAX 10 to use the JTAG pins as I/Os. |
| S1 | CPU RESETn | Sends an active low signal to the FPGA and Intel MAX 10 which can be used as the RESET for internal designs. |
| S2 | HPS RESETn | Sends an active low signal to the Intel MAX 10. Intel MAX 10 can then send HPS_DC_RSTn to the HPS IO48 daughter card is present. |
| S3 | 1st_PCIe_PERSTN push-button | Sends an active low signal to the dedicated PCIe_PERSTN pin of transceiver Bank 13A. |
| S4 | 2nd_PCIe_PERSTN push-button | Sends an active low signal to a GPIO pin in Bank 3A. This pin can be used as a secondary PERSTN signal. |
| S6 | CXL_PCIe_PERSTN push-button | Sends an active low signal to the CXL connector PERSTN pin. |
| J105 | Configuration image selection | Use together with J106 to select image stored in **U4** for Avalon-ST x16. |
| J106 | Configuration image selection | Use together with J105 to select image stored in **U4** for Avalon-ST x16. |

## Table 10. Status Elements

| Board Reference | Type | Description |
|---|---|---|
| D1 | Green Intel MAX 10 CONF_DONE LED | LED is on when the Intel MAX 10 is successfully configured. |
| D2 | Blue power good LED | LED is on when Intel MAX 10 detects that all power on the board is good. |

*continued...*

| Board Reference | Type | Description |
|---|---|---|
| D5 | Red over temperature LED | LED is on when the Intel MAX 10 detects an over-temperature condition on the board. |
| D12 | Green FPGA CONF_DONE LED | LED is on when the FPGA is successfully configured. |
| D[11:D8] | 4 green user LEDs | FPGA connected LEDs for user designs. |
| D[25:24] | 2 green configuration image LEDs | Indicates which FPGA configuration image is loaded. |

## Table 11. Clock Circuits

| Board Reference | Type | Description |
|---|---|---|
| U23 | ZL30733 IEEE 1588 clock device $I^2C$ programmable by Intel MAX 10 | Default frequencies:<br>• Out 0: 100 MHz<br>• Out 1: 125 MHz<br>• Out 2: 166.25 MHz<br>• Out 3: 166.25 MHz<br>• Out 4: 166.25 MHz<br>• Out 5: 156.25 MHz<br>• Out 6: 156.25 MHz<br>• Out 7: 250 MHz<br>• Out 8: 184.32 MHz<br>• Out 9: 153.6 MHz |
| U25, U26, U27 | PCIe reference clocks<br>• U25: $I^2C$ programmable by Intel MAX 10 local<br>• U26, U27: PCIe fan-out clock buffers | Default frequencies:<br>• U25:<br>— Out 0: Local 100 MHz PCIe to U26<br>— Out 1: Local 100 MHz PCIe to U27<br>— Out 2: 100 MHz CXL PCIe root port clock to CXL connector J9<br>• U26:<br>— Out 0: 100 MHz PCIe Bank 13A, CH5<br>— Out 1: 100 MHz PCIe Bank 13A, CH2<br>• U27:<br>— Out 0: 100 MHz PCIe Bank 12C, CH0<br>— Out 1: 100 MHz PCIe Bank 12C, CH1 |

## Table 12. Transceiver Interfaces

| Board Reference | Type | Description |
|---|---|---|
| J1 | PCIe x16 gold fingers | PCIe TX/RX x16 interface from FPGA Bank 13A. |
| J7, B1 | QSFPDD-56 pluggable optics interface | 8 TX/RX channels from FPGA Bank 12C, Quad2 and Quad3. |
| J8, B2 | QSFP-56 pluggable optics interface | 4 TX/RX channels from FPGA Bank 12C, Quad1. |
| J9 | PCIe x4 over CXL connector | PCIe TX/RX x4 interface from FPGA Bank 12C, Quad0. |

## Table 13. Memory Devices

| Board Reference | Type | Description |
|---|---|---|
| J4 | DDR4 DIMM1 connector | DDR4 x72 DIMM module installed by default. |
| J5 | DDR4 DIMM2 connector | No DDR4 DIMM module installed by default. |
| U15–U19 | DDR4 components | DDR4 x40 interface for HPS. |
| U3, U4 | 2 x 2 Gbit QSPI flash | FPGA Avalon-ST x16 configuration flash memory. |

***continued...***

| Board Reference | Type | Description |
|---|---|---|
| U9 | 2 Gbit QSPI flash | FPGA AS x4 configuration flash memory. |
| U45 | 64 Mbit serial nor flash | Intel MAX 10 Nios II flash. |
| U44 | 128 Kbit $I^2C$ EEPROM | MAC address EEPROM. |
| U46 | 128 Kbit $I^2C$ EEPROM | Security certificate EEPROM. |

### Table 14. Communication Ports

| Board Reference | Type | Description |
|---|---|---|
| J3 | 10-pin JTAG header | For connecting an external Intel FPGA Download Cable II dongle. |
| J10 | Micro-USB connector | For connecting to the on-board Intel FPGA Download Cable II. |

### Table 15. Miscellaneous Ports

| Board Reference | Type | Description |
|---|---|---|
| J2 | FAN header | 4-pin FAN header |
| J13 | LTC3888 (U61) programming header | Programming header for LTC3888 VCC Core, VCC_HSSI voltage regulator |
| J107 | LTC7132 (U93, U96) programming header | Programming header for U93 (LTC7132 VCCERT_FGT_GXF, VCCR_CORE) and U96 (LTC7132 VCC_PT, VCCIO_1V2) |

### Table 16. Power Supplies

| Board Reference | Type | Description |
|---|---|---|
| J11 | 12V_AUX power connector | 8-pin 12V_AUX input power connector |
| U50 | MAX16545B device | Input power conditioner for 12V_PCIe |
| U54 | MAX16545B device | Input power conditioner for 12V_AUX |
| U94 | Analog devices LTM4625 | 5V DC-DC voltage regulator |
| U56 | Intersil ISL80101 | 2.5V LDO voltage regulator |
| U57 | Intersil ISL80101 | 1.8V LDO voltage regulator |
| U58 | Intersil ISL80101 | 1.2V LDO voltage regulator |
| U95 | Analog devices LTM4620A | 3.3V DC-DC voltage regulator |
| U60, Q18 | Analog devices LTC1981, pass FET | 3.3V_SYS voltage |
| U61, U62–U65 | Analog devices LTC3888 multiphase controller and FET power stage | 0.8V VCC core VID voltage regulator |
| U61, U66 | Analog devices LTC3888 multiphase controller and FET power stage | 0.8V VCC_HSSI_GXF voltage regulator |
| U80 | Intersil ISL80101 | 0.9V VCCH_SDM LDO voltage regulator |
| U93 | Analog devices LTC7132 dual-output regulator | 1.0V VCCERT_FGT_GXF voltage regulator |
| | | 1.2V VCCR_CORE voltage regulator |
| U96 | Analog devices LTC7132 dual-output regulator | 1.8V VCCPT voltage regulator |
| | | 1.2V VCCIO_1V2 voltage regulator |
| U70 | Intersil ISL80101 | 1.0V VCCFUSEWR_GXF LDO voltage regulator |

*continued...*

| Board Reference | Type | Description |
|---|---|---|
| D28 | LT1389 VREF generation | 1.25V VREF for VCCBAT |
| U74 | Intersil ISL80101 | 1.8V VCCIO_SDM_HPS LDO voltage regulator |
| U75 | Intersil ISL80101 | 2.5V DDR4 DIMM LDO voltage regulator |
| U76 | Intersil ISL80101 | 2.5V DDR4 COMP LDO voltage regulator |
| U77 | Texas Instruments TPS51200 | 0.6V DDR4 DIMM VTT/VREF generation |
| U78 | Texas Instruments TPS51200 | 0.6V DDR4 COMP VTT/VREF generation |

### A.1.3. Intel MAX 10 CPLD System Controller

The development board utilizes the 10M50 system controller, an Intel MAX 10 CPLD for the following purposes:

- Power sequencing control
- FPGA configuration from flash memory
- On-board Intel FPGA Download Cable II
- Power monitoring
- Temperature monitoring
- Fan control
- Clock control

## A.2. FPGA Configuration

You can use the Intel Quartus Prime Programmer to configure the FPGA with your SRAM Object File (**.sof**).

Ensure the following:

- The Intel Quartus Prime Programmer and the Intel FPGA Download Cable II driver are installed on the host computer.
- The micro-USB cable is connected to the FPGA development board.
- Power to the board is ON, and no other applications that use the JTAG chain are running.

To configure the FPGA, follow these steps:

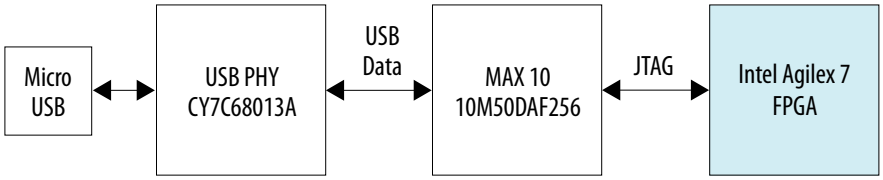
1. Start the Intel Quartus Prime Programmer.
2. Click **Auto Detect** to display the devices in the JTAG chain.
3. Click **Change File** and select the path to the desired **.sof**.
4. Turn on the **Program/Configure** option for the added file.
5. Click **Start** to download the selected file to the FPGA. Configuration is complete when the progress bar reaches 100%.

Using the Intel Quartus Prime Programmer to configure a device on the board causes other JTAG based applications such as the Board Test System and the Power Monitor to lose their connection to the board. Restart those applications after configuration is complete.

### A.2.1. Programming the FPGA over On-Board Intel FPGA Download Cable II

The figure below shows the high-level conceptual block diagram for programming the Intel Agilex 7 FPGA over the on-board Intel FPGA Download Cable II.

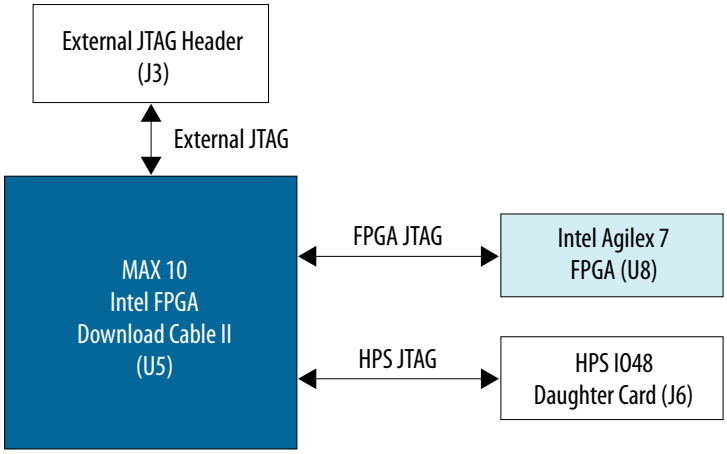
**Figure 22. Programming the FPGA over On-Board Intel FPGA Download Cable II Block Diagram**




### A.2.2. Programming the FPGA over an External Intel FPGA Download Cable II

The figure below shows the high-level conceptual block diagram for programming the Intel Agilex 7 FPGA over an external Intel FPGA Download Cable II.

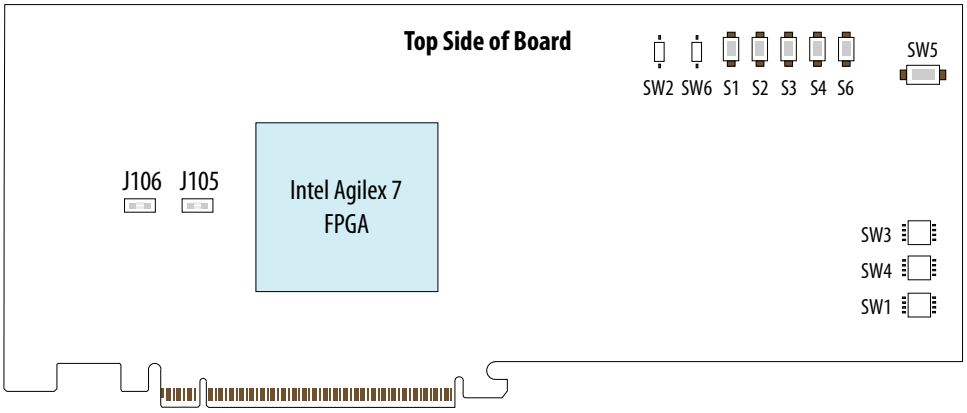
**Figure 23. Programming the FPGA over an External Intel FPGA Download Cable II Block Diagram**




## A.3. Default Switch and Jumper Settings

This section shows you how to restore the default factory settings and explains their functions.

**Figure 24. Switch and Jumper Locations**




## A.3.1. Switch Description

**Table 17. SW1—4 Position DIP for PCIe Lane Width Selection**

| Switch position | Board Label | Function | Default Position |
|---|---|---|---|
| 1 | x16 | ON for PCIe x16 | ON |
| 2 | x8 | ON for PCIe x8 | OFF |
| 3 | x4 | ON for PCIe x4 | OFF |
| 4 | x1 | ON for PCIe x1 | OFF |

**Table 18. SW2—Single DIP for Intel FPGA Download Cable II Selection**

| Switch position | Board Label | Function | Default Position |
|---|---|---|---|
| SW2 | USB MAX JTAG SEL | ON for on-board Intel FPGA Download Cable II | ON |
| | | OFF for external Intel FPGA Download Cable II | |

**Table 19. SW3—4 position DIP for Configuration Mode Selection and JTAG Control**

By default, `MSEL[2:0]` is set to '001' for AS x4 with CvP support. `MSEL0` is tied to logic high.

| Switch position | Board Label | Function | Default Position |
|---|---|---|---|
| 1 | MSEL1 | Configuration MSEL1 | ON |
| 2 | MSEL2 | Configuration MSEL2 | ON |
| 3 | BMC JTAG SEL | ON Selects On-board Blaster | ON |
| 4 | HPS JTAG BYPASS | OFF Bypass HPS JTAG | OFF |

The board only supports the following configuration modes.

**Table 20. Supported Configuration Modes**

MSEL0 is tied to logic high.

| Configuration Mode | MSEL2 | MSEL1 | MSEL0 |
|---|---|---|---|
| JTAG | 1 | 1 | 1 |
| Avalon-ST x16 | 1 | 0 | 1 |
| AS x4 Fast (CVP support) | 0 | 0 | 1 |
| AS x4 Normal | 0 | 1 | 1 |

**Table 21. SW4**

| Switch position | Board Label | Function | Default Position |
|---|---|---|---|
| 1 | SSEN | ON enables PCIe Spread Spectrum | OFF |
| 2 | CXL REFCLK Select | ON for local PCIe REFCLK on Bank12C | OFF |
| 3 | PCIe REFCLK Select | ON for local PCIe REFCLK on Bank13A | OFF |
| 4 | PCIe Clock Power-down | On powers down PCIe clock sources | OFF |

**Table 22. SW5—Slide Switch to Power On the Board**

| Switch position | Board Label | Function | Default Position |
|---|---|---|---|
| SW5 | Power On | ON to power on the board | OFF |

**Table 23. SW6—Single DIP for Intel MAX 10 JTAG Enable**

| Switch position | Board Label | Function | Default Position |
|---|---|---|---|
| SW6 | Intel MAX 10 JTAG Enable | ON to share Intel MAX 10 JTAG Pins | OFF |

**Table 24. S[1–4, 6]—Various Push-Button RESET Switches**

| Switch | Function |
|---|---|
| S1 | Used to send RESET to CPU |
| S2 | Used to send RESET to HPS |
| S3 | Used to send PERSTN to PCIe |
| S4 | Used to send 2nd PERSTN to PCIe |
| S6 | Used to send PERSTN to CXL PCIe |

## A.3.2. Jumper Description

In Avalon-ST x16 configuration mode, the board provides one QSPI flash for storing up to four configuration images. Configuration of the FPGA with one of these images is managed by the Intel MAX 10, depending on the selection of jumpers **J105** and **J106**.

**Table 25. Selected Configuration Image**

| J106 | J105 | Selected Configuration Image |
|---|---|---|
| ON | ON | Image 0 (Default) |
| ON | OFF | Image 1 |
| OFF | ON | Image 2 |
| OFF | OFF | Image 3 |

## A.4. Input and Output Components

### A.4.1. Push Buttons

The Intel Agilex 7 FPGA (two F-tiles) development board includes several dedicated push buttons for you. When you press and hold down the button, the device pin is set to logic 0. When you release the button, the device pin is set to logic 1. There are no board-specific functions for these general user push buttons.

**Table 26. Push Buttons**

| Board Reference | Schematic Signal Name | I/O Standard |
|---|---|---|
| S1 | CPU_RESETn | 3.3V |
| S2 | HPS_RESETn | 3.3V |
| S3 | PCIE_PERSTn | 1.8V |
| S4 | GFX_2ND_PERSTn | 1.8V |
| S6 | CXL_PERSTn | 3.3V |

### A.4.2. Switches

The Intel Agilex 7 FPGA (two F-tiles) development board includes user-controlled switches for selecting various features on the board. When the switch is in the OFF position, logic 1 is selected. When the switch is in the ON position, logic 0 is selected.

**Table 27. Switches**

| Board Reference | Schematic Signal Name | I/O Standard |
|---|---|---|
| SW1.1 | PCIE_EP_PRSNT_Nx16 | 3.3V |
| SW1.2 | PCIE_EP_PRSNT_Nx8 | 3.3V |
| SW1.3 | PCIE_EP_PRSNT_Nx4 | 3.3V |
| SW1.4 | PCIE_EP_PRSNT_Nx1 | 3.3V |
| SW2 | USB_MAX_JTAG_SEL | 3.3V |
| SW3.1 | FPGA_1V8_MSEL1 | 1.8V |
| SW3.2 | FPGA_1V8_MSEL2 | 1.8V |
| SW3.3 | BMC_JTAG_EN | 1.8V |
| SW3.4 | HPS_JTAG_BYPASS | 1.8V |
| SW4.1 | SI52204_SSEN | 1.8V |

*continued...*

| Board Reference | Schematic Signal Name | I/O Standard |
|---|---|---|
| SW4.2 | SEL_CXL_REFCLK | 1.8V |
| SW4.3 | SEL_PCIE_REFCLK | 1.8V |
| SW4.4 | SI52204_PWRDNB | 1.8V |
| SW5 | POWER_ON | 2.5V |
| SW6 | MAX10_JTAG_EN | 3.3V |

### A.4.3. LEDs

The Intel Agilex 7 FPGA development board provides various LEDs for indicating board status information. The LEDs illuminate when a logic 1 is driven and turn OFF when a logic 0 is driven. There are no board-specific functions for these LEDs.

**Table 28. LEDs**

| Board Reference | Schematic Signal Name | I/O Standard |
|---|---|---|
| D1 | MAX_CONF_DONE | 3.3V |
| D2 | PWRGD_OUT | 3.3V |
| D3 | QSFPDD_LED2 | 1.2V |
| D4 | QSFP_LED2 | 1.2V |
| D5 | OVERTEMP_LEDn | 3.3V |
| D6 | QSFPDD_LED1 | 1.2V |
| D7 | QSFP_LED1 | 1.2V |
| D8 | FPGA_3V3_LED0 | 1.2V |
| D9 | FPGA_3V3_LED1 | 1.2V |
| D10 | FPGA_3V3_LED2 | 1.2V |
| D11 | FPGA_3V3_LED3 | 1.2V |
| D12 | FPGA_1V8_CONF_DONE | 1.8V |
| D24 | CFG_IMAGE0 | 3.3V |
| D25 | CFG_IMAGE1 | 3.3V |

## A.5. Components and Interfaces

This section describes the development board's communication ports and interface cards relative to the Intel Agilex 7 FPGA device.

### A.5.1. PCI Express (PCIe) Interface

The Intel Agilex 7 FPGA (two F-tiles) development board is designed to fit entirely into a PC motherboard with a x16 PCI Express slot that can accommodate a full height, 2-slot, ¾ length form factor add-in card. This interface uses the Intel Agilex 7 FPGA's PCI Express hard IP block, saving logic resources for the user logic application. The PCI Express edge connector has a presence detect feature to allow the motherboard to determine if a card is installed.

The PCI Express interface supports auto-negotiating channel width from x1 to x4 to x8 to x16 by using PCIe Intel FPGA IP. You can also configure this board to a x1, x4, x8, or x16 interface through a DIP switch that connects the PRSTn pins for each bus width.

The PCI Express edge connector has a connection speed of 2.5 Gbps/lane for a maximum of 40 Gbps full-duplex (Gen 1), 5.0 Gbps/lane for maximum of 80 Gbps full-duplex (Gen 2), or 8.0 Gbps/lane for a maximum of 128 Gbps full-duplex (Gen 3), and 16.0 Gbps/lane for a maximum of 256 Gbps full-duplex (Gen 4).

The power for the board can be sourced entirely from the PC host when installed into a PC motherboard with the PC's 2x4 ATX auxiliary power connected to the 12V ATX inputs (**J11**) of the Intel Agilex 7 FPGA (two F-tiles) development board. Although the board can also be powered by an externally supplied power supply for use on a lab bench, Intel recommends that you do not power up from both supplies at the same time. Ideal diode power sharing devices have been designed into this board to prevent damages or backcurrent from one supply to the other.

The REFCLK_PCIE_EP_EDGE_P/N signal is a 100 MHz differential input that is driven from the PC motherboard onto this board through the edge connector. This signal connects directly to a Intel Agilex 7 FPGA REFCLK input pin pair using DC coupling. This clock is terminated on the motherboard. Therefore, no on-board termination is required. This clock can have spread-spectrum properties that change its period between 9.847 ps to 10.203 ps. The I/O standard is high-speed current steering logic (HCSL).

**Table 29. PCI Express (PCIe) Pin Assignments**

| Edge Finger pin Number | Schematic Signal Name | FPGA Pin Number | I/O Standard | Description |
|---|---|---|---|---|
| A11 | PCIE_3V3_EP_PERSTN | MAX10 (U5) | 3V LVCMOS | Reset |
| A14 | REFCLK_PCIE_EP_EDGE_N | Clock Buffer (U26) | LVDS | Motherboard reference clock |
| A13 | REFCLK_PCIE_EP_EDGE_P | Clock Buffer (U26) | LVDS | Motherboard reference clock |
| B5 | PCIE_3V3_EP_SMBCLK | FRUID EEPROM (U2) | 1.8V | SMB clock |
| B6 | PCIE_3V3_EP_SMBDAT | FRUID EEPROM (U2) | 1.8V | SMB data |
| A1 | PCIE_EP_PRSNT_N | — | — | Link with DIP switch (SW1) |
| B17 | PCIE_EP_PRSNT_Nx1 | — | — | Link with DIP switch (SW1) |
| B31 | PCIE_EP_PRSNT_Nx4 | — | — | Link with DIP switch (SW1) |
| B48 | PCIE_EP_PRSNT_Nx8 | — | — | Link with DIP switch (SW1) |
| B81 | PCIE_EP_PRSNT_Nx16 | — | — | Link with DIP switch (SW1) |
| B15 | PCIE_EP_TX_N0 | AG5 | 1.4 V PCML | Receive bus |

*continued...*

| Edge Finger pin Number | Schematic Signal Name | FPGA Pin Number | I/O Standard | Description |
|---|---|---|---|---|
| B20 | PCIE_EP_TX_N1 | AH2 | 1.4 V PCML | Receive bus |
| B24 | PCIE_EP_TX_N2 | AM2 | 1.4 V PCML | Receive bus |
| B28 | PCIE_EP_TX_N3 | AT2 | 1.4 V PCML | Receive bus |
| B34 | PCIE_EP_TX_N4 | AY2 | 1.4 V PCML | Receive bus |
| B38 | PCIE_EP_TX_N5 | BD2 | 1.4 V PCML | Receive bus |
| B42 | PCIE_EP_TX_N6 | BH2 | 1.4 V PCML | Receive bus |
| B46 | PCIE_EP_TX_N7 | BM2 | 1.4 V PCML | Receive bus |
| B51 | PCIE_EP_TX_N8 | BT2 | 1.4 V PCML | Receive bus |
| B55 | PCIE_EP_TX_N9 | BY2 | 1.4 V PCML | Receive bus |
| B59 | PCIE_EP_TX_N10 | CD2 | 1.4 V PCML | Receive bus |
| B63 | PCIE_EP_TX_N11 | CH2 | 1.4 V PCML | Receive bus |
| B67 | PCIE_EP_TX_N12 | CM2 | 1.4 V PCML | Receive bus |
| B71 | PCIE_EP_TX_N13 | CR5 | 1.4 V PCML | Receive bus |
| B75 | PCIE_EP_TX_N14 | CT2 | 1.4 V PCML | Receive bus |
| B79 | PCIE_EP_TX_N5 | CW5 | 1.4 V PCML | Receive bus |
| B14 | PCIE_EP_TX_P0 | AF4 | 1.4 V PCML | Receive bus |
| B19 | PCIE_EP_TX_P1 | AJ1 | 1.4 V PCML | Receive bus |
| B23 | PCIE_EP_TX_P2 | AN1 | 1.4 V PCML | Receive bus |
| B27 | PCIE_EP_TX_P3 | AU1 | 1.4 V PCML | Receive bus |
| B33 | PCIE_EP_TX_P4 | BA1 | 1.4 V PCML | Receive bus |
| B37 | PCIE_EP_TX_P5 | BE1 | 1.4 V PCML | Receive bus |
| B41 | PCIE_EP_TX_P6 | BJ1 | 1.4 V PCML | Receive bus |
| B45 | PCIE_EP_TX_P7 | BN1 | 1.4 V PCML | Receive bus |
| B50 | PCIE_EP_TX_P8 | BU1 | 1.4 V PCML | Receive bus |
| B54 | PCIE_EP_TX_P9 | CA1 | 1.4 V PCML | Receive bus |
| B58 | PCIE_EP_TX_P10 | CE1 | 1.4 V PCML | Receive bus |
| B62 | PCIE_EP_TX_P11 | CJ1 | 1.4 V PCML | Receive bus |
| B66 | PCIE_EP_TX_P12 | CN1 | 1.4 V PCML | Receive bus |
| B70 | PCIE_EP_TX_P13 | CP4 | 1.4 V PCML | Receive bus |
| B74 | PCIE_EP_TX_P14 | CU1 | 1.4 V PCML | Receive bus |
| B78 | PCIE_EP_TX_P15 | CV4 | 1.4 V PCML | Receive bus |
| A17 | PCIE_EP_RX_N0 | AL5 | 1.4 V PCML | Transmit bus |
| A22 | PCIE_EP_RX_N1 | AM8 | 1.4 V PCML | Transmit bus |
| A26 | PCIE_EP_RX_N2 | AR5 | 1.4 V PCML | Transmit bus |
| A30 | PCIE_EP_RX_N3 | AT8 | 1.4 V PCML | Transmit bus |
| A36 | PCIE_EP_RX_N4 | AW5 | 1.4 V PCML | Transmit bus |

*continued...*

| Edge Finger pin Number | Schematic Signal Name | FPGA Pin Number | I/O Standard | Description |
|---|---|---|---|---|
| A40 | PCIE_EP_RX_N5 | AY8 | 1.4 V PCML | Transmit bus |
| A44 | PCIE_EP_RX_N6 | BC5 | 1.4 V PCML | Transmit bus |
| A48 | PCIE_EP_RX_N7 | BG5 | 1.4 V PCML | Transmit bus |
| A53 | PCIE_EP_RX_N8 | BL5 | 1.4 V PCML | Transmit bus |
| A57 | PCIE_EP_RX_N9 | BR5 | 1.4 V PCML | Transmit bus |
| A61 | PCIE_EP_RX_N10 | BW5 | 1.4 V PCML | Transmit bus |
| A65 | PCIE_EP_RX_N11 | CC5 | 1.4 V PCML | Transmit bus |
| A69 | PCIE_EP_RX_N12 | CG5 | 1.4 V PCML | Transmit bus |
| A73 | PCIE_EP_RX_N13 | CL5 | 1.4 V PCML | Transmit bus |
| A77 | PCIE_EP_RX_N14 | CM8 | 1.4 V PCML | Transmit bus |
| A81 | PCIE_EP_RX_N15 | CT8 | 1.4 V PCML | Transmit bus |
| A16 | PCIE_EP_RX_P0 | AK4 | 1.4 V PCML | Transmit bus |
| A21 | PCIE_EP_RX_P1 | AN7 | 1.4 V PCML | Transmit bus |
| A25 | PCIE_EP_RX_P2 | AP4 | 1.4 V PCML | Transmit bus |
| A29 | PCIE_EP_RX_P3 | AU7 | 1.4 V PCML | Transmit bus |
| A35 | PCIE_EP_RX_P4 | AV4 | 1.4 V PCML | Transmit bus |
| A39 | PCIE_EP_RX_P5 | BA7 | 1.4 V PCML | Transmit bus |
| A43 | PCIE_EP_RX_P6 | BB4 | 1.4 V PCML | Transmit bus |
| A47 | PCIE_EP_RX_P7 | BF4 | 1.4 V PCML | Transmit bus |
| A52 | PCIE_EP_RX_P8 | BK4 | 1.4 V PCML | Transmit bus |
| A56 | PCIE_EP_RX_P9 | BP4 | 1.4 V PCML | Transmit bus |
| A60 | PCIE_EP_RX_P10 | BV4 | 1.4 V PCML | Transmit bus |
| A64 | PCIE_EP_RX_p11 | CB4 | 1.4 V PCML | Transmit bus |
| A68 | PCIE_EP_RX_P12 | CF4 | 1.4 V PCML | Transmit bus |
| A72 | PCIE_EP_RX_P13 | CK4 | 1.4 V PCML | Transmit bus |
| A76 | PCIE_EP_RX_P14 | CN7 | 1.4 V PCML | Transmit bus |
| A80 | PCIE_EP_RX_P15 | CU7 | 1.4 V PCML | Transmit bus |
| B11 | PCIE_3V3_EP_WAKE | — | 3.3V | Wake Signal |
| B12 | PCIE_3V3_EP_CLKREQn | — | 3.3V | Clock Request |

## A.5.2. QSFP-DD Interface

The Intel Agilex 7 FPGA (two F-tiles) development board includes a connector and cages system for mounting a Double Density Quad Small Form-Factor Pluggable (QSFP-DD) module. The interface connects to eight 56 Gbps PAM4 capable F-tile lanes of the Intel Agilex 7 FPGA, supporting QSFP-DD modules, with capability of 400 Gbps aggregate bandwidth with power classifications up to 10 W.

## Table 30. QSFP-DD Pin Assignments

| Schematic Signal Name | FPGA Pin Number | I/O Standard | Description |
|---|---|---|---|
| QSFPDD_TX0_P | AV52 | True Differential Signaling | QSFPDD Transmit Channel 0 Positive |
| QSFPDD_TX0_N | AU51 | True Differential Signaling | QSFPDD Transmit Channel 0 negative |
| QSFPDD_TX1_P | R49 | True Differential Signaling | QSFPDD Transmit Channel 1 Positive |
| QSFPDD_TX1_N | T48 | True Differential Signaling | QSFPDD Transmit Channel 1 negative |
| QSFPDD_TX2_P | AN51 | True Differential Signaling | QSFPDD Transmit Channel 2 Positive |
| QSFPDD_TX2_N | AP52 | True Differential Signaling | QSFPDD Transmit Channel 2 negative |
| QSFPDD_TX3_P | U51 | True Differential Signaling | QSFPDD Transmit Channel 3 Positive |
| QSFPDD_TX3_N | V52 | True Differential Signaling | QSFPDD Transmit Channel 3 negative |
| QSFPDD_TX4_P | AF52 | True Differential Signaling | QSFPDD Transmit Channel 4 Positive |
| QSFPDD_TX4_N | AE51 | True Differential Signaling | QSFPDD Transmit Channel 4 negative |
| QSFPDD_TX5_P | Y48 | True Differential Signaling | QSFPDD Transmit Channel 5 Positive |
| QSFPDD_TX5_N | W49 | True Differential Signaling | QSFPDD Transmit Channel 5 negative |
| QSFPDD_TX6_P | AJ51 | True Differential Signaling | QSFPDD Transmit Channel 6 Positive |
| QSFPDD_TX6_N | AK52 | True Differential Signaling | QSFPDD Transmit Channel 6 negative |
| QSFPDD_TX7_P | AA51 | True Differential Signaling | QSFPDD Transmit Channel 7 Positive |
| QSFPDD_TX7_N | AB52 | True Differential Signaling | QSFPDD Transmit Channel 7 negative |
| QSFPDD_RX0_P | AR55 | True Differential Signaling | QSFPDD Receive Channel 0 Positive |
| QSFPDD_RX0_N | AT54 | True Differential Signaling | QSFPDD Receive Channel 0 negative |
| QSFPDD_RX1_P | K52 | True Differential Signaling | QSFPDD Receive Channel 1 Positive |
| QSFPDD_RX1_N | J51 | True Differential Signaling | QSFPDD Receive Channel 1 negative |
| QSFPDD_RX2_P | AL55 | True Differential Signaling | QSFPDD Receive Channel 2 Positive |
| QSFPDD_RX2_N | AM54 | True Differential Signaling | QSFPDD Receive Channel 2 negative |
| QSFPDD_RX3_P | P52 | True Differential Signaling | QSFPDD Receive Channel 3 Positive |
| QSFPDD_RX3_N | N51 | True Differential Signaling | QSFPDD Receive Channel 3 negative |
| QSFPDD_RX4_P | AC55 | True Differential Signaling | QSFPDD Receive Channel 4 Positive |
| QSFPDD_RX4_N | AD54 | True Differential Signaling | QSFPDD Receive Channel 4 negative |
| QSFPDD_RX5_P | R55 | True Differential Signaling | QSFPDD Receive Channel 5 Positive |
| QSFPDD_RX5_N | T54 | True Differential Signaling | QSFPDD Receive Channel 5 negative |
| QSFPDD_RX6_P | AG55 | True Differential Signaling | QSFPDD Receive Channel 6 Positive |
| QSFPDD_RX6_N | AH54 | True Differential Signaling | QSFPDD Receive Channel 6 negative |
| QSFPDD_RX7_P | W55 | True Differential Signaling | QSFPDD Receive Channel 7 Positive |
| QSFPDD_RX7_N | Y54 | True Differential Signaling | QSFPDD Receive Channel 7 negative |
| QSFPDD_REFCLK_P | AD48 | LVPECL | QSFPDD Reference Clock Positive |

*continued...*

| Schematic Signal Name | FPGA Pin Number | I/O Standard | Description |
|---|---|---|---|
| QSFPDD_REFCLK_N | AC49 | LVPECL | QSFPDD Reference Clock Negative |
| QSFPDD_LED1 (Yellow LED) | G49 | 1.2V HS LVCMOS | QSFPDD Yellow LED |
| QSFPDD_LED2 (Green LED) | F48 | 1.2V HS LVCMOS | QSFPDD Green LED |

*Note:* For more information about Intel's True Differential Signaling technology, refer to the *Intel Agilex 7 Device Data Sheet*.

## A.5.3. QSFP Interface

The Intel Agilex 7 FPGA (two F-tiles) development board includes a connector and cages system for mounting a Quad Small Form-Factor Pluggable (QSFP) module. The interface connects to four 56 Gbps PAM4 capable F-tile lanes of the Intel Agilex 7 FPGA, supporting QSFP modules, with capability of 200 Gbps aggregate bandwidth with power classifications up to 3.5 W.

### Table 31. QSFP Pin Assignments

For more information about Intel's True Differential Signaling technology, refer to the *Intel Agilex 7* Device Data Sheet.

| Schematic Signal Name | FPGA Pin Number | I/O Standard | Description |
|---|---|---|---|
| QSFP_TX0_P | BL49 | True Differential Signaling | QSFP Transmit Channel 0 Positive |
| QSFP_TX0_N | BM48 | True Differential Signaling | QSFP Transmit Channel 0 negative |
| QSFP_TX1_P | BB52 | True Differential Signaling | QSFP Transmit Channel 1 Positive |
| QSFP_TX1_N | BA51 | True Differential Signaling | QSFP Transmit Channel 1 negative |
| QSFP_TX2_P | BJ51 | True Differential Signaling | QSFP Transmit Channel 2 Positive |
| QSFP_TX2_N | BK52 | True Differential Signaling | QSFP Transmit Channel 2 negative |
| QSFP_TX3_P | BE51 | True Differential Signaling | QSFP Transmit Channel 3 Positive |
| QSFP_TX3_N | BF52 | True Differential Signaling | QSFP Transmit Channel 3 negative |
| QSFP_RX0_P | BL55 | True Differential Signaling | QSFP Receive Channel 0 Positive |
| QSFP_RX0_N | BM54 | True Differential Signaling | QSFP Receive Channel 0 negative |
| QSFP_RX1_P | AW55 | True Differential Signaling | QSFP Receive Channel 1 Positive |
| QSFP_RX1_N | AY54 | True Differential Signaling | QSFP Receive Channel 1 negative |
| QSFP_RX2_P | BH54 | True Differential Signaling | QSFP Receive Channel 2 Positive |
| QSFP_RX2_N | BG55 | True Differential Signaling | QSFP Receive Channel 2 negative |
| QSFP_RX3_P | BC55 | True Differential Signaling | QSFP Receive Channel 3 Positive |
| QSFP_RX3_N | BD54 | True Differential Signaling | QSFP Receive Channel 3 negative |
| QSFP_REFCLK_P | AW49 | 156.25 MHz LVPECL | QSFP Reference Clock |
| | | | Positive |
| QSFP_REFCLK_N | AV48 | 156.25 MHz LVPECL | QSFP Reference Clock Negative |
| QSFP_LED1 (Yellow LED) | B48 | 1.2 V HS LVCMOS | QSFPDD Yellow LED |
| QSFP_LED2 (Green LED) | A47 | 1.2 V HS LVCMOS | QSFPDD Green LED |

## A.5.4. CXL Interface

The Intel Agilex 7 FPGA (two F-tiles) development board provides a CXL connector interface for cabling to an Intel-designed M.2 SSD daughter card supporting M-Keying. This interface connects to four 28 Gbps F-tile lanes of the Intel Agilex 7 FPGA. When connecting the development board to this SSD daughter card, the development board connects four transceiver channels from the F-tile bank 12C to M2 channels 8-11 (**J5**) of the M.2 daughter card.

**Table 32. CXL Pin Assignments**

| Schematic Signal Name | FPGA Pin Number | I/O Standard | Description |
|---|---|---|---|
| CXL_TX_P0 | BW49 | True Differential Signaling | CXL Transmit Channel 0 Positive |
| CXL_TX_N0 | BY48 | True Differential Signaling | CXL Transmit Channel 0 Negative |
| CXL_TX_P1 | BV52 | True Differential Signaling | CXL Transmit Channel 1 Positive |
| CXL_TX_N1 | BU51 | True Differential Signaling | CXL Transmit Channel 1 Negative |
| CXL_TX_P2 | BR49 | True Differential Signaling | CXL Transmit Channel 2 Positive |
| CXL_TX_N2 | BT48 | True Differential Signaling | CXL Transmit Channel 2 Negative |
| CXL_TX_P3 | BP52 | True Differential Signaling | CXL Transmit Channel 3 Positive |
| CXL_TX_N3 | BN51 | True Differential Signaling | CXL Transmit Channel 3 Negative |
| CXL_RX_P0 | CC55 | True Differential Signaling | CXL Receive Channel 0 |
| | | | Positive |
| CXL_RX_N0 | CD54 | True Differential Signaling | CXL Receive Channel 0 Negative |
| CXL_RX_P1 | CB52 | True Differential Signaling | CXL Receive Channel 1 |
| | | | Positive |
| CXL_RX_N1 | CA51 | True Differential Signaling | CXL Receive Channel 1 Negative |
| CXL_RX_P2 | BW55 | True Differential Signaling | CXL Receive Channel 2 |
| | | | Positive |
| CXL_RX_N2 | BY54 | True Differential Signaling | CXL Receive Channel 2 Negative |
| CXL_RX_P3 | BR55 | True Differential Signaling | CXL Receive Channel 3 |
| | | | Positive |
| CXL_RX_N3 | BT54 | True Differential Signaling | CXL Receive Channel 3 Negative |
| REFCLK_CXL_EP_P | BC49 | 100 MHz LVPECL | CXL Reference Clock |
| | | | Positive, Local board clock |
| REFCLK_CXL_EP_N | BE49 | 100 MHz LVPECL | CXL Reference Clock |
| | | | Negative, Local board clock |
| REFCLK_CXL_CONN_P | BG49 | 100 MHz LVPECL | CXL Reference Clock |
| | | | Positive, Remote board clock |
| REFCLK_CLK_CONN_N | BF48 | 100 MHz LVPECL | CXL Reference Clock |

*continued...*

| Schematic Signal Name | FPGA Pin Number | I/O Standard | Description |
|---|---|---|---|
| | | | Negative, Remote board clock |
| CXL_PERSTN | D43 | 1.2 V HS LVCMOS | CXL Reset |
| CXL_PRSNTx4_N | F50 | 1.2 V HS LVCMOS | CXL Present |

## A.5.5. DDR4 DIMM1 Interface

The Intel Agilex 7 FPGA (two F-tiles) development board provides two DDR4 x72 DIMM interfaces connected to the FPGA fabric. DIMM1 is connected to the Intel Agilex 7 I/O96 of banks 2C and 2D. Only one DIMM memory module is included with the development kit for evaluation of the DDR4 interfaces.

**Table 33. DIMM1 Pin Assignments**

| Schematic Signal Name | FPGA Pin Number | I/O Standard | Description |
|---|---|---|---|
| DDR4_DIMM1_DQ0 | DC31 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ0 data |
| DDR4_DIMM1_DQ1 | DD30 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ1 data |
| DDR4_DIMM1_DQ2 | CY30 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ2 data |
| DDR4_DIMM1_DQ3 | DA31 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ3 data |
| DDR4_DIMM1_DQ4 | DA27 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ4 data |
| DDR4_DIMM1_DQ5 | CY26 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ5 data |
| DDR4_DIMM1_DQ6 | DC27 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ6 data |
| DDR4_DIMM1_DQ7 | DD26 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ7 data |
| DDR4_DIMM1_DQS_P0 | DD28 | 1.2 V HS LVCMOS | DDR4 DIMM1 Data Strobe |
| | | | Positive for byte lane 0 |
| DDR4_DIMM1_DQS_N0 | DC29 | 1.2 V HS LVCMOS | DDR4 DIMM1 Data Strobe |
| | | | Negative for byte lane 0 |
| DDR4_DIMM1_DBI_N0 | CY28 | 1.2 V HS LVCMOS | DDR4 DIMM1 Data Bus Inversion for byte lane 0 |
| DDR4_DIMM1_TDQS_N9 | DA29 | 1.2 V HS LVCMOS | DDR4 DIMM1 Termination Data Strobe for byte lane 0 |
| DDR4_DIMM1_DQ8 | DF20 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ8 data |
| DDR4_DIMM1_DQ9 | DJ21 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ9 data |
| DDR4_DIMM1_DQ10 | DH20 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ10 data |
| DDR4_DIMM1_DQ11 | DE21 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ11 data |
| DDR4_DIMM1_DQ12 | DF16 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ12 data |
| DDR4_DIMM1_DQ13 | DH16 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ13 data |
| DDR4_DIMM1_DQ14 | DE17 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ14 data |
| DDR4_DIMM1_DQ15 | DJ17 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ15 data |
| DDR4_DIMM1_DQS_P1 | DH18 | 1.2 V HS LVCMOS | DDR4 DIMM1 Data Strobe |
| | | | Positive for byte lane 1 |
| DDR4_DIMM1_DQS_N1 | DJ19 | 1.2 V HS LVCMOS | DDR4 DIMM1 Data Strobe |

*continued...*

| Schematic Signal Name | FPGA Pin Number | I/O Standard | Description |
|---|---|---|---|
| | | | Negative for byte lane 1 |
| DDR4_DIMM1_DBI_N1 | DF18 | 1.2 V HS LVCMOS | DDR4 DIMM1 Data Bus Inversion for byte lane 1 |
| DDR4_DIMM1_TDQS_N10 | DE19 | 1.2 V HS LVCMOS | DDR4 DIMM1 Termination Data Strobe for byte lane 1 |
| DDR4_DIMM1_DQ16 | DF8 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ16 data |
| DDR4_DIMM1_DQ17 | DH8 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ17 data |
| DDR4_DIMM1_DQ18 | DE9 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ18 data |
| DDR4_DIMM1_DQ19 | DJ9 | 1.2 V HS LVCMOS | DDR4 DIMM1 D19 data |
| DDR4_DIMM1_DQ20 | DF2 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ20 data |
| DDR4_DIMM1_DQ21 | DE3 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ21 data |
| DDR4_DIMM1_DQ22 | DF4 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ22 data |
| DDR4_DIMM1_DQ23 | DE5 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ23 data |
| DDR4_DIMM1_DQS_P2 | DH6 | 1.2 V HS LVCMOS | DDR4 DIMM1 Data Strobe |
| | | | Positive for byte lane 2 |
| DDR4_DIMM1_DQS_N2 | DJ7 | 1.2 V HS LVCMOS | DDR4 DIMM1 Data Strobe |
| | | | Negative for byte lane 2 |
| DDR4_DIMM1_DBI_N2 | DF6 | 1.2 V HS LVCMOS | DDR4 DIMM1 Data Bus Inversion for byte lane 2 |
| DDR4_DIMM1_TDQS_N11 | DE7 | 1.2 V HS LVCMOS | DDR4 DIMM1 Termination Data Strobe for byte lane 2 |
| DDR4_DIMM1_DQ24 | DE15 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ24 data |
| DDR4_DIMM1_DQ25 | DF14 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ25 data |
| DDR4_DIMM1_DQ26 | DJ15 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ26 data |
| DDR4_DIMM1_DQ27 | DH14 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ27 data |
| DDR4_DIMM1_DQ28 | DF10 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ28 data |
| DDR4_DIMM1_DQ29 | DH10 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ29 data |
| DDR4_DIMM1_DQ30 | DJ11 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ30 data |
| DDR4_DIMM1_DQ31 | DE11 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ31 data |
| DDR4_DIMM1_DQS_P3 | DH12 | 1.2 V HS LVCMOS | DDR4 DIMM1 Data Strobe |
| | | | Positive for byte lane 3 |
| DDR4_DIMM1_DQS_N3 | DJ13 | 1.2 V HS LVCMOS | DDR4 DIMM1 Data Strobe |
| | | | Negative for byte lane 3 |
| DDR4_DIMM1_DBI_N3 | DF12 | 1.2 V HS LVCMOS | DDR4 DIMM1 Data Bus Inversion for byte lane 3 |
| DDR4_DIMM1_TDQS_N12 | DE13 | 1.2 V HS LVCMOS | DDR4 DIMM1 Termination Data Strobe for byte lane 3 |
| DDR4_DIMM1_DQ32 | DH26 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ32 data |
| DDR4_DIMM1_DQ33 | DE27 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ33 data |
| DDR4_DIMM1_DQ34 | DF26 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ34 data |
| DDR4_DIMM1_DQ35 | DJ27 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ35 data |
| DDR4_DIMM1_DQ36 | DE23 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ36 data |

*continued...*

| Schematic Signal Name | FPGA Pin Number | I/O Standard | Description |
|---|---|---|---|
| DDR4_DIMM1_DQ37 | DF22 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ37 data |
| DDR4_DIMM1_DQ38 | DJ23 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ38 data |
| DDR4_DIMM1_DQ39 | DH22 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ39 data |
| DDR4_DIMM1_DQS_P4 | DH24 | 1.2 V HS LVCMOS | DDR4 DIMM1 Data Strobe |
| | | | Positive for byte lane 4 |
| DDR4_DIMM1_DQS_N4 | DJ25 | 1.2 V HS LVCMOS | DDR4 DIMM1 Data Strobe |
| | | | Negative for byte lane 4 |
| DDR4_DIMM1_DBI_N4 | DF24 | 1.2 V HS LVCMOS | DDR4 DIMM1 Data Bus Inversion for byte lane 4 |
| DDR4_DIMM1_TDQS_N13 | DE25 | 1.2 V HS LVCMOS | DDR4 DIMM1 Termination Data Strobe for byte lane 4 |
| DDR4_DIMM1_DQ40 | DC19 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ40 data |
| DDR4_DIMM1_DQ41 | DD18 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ41 data |
| DDR4_DIMM1_DQ42 | CY18 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ42 data |
| DDR4_DIMM1_DQ43 | DA19 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ43 data |
| DDR4_DIMM1_DQ44 | CY14 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ44 data |
| DDR4_DIMM1_DQ45 | DA15 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ45 data |
| DDR4_DIMM1_DQ46 | DC15 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ46 data |
| DDR4_DIMM1_DQ47 | DD14 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ47 data |
| DDR4_DIMM1_DQS_P5 | DD16 | 1.2 V HS LVCMOS | DDR4 DIMM1 Data Strobe |
| | | | Positive for byte lane 5 |
| DDR4_DIMM1_DQS_N5 | DC17 | 1.2 V HS LVCMOS | DDR4 DIMM1 Data Strobe |
| | | | Negative for byte lane 5 |
| DDR4_DIMM1_DBI_N5 | CY16 | 1.2 V HS LVCMOS | DDR4 DIMM1 Data Bus Inversion for byte lane 5 |
| DDR4_DIMM1_TDQS_N14 | DA17 | 1.2 V HS LVCMOS | DDR4 DIMM1 Termination Data Strobe for byte lane 5 |
| DDR4_DIMM1_DQ48 | CY24 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ48 data |
| DDR4_DIMM1_DQ49 | DD24 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ49 data |
| DDR4_DIMM1_DQ50 | DC25 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ50 data |
| DDR4_DIMM1_DQ51 | DA25 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ51 data |
| DDR4_DIMM1_DQ52 | CY20 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ52 data |
| DDR4_DIMM1_DQ53 | DC21 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ53 data |
| DDR4_DIMM1_DQ54 | DA21 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ54 data |
| DDR4_DIMM1_DQ55 | DD20 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ55 data |
| DDR4_DIMM1_DQS_P6 | DD22 | 1.2 V HS LVCMOS | DDR4 DIMM1 Data Strobe |
| | | | Positive for byte lane 6 |
| DDR4_DIMM1_DQS_N6 | DC23 | 1.2 V HS LVCMOS | DDR4 DIMM1 Data Strobe |
| | | | Negative for byte lane 6 |
| DDR4_DIMM1_DBI_N6 | CY22 | 1.2 V HS LVCMOS | DDR4 DIMM1 Data Bus Inversion for byte lane 6 |

*continued...*

| Schematic Signal Name | FPGA Pin Number | I/O Standard | Description |
|---|---|---|---|
| DDR4_DIMM1_TDQS_N15 | DA23 | 1.2 V HS LVCMOS | DDR4 DIMM1 Termination Data Strobe for byte lane 6 |
| DDR4_DIMM1_DQ56 | CY12 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ56 data |
| DDR4_DIMM1_DQ57 | DC13 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ57 data |
| DDR4_DIMM1_DQ58 | DA13 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ58 data |
| DDR4_DIMM1_DQ59 | DD12 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ59 data |
| DDR4_DIMM1_DQ60 | DC9 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ60 data |
| DDR4_DIMM1_DQ61 | DA9 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ61 data |
| DDR4_DIMM1_DQ62 | CY8 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ62 data |
| DDR4_DIMM1_DQ63 | DD8 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ63 data |
| DDR4_DIMM1_DQS_P7 | DD10 | 1.2 V HS LVCMOS | DDR4 DIMM1 Data Strobe |
| | | | Positive for byte lane 7 |
| DDR4_DIMM1_DQS_N7 | DC11 | 1.2 V HS LVCMOS | DDR4 DIMM1 Data Strobe |
| | | | Negative for byte lane 7 |
| DDR4_DIMM1_DBI_N7 | CY10 | 1.2 V HS LVCMOS | DDR4 DIMM1 Data Bus Inversion for byte lane 7 |
| DDR4_DIMM1_TDQS_N16 | DA11 | 1.2 V HS LVCMOS | DDR4 DIMM1 Termination Data Strobe for byte lane 7 |
| DDR4_DIMM1_DQ64 | CW23 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ64 data |
| DDR4_DIMM1_DQ65 | CV22 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ65 data |
| DDR4_DIMM1_DQ66 | CT22 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ66 data |
| DDR4_DIMM1_DQ67 | CR23 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ67 data |
| DDR4_DIMM1_DQ68 | CR19 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ68 data |
| DDR4_DIMM1_DQ69 | CV18 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ69 data |
| DDR4_DIMM1_DQ70 | CW19 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ70 data |
| DDR4_DIMM1_DQ71 | CT18 | 1.2 V HS LVCMOS | DDR4 DIMM1 DQ71 data |
| DDR4_DIMM1_DQS_P8 | CV20 | 1.2 V HS LVCMOS | DDR4 DIMM1 Data Strobe |
| | | | Positive for byte lane 8 |
| DDR4_DIMM1_DQS_N8 | CW21 | 1.2 V HS LVCMOS | DDR4 DIMM1 Data Strobe |
| | | | Negative for byte lane 8 |
| DDR4_DIMM1_DBI_N8 | CT20 | 1.2 V HS LVCMOS | DDR4 DIMM1 Data Bus Inversion for byte lane 8 |
| DDR4_DIMM1_TDQS_N17 | CR21 | 1.2 V HS LVCMOS | DDR4 DIMM1 Termination Data Strobe for byte lane 8 |
| DDR4_DIMM1_C1 | CN29 | 1.2 V HS LVCMOS | DDR4 DIMM1 Stacked Device Chip ID 1 |
| DDR4_DIMM1_C0 | CP28 | 1.2 V HS LVCMOS | DDR4 DIMM1 Stacked Device Chip ID 0 |
| DDR4_DIMM1_BG0 | CR25 | 1.2 V HS LVCMOS | DDR4 DIMM1 Bank Group 0 |
| DDR4_DIMM1_BA1 | CT24 | 1.2 V HS LVCMOS | DDR4 DIMM1 Bank Address 1 |
| DDR4_DIMM1_BA0 | CW25 | 1.2 V HS LVCMOS | DDR4 DIMM1 Bank Address 0 |
| DDR4_DIMM1_A17 | CV24 | 1.2 V HS LVCMOS | DDR4 DIMM1 Address 17 |
| DDR4_DIMM1_A16 | CR27 | 1.2 V HS LVCMOS | DDR4 DIMM1 Address 16 |

*continued...*

| Schematic Signal Name | FPGA Pin Number | I/O Standard | Description |
|---|---|---|---|
| DDR4_DIMM1_A15 | CT26 | 1.2 V HS LVCMOS | DDR4 DIMM1 Address 15 |
| DDR4_DIMM1_A14 | CW27 | 1.2 V HS LVCMOS | DDR4 DIMM1 Address 14 |
| DDR4_DIMM1_A13 | CV26 | 1.2 V HS LVCMOS | DDR4 DIMM1 Address 13 |
| DDR4_DIMM1_A12 | CR29 | 1.2 V HS LVCMOS | DDR4 DIMM1 Address 12 |
| DDR4_DIMM1_A11 | CR31 | 1.2 V HS LVCMOS | DDR4 DIMM1 Address 11 |
| DDR4_DIMM1_A10 | CT30 | 1.2 V HS LVCMOS | DDR4 DIMM1 Address 10 |
| DDR4_DIMM1_A9 | CW31 | 1.2 V HS LVCMOS | DDR4 DIMM1 Address 9 |
| DDR4_DIMM1_A8 | CV30 | 1.2 V HS LVCMOS | DDR4 DIMM1 Address 8 |
| DDR4_DIMM1_A7 | CR33 | 1.2 V HS LVCMOS | DDR4 DIMM1 Address 7 |
| DDR4_DIMM1_A6 | CT32 | 1.2 V HS LVCMOS | DDR4 DIMM1 Address 6 |
| DDR4_DIMM1_A5 | CW33 | 1.2 V HS LVCMOS | DDR4 DIMM1 Address 5 |
| DDR4_DIMM1_A4 | CV32 | 1.2 V HS LVCMOS | DDR4 DIMM1 Address 4 |
| DDR4_DIMM1_A3 | CR35 | 1.2 V HS LVCMOS | DDR4 DIMM1 Address 3 |
| DDR4_DIMM1_A2 | CT34 | 1.2 V HS LVCMOS | DDR4 DIMM1 Address 2 |
| DDR4_DIMM1_A1 | CW35 | 1.2 V HS LVCMOS | DDR4 DIMM1 Address 1 |
| DDR4_DIMM1_A0 | CV34 | 1.2 V HS LVCMOS | DDR4 DIMM1 Address 0 |
| DDR4_DIMM1_PAR | CL31 | 1.2 V HS LVCMOS | DDR4 DIMM1 Parity |
| DDR4_DIMM1_CS_N1 | CK30 | 1.2 V HS LVCMOS | DDR4 DIMM1 Chip Select 1 |
| DDR4_DIMM1_CK_N0 | CN31 | 1.2 V HS LVCMOS | DDR4 DIMM1 Clock 0, |
| | | | Positive |
| DDR4_DIMM1_CK_P0 | CP30 | 1.2 V HS LVCMOS | DDR4 DIMM1 Clock 0, |
| | | | Negative |
| DDR4_DIMM1_CKE1 | CL33 | 1.2 V HS LVCMOS | DDR4 DIMM1 Clock Enable 1 |
| DDR4_DIMM1_CKE0 | CK32 | 1.2 V HS LVCMOS | DDR4 DIMM1 Clock Enable 0 |
| DDR4_DIMM1_ODT1 | CN33 | 1.2 V HS LVCMOS | DDR4 DIMM1 On Die Termination 1 |
| DDR4_DIMM1_ODT0 | CP32 | 1.2 V HS LVCMOS | DDR4 DIMM1 On Die Termination 0 |
| DDR4_DIMM1_ACT_N | CL35 | 1.2 V HS LVCMOS | DDR4 DIMM1 Activate Command |
| DDR4_DIMM1_CS_N0 | CK34 | 1.2 V HS LVCMOS | DDR4 DIMM1 Chip Select 0 |
| DDR4_DIMM1_RESET_N | CN35 | 1.2 V HS LVCMOS | DDR4 DIMM1 Reset |
| DDR4_DIMM1_BG1 | CP34 | 1.2 V HS LVCMOS | DDR4 DIMM1 Bank Group 1 |

## A.5.6. DDR4 DIMM2 Interface

The Intel Agilex 7 FPGA (two F-tiles) development board provides two DDR4 x72 DIMM interfaces connected to the FPGA fabric. DIMM2 is connected to the Intel Agilex 7 I/O96 of banks 2E and 2F. Only one DIMM memory module is included with the development kit for evaluation of the DIMM interfaces.

## Table 34. DIMM2 Pin Assignments

| Schematic Signal Name | FPGA Pin Number | I/O Standard | Description |
|---|---|---|---|
| DDR4_DIMM2_DQ0 | CK46 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ0 data |
| DDR4_DIMM2_DQ1 | CL47 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ1 data |
| DDR4_DIMM2_DQ2 | CN47 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ2 data |
| DDR4_DIMM2_DQ3 | CP46 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ3 data |
| DDR4_DIMM2_DQ4 | CL43 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ4 data |
| DDR4_DIMM2_DQ5 | CK42 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ5 data |
| DDR4_DIMM2_DQ6 | CN43 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ6 data |
| DDR4_DIMM2_DQ7 | CP42 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ7 data |
| DDR4_DIMM2_DQS_P0 | CP44 | 1.2 V HS LVCMOS | DDR4 DIMM2 Data Strobe |
| | | | Positive for byte lane 0 |
| DDR4_DIMM2_DQS_N0 | CN45 | 1.2 V HS LVCMOS | DDR4 DIMM2 Data Strobe |
| | | | Negative for byte lane 0 |
| DDR4_DIMM2_DBI_N0 | CK44 | 1.2 V HS LVCMOS | DDR4 DIMM2 Data Bus Inversion for byte lane 0 |
| DDR4_DIMM2_TDQS_N9 | CL45 | 1.2 V HS LVCMOS | DDR4 DIMM2 Termination Data Strobe for byte lane 0 |
| DDR4_DIMM2_DQ8 | DA45 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ8 data |
| DDR4_DIMM2_DQ9 | DC45 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ9 data |
| DDR4_DIMM2_DQ10 | DD44 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ10 data |
| DDR4_DIMM2_DQ11 | CY44 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ11 data |
| DDR4_DIMM2_DQ12 | DA49 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ12 data |
| DDR4_DIMM2_DQ13 | CY48 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ13 data |
| DDR4_DIMM2_DQ14 | DD48 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ14 data |
| DDR4_DIMM2_DQ15 | DC49 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ15 data |
| DDR4_DIMM2_DQS_P1 | DD46 | 1.2 V HS LVCMOS | DDR4 DIMM2 Data Strobe |
| | | | Positive for byte lane 1 |
| DDR4_DIMM2_DQS_N1 | DC47 | 1.2 V HS LVCMOS | DDR4 DIMM2 Data Strobe |
| | | | Negative for byte lane 1 |
| DDR4_DIMM2_DBI_N1 | CY46 | 1.2 V HS LVCMOS | DDR4 DIMM2 Data Bus Inversion for byte lane 1 |
| DDR4_DIMM2_TDQS_N10 | DA47 | 1.2 V HS LVCMOS | DDR4 DIMM2 Termination Data Strobe for byte lane 1 |
| DDR4_DIMM2_DQ16 | CN49 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ16 data |
| DDR4_DIMM2_DQ17 | CP48 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ17 data |
| DDR4_DIMM2_DQ18 | CL49 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ18 data |
| DDR4_DIMM2_DQ19 | CK48 | 1.2 V HS LVCMOS | DDR4 DIMM2 D19 data |
| DDR4_DIMM2_DQ20 | CM52 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ20 data |
| DDR4_DIMM2_DQ21 | CT52 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ21 data |
| DDR4_DIMM2_DQ22 | CN53 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ22 data |

*continued...*

| Schematic Signal Name | FPGA Pin Number | I/O Standard | Description |
|---|---|---|---|
| DDR4_DIMM2_DQ23 | CR53 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ23 data |
| DDR4_DIMM2_DQS_P2 | CP50 | 1.2 V HS LVCMOS | DDR4 DIMM2 Data Strobe |
| | | | Positive for byte lane 2 |
| DDR4_DIMM2_DQS_N2 | CN51 | 1.2 V HS LVCMOS | DDR4 DIMM2 Data Strobe |
| | | | Negative for byte lane 2 |
| DDR4_DIMM2_DBI_N2 | CK50 | 1.2 V HS LVCMOS | DDR4 DIMM2 Data Bus Inversion for byte lane 2 |
| DDR4_DIMM2_TDQS_N11 | CL51 | 1.2 V HS LVCMOS | DDR4 DIMM2 Termination Data Strobe for byte lane 2 |
| DDR4_DIMM2_DQ24 | CR47 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ24 data |
| DDR4_DIMM2_DQ25 | CT46 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ25 data |
| DDR4_DIMM2_DQ26 | CV46 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ26 data |
| DDR4_DIMM2_DQ27 | CW47 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ27 data |
| DDR4_DIMM2_DQ28 | CW43 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ28 data |
| DDR4_DIMM2_DQ29 | CV42 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ29 data |
| DDR4_DIMM2_DQ30 | CR43 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ30 data |
| DDR4_DIMM2_DQ31 | CT42 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ31 data |
| DDR4_DIMM2_DQS_P3 | CV44 | 1.2 V HS LVCMOS | DDR4 DIMM2 Data Strobe |
| | | | Positive for byte lane 3 |
| DDR4_DIMM2_DQS_N3 | CW45 | 1.2 V HS LVCMOS | DDR4 DIMM2 Data Strobe |
| | | | Negative for byte lane 3 |
| DDR4_DIMM2_DBI_N3 | CT44 | 1.2 V HS LVCMOS | DDR4 DIMM2 Data Bus Inversion for byte lane 3 |
| DDR4_DIMM2_TDQS_N12 | CR45 | 1.2 V HS LVCMOS | DDR4 DIMM2 Termination Data Strobe for byte lane 3 |
| DDR4_DIMM2_DQ32 | CV48 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ32 data |
| DDR4_DIMM2_DQ33 | CT48 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ33 data |
| DDR4_DIMM2_DQ34 | CW49 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ34 data |
| DDR4_DIMM2_DQ35 | CR49 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ35 data |
| DDR4_DIMM2_DQ36 | CW53 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ36 data |
| DDR4_DIMM2_DQ37 | CV52 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ37 data |
| DDR4_DIMM2_DQ38 | CW55 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ38 data |
| DDR4_DIMM2_DQ39 | CV54 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ39 data |
| DDR4_DIMM2_DQS_P4 | CV50 | 1.2 V HS LVCMOS | DDR4 DIMM2 Data Strobe |
| | | | Positive for byte lane 4 |
| DDR4_DIMM2_DQS_N4 | CW51 | 1.2 V HS LVCMOS | DDR4 DIMM2 Data Strobe |
| | | | Negative for byte lane 4 |
| DDR4_DIMM2_DBI_N4 | CT50 | 1.2 V HS LVCMOS | DDR4 DIMM2 Data Bus Inversion for byte lane 4 |
| DDR4_DIMM2_TDQS_N13 | CR51 | 1.2 V HS LVCMOS | DDR4 DIMM2 Termination Data Strobe for byte lane 4 |
| DDR4_DIMM2_DQ40 | CY50 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ40 data |

*continued...*

| Schematic Signal Name | FPGA Pin Number | I/O Standard | Description |
|---|---|---|---|
| DDR4_DIMM2_DQ41 | DC51 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ41 data |
| DDR4_DIMM2_DQ42 | DA51 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ42 data |
| DDR4_DIMM2_DQ43 | DD50 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ43 data |
| DDR4_DIMM2_DQ44 | CY54 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ44 data |
| DDR4_DIMM2_DQ45 | DA55 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ45 data |
| DDR4_DIMM2_DQ46 | DD54 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ46 data |
| DDR4_DIMM2_DQ47 | DC55 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ47 data |
| DDR4_DIMM2_DQS_P5 | DD52 | 1.2 V HS LVCMOS | DDR4 DIMM2 Data Strobe |
| | | | Positive for byte lane 5 |
| DDR4_DIMM2_DQS_N5 | DC52 | 1.2 V HS LVCMOS | DDR4 DIMM2 Data Strobe |
| | | | Negative for byte lane 5 |
| DDR4_DIMM2_DBI_N5 | CY52 | 1.2 V HS LVCMOS | DDR4 DIMM2 Data Bus Inversion for byte lane 5 |
| DDR4_DIMM2_TDQS_N14 | DA53 | 1.2 V HS LVCMOS | DDR4 DIMM2 Termination Data Strobe for byte lane 5 |
| DDR4_DIMM2_DQ48 | CL41 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ48 data |
| DDR4_DIMM2_DQ49 | CN41 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ49 data |
| DDR4_DIMM2_DQ50 | CK40 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ50 data |
| DDR4_DIMM2_DQ51 | CP40 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ51 data |
| DDR4_DIMM2_DQ52 | CK36 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ52 data |
| DDR4_DIMM2_DQ53 | CN37 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ53 data |
| DDR4_DIMM2_DQ54 | CL37 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ54 data |
| DDR4_DIMM2_DQ55 | CP36 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ55 data |
| DDR4_DIMM2_DQS_P6 | CP38 | 1.2 V HS LVCMOS | DDR4 DIMM2 Data Strobe |
| | | | Positive for byte lane 6 |
| DDR4_DIMM2_DQS_N6 | CN39 | 1.2 V HS LVCMOS | DDR4 DIMM2 Data Strobe |
| | | | Negative for byte lane 6 |
| DDR4_DIMM2_DBI_N6 | CK38 | 1.2 V HS LVCMOS | DDR4 DIMM2 Data Bus Inversion for byte lane 6 |
| DDR4_DIMM2_TDQS_N15 | CL39 | 1.2 V HS LVCMOS | DDR4 DIMM2 Termination Data Strobe for byte lane 6 |
| DDR4_DIMM2_DQ56 | DF46 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ56 data |
| DDR4_DIMM2_DQ57 | DE47 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ57 data |
| DDR4_DIMM2_DQ58 | DH46 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ58 data |
| DDR4_DIMM2_DQ59 | DJ47 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ59 data |
| DDR4_DIMM2_DQ60 | DE53 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ60 data |
| DDR4_DIMM2_DQ61 | DF52 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ61 data |
| DDR4_DIMM2_DQ62 | DG51 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ62 data |
| DDR4_DIMM2_DQ63 | DH50 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ63 data |
| DDR4_DIMM2_DQS_P7 | DH48 | 1.2 V HS LVCMOS | DDR4 DIMM2 Data Strobe |

*continued...*

| Schematic Signal Name | FPGA Pin Number | I/O Standard | Description |
|---|---|---|---|
| | | | Positive for byte lane 7 |
| DDR4_DIMM2_DQS_N7 | DJ49 | 1.2 V HS LVCMOS | DDR4 DIMM2 Data Strobe |
| | | | Negative for byte lane 7 |
| DDR4_DIMM2_DBI_N7 | DF48 | 1.2 V HS LVCMOS | DDR4 DIMM2 Data Bus Inversion for byte lane 7 |
| DDR4_DIMM2_TDQS_N16 | DE49 | 1.2 V HS LVCMOS | DDR4 DIMM2 Termination Data Strobe for byte lane 7 |
| DDR4_DIMM2_DQ64 | CW41 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ64 data |
| DDR4_DIMM2_DQ65 | CV40 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ65 data |
| DDR4_DIMM2_DQ66 | CR41 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ66 data |
| DDR4_DIMM2_DQ67 | CT40 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ67 data |
| DDR4_DIMM2_DQ68 | CR37 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ68 data |
| DDR4_DIMM2_DQ69 | CV36 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ69 data |
| DDR4_DIMM2_DQ70 | CW37 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ70 data |
| DDR4_DIMM2_DQ71 | CT36 | 1.2 V HS LVCMOS | DDR4 DIMM2 DQ71 data |
| DDR4_DIMM2_DQS_P8 | CV38 | 1.2 V HS LVCMOS | DDR4 DIMM2 Data Strobe |
| | | | Positive for byte lane 8 |
| DDR4_DIMM2_DQS_N8 | CW39 | 1.2 V HS LVCMOS | DDR4 DIMM2 Data Strobe |
| | | | Negative for byte lane 8 |
| DDR4_DIMM2_DBI_N8 | CT38 | 1.2 V HS LVCMOS | DDR4 DIMM2 Data Bus Inversion for byte lane 8 |
| DDR4_DIMM2_TDQS_N17 | CR39 | 1.2 V HS LVCMOS | DDR4 DIMM2 Termination Data Strobe for byte lane 8 |
| DDR4_DIMM2_C1 | DJ33 | 1.2 V HS LVCMOS | DDR4 DIMM2 Stacked Device Chip ID 1 |
| DDR4_DIMM2_C0 | DH32 | 1.2 V HS LVCMOS | DDR4 DIMM2 Stacked Device Chip ID 0 |
| DDR4_DIMM2_BG0 | DA33 | 1.2 V HS LVCMOS | DDR4 DIMM2 Bank Group 0 |
| DDR4_DIMM2_BA1 | CY32 | 1.2 V HS LVCMOS | DDR4 DIMM2 Bank Address 1 |
| DDR4_DIMM2_BA0 | DC33 | 1.2 V HS LVCMOS | DDR4 DIMM2 Bank Address 0 |
| DDR4_DIMM2_A17 | DD32 | 1.2 V HS LVCMOS | DDR4 DIMM2 Address 17 |
| DDR4_DIMM2_A16 | DA35 | 1.2 V HS LVCMOS | DDR4 DIMM2 Address 16 |
| DDR4_DIMM2_A15 | CY34 | 1.2 V HS LVCMOS | DDR4 DIMM2 Address 15 |
| DDR4_DIMM2_A14 | DC35 | 1.2 V HS LVCMOS | DDR4 DIMM2 Address 14 |
| DDR4_DIMM2_A13 | DD34 | 1.2 V HS LVCMOS | DDR4 DIMM2 Address 13 |
| DDR4_DIMM2_A12 | DA37 | 1.2 V HS LVCMOS | DDR4 DIMM2 Address 12 |
| DDR4_DIMM2_A11 | DE35 | 1.2 V HS LVCMOS | DDR4 DIMM2 Address 11 |
| DDR4_DIMM2_A10 | DF34 | 1.2 V HS LVCMOS | DDR4 DIMM2 Address 10 |
| DDR4_DIMM2_A9 | DJ35 | 1.2 V HS LVCMOS | DDR4 DIMM2 Address 9 |
| DDR4_DIMM2_A8 | DH34 | 1.2 V HS LVCMOS | DDR4 DIMM2 Address 8 |
| DDR4_DIMM2_A7 | DE37 | 1.2 V HS LVCMOS | DDR4 DIMM2 Address 7 |
| DDR4_DIMM2_A6 | DF36 | 1.2 V HS LVCMOS | DDR4 DIMM2 Address 6 |

*continued...*

| Schematic Signal Name | FPGA Pin Number | I/O Standard | Description |
|---|---|---|---|
| DDR4_DIMM2_A5 | DJ37 | 1.2 V HS LVCMOS | DDR4 DIMM2 Address 5 |
| DDR4_DIMM2_A4 | DH36 | 1.2 V HS LVCMOS | DDR4 DIMM2 Address 4 |
| DDR4_DIMM2_A3 | DE39 | 1.2 V HS LVCMOS | DDR4 DIMM2 Address 3 |
| DDR4_DIMM2_A2 | DF38 | 1.2 V HS LVCMOS | DDR4 DIMM2 Address 2 |
| DDR4_DIMM2_A1 | DJ39 | 1.2 V HS LVCMOS | DDR4 DIMM2 Address 1 |
| DDR4_DIMM2_A0 | DH38 | 1.2 V HS LVCMOS | DDR4 DIMM2 Address 0 |
| DDR4_DIMM2_PAR | DA39 | 1.2 V HS LVCMOS | DDR4 DIMM2 Parity |
| DDR4_DIMM2_CS_N1 | CY38 | 1.2 V HS LVCMOS | DDR4 DIMM2 Chip Select 1 |
| DDR4_DIMM2_CK_N0 | DC39 | 1.2 V HS LVCMOS | DDR4 DIMM2 Clock 0, |
| | | | Positive |
| DDR4_DIMM2_CK_P0 | DD38 | 1.2 V HS LVCMOS | DDR4 DIMM2 Clock 0, |
| | | | Negative |
| DDR4_DIMM2_CKE1 | DA41 | 1.2 V HS LVCMOS | DDR4 DIMM2 Clock Enable 1 |
| DDR4_DIMM2_CKE0 | DD40 | 1.2 V HS LVCMOS | DDR4 DIMM2 Clock Enable 0 |
| DDR4_DIMM2_ODT1 | DC41 | 1.2 V HS LVCMOS | DDR4 DIMM2 On Die Termination 1 |
| DDR4_DIMM2_ODT0 | DD40 | 1.2 V HS LVCMOS | DDR4 DIMM2 On Die Termination 0 |
| DDR4_DIMM2_ACT_N | DA43 | 1.2 V HS LVCMOS | DDR4 DIMM2 Activate Command |
| DDR4_DIMM2_CS_N0 | CY42 | 1.2 V HS LVCMOS | DDR4 DIMM2 Chip Select 0 |
| DDR4_DIMM2_RESET_N | DC43 | 1.2 V HS LVCMOS | DDR4 DIMM2 Reset |
| DDR4_DIMM2_BG1 | DD42 | 1.2 V HS LVCMOS | DDR4 DIMM2 Bank Group 1 |

## A.5.7. DDR4 Component Interface

The Intel Agilex 7 FPGA (two F-tiles) development board provides a DDR4 x40 Interface comprised of five DDR4 x8 components for HPS access. This gives 32-bits data plus 8-bits ECC, which are connected to I/O96 of bank 3D.

### Table 35. DDR4 Component Pin Assignments

| Schematic Signal Name | FPGA Pin Number | I/O Standard | Description |
|---|---|---|---|
| DDR4_COMP_DQ0 | F12 | 1.2 V HS LVCMOS | DDR4 component DQ0 data |
| DDR4_COMP_DQ1 | F8 | 1.2 V HS LVCMOS | DDR4 component DQ1 data |
| DDR4_COMP_DQ2 | G11 | 1.2 V HS LVCMOS | DDR4 component DQ2 data |
| DDR4_COMP_DQ3 | K8 | 1.2 V HS LVCMOS | DDR4 component DQ3 data |
| DDR4_COMP_DQ4 | J11 | 1.2 V HS LVCMOS | DDR4 component DQ4 data |
| DDR4_COMP_DQ5 | G7 | 1.2 V HS LVCMOS | DDR4 component DQ5 data |
| DDR4_COMP_DQ6 | K12 | 1.2 V HS LVCMOS | DDR4 component DQ6 data |
| DDR4_COMP_DQ7 | J7 | 1.2 V HS LVCMOS | DDR4 component DQ7 data |
| DDR4_COMP_DQS_P0 | G9 | 1.2 V HS LVCMOS | DDR4 component DQS 0 strobe positive |

*continued...*

| Schematic Signal Name | FPGA Pin Number | I/O Standard | Description |
|---|---|---|---|
| DDR4_COMP_DQS_N0 | F10 | 1.2 V HS LVCMOS | DDR4 component DQS 0 strobe negative |
| DDR4_COMP_DBI_N0 | J9 | 1.2 V HS LVCMOS | DDR4 component Data Bus Inversion for byte lane 0 |
| DDR4_COMP_DQ8 | M6 | 1.2 V HS LVCMOS | DDR4 component DQ8 data |
| DDR4_COMP_DQ9 | P2 | 1.2 V HS LVCMOS | DDR4 component DQ9 data |
| DDR4_COMP_DQ10 | L5 | 1.2 V HS LVCMOS | DDR4 component DQ10 data |
| DDR4_COMP_DQ11 | R1 | 1.2 V HS LVCMOS | DDR4 component DQ11 data |
| DDR4_COMP_DQ12 | P6 | 1.2 V HS LVCMOS | DDR4 component DQ12 data |
| DDR4_COMP_DQ13 | R5 | 1.2 V HS LVCMOS | DDR4 component DQ13 data |
| DDR4_COMP_DQ14 | M2 | 1.2 V HS LVCMOS | DDR4 component DQ14 data |
| DDR4_COMP_DQ15 | L1 | 1.2 V HS LVCMOS | DDR4 component DQ15 data |
| DDR4_COMP_DQS_P1 | L3 | 1.2 V HS LVCMOS | DDR4 component DQS 1 strobe positive |
| DDR4_COMP_DQS_N1 | M4 | 1.2 V HS LVCMOS | DDR4 component DQS 1 strobe negative |
| DDR4_COMP_DBI_N1 | R3 | 1.2 V HS LVCMOS | DDR4 component Data Bus Inversion for byte lane 1 |
| DDR4_COMP_DQ16 | A9 | 1.2 V HS LVCMOS | DDR4 component DQ16 data |
| DDR4_COMP_DQ17 | B6 | 1.2 V HS LVCMOS | DDR4 component DQ17 data |
| DDR4_COMP_DQ18 | E9 | 1.2 V HS LVCMOS | DDR4 component DQ18 data |
| DDR4_COMP_DQ19 | D6 | 1.2 V HS LVCMOS | DDR4 component DQ19 data |
| DDR4_COMP_DQ20 | D10 | 1.2 V HS LVCMOS | DDR4 component DQ20 data |
| DDR4_COMP_DQ21 | C5 | 1.2 V HS LVCMOS | DDR4 component DQ21 data |
| DDR4_COMP_DQ22 | B10 | 1.2 V HS LVCMOS | DDR4 component DQ22 data |
| DDR4_COMP_DQ23 | E5 | 1.2 V HS LVCMOS | DDR4 component DQ23 data |
| DDR4_COMP_DQS_P2 | A7 | 1.2 V HS LVCMOS | DDR4 component DQS 2 strobe positive |
| DDR4_COMP_DQS_N2 | B8 | 1.2 V HS LVCMOS | DDR4 component DQS 2 strobe negative |
| DDR4_COMP_DBI_N2 | E7 | 1.2 V HS LVCMOS | DDR4 component Data Bus Inversion for byte lane 2 |
| DDR4_COMP_DQ24 | F6 | 1.2 V HS LVCMOS | DDR4 component DQ24 data |
| DDR4_COMP_DQ25 | J1 | 1.2 V HS LVCMOS | DDR4 component DQ25 data |
| DDR4_COMP_DQ26 | F2 | 1.2 V HS LVCMOS | DDR4 component DQ26 data |
| DDR4_COMP_DQ27 | K2 | 1.2 V HS LVCMOS | DDR4 component DQ27 data |
| DDR4_COMP_DQ28 | K6 | 1.2 V HS LVCMOS | DDR4 component DQ28 data |
| DDR4_COMP_DQ29 | J5 | 1.2 V HS LVCMOS | DDR4 component DQ29 data |
| DDR4_COMP_DQ30 | G5 | 1.2 V HS LVCMOS | DDR4 component DQ30 data |
| DDR4_COMP_DQ31 | G1 | 1.2 V HS LVCMOS | DDR4 component DQ31 data |
| DDR4_COMP_DQS_P3 | G3 | 1.2 V HS LVCMOS | DDR4 component DQS 3 strobe positive |
| DDR4_COMP_DQS_N3 | F4 | 1.2 V HS LVCMOS | DDR4 component DQS 3 strobe negative |
| DDR4_COMP_DBI_N3 | J3 | 1.2 V HS LVCMOS | DDR4 component Data Bus Inversion for byte lane 3 |
| DDR4_COMP_DQ32 | AA7 | 1.2 V HS LVCMOS | DDR4 component DQ32 data |

***continued...***

| Schematic Signal Name | FPGA Pin Number | I/O Standard | Description |
|---|---|---|---|
| DDR4_COMP_DQ33 | AD2 | 1.2 V HS LVCMOS | DDR4 component DQ33 data |
| DDR4_COMP_DQ34 | AB2 | 1.2 V HS LVCMOS | DDR4 component DQ34 data |
| DDR4_COMP_DQ35 | AB8 | 1.2 V HS LVCMOS | DDR4 component DQ35 data |
| DDR4_COMP_DQ36 | AA1 | 1.2 V HS LVCMOS | DDR4 component DQ36 data |
| DDR4_COMP_DQ37 | AE7 | 1.2 V HS LVCMOS | DDR4 component DQ37 data |
| DDR4_COMP_DQ38 | AE1 | 1.2 V HS LVCMOS | DDR4 component DQ38 data |
| DDR4_COMP_DQ39 | AD6 | 1.2 V HS LVCMOS | DDR4 component DQ39 data |
| DDR4_COMP_DQS_P4 | AA5 | 1.2 V HS LVCMOS | DDR4 component DQS 4 strobe positive |
| DDR4_COMP_DQS_N4 | AB6 | 1.2 V HS LVCMOS | DDR4 component DQS 4 strobe negative |
| DDR4_COMP_DBI_N4 | AA3 | 1.2 V HS LVCMOS | DDR4 component Data Bus Inversion for byte lane 4 |
| DDR4_COMP_BG0 | Y2 | 1.2 V HS LVCMOS | DDR4 Component Bank |
| | | | Group 0 |
| DDR4_COMP_BA1 | W1 | 1.2 V HS LVCMOS | DDR4 Component Bank Address 1 |
| DDR4_COMP_BA0 | T2 | 1.2 V HS LVCMOS | DDR4 Component Bank Address 0 |
| DDR4_COMP_ALERT_N | U1 | 1.2 V HS LVCMOS | DDR4 Component Alert |
| DDR4_COMP_A16 | Y4 | 1.2 V HS LVCMOS | DDR4 Component Address 16 |
| DDR4_COMP_A15 | W3 | 1.2 V HS LVCMOS | DDR4 Component Address 15 |
| DDR4_COMP_A14 | T4 | 1.2 V HS LVCMOS | DDR4 Component Address 14 |
| DDR4_COMP_A13 | U3 | 1.2 V HS LVCMOS | DDR4 Component Address 13 |
| DDR4_COMP_A12 | Y6 | 1.2 V HS LVCMOS | DDR4 Component Address 12 |
| DDR4_COMP_A11 | Y8 | 1.2 V HS LVCMOS | DDR4 Component Address 11 |
| DDR4_COMP_A10 | W7 | 1.2 V HS LVCMOS | DDR4 Component Address 10 |
| DDR4_COMP_A9 | T8 | 1.2 V HS LVCMOS | DDR4 Component Address 9 |
| DDR4_COMP_A8 | U7 | 1.2 V HS LVCMOS | DDR4 Component Address 8 |
| DDR4_COMP_A7 | Y10 | 1.2 V HS LVCMOS | DDR4 Component Address 7 |
| DDR4_COMP_A6 | W9 | 1.2 V HS LVCMOS | DDR4 Component Address 6 |
| DDR4_COMP_A5 | T10 | 1.2 V HS LVCMOS | DDR4 Component Address 5 |
| DDR4_COMP_A4 | U9 | 1.2 V HS LVCMOS | DDR4 Component Address 4 |
| DDR4_COMP_A3 | Y12 | 1.2 V HS LVCMOS | DDR4 Component Address 3 |
| DDR4_COMP_A2 | W11 | 1.2 V HS LVCMOS | DDR4 Component Address 2 |
| DDR4_COMP_A1 | T12 | 1.2 V HS LVCMOS | DDR4 Component Address 1 |
| DDR4_COMP_A0 | U11 | 1.2 V HS LVCMOS | DDR4 Component Address 0 |
| DDR4_COMP_PAR | P8 | 1.2 V HS LVCMOS | DDR4 Component Parity |
| DDR4_COMP_CK_N | M8 | 1.2 V HS LVCMOS | DDR4 DIMM2 Clock Negative |
| DDR4_COMP_CK_P | L7 | 1.2 V HS LVCMOS | DDR4 DIMM2 Clock Positive |
| DDR4_COMP_CKE | R9 | 1.2 V HS LVCMOS | DDR4 Component Clock Enable |

*continued...*

| Schematic Signal Name | FPGA Pin Number | I/O Standard | Description |
|---|---|---|---|
| DDR4_COMP_ODT | L9 | 1.2 V HS LVCMOS | DDR4 Component On Die Termination |
| DDR4_COMP_ACT_N | P12 | 1.2 V HS LVCMOS | DDR4 Component Activate |
| DDR4_COMP_CS_N | R11 | 1.2 V HS LVCMOS | DDR4 Component Chip Select |
| DDR4_COMP_RESET_N | M12 | 1.2 V HS LVCMOS | DDR4 Component Reset |
| DDR4_COMP_BG1 | L11 | 1.2 V HS LVCMOS | DDR4 Component Bank Group 1 |

## A.5.8. HPS I/O48 Interface

An HPS I/O48 daughter card is pre-installed with each development kit board.

The Intel Agilex 7 FPGA (two F-tiles) development board connects the 48 HPS I/Os (HPS_IOA[24:1] and HPS_IOB[24:1]) to a mezzanine connector for installing the Intel HPS I/O48 daughter card. This daughter card provides the HPS with USB, UART, Ethernet, SD card, $I^2C$, and JTAG accessibility.

**Table 36. HPS Pin Assignments**

| Schematic Signal Name | FPGA Pin Number | I/O Standard | Description |
|---|---|---|---|
| HPS_GPIO0 | AC15 | 1.8 V LVCMOS | USB Clock |
| HPS_GPIO1 | AL15 | 1.8 V LVCMOS | USB STP |
| HPS_GPIO2 | AJ11 | 1.8 V LVCMOS | USB DIR |
| HPS_GPIO3 | AM16 | 1.8 V LVCMOS | USB Data 0 |
| HPS_GPIO4 | AH12 | 1.8 V LVCMOS | USB Data 1 |
| HPS_GPIO5 | AN15 | 1.8 V LVCMOS | USB NXT |
| HPS_GPIO6 | AG13 | 1.8 V LVCMOS | USB Data 2 |
| HPS_GPIO7 | AP16 | 1.8 V LVCMOS | USB Data 3 |
| HPS_GPIO8 | AF14 | 1.8 V LVCMOS | USB Data 4 |
| HPS_GPIO9 | AT16 | 1.8 V LVCMOS | USB Data 5 |
| HPS_GPIO10 | AH10 | 1.8 V LVCMOS | USB Data 6 |
| HPS_GPIO11 | AU15 | 1.8 V LVCMOS | USB Data 7 |
| HPS_GPIO12 | AJ7 | 1.8 V LVCMOS | Ethernet TX Clock |
| HPS_GPIO13 | AL13 | 1.8 V LVCMOS | Ethernet TX Enable |
| HPS_GPIO14 | AH8 | 1.8 V LVCMOS | Ethernet RX Clock |
| HPS_GPIO15 | AM14 | 1.8 V LVCMOS | Ethernet RX Data Valid |
| HPS_GPIO16 | AD14 | 1.8 V LVCMOS | Ethernet TX Data 0 |
| HPS_GPIO17 | AN13 | 1.8 V LVCMOS | Ethernet TX Data 1 |
| HPS_GPIO18 | AG11 | 1.8 V LVCMOS | Ethernet RX Data 0 |
| HPS_GPIO19 | AP14 | 1.8 V LVCMOS | Ethernet RX Data 1 |
| HPS_GPIO20 | AG9 | 1.8 V LVCMOS | Ethernet TX Data 2 |
| HPS_GPIO21 | AT14 | 1.8 V LVCMOS | Ethernet TX Data 3 |

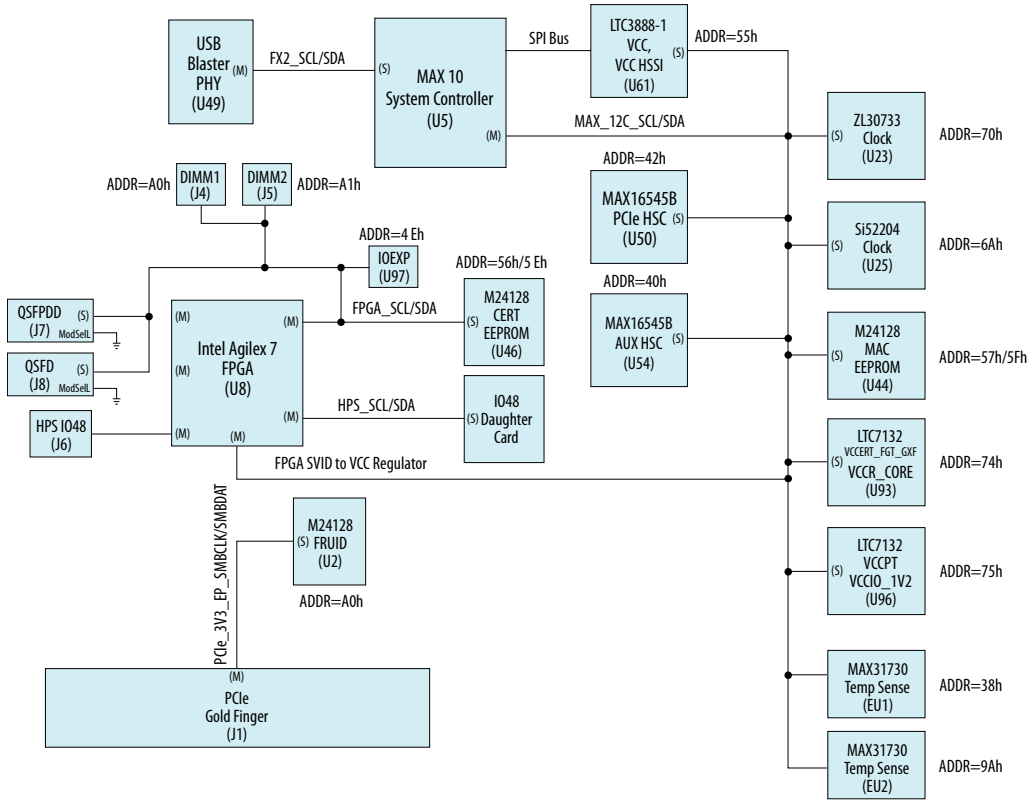
*continued...*

| Schematic Signal Name | FPGA Pin Number | I/O Standard | Description |
|---|---|---|---|
| HPS_GPIO22 | AF12 | 1.8 V LVCMOS | Ethernet RX Data 2 |
| HPS_GPIO23 | AU13 | 1.8 V LVCMOS | Ethernet RX Data 3 |
| HPS_GPIO24 | AF10 | 1.8 V LVCMOS | GPIO IO0 |
| HPS_GPIO25 | AU11 | 1.8 V LVCMOS | GPIO IO1 |
| HPS_GPIO26 | AF8 | 1.8 V LVCMOS | UART TX |
| HPS_GPIO27 | AT12 | 1.8 V LVCMOS | UART RX |
| HPS_GPIO28 | AG7 | 1.8 V LVCMOS | GPIO IO4 |
| HPS_GPIO29 | AP12 | 1.8 V LVCMOS | GPIO IO5 |
| HPS_GPIO30 | AC13 | 1.8 V LVCMOS | I2C SDA |
| HPS_GPIO31 | AN11 | 1.8 V LVCMOS | I2C SCL |
| HPS_GPIO32 | AD12 | 1.8 V LVCMOS | JTAG TCK |
| HPS_GPIO33 | AM12 | 1.8 V LVCMOS | JTAG TMS |
| HPS_GPIO34 | AD10 | 1.8 V LVCMOS | JTAG TDO |
| HPS_GPIO35 | AL11 | 1.8 V LVCMOS | JTAG TDI |
| HPS_GPIO36 | AC11 | 1.8 V LVCMOS | SD Card Data 0 |
| HPS_GPIO37 | AT10 | 1.8 V LVCMOS | SD Card Command |
| HPS_GPIO38 | AD8 | 1.8 V LVCMOS | SD Card Clock |
| HPS_GPIO39 | AP10 | 1.8 V LVCMOS | SD Card Data 1 |
| HPS_GPIO40 | AC9 | 1.8 V LVCMOS | SD Card Data 2 |
| HPS_GPIO41 | AM10 | 1.8 V LVCMOS | SD Card Data 3 |
| HPS_GPIO42 | AB10 | 1.8 V LVCMOS | OSC Clock |
| HPS_GPIO43 | AJ13 | 1.8 V LVCMOS | GPIO IO19 |
| HPS_GPIO44 | AB14 | 1.8 V LVCMOS | GPIO IO20 |
| HPS_GPIO45 | AH14 | 1.8 V LVCMOS | GPIO IO21 |
| HPS_GPIO46 | AB12 | 1.8 V LVCMOS | Ethernet MDIO |
| HPS_GPIO47 | AJ9 | 1.8 V LVCMOS | Ethernet MDC |

## A.6. $I^2C$

The Intel MAX 10 and Intel Agilex 7 devices use the $I^2C$ for reading and writing to the various components on the board such as programmable clock generators, voltage regulators, temperature sensors, and EEPROMs. You can use the Intel Agilex 7 or Intel MAX 10 as the $I^2C$ host to access these devices, change clock frequencies, or get board status information such as the voltage and temperature readings.

## Figure 25. I²C Block Diagram




## Table 37. Intel MAX 10 I²C Signals

| Schematic Signal Name | MAX Pin Number | I/O Standard | Description |
|---|---|---|---|
| MAX_I2C_SCL | J11 | 3.3 V open drain | Intel MAX 10 I²C clock |
| MAX_I2C_SDA | J12 | 3.3 V open drain | Intel MAX 10 I²C data |
| FX2_SCL | R1 | 3.3 V open drain | USB PHY I²C clock |
| FX2_SDA | R3 | 3.3 V open drain | USB PHY I²C data |

## Table 38. FPGA I²C Signals

| Schematic Signal Name | FPGA Pin Number | I/O Standard | Description |
|---|---|---|---|
| FPGA_1V8_SVID_SCL | CG47 | 1.8 V open drain | Serial voltage ID I²C clock |
| FPGA_1V8_SVID_SDA | CB46 | 1.8 V open drain | Serial voltage ID I²C data |
| FPGA_1V2_SCL | K44 | 1.2 V open drain | FPGA I²C clock for DDR4 DIMMs, QSFP, QSFPDD, IO expander, and certificate EEPROM |
| FPGA_1V2_SDA | J43 | 1.2 V open drain | FPGA I²C data for DDR4 DIMMs, QSFP, QSFPDD, IO expander, and certificate EEPROM |
| HPS_SCL | N3 | 1.8 V open drain | HPS I/O48 daughter card I²C clock |
| HPS_SDA | L6 | 1.8 V open drain | HPS I/O48 daughter card I²C data |

## A.7. Intel MAX 10 SPI Bus

The Intel MAX 10 device uses the SPI bus for reading telemetry information from the Analog Devices LTC3888 VCC core controller.

**Table 39. SPI Signals**

| Schematic Signal Name | FPGA Pin Number | I/O Standard | Description |
|---|---|---|---|
| LTC_1V8_SDI | L2 | 1.8 V CMOS | SPI data |
| LTC_1V8_SCK | N2 | 1.8 V CMOS | SPI clock |
| LTC_1V8_SPI_ERRn | M1 | 1.8 V CMOS | SPI error status |
| LTC_1V8_SCSn | P1 | 1.8 V CMOS | SPI chip select |

## A.8. Clock Circuits

**Figure 26. Intel Agilex 7 F-Series FPGA Development Kit Clocks and Default Frequencies**

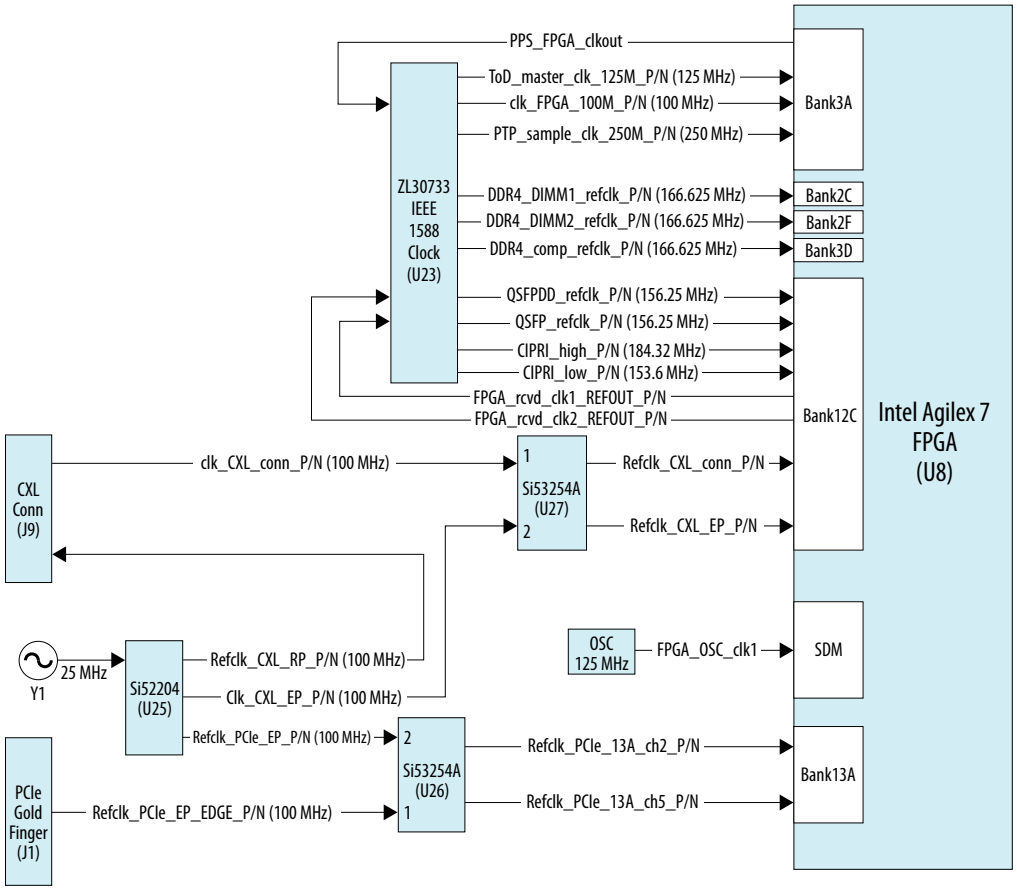


**Table 40. On-Board Oscillators Sources for the FPGA**

| Source | Schematic Signal Name | Frequency | I/O Standard | Intel Agilex 7 Pin Number (P/N) | Application |
|---|---|---|---|---|---|
| U23 | TOD_MASTER_CLK_125M_P/N | 125 Mhz | Differential | G43/F44 | IEEE 1588 TOD master clock |
| | CLK_FPGA_100M_P/N | 100 Mhz | LVDS | CK18/CL19 | General-purpose FPGA clock |
| | PTP_SAMPLE_CLK_250M_P/N | 250 Mhz | Differential | E45/D46 | IEEE 1588 PTP clock |
| | DDR4_DIMM1_REFCLK_P/N | 166.625 Mhz | LVDS | CV28/CW29 | DDR4 DIMM1 clock |
| | DDR4_DIMM2_REFCLK_P/N | 166.625 Mhz | LVDS | DD36/DC37 | DDR4 DIMM2 clock |
| | DDR4_COMP_REFCLK_P/N | 166.625 Mhz | LVDS | U5/T6 | DDR4 component clock |
| | QSFP_REFCLK_P/N | 156.25 Mhz | Differential | AW49/AV48 | QSFP clock |
| | QSFPDD_REFCLK_P/N | 156.25 Mhz | Differential | AD48/AC49 | QSFPDD clock |
| | CIPRI_HIGH_REFCLK_P/N | 184.32 Mhz | Differential | AJ48/AH49 | CIPRI high clock |
| | CIPRI_LOW_REFCLK_P/N | 153.6 Mhz | Differential | AR49/AU49 | CIPRI low clock |
| U27 | REFCLK_CXL_CONN_P/N | 100 Mhz | HCSL | BG49/BF48 | PCIe REFCLK bank 12C channel 1 |
| | REFCLK_CXL_EP_P/N | 100 Mhz | HCSL | BC49/BE49 | PCIe REFCLK bank 12C channel 0 |
| U26 | REFCLK_PCIE_13A_CH2_P/N | 100 Mhz | HCSL | BR7/BU7 | PCIe REFCLK bank 13A channel 2 |
| | REFCLK_PCIE_13A_CH5_P/N | 100 Mhz | HCSL | CD8/CC7 | PCIe REFCLK bank 13A channel 5 |
| U10 | FPGA_OSC_CLK1 | 125 Mhz | 1.8 V LVCMOS | CB42 | Configuration clock |

## A.9. HPS Daughter Card

The development kit includes an Intel HPS daughter card that mounts to a Samtec 48-pin connector (**J6**) and connects to the Intel Agilex 7 HPS I/O 48 bank. The HPS daughter card provides SoC port functionality to the development kit. These ports include Ethernet, USB, UART, $I^2C$, JTAG, and a SD memory card slot. For more information, refer to the HPS IO-48 OOBE Daughter Card.

**Figure 27. HPS Daughter Card**

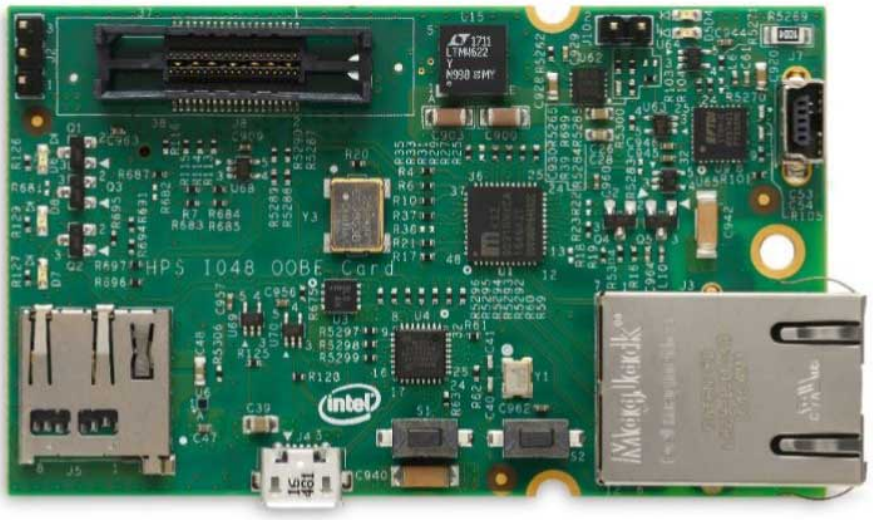



**Table 41. HPS I/O 48 Signals**

| Schematic Signal Name | FPGA Pin Number | I/O Standard | Description |
|---|---|---|---|
| HPS_GPIO0 | AC15 | 1.8 V LVCMOS | USB clock |
| HPS_GPIO1 | AL15 | 1.8 V LVCMOS | USB STP |
| HPS_GPIO2 | AJ11 | 1.8 V LVCMOS | USB DIR |
| HPS_GPIO3 | AM16 | 1.8 V LVCMOS | USB DATA0 |
| HPS_GPIO4 | AH12 | 1.8 V LVCMOS | USB DATA1 |
| HPS_GPIO5 | AN15 | 1.8 V LVCMOS | USB NXT |
| HPS_GPIO6 | AG13 | 1.8 V LVCMOS | USB DATA2 |
| HPS_GPIO7 | AP16 | 1.8 V LVCMOS | USB DATA3 |
| HPS_GPIO8 | AF14 | 1.8 V LVCMOS | USB DATA4 |
| HPS_GPIO9 | AT16 | 1.8 V LVCMOS | USB DATA5 |
| HPS_GPIO10 | AH10 | 1.8 V LVCMOS | USB DATA6 |
| HPS_GPIO11 | AU15 | 1.8 V LVCMOS | USB DATA7 |
| HPS_GPIO12 | AJ7 | 1.8 V LVCMOS | Ethernet TX clock |
| HPS_GPIO13 | AL13 | 1.8 V LVCMOS | Ethernet TX CTL |
| HPS_GPIO14 | AH8 | 1.8 V LVCMOS | Ethernet RX clock |
| HPS_GPIO15 | AM14 | 1.8 V LVCMOS | Ethernet RX CTL |
| HPS_GPIO16 | AD14 | 1.8 V LVCMOS | Ethernet TX Data0 |
| HPS_GPIO17 | AN13 | 1.8 V LVCMOS | Ethernet TX Data1 |
| HPS_GPIO18 | AG11 | 1.8 V LVCMOS | Ethernet RX Data0 |
| HPS_GPIO19 | AP14 | 1.8 V LVCMOS | Ethernet RX Data1 |

*continued...*

| Schematic Signal Name | FPGA Pin Number | I/O Standard | Description |
|---|---|---|---|
| HPS_GPIO20 | AG9 | 1.8 V LVCMOS | Ethernet TX Data2 |
| HPS_GPIO21 | AT14 | 1.8 V LVCMOS | Ethernet TX Data3 |
| HPS_GPIO22 | AF12 | 1.8 V LVCMOS | Ethernet RX Data2 |
| HPS_GPIO23 | AU13 | 1.8 V LVCMOS | Ethernet RX Data3 |
| HPS_GPIO24 | AF10 | 1.8 V LVCMOS | GPIO I/O 0 |
| HPS_GPIO25 | AU11 | 1.8 V LVCMOS | GPIO I/O 1 |
| HPS_GPIO26 | AF8 | 1.8 V LVCMOS | UART TX |
| HPS_GPIO27 | AT12 | 1.8 V LVCMOS | UART RX |
| HPS_GPIO28 | AG7 | 1.8 V LVCMOS | GPIO I/O 4 |
| HPS_GPIO29 | AP12 | 1.8 V LVCMOS | GPIO I/O 5 |
| HPS_GPIO30 | AC13 | 1.8 V LVCMOS | $I^2C$ SDA |
| HPS_GPIO31 | AN11 | 1.8 V LVCMOS | $I^2C$ SCL |
| HPS_GPIO32 | AD12 | 1.8 V LVCMOS | JTAG TCK |
| HPS_GPIO33 | AM12 | 1.8 V LVCMOS | JTAG TMS |
| HPS_GPIO34 | AD10 | 1.8 V LVCMOS | JTAG TDO |
| HPS_GPIO35 | AL11 | 1.8 V LVCMOS | JTAG TDI |
| HPS_GPIO36 | AC11 | 1.8 V LVCMOS | SDMMC Data0 |
| HPS_GPIO37 | AT10 | 1.8 V LVCMOS | SDMMC CMD |
| HPS_GPIO38 | AD8 | 1.8 V LVCMOS | SDMMC clock |
| HPS_GPIO39 | AP10 | 1.8 V LVCMOS | SDMMC Data1 |
| HPS_GPIO40 | AC9 | 1.8 V LVCMOS | SDMMC Data2 |
| HPS_GPIO41 | AM10 | 1.8 V LVCMOS | SDMMC Data3 |
| HPS_GPIO42 | AB10 | 1.8 V LVCMOS | Clock |
| HPS_GPIO43 | AJ13 | 1.8 V LVCMOS | GPIO I/O 19 |
| HPS_GPIO44 | AB14 | 1.8 V LVCMOS | GPIO I/O 20 |
| HPS_GPIO45 | AH14 | 1.8 V LVCMOS | GPIO I/O 21 |
| HPS_GPIO46 | AB12 | 1.8 V LVCMOS | Ethernet MDIO |
| HPS_GPIO47 | AJ9 | 1.8 V LVCMOS | Ethernet MDC |

## A.10. System Power

This section describes the Intel Agilex 7 FPGA development board's power supply. A laptop style DC power supply is provided with the development kit. Use only the supplied power supply. The power supply has an auto sensing input voltage of 100 – 240 V AC power and output of 12 V DC power at 20 A to the development board. The 12 V DC input power is then stepped down to various power rails used by the board components.

Power telemetry is provided via the Intel MAX 10 and $I^2C$ interface to the various voltage regulators and temperature sensors on the board. The power utilization is displayed on a GUI that shows power consumption versus time.

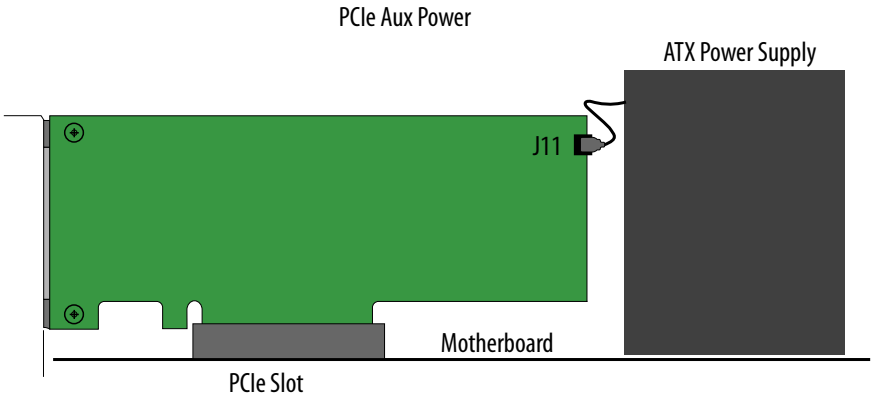
## A.11. Power Guidelines

The Intel Agilex 7 FPGA development kit has two modes of operation.

### A.11.1. In a Standard PCIe-Compliant System

In this mode, plug the board into an available PCI Express (PCIe) slot and connect the standard 2 x 4 auxiliary power cord available from the PC's ATX power supply to the respective mating power connector on the board (**J11**). The PCIe slot together with the auxiliary PCIe power are required to power the entire board. If you do not connect the 2 x 4 auxiliary power connections, the board will not power on when installed in a PCIe system. The power switch SW5 is ignored when the board is used in the PCIe system.

**Figure 28. In a Standard PCIe-Compliant System**



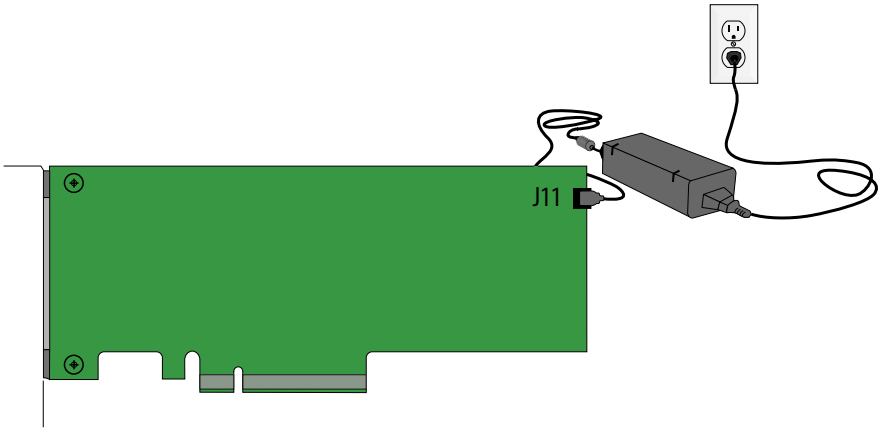

### A.11.2. As a Standalone Evaluation Board Powered by Included Power Supply

In this mode, plug the included power supply into the 2 x 4 pin connector (**J11**) and the AC power cord of the power supply into a power outlet.

*Note:* The power supply connector is a 2 x 3 pin connector but is keyed to mate with 6 pins of the **J11** power input on the board.

This power supply provides the entire power to the board without the need to obtain power from the PCIe slot. The power switch SW5 controls powering the board on or off.

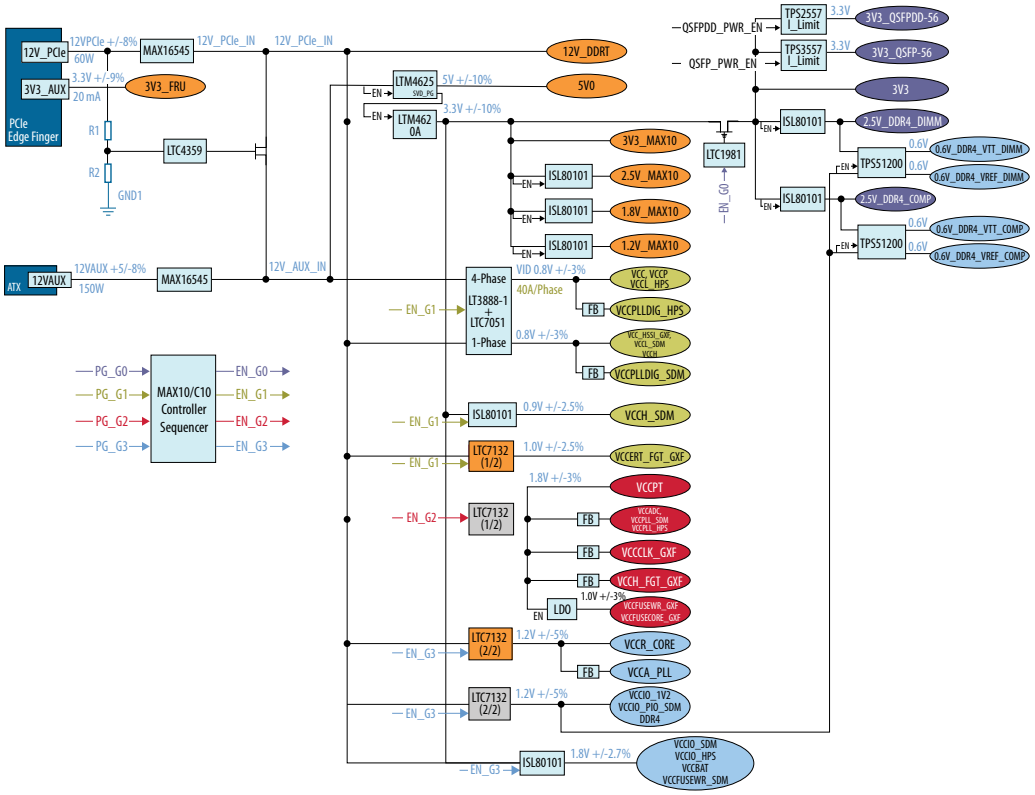
**Figure 29. As a Standalone Evaluation Board Powered by Included Power Supply**




## A.12. Power Distribution System

The following figure shows the power distribution system on the Intel Agilex 7 FPGA development board.

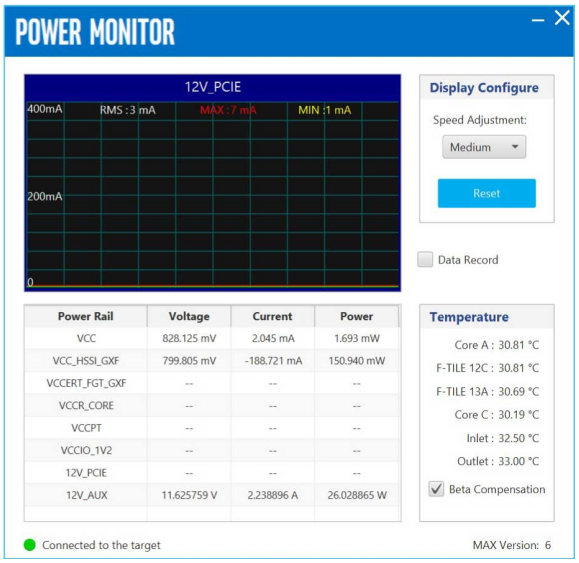
**Figure 30. Power Tree**



## A.13. Power Measurement

There are eight power supply rails that have on-board voltage, current, and wattage sense capabilities. An $I^2C$ bus connects seven of these voltage regulator devices to the Intel MAX 10 system controller for power telemetry data reporting. The $V_{CC}$ rail for the FPGA core power is measured by the Intel MAX 10 using the SPI bus interface between the Intel MAX 10 and VCC core controller. The Intel MAX 10 provides power data through the Power Monitor GUI.

**Figure 31. Power Monitor GUI**




## A.14. Thermal Limitations and Protection

The Intel Agilex 7 FPGA development kit is designed to operate in a typical laboratory environment with an ambient temperature of approximately 25 °C. The cooling solution provided with the development kit allows sufficient cooling for the board to operate up to a maximum power consumption of 150 W (under this environment).

Two MAX31730 3-channel remote temperature sensor devices are connected to the Intel Agilex 7 FPGA's internal temperature diodes. The function is to continuously monitor the FPGA's internal core and transceiver tile die temperatures as well as the board inlet and exhaust airflow temperatures when the board is installed inside a server system. Based on the data from both temperature sensors, the Intel Agilex 7 FPGA and Intel MAX 10 run at its maximum speed whenever any temperature is over 60 °C or immediately power off the board whenever the temperature crosses 100 °C to protect the board from damage.

***Caution:*** Ensure you unplug the power supply when the board is powered off when the temperature crosses 100 °C. Plug the power supply back again to ensure that the board can be turned on or off again.

# B. Additional Information

## B.1. Safety and Regulatory Information

**ENGINEERING DEVELOPMENT PRODUCT - NOT FOR RESALE OR LEASE**

This development kit is intended for laboratory development and engineering use only.

This development kit is designed to allow:

- Product developers and system engineers to evaluate electronic components, circuits, or software associated with the development kit to determine whether to incorporate such items in a finished product.
- Software developers to write software applications for use with the end product.

This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required Federal Communications Commission (FCC) equipment authorizations are first obtained.

Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference.

Unless the assembled kit is designed to operate under Part 15, Part 18 or Part 95 of the United States Code of Federal Regulations (CFR) Title 47, the operator of the kit must operate under the authority of an FCC licenseholder or must secure an experimental authorization under Part 5 of the United States CFR Title 47.

Safety Assessment and CE & UKCA mark requirements have been completed, however, other certifications that may be required for installation and operation in your region have not been obtained.

## B.1.1. Safety Warnings

### Power Supply Hazardous Voltage

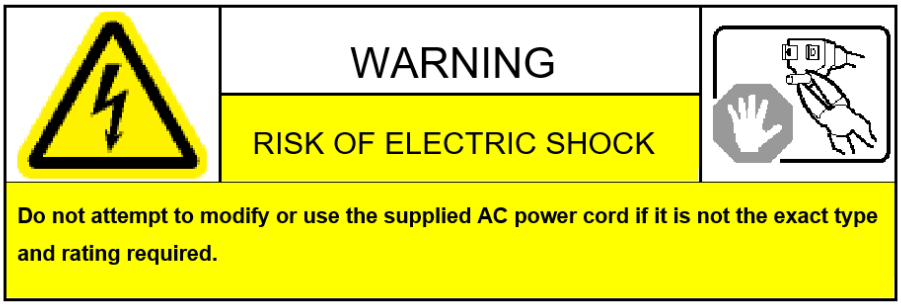
AC mains voltages are present within the power supply assembly. No user serviceable parts are present inside the power supply.

### Power Connect and Disconnect

The AC power supply cord is the primary disconnect device from mains (AC power) and used to remove all DC power from the board/system. The socket outlet must be installed near the equipment and must be readily accessible.


### System Grounding (Earthing)

To avoid shock, you must ensure that the power cord is connected to a properly wired and grounded receptacle. Ensure that any equipment to which this product is attached to is also connected to properly wired and grounded receptacles.



### Power Cord Requirements

The plug on the power cord must be a grounding-type male plug designed for use in your region. It must have certification marks showing certification by an agency in your region. The connector that plugs into the appliance inlet of the power supply must be an IEC 320, sheet C13, female connector. If the power cord supplied with the system does not meet requirements for use in your region, discard the cord, and do not use it with adapters. Use only certified power supply cord with appropriate gauge, designed for use in your region.

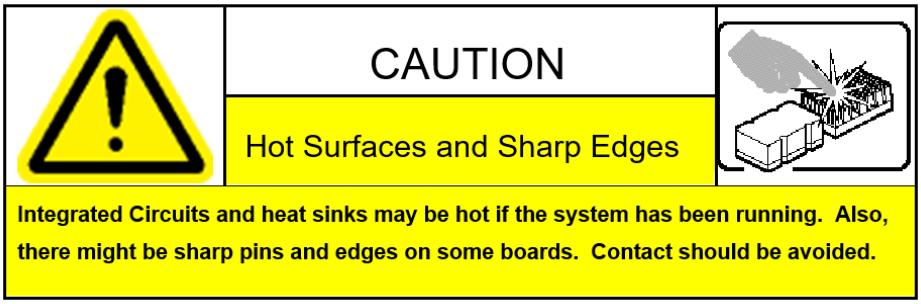
### Lightning/Electrical Storm

Do not connect/disconnect any cables or perform installation/maintenance of this product during an electrical storm.

### Risk of Fire

To reduce the risk of fire, keep all flammable materials a safe distance away from the boards and power supply. You must configure the development kit on a flame retardant surface.

## B.1.2. Safety Cautions




### Thermal and Mechanical Injury

Certain components such as heat sinks, power regulators, and processors may be hot. Heatsink fans are not guarded. Power supply fan may be accessible through guard. Care should be taken to avoid contact with these components.


### Cooling Requirements

Maintain a minimum clearance area of 5 centimeters (2 inches) around the side, front and back of the board for cooling purposes. Do not block power supply ventilation holes and fan.

### Electro-Magnetic Interference (EMI)

This equipment has not been tested for compliance with emission limits of FCC and similar international regulations. Use of this equipment in a residential location is prohibited. This equipment generates, uses and can radiate radio frequency energy which may result in harmful interference to radio communications. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment on and off, you are required to take measures to eliminate this interference.

### Telecommunications Port Restrictions

The wireline telecommunications ports (modem, xDSL, T1/E1) on this product must not be connected to the Public Switched Telecommunication Network (PSTN) as it might result in disruption of the network. No formal telecommunication certification to FCC, R&TTE Directive, or other national requirements have been obtained.

### Electrostatic Discharge (ESD) Warning

A properly grounded ESD wrist strap must be worn during operation/installation of the boards, connection of cables, or during installation or removal of daughter cards. Failure to use wrist straps can damage components within the system.

***Attention:*** Please return this product to Intel for proper disposition. If it is not returned, refer to local environmental regulations for proper recycling. Do not dispose of this product in unsorted municipal waste.

### Lithium Ion Battery Warnings

**Lithium Battery**: Risk of explosion if the lithium battery is replaced by an incorrect type. Risk of fire, explosion, or chemical burn if the battery is mistreated (punctured or crushed). Do not attempt to disassemble. Do not incinerate. Observe proper polarity when replacing battery. Do not dispose—the battery is intended to be serviced and disposed by qualified Intel service personnel only.

**Perchlorate Material**: Special handling may apply. For more details, refer to www.dtsc.ca.gov/hazardouswaste/perchlorate. This notice is required by California Code of Regulations, Title 22, Division 4.5, Chapter 33: Best Management Practices for Perchlorate Materials. This product includes a battery which contains perchlorate material.

**Taiwan battery recycling**:


(Translation - please recycle batteries)

**Please return this product to Intel for proper disposition. If it is not returned, refer to local environmental regulations for proper recycling. Do not dispose of product in unsorted municipal waste.**

## B.2. Compliance Information

### CE EMI Conformity Caution

This development board is delivered conforming to relevant standards mandated by Directive 2014/30/EU. Because of the nature of programmable logic devices, it is possible for the user to modify the development kit in such a way as to generate electromagnetic interference (EMI) that exceeds the limits established for this equipment. Any EMI caused as a result of modifications to the delivered material is the responsibility of the user of this development kit.